

BLM9D2324-08AM

LDMOS 2-stage integrated Doherty MMIC

Rev. 1 — 13 October 2020

AMPLEON

Product data sheet

1. Product profile

1.1 General description

The BLM9D2324-08AM is a 2-stage 8 W fully integrated Doherty MMIC solution using Ampleon's state of the art GEN9 LDMOS technology. The carrier and peaking device, input splitter and output combiner are integrated in a single package. This multiband device is perfectly suited as a device in the frequency range from 2300 MHz to 2400 MHz. Available in LGA outline.

Table 1. Performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $I_{DQ} = 18\text{ mA}$ (driver and final stages) in a demo circuit; $V_{GSQ(peaking)} = V_{GSQ(carrier)} - 0.55\text{ V}$.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA [1]	2350	28	1.12	27	41	-30

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

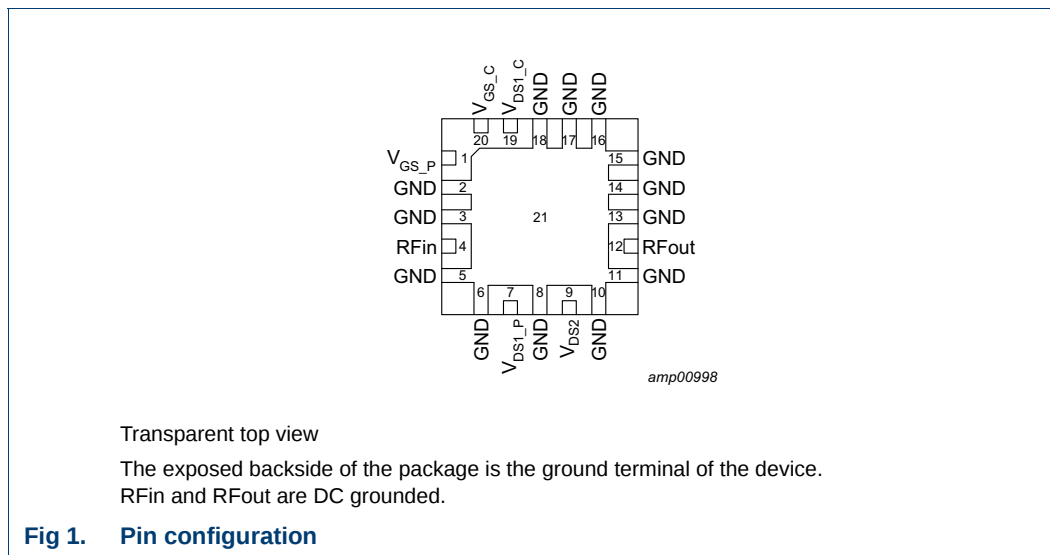
- Integrated input splitter
- Integrated output combiner
- Very high efficiency
- Designed for broadband operation (frequency 2300 MHz to 2400 MHz)
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Excellent thermal stability
- High power gain, input and output matched to impedance $50\text{ }\Omega$
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA, LTE and NR small cell base stations in the 2300 MHz to 2400 MHz frequency range

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{GS_P}	1	gate-source voltage of peaking
GND	2	ground
GND	3	ground
RFin	4	RF input
GND	5	ground
GND	6	ground
V _{DS1_P}	7	drain-source voltage of peaking driver
GND	8	ground
V _{DS2}	9	drain-source voltage of final stages
GND	10	ground
GND	11	ground
RFout	12	RF output
GND	13	ground
GND	14	ground
GND	15	ground
GND	16	ground
GND	17	ground
GND	18	ground

Table 2. Pin description ...continued

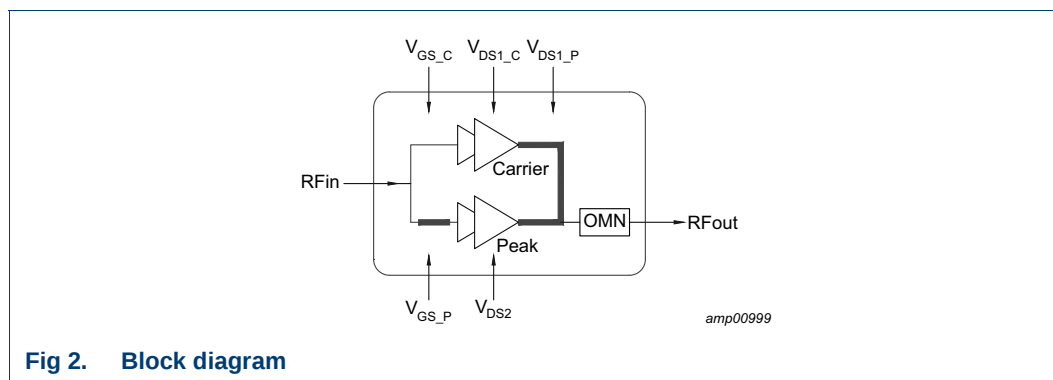
Symbol	Pin	Description
V_{DS1_C}	19	drain-source voltage of carrier driver
V_{GS_C}	20	gate-source voltage of carrier driver
GND	21	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM9D2324-08AM	-	plastic thermal enhanced package; no leads; 20 terminals; body 7.0 x 7.0 x 0.98 mm	LGA-7x7-20-1

4. Block diagram



5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-55	+125	°C
T_j	junction temperature	[1]	-	175	°C
T_{case}	case temperature	[1]	-	125	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_{L(AV)} = 1.12\text{ W}$ [1]	9.2	K/W
		$T_{case} = 80\text{ °C}; P_{L(AV)} = 1.78\text{ W}$ [1]	8.3	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 7.2 dB.

7. Characteristics

Table 6. DC characteristics

$T_{case} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 18\text{ mA}$	1.65	2.05	2.75	V
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}/-5\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}/-5\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 60\text{ V}$	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 60\text{ V}$	-	-	1.4	μA

Table 7. RF Characteristics

Typical RF performance at $T_{case} = 25\text{ °C}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 18\text{ mA}$ (carrier);

$V_{GSq(peaking)} = V_{GSq(carrier)} - 0.55\text{ V}$; $P_L = 1.12\text{ W}$; $f = 2.4\text{ GHz}$. Unless otherwise specified, measured in an Ampleon production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: CW pulsed						
G_p	power gain		25	27	29	dB
η_D	drain efficiency		36	42.5	-	%
RL_{in}	input return loss		-	-19	-13	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		39	40	-	dBm

8. Application information

Table 8. Typical performance

Test signal: 1-carrier W-CDMA; $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ} = 18\text{ mA}$ (driver and final stages); test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability CCDF; unless otherwise specified, measured in an Ampleon 2300 MHz to 2400 MHz frequency band demo circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	$f = 2350\text{ MHz}$ [1]	-	40	-	dBm
η_D	drain efficiency	$P_{L(AV)} = 30.5\text{ dBm}$; $f = 2300\text{ MHz}$	-	41	-	%
G_p	power gain	$P_{L(AV)} = 30.5\text{ dBm}$; $f = 2300\text{ MHz}$	-	27	-	dB
G_{flat}	gain flatness	$P_{L(AV)} = 30.5\text{ dBm}$; $f = 2300\text{ MHz}$ to 2400 MHz	-	0.8	-	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 30.5\text{ dBm}$; $f = 2300\text{ MHz}$	-	-30	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	$f = 2300\text{ MHz}$	-	0.04	-	dB/ $^{\circ}\text{C}$
K	Rollett stability factor	$T_{case} = -40\text{ }^{\circ}\text{C}$; $f = 0.15\text{ GHz}$ to 5 GHz [2]	-	>1	-	

[1] Pulsed CW power sweep measurement ($\delta = 10\%$, $t_p = 100\text{ }\mu\text{s}$).

[2] S-parameters measured in a demo circuit.

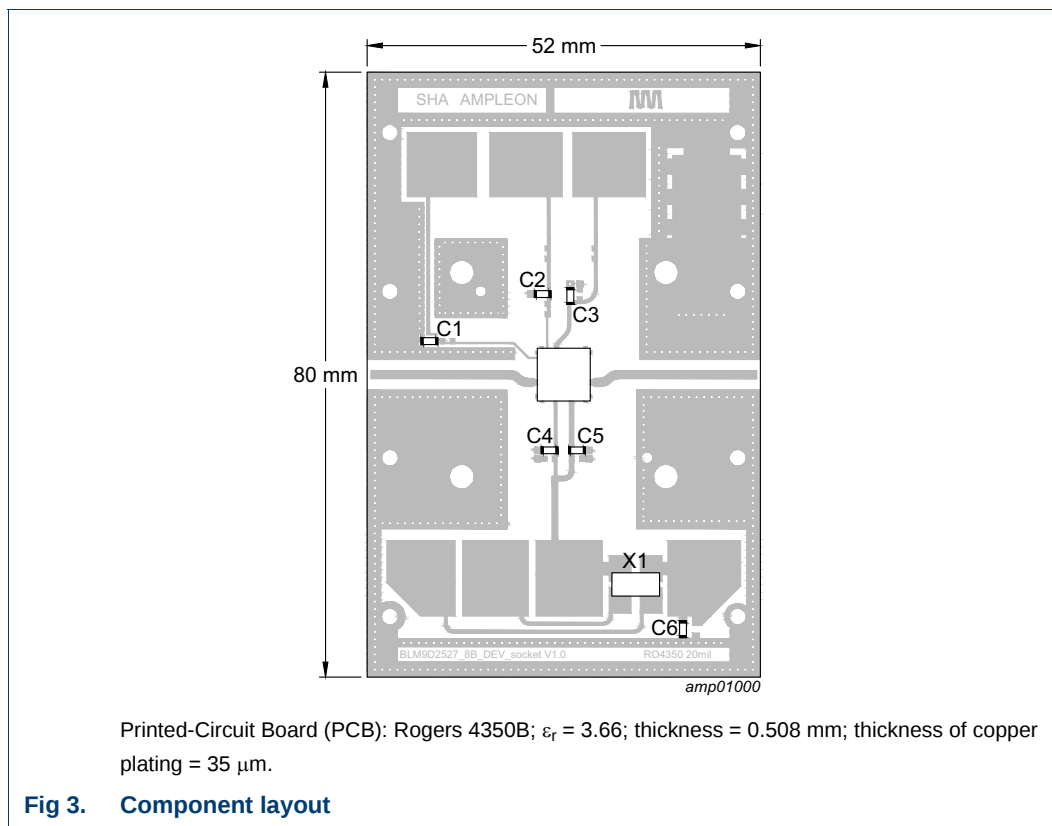


Table 9. Demo test circuit list of components

See [Figure 3](#) for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5	multilayer ceramic chip capacitor	1 μF [1]	
C6	multilayer ceramic chip capacitor	1 μF [2]	
X1	current sense resistor	100 m Ω , 1 W	Y44870R10000B0R

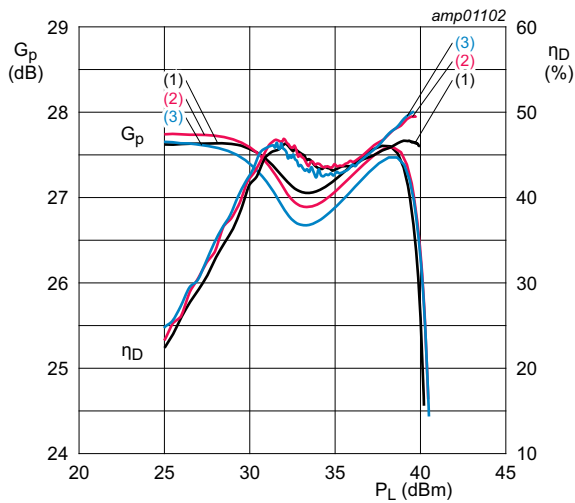
[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

8.1 Ruggedness in a Doherty operation

The BLM9D2324-08AM is capable of withstanding a load mismatch corresponding to $V_{\text{SWR}} = 10 : 1$ through all phases under the following conditions: $V_{\text{DS}} = 28 \text{ V}$; $I_{\text{Dq}} = 18 \text{ mA}$ (carrier); $V_{\text{GSq(peak)}} = V_{\text{GSq(carrier)}} - 0.55 \text{ V}$; P_i corresponding to $P_{\text{L(3dB)}}$ under $Z_{\text{S}} = 50 \Omega$ load; $f = 2300 \text{ MHz}$ (CW); $T_{\text{case}} = 25 \text{ }^\circ\text{C}$.

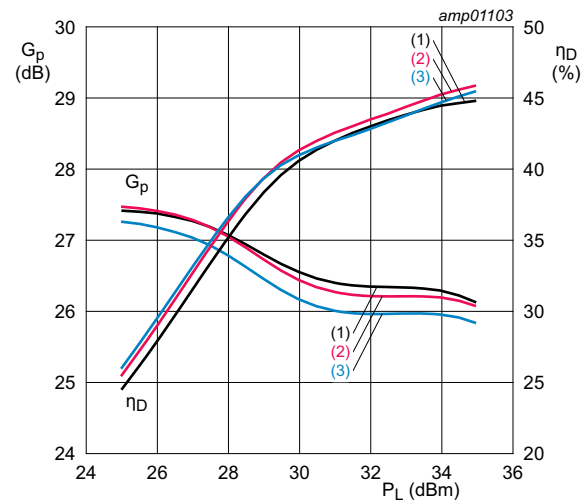
8.2 Graphs



$V_{DS} = 28 \text{ V}$; $V_{GS(amp)peak} = 1.51 \text{ V}$; $I_{Dq} = 18 \text{ mA}$;
 $t_p = 100 \text{ } \mu\text{s}$; $\delta = 10 \text{ } \%$.

- (1) $f = 2300 \text{ MHz}$
- (2) $f = 2350 \text{ MHz}$
- (3) $f = 2400 \text{ MHz}$

Fig 4. Power gain and drain efficiency as function of output power; typical values

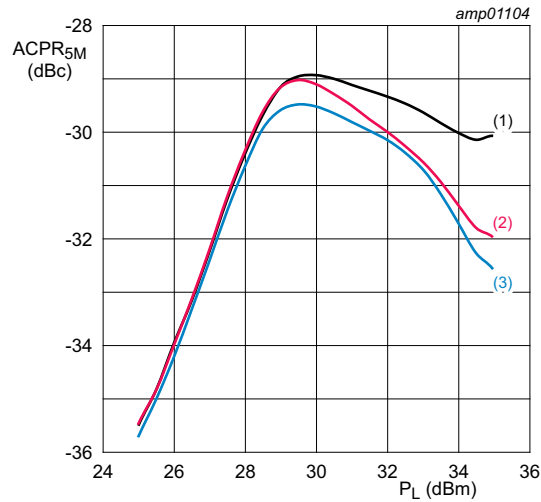


$V_{DS} = 28 \text{ V}$; $V_{GS(amp)peak} = 1.51 \text{ V}$; $I_{Dq} = 18 \text{ mA}$.

Test signal: 1-carrier W-CDMA; 3GPP test model 1;
 64 DPCH; PAR = 7.2 dB at 0.01 % probability CCDF.

- (1) $f = 2300 \text{ MHz}$
- (2) $f = 2350 \text{ MHz}$
- (3) $f = 2400 \text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values

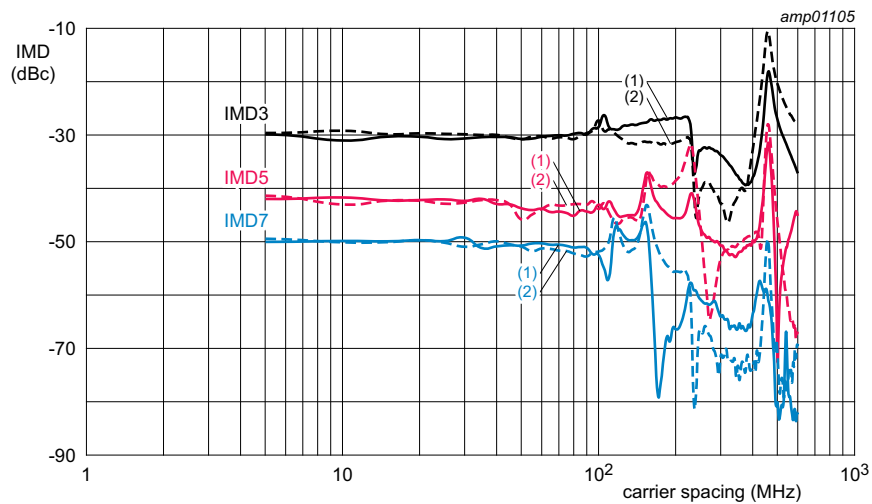


$V_{DS} = 28 \text{ V}$; $V_{GS(amp)peak} = 1.51 \text{ V}$; $I_{Dq} = 18 \text{ mA}$.

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability CCDF.

- (1) $f = 2300 \text{ MHz}$
- (2) $f = 2350 \text{ MHz}$
- (3) $f = 2400 \text{ MHz}$

Fig 6. Adjacent channel power ratio as a function of output power; typical values



$V_{DS} = 28 \text{ V}$; $V_{GS(amp)peak} = 1.51 \text{ V}$; $I_{Dq} = 18 \text{ mA}$; $f = 2350 \text{ MHz}$.

Test signal: 2-carrier pulsed CW; $t_p = 100 \mu\text{s}$; $\delta = 10 \%$.

- (1) IMD low
- (2) IMD high

Fig 7. VBW capability

9. Package outline

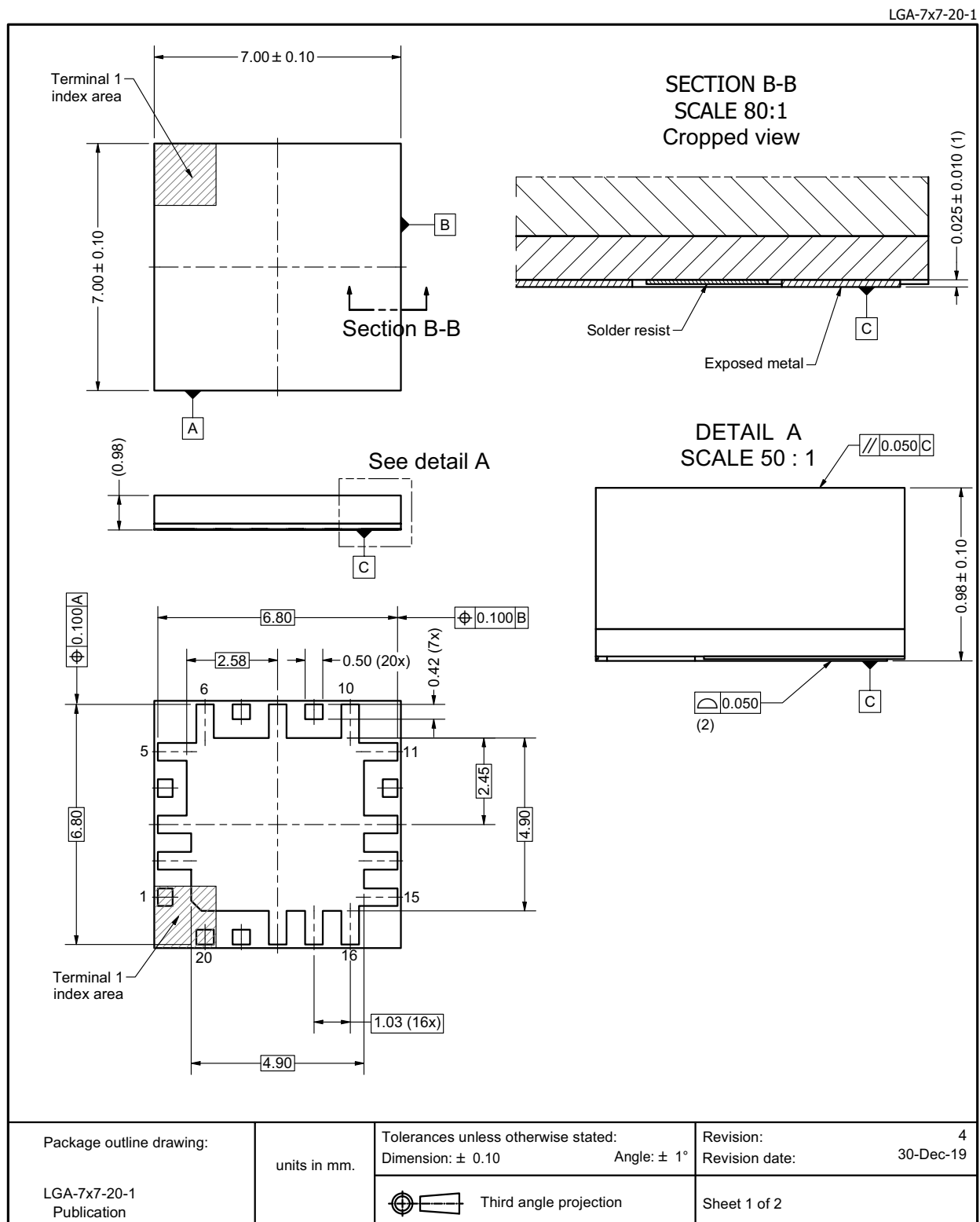


Fig 8. Package outline LGA-7x7-20-1 (sheet 1 of 2)

LGA-7x7-20-1

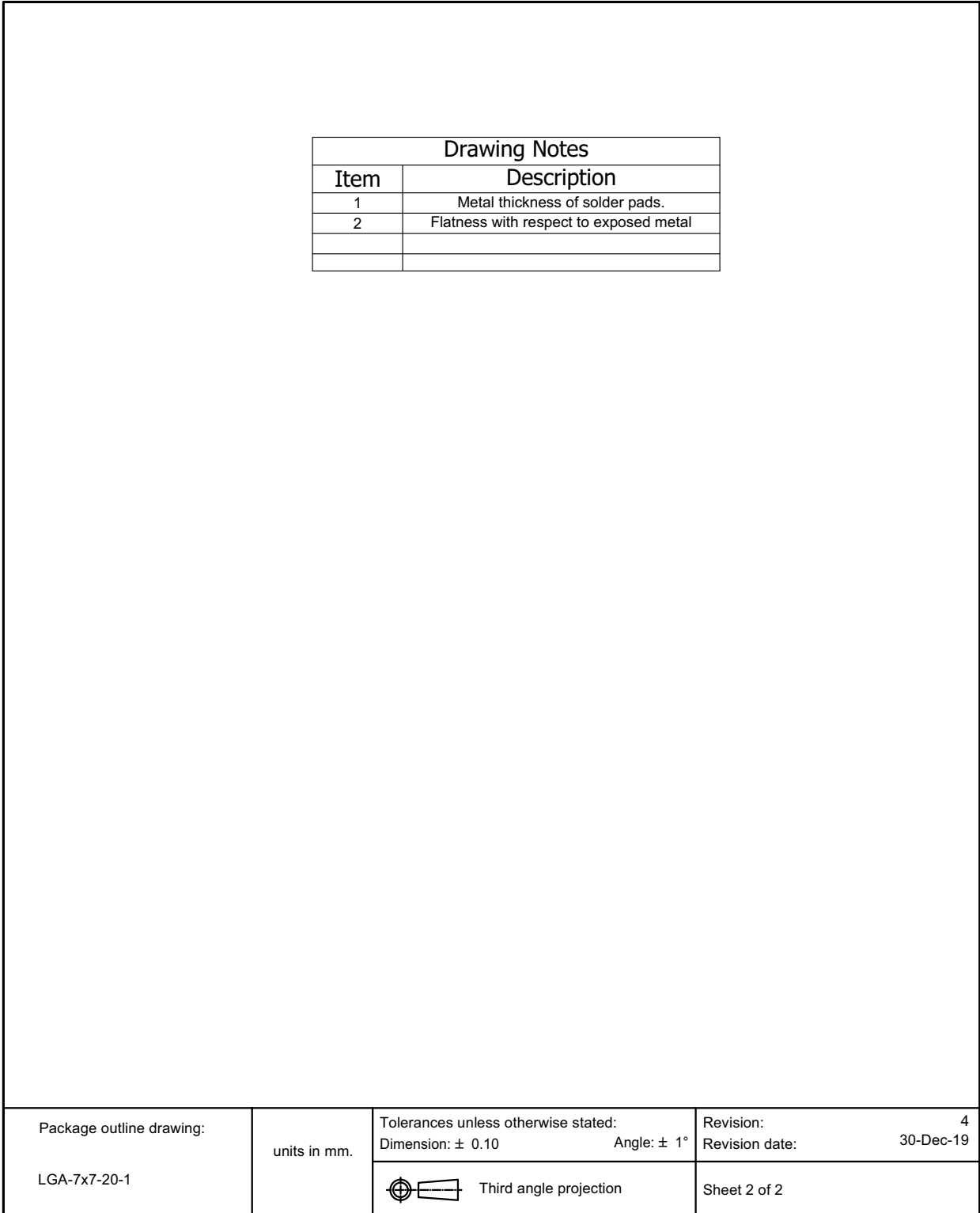


Fig 9. Package outline LGA-7x7-20-1 (sheet 2 of 2)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN9	Ninth Generation
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
NR	New Radio
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM9D2324-08AM v.1	20201013	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
2.1	Pinning	2
2.2	Pin description	2
3	Ordering information	3
4	Block diagram	3
5	Limiting values	3
6	Thermal characteristics	4
7	Characteristics	4
8	Application information	5
8.1	Ruggedness in a Doherty operation	6
8.2	Graphs	7
9	Package outline	9
10	Handling information	11
11	Abbreviations	11
12	Revision history	11
13	Legal information	12
13.1	Data sheet status	12
13.2	Definitions	12
13.3	Disclaimers	12
13.4	Trademarks	13
14	Contact information	13
15	Contents	14

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