ISL43L110, ISL43L111

Ultra Low ON-Resistance, +1.1V to +4.5V Single Supply, SPST Analog Switches

FN6130
Rev 1.00
August 24, 2015

The Intersil ISL43L110 and ISL43L111 devices are low ON-resistance, low voltage, bidirectional, single pole/single throw (SPST) analog switches designed to operate from a single +1.1V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low R_{ON} resistance, excellent R_{ON} flatness, and fast switching speeds (t_{ON} = 8ns, t_{OFF} = 5ns). The digital logic input is 1.8V CMOS compatible when using a single +3V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to switch in additional functionality while reducing ASIC design risk. The ISL43L11X are offered in a 5 lead SC70 package, alleviating board space limitations.

The ISL43L110 has one normally open (NO) switch and ISL43L111 has one normally closed (NC) switch.

TABLE 1. FEATURES AT A GLANCE

	ISL43L110	ISL43L111 (No longer available or supported)
Number of Switches	1	1
SW	NO	NC
1.8V R_{ON}	0.45Ω	0.45Ω
1.8V t_{ON}/t_{OFF}	17ns/7ns	17ns/7ns
3V R_{ON}	0.24Ω	0.24Ω
3V t_{ON}/t_{OFF}	9ns/6ns	9ns/6ns
4.3V R_{ON}	0.21Ω	0.21Ω
4.3V t_{ON}/t_{OFF}	8ns/5ns	8ns/5ns
Package	5 Ld SC70	

Features

- Pb-Free available (RoHS compliant)
- Drop in replacement for the MAX4715 and MAX4716
- ON resistance (R_{ON})
  - V_{CC} = +4.3V 0.21Ω
  - V_{CC} = +3.0V 0.24Ω
  - V_{CC} = +1.8V 0.45Ω
- R_{ON} flatness 0.03Ω
- Single supply operation . . . . . +1.1V to +4.5V
- Fast switching action (+3.9V Supply)
  - t_{ON} 8ns
  - t_{OFF} 5ns
- ESD HBM rating . . . . . >4kV
- 1.8V, CMOS logic compatible (+3V supply)
- 5 lead SC70 packaging

Applications

- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable test and measurement
- Medical equipment
- Audio and video switching

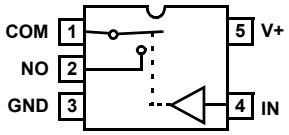
Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

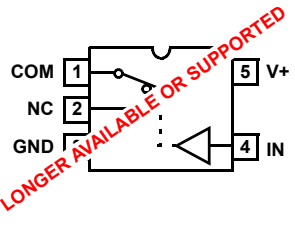
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Pinouts (Note 1)

ISL43L110 (SC70)
TOP VIEW



ISL43L111 (SC70)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	ISL43L110	ISL43L111
0	Off	On
1	On	Off

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.1V to +4.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Ordering Information

PART NO. (BRAND)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL43L110IHZ-T (CKA) (See Note)	-40 to 85	5 Ld SC70 Tape and Reel	P5.049
ISL43L111IHZ-T (CLA) (See Note) **(No longer available, recommended replacement: ISL43L210IHZ-T)**	-40 to 85	5 Ld SC70 Tape and Reel	P5.049

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
NO, NC, IN (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ± 600mA
ESD Rating:
HBM > . . . . . >4kV
MM . . . . . >300V
CDM . . . . . >1000V

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
5 Ld SC70 Package	660

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 2.2V (See Figure 4)	25	-	0.22	-	Ω
		Full	-	0.25	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0.8V, 2.2V, 3.5V, (Note 7)	25	-	0.03	-	Ω
		Full	-	0.05	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-30	-	30	nA
		Full	-200	-	200	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-3	-	3	nA
		Full	-35	-	35	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	8	15	ns
		Full	-	-	20	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	5	10	ns
		Full	-	-	15	ns
Charge Injection, Q	V_G = V+/2, R_G = 0Ω, C_L = 1.0nF (See Figure 2)	25	-	89	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 3)	25	-	-65	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.003	-	%
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	68	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	160	-	pF

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Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Notes 4, 6), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.1		4.5	V
Positive Supply Current, I+	V+ =+4.5V, V_{IN} = 0V or V+	25	-	-	0.05	µA
		Full	-	-	0.4	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.6	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+ (Note 8)	Full	-0.5	-	0.5	µA

NOTES:

4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Guaranteed but not tested.

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 1.5V (See Figure 4)	25	-	0.26	0.4	Ω
		Full	-	-	0.45	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0.6V, 1.5V, 2.1V (Note 7)	25	-	0.038	0.07	Ω
		Full	-	-	0.09	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-	1.8	-	nA
		Full	-	8	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-	1.8	-	nA
		Full	-	16	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	9	15	ns
		Full	-	-	20	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	6	12	ns
		Full	-	-	15	ns
Charge Injection, Q	V_G = V+/2, R_G = 0Ω,C_L = 1.0nF (See Figure 2)	25	-	72	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 3)	25	-	-65	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 32Ω	25	-	0.003	-	%
NO or NC or COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	68	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 5)	25	-	160	-	pF

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Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 4, 6), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+	25	-	0.018	-	µA
		Full	-	0.13	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+ (Note 8)	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.8V Supply

Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.8V, I_{COM} = 10mA, V_{NO} or V_{NC} = 0.9V (See Figure 4)	25	-	0.45	0.6	Ω
		Full	-	-	0.8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 1.8V, V_{COM} = 0.3V, 1.5V, V_{NO} or V_{NC} = 1.5V, 0.3V	25	-	0.4	-	nA
		Full	-	7	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 1.8V, V_{COM} = 0.3V, 1.5V, or V_{NO} or V_{NC} = 0.3V, 1.5V, or Floating	25	-	0.8	-	nA
		Full	-	14	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	17	25	ns
		Full	-	-	30	ns
Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 8)	25	-	7	15	ns
		Full	-	-	20	ns
Charge Injection, Q	V_G = V+/2, R_G = 0Ω,C_L = 1.0nF (See Figure 2)	25	-	52	-	pC
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 1.8V, V_{IN} = 0V or V+	25	-	0.018	-	µA
		Full	-	0.13	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.4	V
Input Voltage High, V_{INH}		Full	1	-	-	V
Input Current, I_{INH}, I_{INL}	V_{IN} = 0V or V+ (Note 8)	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.1V Supply

Test Conditions: V+ = +1.1V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.3V (Notes 4, 6), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.1V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0.6V (See Figure 4)	25	-	2.4	-	Ω
		Full	-	3	-	Ω

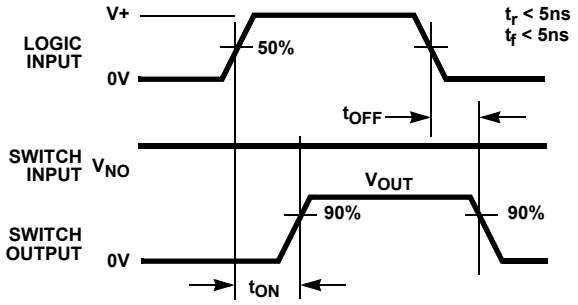
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Electrical Specifications - 1.1V Supply

Test Conditions: V+ = +1.1V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.3V (Notes 4, 6), Unless Otherwise Specified **(Continued)**

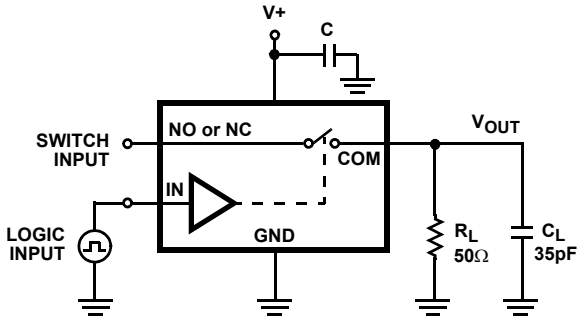
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.1V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	41	-	ns
		Full	-	42	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.1V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1)	25	-	11	-	ns
		Full	-	12	-	ns
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	0.42	-	V
Input Voltage High, V_{INH}		Full	-	0.58	-	V

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

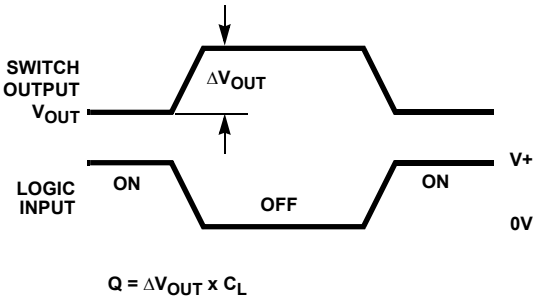


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

FIGURE 2A. MEASUREMENT POINTS

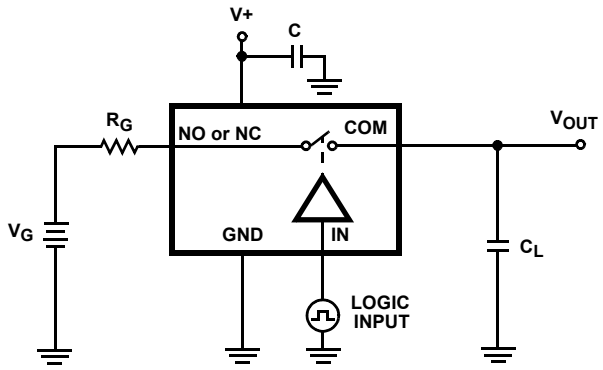


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

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Test Circuits and Waveforms (Continued)

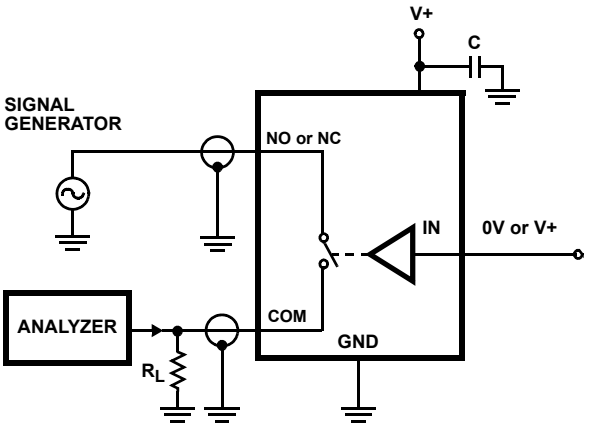


FIGURE 3. OFF ISOLATION TEST CIRCUIT

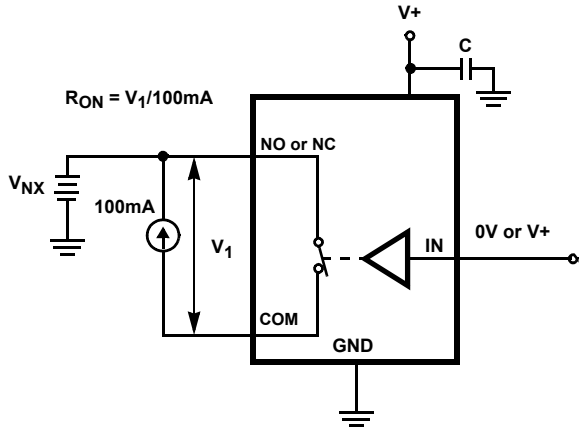


FIGURE 4. R_{ON} TEST CIRCUIT

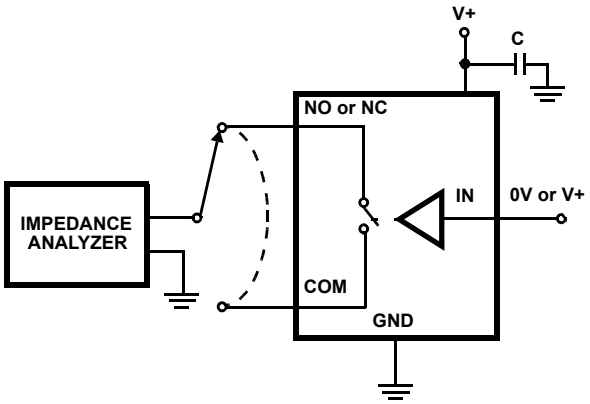


FIGURE 5. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43L110 and ISL43L111 are bidirectional, single pole/single throw (SPST) analog switches. They offer precise switching capability from a single +1.1V to 4.5V supply with ultra low on-resistance and high speed operation. With a single supply of 4.3V the typical on-resistance is only 0.21Ω, with a typical turn-on and turn-off time of: t_{ON} = 8ns, t_{OFF} = 5ns. The devices are especially well suited for portable battery powered equipment due to its low operating supply voltage (1.1V), low power consumption (1.8µW max), low leakage currents (200nA max), and the tiny SC70 packaging.

The ISL43L110 is a normally open (NO) SPST analog switch. The ISL43L111 is a normally closed (NC) SPST analog switch.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 6). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the input (see Figure 6). The resistor limits the input current below the threshold that produces permanent

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damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch. Connecting Schottky diodes to the signal pins as shown in Figure 6 will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current.

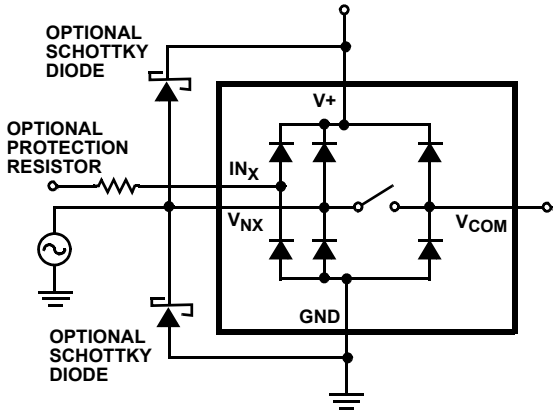


FIGURE 6. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43L11X construction is typical of most single supply CMOS analog switches in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL43L11X 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 4.2V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.1V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shiftier. The level shiftier converts the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2V to 3.6V (See Figure 15). At 3.6V the V_{IH} level is about 1.1V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (See Figure 16). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough. Figure 17 details the high Off Isolation rejection provided by this family. At 100kHz, Off Isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

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Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

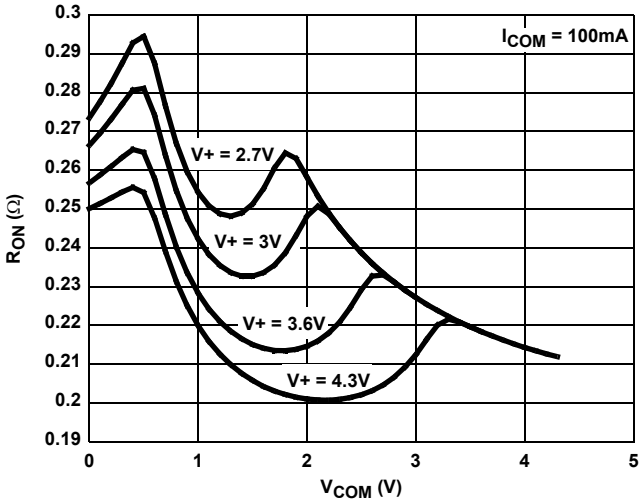


FIGURE 7. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

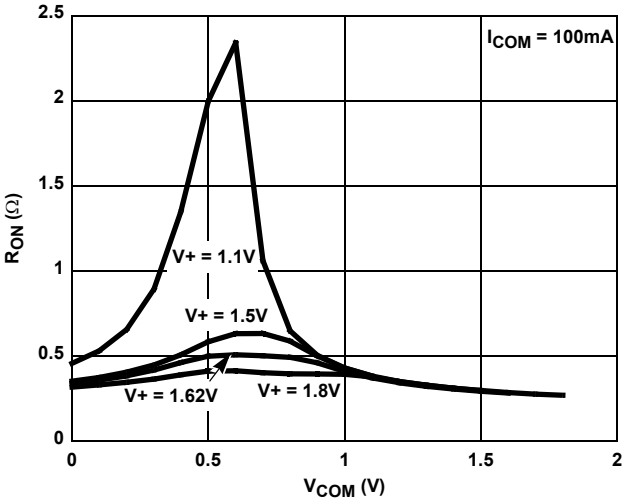


FIGURE 8. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

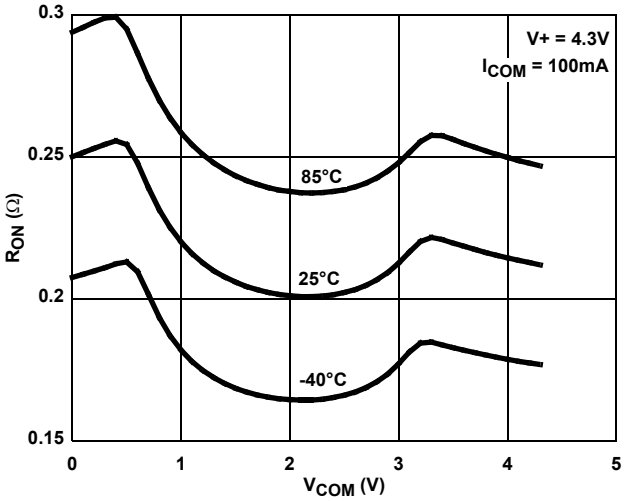


FIGURE 9. ON RESISTANCE vs SWITCH VOLTAGE

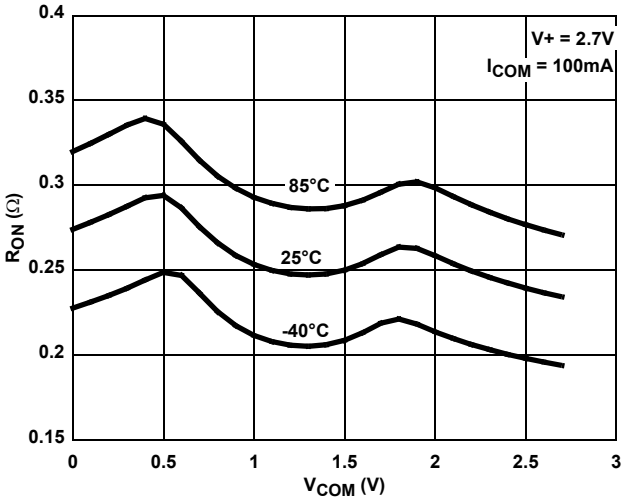


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

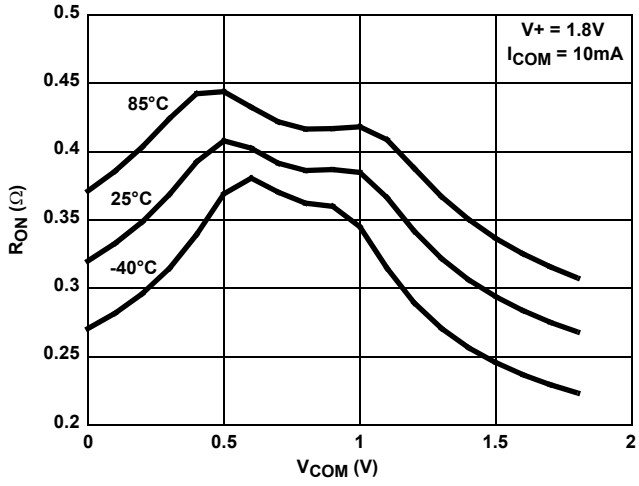


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

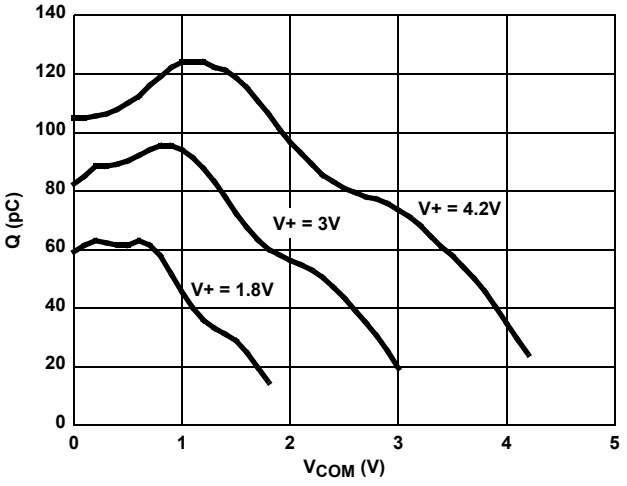


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

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Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

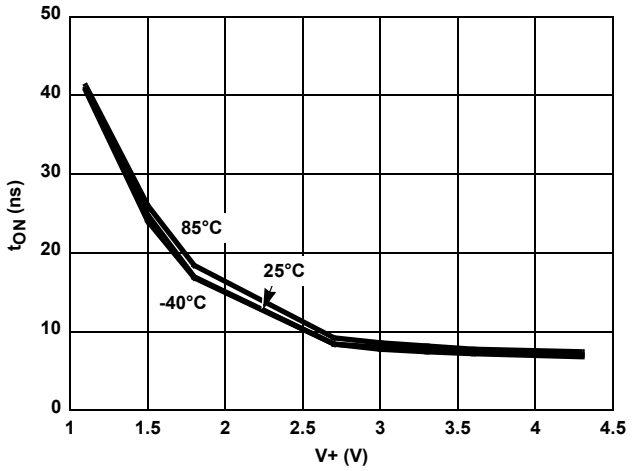


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

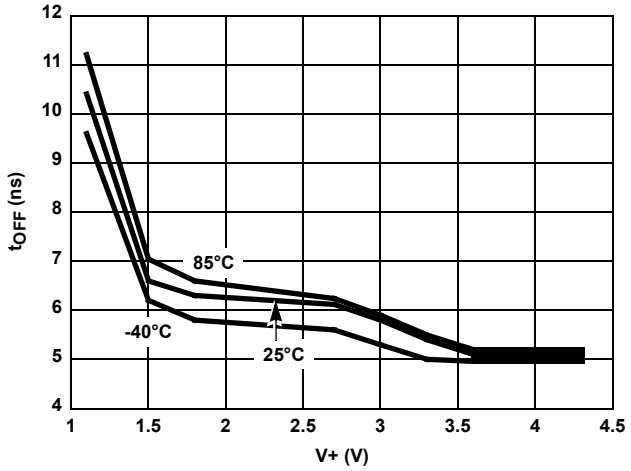


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

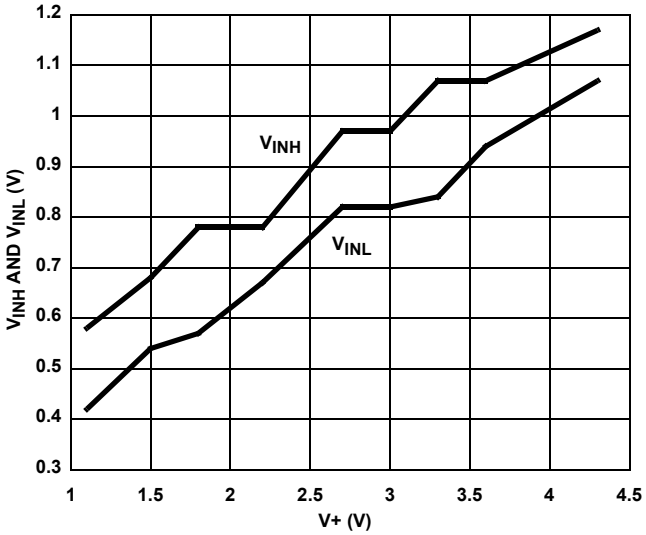


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

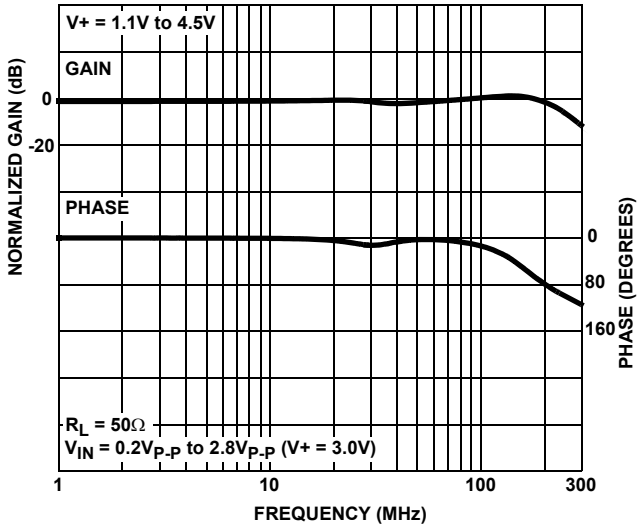


FIGURE 16. FREQUENCY RESPONSE

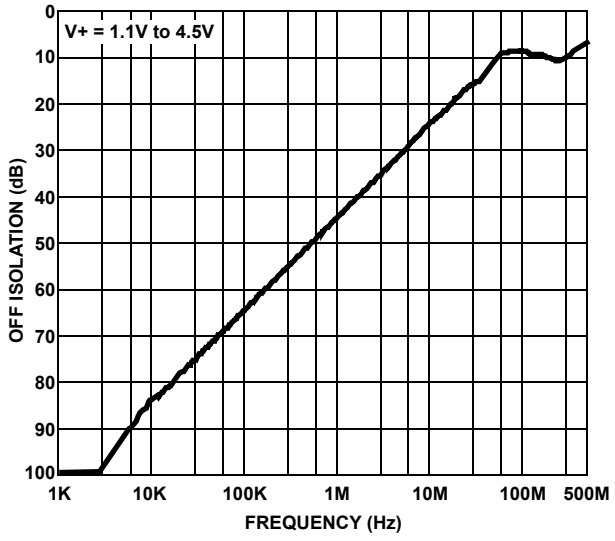


FIGURE 17. OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

57

PROCESS:

Submicron CMOS

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 24, 2015	FN6130.1	Updated the Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing (POD) P5.049 to the latest revision. -Revision 2 to Revision 3 changes - Added "Typical Recommended Land Pattern.

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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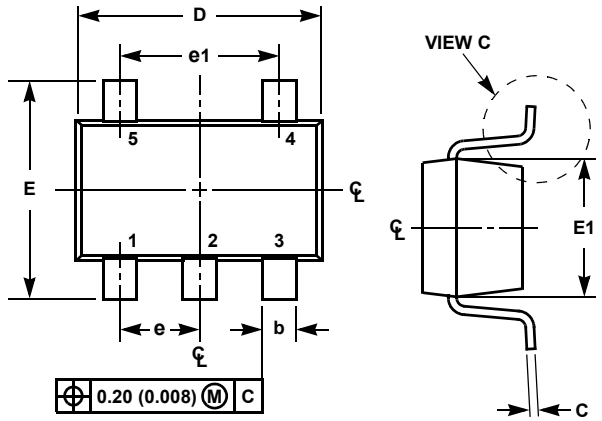
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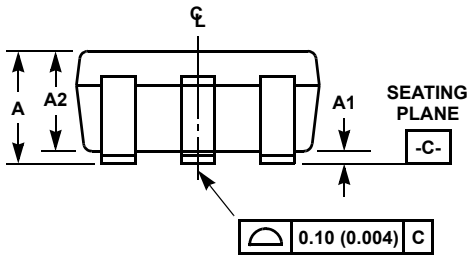
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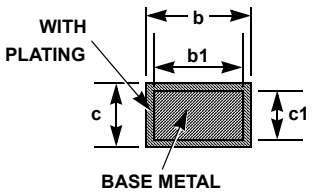
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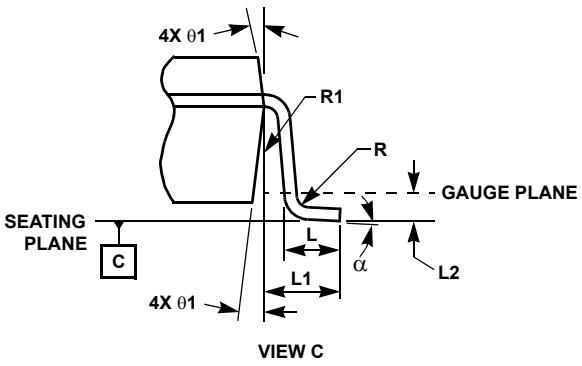
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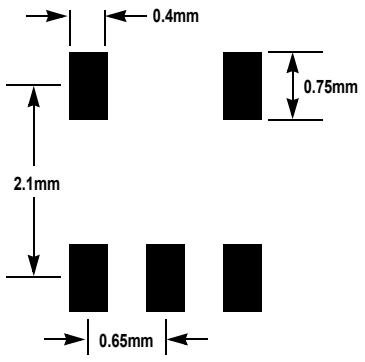
Small Outline Transistor Plastic Packages (SC70-5)











TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

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