



## TPS6211x 17-V, 1.5-A, Synchronous Step-Down Converter

### 1 Features

- High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency
- 3.1-V to 17-V Operating Input Voltage Range
- Adjustable Output Voltage Range: 1.2 V to 16 V
- Fixed Output Voltage Options Available in 3.3 V and 5 V
- Synchronizable to External Clock: Up to 1.4 MHz
- Up to 1.5-A Output Current
- High Efficiency Over a Wide Load-Current Range Due to PFM/PWM Operation Mode
- 100% Maximum Duty Cycle for Lowest Dropout
- 20- $\mu$ A Quiescent Current (Typical)
- Overtemperature and Overcurrent Protected
- Available in 16-Pin VQFN Package

### 2 Applications

- Point-of-Load Regulation From 12-V Buses
- Organizers, PDAs, and Handheld PCs
- Handheld Scanners

### 3 Description

The TPS6211x devices are a family of low-noise synchronous step-down DC-DC converters that are ideally suited for systems powered from a 2- to 4-cell Li-ion battery or from a 12-V or 15-V rail.

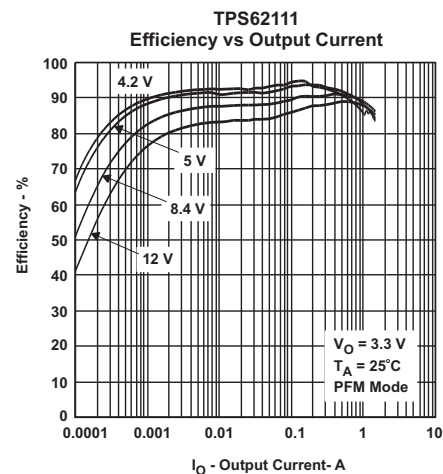
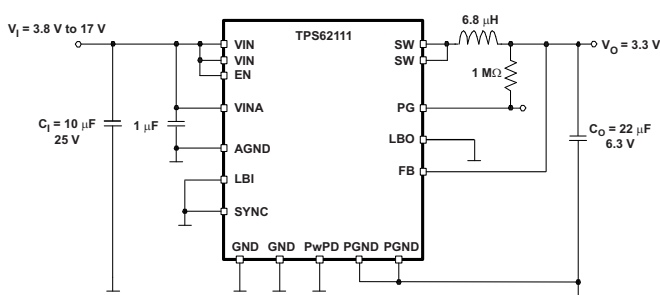
The TPS6211x devices are synchronous pulse width modulation (PWM) converters with integrated N- and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve highest efficiency over a wide load-current range, the converter enters a power-saving, pulse frequency modulation (PFM) mode at light load currents. Operating frequency is typically 1 MHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 0.8 MHz to 1.4 MHz. For low-noise operation, the converter can be operated in PWM-only mode. In shutdown mode, the current consumption is reduced to less than 2  $\mu$ A. The TPS6211x family of devices are available in the 16-pin (RSA) VQFN package, and operate over a free-air temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)          |
|-------------|-----------|--------------------------|
| TPS62110    | VQFN (16) | 4.00 mm $\times$ 4.00 mm |
| TPS62111    |           |                          |
| TPS62112    |           |                          |
| TPS62113    |           |                          |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Typical Application Schematic



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 9.4 Device Functional Modes.....                                 | <b>12</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | <b>10 Application and Implementation</b> .....                   | <b>15</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | 10.1 Application Information.....                                | <b>15</b> |
| <b>4 Typical Application Schematic</b> .....   | <b>1</b>  | 10.2 Typical Applications .....                                  | <b>15</b> |
| <b>5 Revision History</b> .....                | <b>2</b>  | 10.3 System Examples .....                                       | <b>22</b> |
| <b>6 Device Comparison Table</b> .....         | <b>4</b>  | <b>11 Power Supply Recommendations</b> .....                     | <b>23</b> |
| <b>7 Pin Configuration and Functions</b> ..... | <b>4</b>  | <b>12 Layout</b> .....   | <b>23</b> |
| <b>8 Specifications</b> .....                  | <b>5</b>  | 12.1 Layout Guidelines .....                                     | <b>23</b> |
| 8.1 Absolute Maximum Ratings .....             | <b>5</b>  | 12.2 Layout Example .....  | <b>24</b> |
| 8.2 ESD Ratings.....                           | <b>5</b>  | <b>13 Device and Documentation Support</b> .....                 | <b>25</b> |
| 8.3 Recommended Operating Conditions.....      | <b>5</b>  | 13.1 Device Support.....   | <b>25</b> |
| 8.4 Thermal Information .....                  | <b>5</b>  | 13.2 Related Links .....   | <b>25</b> |
| 8.5 Electrical Characteristics.....            | <b>6</b>  | 13.3 Community Resources.....                                    | <b>25</b> |
| 8.6 Typical Characteristics.....               | <b>8</b>  | 13.4 Trademarks .....  | <b>25</b> |
| <b>9 Detailed Description</b> .....            | <b>9</b>  | 13.5 Electrostatic Discharge Caution.....                        | <b>25</b> |
| 9.1 Overview .....                             | <b>9</b>  | 13.6 Glossary .....  | <b>25</b> |
| 9.2 Functional Block Diagram .....             | <b>10</b> | <b>14 Mechanical, Packaging, and Orderable Information</b> ..... | <b>25</b> |
| 9.3 Feature Description.....                   | <b>10</b> |  |           |

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (January 2014) to Revision E Page

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

### Changes from Revision C (October 2012) to Revision D Page

- Changed the FUNCTIONAL BLOCK DIAGRAM to include the SYNC pin ..... **10**
- Changed the Revision History list..... **22**

### Changes from Revision B (October 2012) to Revision C Page

- Changed ESD - HBM From: 4 kV To: 2 kV ..... **5**
- Deleted ESD - MM..... **5**
- Changed ESD - CDM From: 1.5 kV To: 500 V..... **5**
- Changed the CONSTANT-FREQUENCY MODE OF OPERATION (SYNC = HIGH) section ..... **13**

### Changes from Revision A (February 2009) to Revision B Page

- Changed Description text From: 2-cell Li-ion battery To: 2 to 4-cell Li-ion battery.. ..... **1**
- Added text to the Terminal Functions EN pin description - Do not leave floating..... **4**
- Added ESD information to the ABSOLUTE MAXIMUM RATINGS table ..... **5**
- Changed From: Dissipation Ratings table To: Thermal Information table ..... **5**
- Added TPS62113 to the OUTPUT section of the Electrical Characteristics ..... **7**
- Changed Note A of the Functional Block Diagram..... **10**
- Changed the ENABLE section ..... **10**
- Changed the LOW-BATTERY DETECTOR (Standard Version) section ..... **11**

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|   |    |
|---|----|
| • Deleted the PwPD pin from <a href="#">Figure 4</a> , .....  | 11 |
| • Changed the ENABLE/Low-Battery Detector (Enhanced Version) TPS62113 Only section .....            | 11 |
| • Changed the POWER-GOOD COMPARATOR section .....   | 11 |
| • Added the THERMAL SHUTDOWN section .....  | 12 |
| • Changed the SOFT START section .....  | 12 |
| • Deleted "by pulling the SYNC pin LOW." - CONSTANT-FREQUENCY MODE OF OPERATION (SYNC = HIGH) ..... | 13 |
| • Changed .....   | 13 |
| • Changed PwPD to ETPad in <a href="#">Figure 6</a> to <a href="#">Figure 21</a> .....              | 15 |
| • Changed the INPUT-CAPACITOR SELECTION section .....   | 18 |
| • Changed <a href="#">Figure 19</a> and <a href="#">Figure 20</a> .....                             | 21 |
| • Added section: Layout Consideration .....   | 23 |

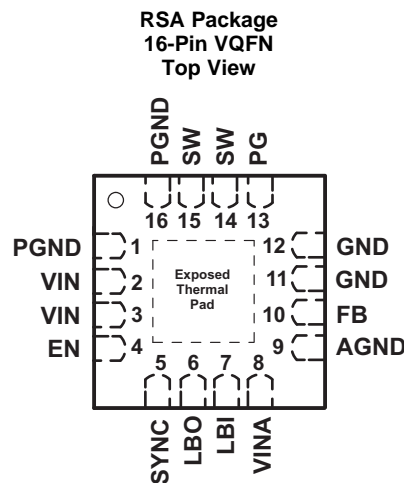
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## 6 Device Comparison Table

| PACKAGED DEVICES<br>PLASTIC VQFN 16 PIN <sup>(1)</sup> (RSA) | OUTPUT VOLTAGE           | LBI/LBO<br>FUNCTIONALITY |
|--|--------------------------|--------------------------|
| TPS62110   | Adjustable 1.2 V to 16 V | Standard                 |
| TPS62111   | Fixed 3.3 V              | Standard                 |
| TPS62112   | Fixed 5 V                | Standard                 |
| TPS62113   | Adjustable 1.2 V to 16 V | Enhanced                 |

(1) The RSA package is available in tape and reel. Add R suffix (TPS62110RSAR) to order quantities of 3000 parts per reel. Add T suffix (TPS62110RSAT) to order quantities of 250 parts per reel.

## 7 Pin Configuration and Functions



**Pin Functions**

| PIN  |        | I/O | DESCRIPTION  |
|------|--------|-----|--|
| NAME | NO.    |     |  |
| AGND | 9      | I   | Analog ground, connect to GND and PGND.  |
| EN   | 4      | I   | Enable. A logic high enables the converter; logic low forces the device into shutdown mode reducing the supply current to less than 2 $\mu$ A. Do not leave floating.  |
| FB   | 10     | I   | Feedback pin for the fixed output voltage versions. Connect to $V_{OUT}$ for these devices. For the adjustable versions, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable versions.                         |
| GND  | 11, 12 | I   | Ground   |
| LBI  | 7      | I   | Low-battery input. Do not leave floating.  |
| LBO  | 6      | O   | Open-drain, low-battery output. This pin is pulled low if LBI is below its threshold. If not used, the pin may be left floating or connected to GND.   |
| PG   | 13     | O   | Power good comparator output. This is an open-drain output. A pullup resistor should be connected between PG and VOUT. The output goes high when the output voltage is greater than 98.4% of the nominal value. If not used, the pin may be left floating or connected to GND. |
| PGND | 1, 16  | I   | Power ground. Connect all power grounds to this pin.   |
| SW   | 14, 15 | O   | Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.   |
| SYNC | 5      | I   | Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level. Also controls power save mode by being tied high or low.   |
|      |        |     | SYNC = HIGH: Low-noise mode enabled, fixed-frequency PWM operation is forced   |
|      |        |     | SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled  |
| VIN  | 2, 3   | I   | Supply voltage input (power stage)   |

### Pin Functions (continued)

| PIN                 |     | I/O | DESCRIPTION  |
|---------------------|-----|-----|--|
| NAME                | NO. |     |  |
| VINA                | 8   | I   | Supply voltage input (support circuits)  |
| Exposed Thermal Pad | –   | –   | Connect to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability. |

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |                                | MIN  | MAX  | UNIT |
|------------------|--------------------------------|------|------|------|
| V <sub>CC</sub>  | Supply voltage at VIN, VINA    | –0.3 | 20   | V    |
| V <sub>I</sub>   | Voltage at SW                  | –1   | 20   | V    |
|                  | Voltage at EN, SYNC, LBO, PG   | –0.3 | 20   |      |
|                  | Voltage at LBI, FB             | –0.3 | 7    |      |
| I <sub>O</sub>   | Output current at SW           |      | 2400 | mA   |
| T <sub>J</sub>   | Maximum junction temperature   |      | 150  | °C   |
| T <sub>A</sub>   | Operating free-air temperature | –40  | 85   | °C   |
| T <sub>stg</sub> | Storage temperature            | –65  | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 8.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

|                 |                                      | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------------|-----|-----|-----|------|
| V <sub>CC</sub> | Supply voltage at VIN, VINA          | 3.1 |     | 17  | V    |
|                 | Maximum voltage at PG, LBO, EN, SYNC |     |     | 17  | V    |
| T <sub>J</sub>  | Operating junction temperature       | –40 |     | 125 | °C   |

### 8.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS6211x   | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RSA (VQFN) |      |
|                               |  | 16 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 48.2       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 45.4       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 16.3       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 16.4       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 3.3        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 8.5 Electrical Characteristics

 $V_I = 12\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $I_O = 600\text{ mA}$ ,  $EN = V_I$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

| PARAMETER            |   | TEST CONDITIONS   | MIN  | TYP                   | MAX  | UNIT |
|----------------------|---|---|------|-----------------------|------|------|
| SUPPLY CURRENT       |   |   |      |                       |      |      |
| V <sub>I</sub>       | Input voltage   |   | 3.1  |                       | 17   | V    |
| I <sub>(Q)</sub>     | Operating quiescent current   | I <sub>O</sub> = 0 mA, SYNC = GND, V <sub>I</sub> = 7.2 V, T <sub>A</sub> = 25°C <sup>(1)</sup> |      | 20                    |      | μA   |
|                      |   | I <sub>O</sub> = 0 mA, SYNC = GND, V <sub>I</sub> = 17 V <sup>(1)</sup>                         |      | 23                    | 26   |      |
| I <sub>Q(LBI)</sub>  | Quiescent current with enhanced LBI comparator version (TPS62113 only). | EN = V <sub>I</sub> , LBI = GND   |      | 10                    |      | μA   |
| I <sub>(SD)</sub>    | Shutdown current  | EN = GND  |      | 1.5                   | 5    | μA   |
|                      |   | EN = GND, T <sub>A</sub> = 25°C, V <sub>I</sub> = 7.2 V   |      | 1.5                   | 3    |      |
| ENABLE               |   |   |      |                       |      |      |
| V <sub>IH</sub>      | EN high-level input voltage   |   | 1.3  |                       |      | V    |
| V <sub>IL</sub>      | EN low-level input voltage  |   |      |                       | 0.3  | V    |
|                      | EN trip-point hysteresis  |   |      | 170                   |      | mV   |
| I <sub>lkg</sub>     | EN input leakage current  | EN = GND or V <sub>I</sub> , V <sub>I</sub> = 12 V  |      | 0.01                  | 0.2  | μA   |
| I <sub>(EN)</sub>    | EN input current  | 0.6 V ≤ V <sub>(EN)</sub> ≤ 4 V   |      | 10                    | 20   | μA   |
| V <sub>(UVLO)</sub>  | Undervoltage lockout threshold  | Input voltage falling   | 2.8  | 3                     | 3.1  | V    |
|                      | Undervoltage lockout hysteresis   |   |      | 250                   | 300  | mV   |
| POWER SWITCH         |   |   |      |                       |      |      |
| R <sub>DS(ON)</sub>  | P-channel MOSFET ON-resistance  | V <sub>I</sub> ≥ 5.4 V; I <sub>O</sub> = 350 mA   |      | 165                   | 250  | mΩ   |
|                      |   | V <sub>I</sub> = 3.5 V; I <sub>O</sub> = 200 mA   |      | 340                   |      |      |
|                      |   | V <sub>I</sub> = 3 V; I <sub>O</sub> = 100 mA   |      | 490                   |      |      |
| I <sub>lkg</sub>     | P-channel MOSFET leakage current  | V <sub>DS</sub> = 17 V  |      | 0.1                   | 1    | μA   |
| I <sub>LIMF</sub>    | P-channel MOSFET current limit  | V <sub>I</sub> = 7.2 V, V <sub>O</sub> = 3.3 V  | 2100 | 2400                  | 2600 | mA   |
| R <sub>DS(ON)</sub>  | N-channel MOSFET ON-resistance  | V <sub>I</sub> ≥ 5.4 V; I <sub>O</sub> = 350 mA   |      | 145                   | 200  | mΩ   |
|                      |   | V <sub>I</sub> = 3.5 V; I <sub>O</sub> = 200 mA   |      | 170                   |      |      |
|                      |   | V <sub>I</sub> = 3 V; I <sub>O</sub> = 100 mA   |      | 200                   |      |      |
| I <sub>lkg</sub>     | N-channel MOSFET leakage current  | V <sub>DS</sub> = 17 V  |      | 0.1                   | 2    | μA   |
| PG OUTPUT, LBI, LBO  |   |   |      |                       |      |      |
| V <sub>(PG)</sub>    | Power good trip voltage   |   |      | V <sub>O</sub> – 1.6% |      | V    |
|                      | Power good delay time   | V <sub>O</sub> ramping positive   |      | 50                    |      | μs   |
|                      |   | V <sub>O</sub> ramping negative   |      | 200                   |      |      |
| V <sub>OL</sub>      | PG, LBO output-low voltage  | V <sub>(FB)</sub> = 0.8 × V <sub>O</sub> nominal, I <sub>OL</sub> = 1 mA                        |      |                       | 0.3  | V    |
| I <sub>OL</sub>      | PG, LBO sink current  |   |      | 1                     |      | mA   |
| I <sub>lkg</sub>     | PG, LBO output leakage current  | V <sub>(FB)</sub> = V <sub>O</sub> nominal, V <sub>(LBI)</sub> = V <sub>I</sub>                 |      | 0.01                  | 0.25 | μA   |
|                      | Minimum supply voltage for valid power good, LBI, LBO signal            |   |      | 3                     |      | V    |
| V <sub>LBI</sub>     | LBI input trip voltage  | Input voltage falling   |      | 1.256                 |      | V    |
| I <sub>lkg</sub>     | LBI input leakage current   |   |      | 10                    | 100  | nA   |
|                      | LBI input trip-point accuracy   |   |      |                       | 1.5% |      |
| V <sub>LBI,HYS</sub> | Low-battery input hysteresis  |   |      | 25                    |      | mV   |

(1) Device is not switching.

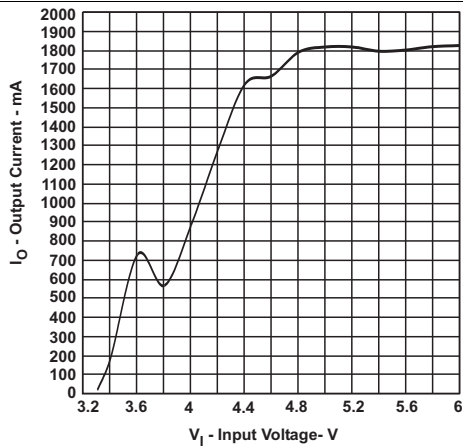
## Electrical Characteristics (continued)

 $V_I = 12\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $I_O = 600\text{ mA}$ ,  $EN = V_I$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

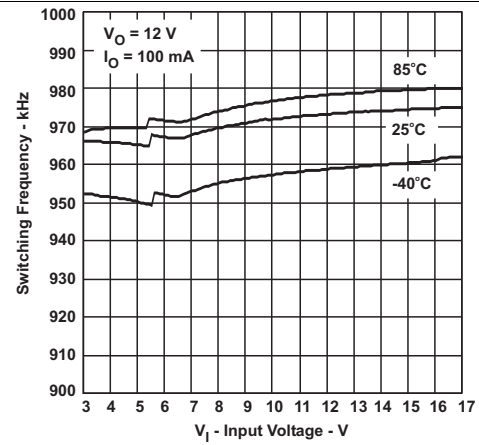
| PARAMETER           |   | TEST CONDITIONS   |   | MIN   | TYP   | MAX  | UNIT |
|---------------------|---|---|---|-------|-------|------|------|
| OSCILLATOR          |   |   |   |       |       |      |      |
| f <sub>S</sub>      | Oscillator frequency  |   |   | 900   | 1000  | 1100 | kHz  |
| f <sub>(SYNC)</sub> | Synchronization range   | CMOS-logic clock signal on SYNC pin                                     |   | 800   |       | 1400 | kHz  |
| V <sub>IH</sub>     | SYNC high-level input voltage                                       |   |   | 1.5   |       |      | V    |
| V <sub>IL</sub>     | SYNC low-level input voltage  |   |   |       |       | 0.3  | V    |
| I <sub>lkg</sub>    | SYNC input leakage current  | SYNC = GND or VIN   |   |       | 0.01  | 0.2  | μA   |
|                     | SYNC trip-point hysteresis  |   |   |       | 170   |      | mV   |
| I <sub>lkg</sub>    | SYNC input leakage current  | 0.6 V ≤ V <sub>(SYNC)</sub> ≤ 4 V                                       |   |       | 10    | 20   | μA   |
|                     | Duty cycle of external clock signal                                 |   |   | 30%   |       | 90%  |      |
| OUTPUT              |   |   |   |       |       |      |      |
| V <sub>O</sub>      | Adjustable output voltage range                                     | TPS62110<br>TPS62113  |   | 1.153 |       | 16   | V    |
| V <sub>FB</sub>     | Feedback voltage  | TPS62110<br>TPS62113  |   |       | 1.153 |      | V    |
| I <sub>lkg</sub>    | FB input leakage current  | TPS62110<br>TPS62113  |   |       | 10    | 100  | nA   |
|                     | Feedback voltage tolerance  | TPS62110<br>TPS62113  | V <sub>I</sub> = 3.1 V to 17 V;<br>0 mA < I <sub>O</sub> < 1500 mA <sup>(2)</sup> | −2%   |       | 2%   |      |
|                     | Fixed output voltage tolerance <sup>(3)</sup>                       | TPS62111  | V <sub>I</sub> = 3.8 V to 17 V;<br>0 mA < I <sub>O</sub> < 1500 mA <sup>(2)</sup> | −3%   |       | 3%   |      |
|                     |   | TPS62112  | V <sub>I</sub> = 5.5 V to 17 V;<br>0 mA < I <sub>O</sub> < 1500 mA <sup>(2)</sup> | −3%   |       | 3%   |      |
| I <sub>O</sub>      | Maximum output current  | V <sub>I</sub> ≥ 3 V (once undervoltage lockout<br>voltage exceeded)    |   |       | 100   |      | mA   |
|                     |   | V <sub>I</sub> ≥ 3.5 V  |   |       | 500   |      |      |
|                     |   | V <sub>I</sub> ≥ 4.3 V  |   |       | 1200  |      |      |
|                     |   | V <sub>I</sub> ≥ 6 V  |   |       | 1500  |      |      |
|                     | Current into internal voltage divider for<br>fixed voltage versions |   |   |       | 5     |      | μA   |
| η                   | Efficiency  | V <sub>I</sub> = 7.2 V; V <sub>O</sub> = 3.3 V; I <sub>O</sub> = 600 mA |   |       | 92%   |      |      |
|                     |   | V <sub>I</sub> = 12 V, V <sub>O</sub> = 5 V, I <sub>O</sub> = 600 mA    |   |       |       |      |      |
|                     | Duty-cycle range for main switches                                  | at 1 MHz  |   | 10%   |       | 100% |      |
|                     | Minimum t <sub>on</sub> time for main switch                        |   |   | 100   |       |      | ns   |
| T <sub>SD</sub>     | Shutdown temperature  |   |   |       | 145   |      | °C   |
|                     | Start-up time   | I <sub>O</sub> = 800 mA, V <sub>I</sub> = 12 V, V <sub>O</sub> = 3.3 V  |   |       | 1     |      | ms   |

- (2) The maximum output current depends on the input voltage. See the *maximum output current* for further restrictions on the minimum input voltage.
- (3) The output voltage accuracy includes line and load regulation over the full temperature range  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ . See [No-Load Operation](#).

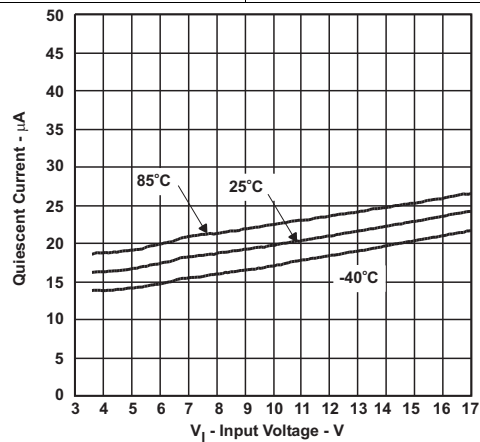
## 8.6 Typical Characteristics



**Figure 1. TPS62111 Maximum Output Current vs Input Voltage**



**Figure 2. Switching Frequency vs Input Voltage**



**Figure 3. Quiescent Current vs Input Voltage**



## 9 Detailed Description

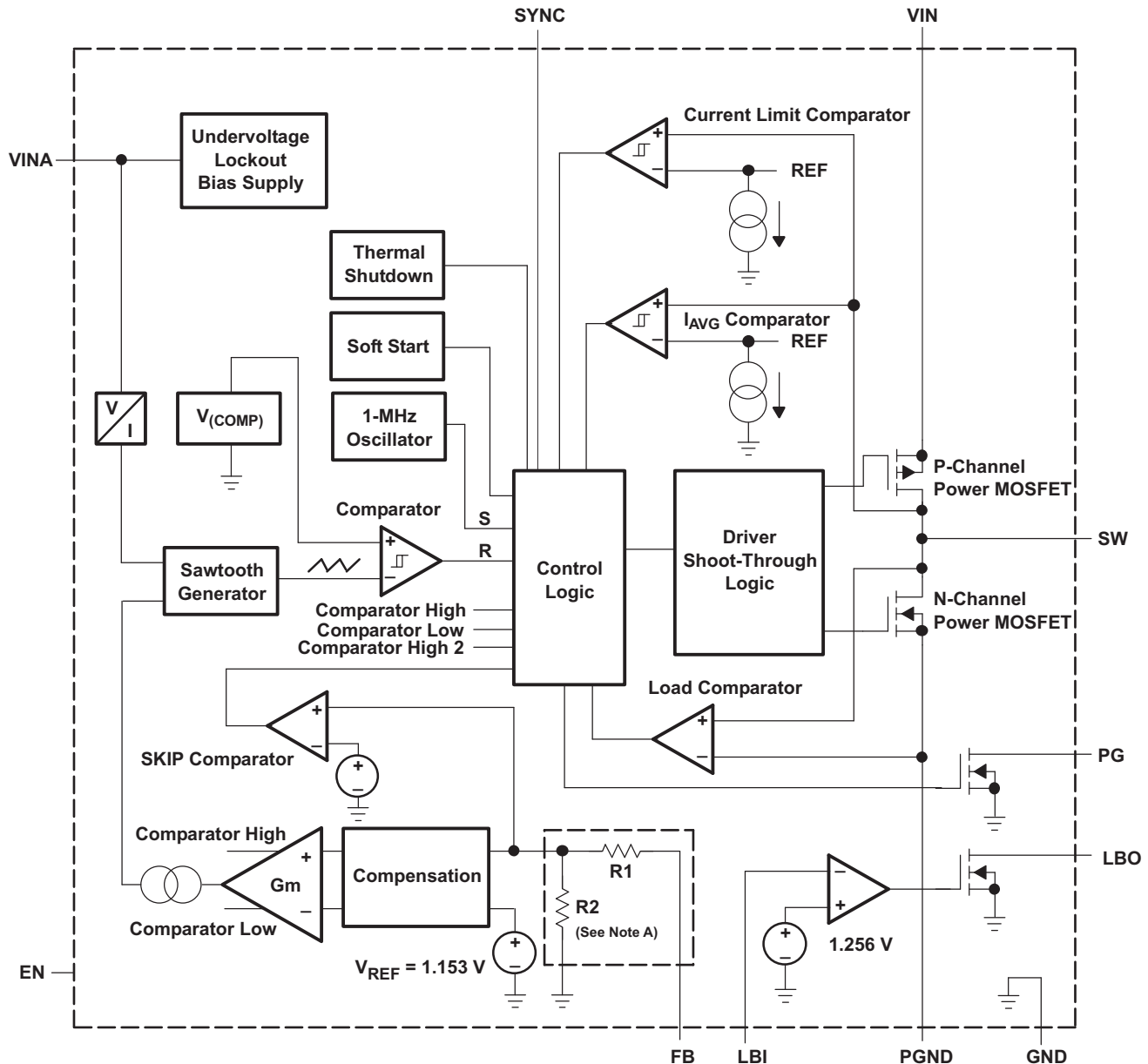
### 9.1 Overview

The TPS6211x family of devices are synchronous step-down converters that operate with a 1-MHz fixed-frequency pulse-width modulation (PWM) at moderate-to-heavy load currents, and enters the power-save mode at light load current.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input-voltage feedforward. Good line and load regulation is achieved with the use of small input and output ceramic capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns the switch off. The switch is turned off by the current limit comparator if the current limit of the P-channel switch is exceeded. After the dead time prevents current shoot through, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the P-channel switch.

The error amplifier as well as the input voltage determines the rise time of the sawtooth generator. Therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter, giving a very good line- and load-transient regulation.

## 9.2 Functional Block Diagram



For the adjustable version (TPS62110 and TPS62113), the internal feedback divider is disabled and the FB pin is directly connected to the internal compensation block.

## 9.3 Feature Description

### 9.3.1 Enable

A logic low on EN forces the TPS6211x devices into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The LBO pin is high impedance, while PG is held low. The supply current is reduced to less than 2  $\mu\text{A}$  in the shutdown mode. When the device is in thermal shutdown, the band gap is forced to be switched on even if the device is set into shutdown by pulling EN to GND.

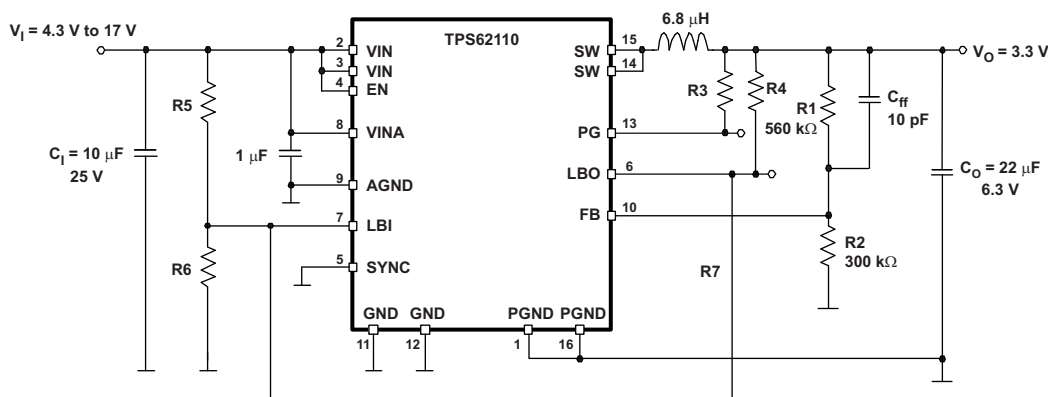
## Feature Description (continued)

If an output voltage is present when the device is disabled, which could be due to an external voltage source or a super capacitor, the reverse leakage current is specified under electrical characteristics. Pulling the enable pin high starts up the TPS6211x devices with the soft-start. If the EN pin is connected to any voltage other than  $V_I$  or GND, an increased leakage current of typically 10  $\mu\text{A}$  and up to 20  $\mu\text{A}$  can occur. See *TPS6211x Driving EN and SYNC Pins* (SLVA295) for details.

### 9.3.2 Low-Battery Detector (Standard Version)

The low-battery output (LBO) is an open-drain type which goes low when the voltage at the low-battery input (LBI) falls below the trip point of  $1.256\text{ V} \pm 1.5\%$ . The voltage at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 4. TI recommends the sum of resistors  $R_1 + R_2$  as well as the sum of resistors  $R_5 + R_6$  to be in the 100-k $\Omega$  to 1-M $\Omega$  range for high efficiency at low output current. An external pullup resistor can be connected to  $V_O$ , or any other voltage rail in the voltage range of 0 V to 17 V. During start-up, the LBO output signal is invalid for the first 500  $\mu\text{s}$ . LBO is high-impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground. The low-battery detector is disabled when the device is disabled.

When the LBI is used to supervise the battery voltage and shut down the TPS6211x devices at low-input voltages, the battery voltage rises when its current drops to zero. The implemented hysteresis on the LBI pin may not be sufficient for all types of batteries. Figure 4 shows how an additional external hysteresis can be implemented. See *Adding Hysteresis to Low-Battery Input on the TPS62113* (SLVA373) for details.



**Figure 4. LBI With Increased Hysteresis**

### 9.3.3 Enable/Low-Battery Detector - Enhanced Version (TPS62113 Only)

The TPS62113 device offers an enhanced LBI functionality to provide a precise, user-programmable undervoltage shutdown. No additional supply voltage supervisor (SVS) is needed to provide this function. When the enable (EN) pin is pulled high, only the internal bandgap voltage reference is switched on to provide a reference source for the LBI comparator. As long as the voltage at LBI is less than the LBI trip point, all other internal circuits are shut down, reducing the supply current to 10  $\mu\text{A}$ . As soon as input voltage at LBI rises above the LBI trip point of 1.256 V, the device is completely enabled and starts switching.

This functionality is the only difference between the TPS62110 and TPS62113 devices.

### 9.3.4 Power Good Comparator

The power good (PG) comparator is an open-drain output capable of sinking 1 mA (typical). The PG is only active when the device is enabled (EN = high). When the device is disabled (EN = low), the PG pin is pulled to GND.

The PG output is only valid after a 250- $\mu\text{s}$  delay when the device is enabled and the supply voltage is greater than the undervoltage lockout  $V_{(UVLO)}$ .

The PG pin becomes active-high when the output voltage exceeds 98.4% (typical) of its nominal value. Leave the PG pin floating or grounded when not used.

## **Feature Description (continued)**

### **9.3.5 Undervoltage Lockout**

The undervoltage lockout (UVLO) circuit prevents the device from misoperation at low-input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The minimum input voltage to start up the TPS6211x devices is 3.4 V (worst case). The device shuts down at 2.8 V minimum.

### **9.3.6 Synchronization**

If no clock signal is applied, the converter operates with a typical switching frequency of 1 MHz. It is possible to synchronize the converter to an external clock within a frequency range from 0.8 MHz to 1.4 MHz only. The device automatically detects the rising edge of the first clock and synchronizes immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation. The switch over is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 6.25  $\mu$ s if the internal clock has its minimum frequency of 800 kHz.

If the device is synchronized to an external clock, the power save mode is disabled, and the devices stay in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power save mode. The converter operates in the PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

### **9.3.7 Thermal Shutdown**

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds 145°C typical, the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When  $T_J$  decreases by typically 10°C, the converter resumes normal operation.

## **9.4 Device Functional Modes**

### **9.4.1 Soft Start**

The TPS6211x has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage when a battery or a high-impedance power source is connected to the input of the TPS6211x devices.

The soft start is implemented as a digital circuit increasing the switch current in steps of 300 mA, 600 mA, and 1200 mA for 250  $\mu$ s each. Then, the switch current limit is set to 2.4 A typical. Therefore, the start-up time depends on the output capacitor and load current. Typical start-up time with a 22- $\mu$ F output capacitor and 800-mA load current is 1 ms.

The TPS6211x devices can start into a prebiased output. During monotonic prebiased start-up, the N-channel MOSFET is not allowed to turn on until the internal ramp of the device sets an output voltage greater than the prebias voltage.

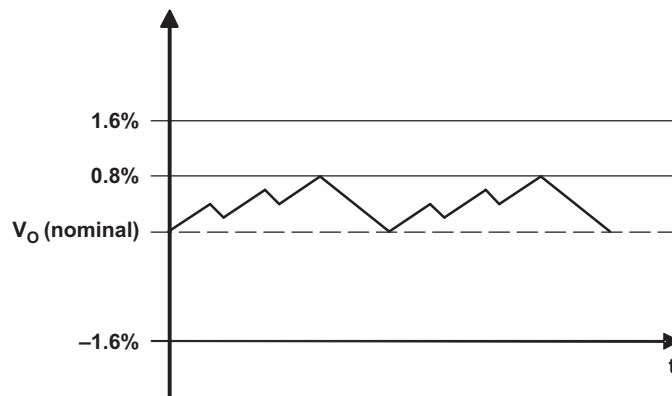
### **9.4.2 Constant-Frequency Mode of Operation (Sync = High)**

In constant-frequency mode, the output voltage is regulated by varying the duty cycle of the PWM signal in the range of 100% to 10%. Connecting the SYNC pin to a voltage greater than 1.5 V forces the converter to operate permanently in the PWM mode even at light- or no-load currents. The advantage is that the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. The N-MOSFET of the devices stays on even when the current into the output drops to zero. This prevents the device from going into discontinuous mode, and the device transfers unused energy back to the input. Therefore, there is no ringing at the output, which usually occurs in discontinuous mode. The duty cycle range in constant-frequency mode is 100% to 10%.

## Device Functional Modes (continued)

### 9.4.3 Power Save Mode of Operation (Sync = Low)

As the load current decreases, the converter enters the power-save mode of operation. During power-save mode, the converter operates with reduced switching frequency in pulse-frequency modulation (PFM), and with a minimum quiescent current to maintain high efficiency. Whenever the average output current goes below the skip threshold, the converter enters the power-save mode. The average current depends on the input voltage. It is about 200 mA at low input voltages and up to 400 mA with maximum input voltage. The average output current must be less than the threshold for at least 32 clock cycles to enter the power-save mode. During the power-save mode, the output voltage is monitored with a comparator, and the output voltage is regulated to a typical value between the nominal output voltage and 0.8% above the nominal output voltage. When the output voltage falls below the nominal output voltage, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The N-channel rectifier is turned on, and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the switch is turned on starting the next pulse. When the output voltage cannot be reached with a single pulse, the device continues to switch with its normal operating frequency until the comparator detects the output voltage to be 0.8% above the nominal output voltage. This control method reduces the quiescent current to 20  $\mu$ A (typical), and reduces the switching frequency to a minimum that achieves the highest converter efficiency. Figure 5 shows the typical power save mode operation.



**Figure 5. Power Save Mode Output-Voltage Thresholds**

Use Equation 1 the typical PFM (SKIP) current threshold for the TPS6211x devices.

$$I_{\text{SKIP}} \approx \frac{V_I}{25 \Omega} \quad (1)$$

Equation 1 is valid for input voltages up to 7 V. For higher voltages, the skip current threshold is not increased further. The converter enters the fixed-frequency PWM mode as soon as the output voltage falls below  $V_O - 1.6\%$  (nominal).

### 9.4.4 100% Duty-Cycle, Low-Dropout Operation

The TPS6211x devices offer the lowest possible input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time, taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and is calculated using Equation 2.

$$V_I(\text{min}) = V_O(\text{max}) + I_O(\text{max}) \times (R_{\text{DS(ON)}}(\text{max}) + R_L)$$

$I_O(\text{max})$  = Maximum output current plus inductor ripple current

$R_{\text{DS(ON)}}(\text{max})$  = Maximum P-Channel switch resistance

$R_L$  = DC resistance of the inductor

$V_O(\text{max})$  = Nominal output voltage plus maximum output voltage tolerance (2)

## Device Functional Modes (continued)

### 9.4.5 No-Load Operation

When the converter operates in the forced PWM mode and there is no load connected to the output, the converter regulates the output voltage by allowing the inductor current to reverse for a short time.

## 10 Application and Implementation

### NOTE

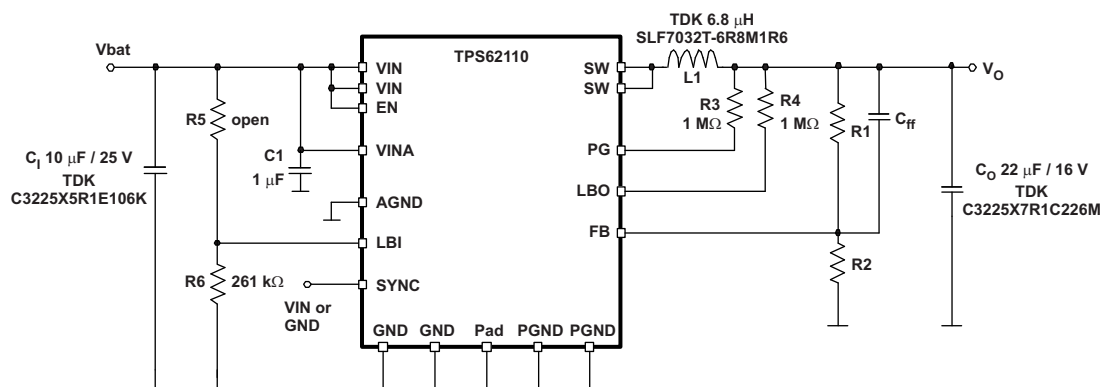
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TPS6211x devices are a family of low-noise synchronous step-down DC-DC converters that are ideally suited for systems powered from a 2- to 4-cell Li-ion battery or from a 12-V or 15-V rail.

### 10.2 Typical Applications

#### 10.2.1 Standard Connection for Adjustable Version



For an output voltage lower than 2.5 V, TI recommends an output capacitor of 33 µF or greater to improve load transient performance.

**Figure 6. Standard Connection for Adjustable Version**

#### 10.2.1.1 Design Requirements

The design guidelines provide a component selection to operate the device within the *Recommended Operating Conditions*.

**Table 1. Bill of Materials for the Adjustable Version**

| REFERENCE | PART NUMBER                               | VALUE  | MANUFACTURER      |
|-----------|---|--|-------------------|
| Ci        | C3225X5R1E106K                            | 10 µF  | TDK               |
| Co        | C3225X7R1C226M                            | 22 µF  | TDK               |
| L1        | SLF7032T-6R8M1R6                          | 6.8 µH                                       | TDK               |
| C1        | TMK212B7105KG-T                           | 1 µF   | Taiyo Yuden       |
| IC1       | TPS62110                                  | -  | Texas Instruments |
| R1        | generic metal film resistor; tolerance 1% | 220 kΩ (depending on desired output voltage) | —                 |
| R2        | generic metal film resistor; tolerance 1% | 390 kΩ (depending on desired output voltage) | —                 |
| R3, R4    | generic metal film resistor; tolerance 1% | 1 MΩ   | —                 |
| R5        | generic metal film resistor; tolerance 1% | open   | —                 |
| R6        | generic metal film resistor; tolerance 1% | 261 kΩ                                       | —                 |

## Typical Applications (continued)

**Table 1. Bill of Materials for the Adjustable Version (continued)**

| REFERENCE | PART NUMBER                    | VALUE                               | MANUFACTURER |
|-----------|--------------------------------|-------------------------------------|--------------|
| C(ff)     | generic ceramic capacitor; COG | 10 pF (depending on output voltage) | —            |

### 10.2.1.2 Detailed Design Procedure

The graphs were generated using the EVM with the setup according to [Figure 6](#), unless otherwise noted. Graphs for an output voltage of 1.5 V and 1.8 V were generated using the TPS62110 device with the output voltage dividers adjusted according to [Table 2](#).

$$V_O = V_{FB} \times \frac{R1+R2}{R2} \quad R1 = R2 \times \left( \frac{V_O}{V_{FB}} \right) - R2$$

$$V_{FB} = 1.153 \text{ V} \quad (3)$$

**Table 2. Recommended Resistors**

| OUTPUT VOLTAGE | R1     | R2     | NOMINAL VOLTAGE | TYPICAL C <sub>ff</sub> |
|----------------|--------|--------|-----------------|-------------------------|
| 9 V            | 680 kΩ | 100 kΩ | 8.993 V         | 22 pF                   |
| 5 V            | 510 kΩ | 150 kΩ | 5.073 V         | 10 pF                   |
| 3.3 V          | 560 kΩ | 300 kΩ | 3.305 V         | 10 pF                   |
| 2.5 V          | 390 kΩ | 330 kΩ | 2.515 V         | 10 pF                   |
| 1.8 V          | 220 kΩ | 390 kΩ | 1.803 V         | 10 pF                   |
| 1.5 V          | 100 kΩ | 330 kΩ | 1.502 V         | 10 pF                   |

### 10.2.1.2.1 External Component Selection

The control loop of the TPS6211x family of devices requires a certain value for the output inductor and the output capacitor for stable operation. As long as the nominal value of  $L \times C \geq 6.2 \mu\text{H} \times 22 \mu\text{F}$ , the control loop has enough phase margin and the device is stable. Reducing the inductor value without increasing the output capacitor (or vice versa) may cause stability problems. There are applications where it may be useful to increase the value of the output capacitor, and so on, for a low-transient output-voltage change. From a stability point of view, the inductor value could be decreased to keep the  $L \times C$  product constant. However, there are drawbacks if the inductor value is decreased. A low inductor value causes a high inductor ripple current, and therefore reduces the maximum DC output current. [Table 3](#) gives the advantages and disadvantages when designing the inductor and output capacitor.

**Table 3. Advantages and Disadvantages When Designing the Inductor and Output Capacitor**

|                                    | INFLUENCE ON STABILITY                           | ADVANTAGE  | DISADVANTAGE   |
|------------------------------------|--|--|--|
| Increase C <sub>out</sub> (>22 μF) | Uncritical                                       | Less output voltage ripple<br>Less output voltage overshoot / undershoot during load transient           | None   |
| Decrease C <sub>out</sub> (<22 μF) | Critical<br>Increase inductor value >6.8 μH also | None   | Higher-output voltage ripple<br>High-output voltage overshoot / undershoot during load transient<br>Less gain and phase margin   |
| Increase L (>6.8 μH)               | Uncritical                                       | Less inductor current ripple<br>Higher DC output current possible if operated close to the current limit | More energy stored in the inductor → higher voltage overshoot during load transient<br>Smaller current rise → higher voltage undershoot during load transient → do not decrease the value of C <sub>out</sub> due to these effects |



**Table 3. Advantages and Disadvantages When Designing the Inductor and Output Capacitor (continued)**

|                      | INFLUENCE ON STABILITY                                   | ADVANTAGE  | DISADVANTAGE   |
|----------------------|--|--|--|
| Decrease L (<6.8 µH) | Critical<br>Increase output capacitor value > 22 µF also | Small voltage overshoot and undershoot during load transient | High inductor current ripple especially at high input voltage and low output voltage |

#### 10.2.1.2.2 Inductor Selection

As shown in [Table 3](#), the inductor value can be increased to greater values. For good performance, the peak-to-peak inductor-current ripple should be less than 30% of the maximum DC output current. Especially at input voltages greater than 12 V, it makes sense to increase the inductor value to keep the inductor-current ripple low. In such applications, the inductor value can be increased to 10 µH or 22 µH. Values greater than 22 µH should be avoided to keep the voltage overshoot during load transient in an acceptable range.

After choosing the inductor value, two additional inductor parameters should be considered:

- Current rating of the inductor
- DC resistance

The DC resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency. To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated using [Equation 4](#).

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \quad I_L \text{ max} = I_O \text{ max} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (1000 kHz typical)
- L = Inductor value
- $\Delta I_L$  = Peak-to-peak inductor ripple current
- $I_L(\text{max})$  = Maximum inductor current

(4)

The highest inductor current occurs at maximum  $V_I$ . A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS6211x, which is 2.4 A (typically). See [Table 4](#) for recommended inductors.

**Table 4. List of Inductors**

| MANUFACTURER | PART NO.         | INDUCTANCE | DC RESISTANCE   | SATURATION CURRENT |
|--------------|------------------|------------|-----------------|--------------------|
| Coilcraft    | MSS6132-682      | 6.8 µH     | 65 mΩ (maximum) | 1.5 A              |
|              | HA3808-AL        | 6.8 µH     | 99 mΩ (typical) | 4.4 A              |
| Epcos        | B82462G4682M     | 6.8 µH     | 50 mΩ (maximum) | 1.5 A              |
| Sumida       | CDRH5D28-6R2     | 6.2 µH     | 33 mΩ (typical) | 1.8 A              |
| TDK          | SLF6028T-6R8M1R5 | 6.8 µH     | 35 mΩ (typical) | 1.5 A              |
|              | SLF7032T-6R8M1R6 | 6.8 µH     | 41 mΩ (typical) | 1.6 A              |
| Würth        | 7447789006       | 6.8 µH     | 44 mΩ (typical) | 2.75 A             |
|              | 7447779006       | 6.8 µH     | 33 mΩ (typical) | 3.3 A              |
|              | 744053006        | 6.2 µH     | 45 mΩ (typical) | 1.8 A              |

#### 10.2.1.2.3 Output Capacitor Selection

A 22-µF (typical) output capacitor is needed with a 6.8-µH inductor. For an output voltage greater than 5 V, a 33-µF (minimum) output capacitor is required for stability. For best performance, a low-ESR ceramic output capacitor is needed.

The RMS ripple current is calculated using [Equation 5](#).

$$I_{RMS}(C_O) = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left( \frac{1}{8 \times C_O \times f} + R_{ESR} \right)$$

where

- the highest output voltage ripple occurs at the highest input voltage  $V_I$ .

#### 10.2.1.2.4 Input Capacitor Selection

The nature of the buck converter is a pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering and for minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10  $\mu\text{F}$  and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current and is calculated using [Equation 7](#).

$$I_{RMS} = I_O \max \times \sqrt{\frac{V_O}{V_I} \times \left( 1 - \frac{V_O}{V_I} \right)} \quad (7)$$

The worst-case RMS ripple current occurs at  $D = 0.5$  and is calculated as:  $I_{RMS} = I_O/2$ . Ceramic capacitors show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors. Place the input capacitor as close as possible to the VIN and PGND pins of the IC for best performance.

An additional 1- $\mu\text{F}$  input capacitor is required from VINA to AGND. VIN and VINA must be connected to the same source. TI does not recommend an RC filter from VIN to VINA.

#### 10.2.1.2.5 Feedforward Capacitor Selection

The feedforward capacitor ( $C_{ff}$ ) is needed to compensate for parasitic capacitance from the feedback pin to GND. Typically, a value of 4.7 pF to 22 pF is needed for an output voltage divider with a equivalent resistance ( $R_1$  in parallel with  $R_2$ ) in the 150-k $\Omega$  range. The value can be chosen based on best transient performance and lowest output voltage ripple in PFM mode.

#### 10.2.1.2.6 Recommended Capacitors

TI recommends using only X5R or X7R ceramic capacitors as input and output capacitors. Ceramic capacitors show a DC-bias effect. This effect reduces the effective capacitance when a DC-bias voltage is applied across a ceramic capacitor, as on the output and input capacitor of a DC-DC converter. The effect may lead to a significant capacitance drop, especially for high input and output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a DC bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value to get the required value at the operating point. The capacitors listed in [Table 5](#) have been tested with the TPS6211x devices with good performance.

**Table 5. List of Capacitors**

| MANUFACTURER | PART NUMBER     | SIZE | VOLTAGE | CAPACITANCE      | TYPE    |
|--------------|-----------------|------|---------|------------------|---------|
| Taiyo Yuden  | TMK316BJ106KL   | 1206 | 25 V    | 10 $\mu\text{F}$ | Ceramic |
|              | EMK325BJ226KM   | 1210 | 16 V    | 22 $\mu\text{F}$ |         |
| TDK          | C3225X5R1E106M  | 1210 | 25 V    | 10 $\mu\text{F}$ | Ceramic |
|              | C3225X7R1C226M  |      | 16 V    | 22 $\mu\text{F}$ |         |
|              | C3216X5R1E106MT | 1206 | 25 V    | 10 $\mu\text{F}$ |         |

### 10.2.1.3 Application Curves

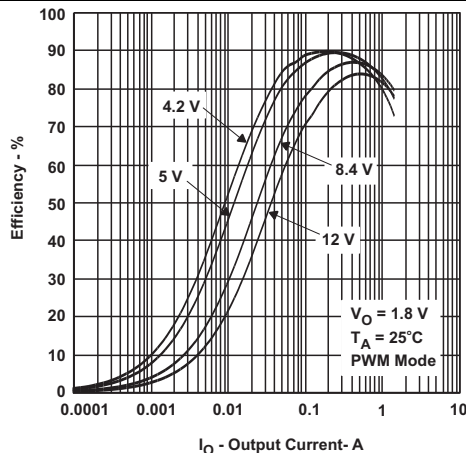


Figure 7. TPS62110 Efficiency vs Output Current

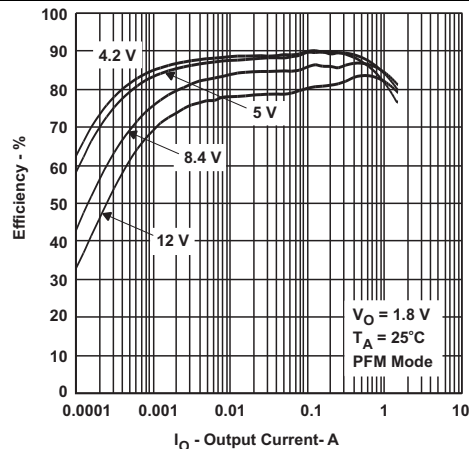


Figure 8. TPS62110 Efficiency vs Output Current

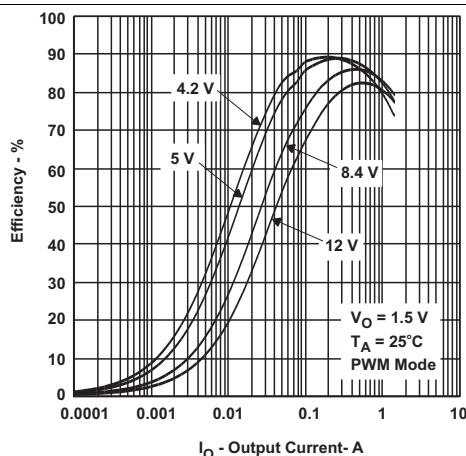


Figure 9. TPS62110 Efficiency vs Output Current

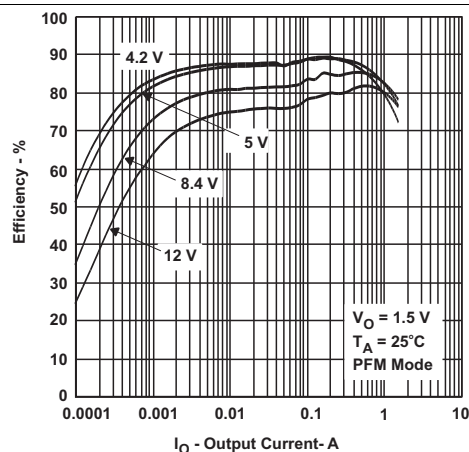


Figure 10. TPS62110 Efficiency vs Output Current

### 10.2.2 Standard Connection for Fixed-Voltage Version

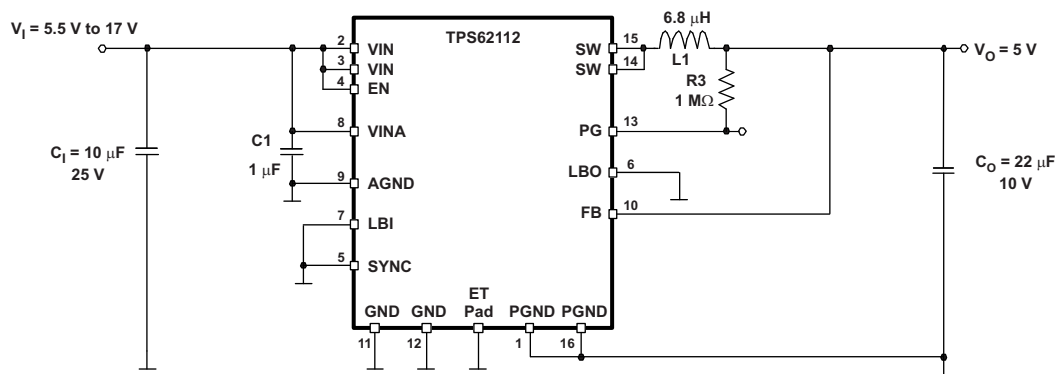


Figure 11. Standard Connection for Fixed-Voltage Version

#### 10.2.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the [Recommended Operating Conditions](#).

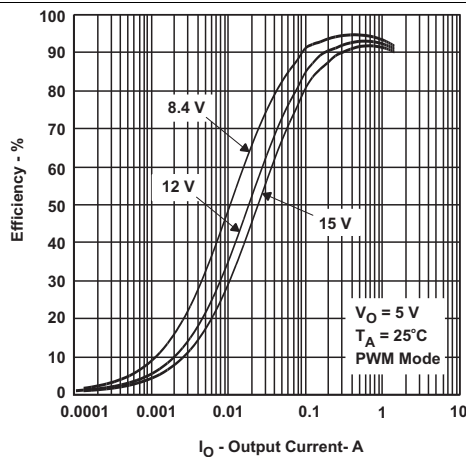
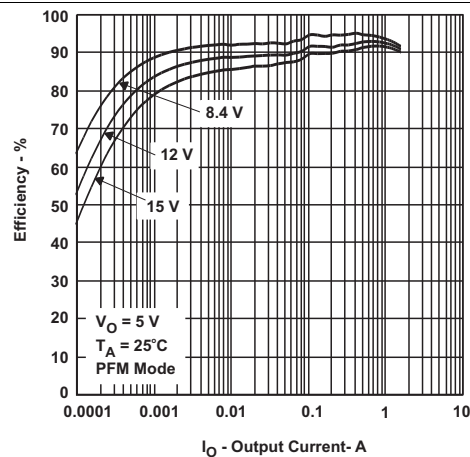
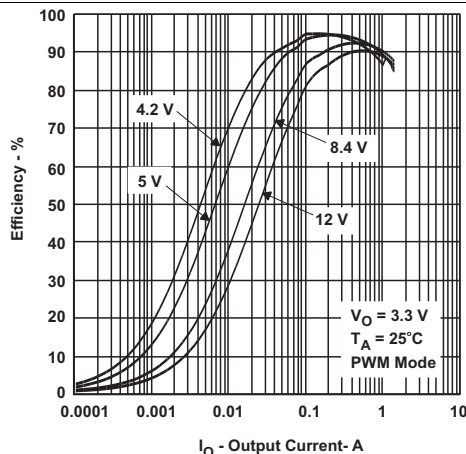
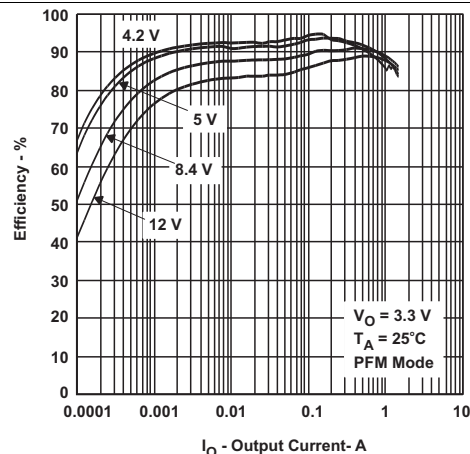
**Table 6. Bill of Materials for the Fixed Voltage Versions**

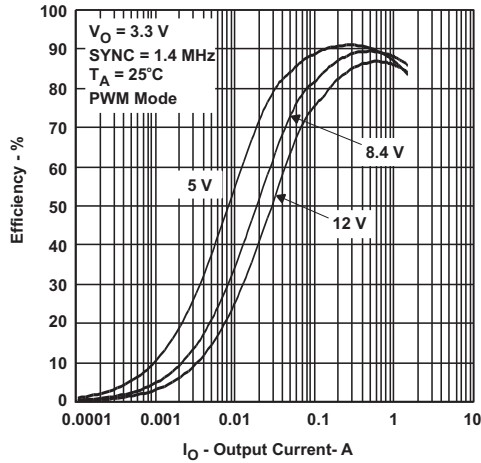
| REFERENCE | PART NUMBER                               | VALUE        | MANUFACTURER      |
|-----------|---|--------------|-------------------|
| Ci        | C3225X5R1E106K                            | 10 $\mu$ F   | TDK               |
| Co        | C3225X7R1C226M                            | 22 $\mu$ F   | TDK               |
| L1        | SLF7032T-6R8M1R6                          | 6.8 $\mu$ H  | TDK               |
| C1        | TMK212B7105KG-T                           | 1 $\mu$ F    | Taiyo Yuden       |
| IC1       | TPS62112                                  | —            | Texas Instruments |
| R3        | generic metal film resistor; tolerance 1% | 1 M $\Omega$ | —                 |

### 10.2.2.2 Detailed Design Procedure

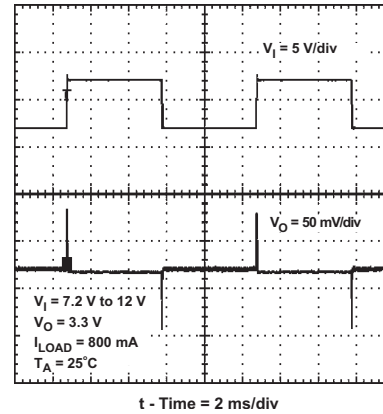
The graphs were generated using the EVM with the setup according to [Figure 6](#), unless otherwise noted. Graphs for an output voltage of 5 V and 3.3 V were generated using the TPS62111 and TPS62112 devices with R1 = 0  $\Omega$  and R2 = open.

### 10.2.2.3 Application Curves

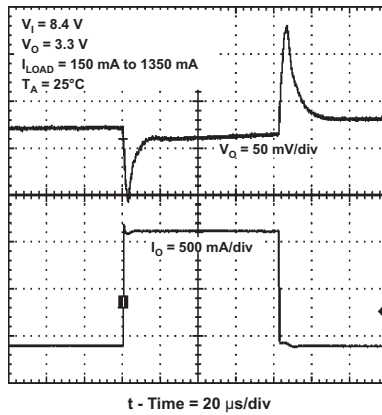

**Figure 12. TPS62112 Efficiency vs Output Current**

**Figure 13. TPS62112 Efficiency vs Output Current**

**Figure 14. TPS62111 Efficiency vs Output Current**

**Figure 15. TPS62111 Efficiency vs Output Current**



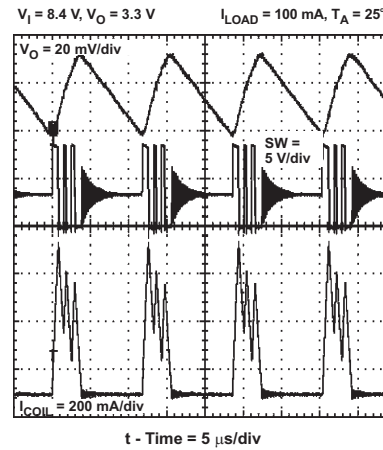
**Figure 16. TPS62111 Efficiency vs Output Current**



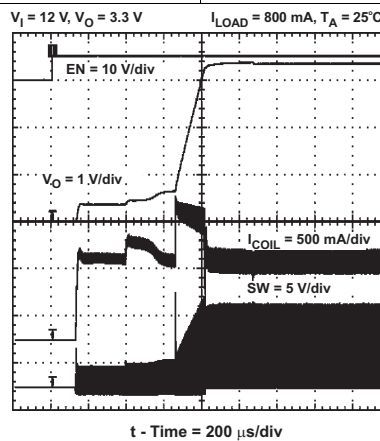
**Figure 17. TPS62111 Line Transient**



**Figure 18. TPS62111 Load Transient**



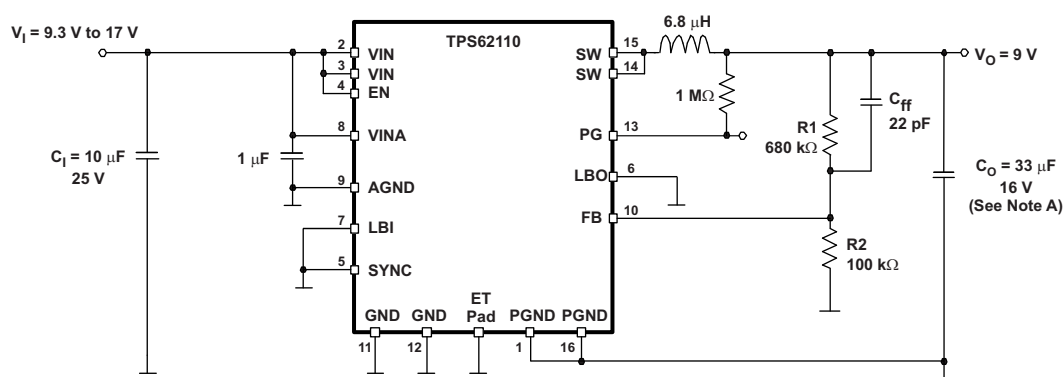
**Figure 19. TPS62111 Output Ripple**



**Figure 20. TPS62111 Start-up Timing**

### 10.3 System Examples

The TPS62110 device can be used within an adjustable output voltage range from 1.2 V to 16 V. [Figure 21](#) shows an application example with 9-V output.



- A. For an output voltage greater than 5 V, an output capacitor of 33 µF minimum is required for stability.

**Figure 21. Application With 9-V Output**

## 11 Power Supply Recommendations

The TPS6211x family of devices has no special requirements for its input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6211x devices.

## 12 Layout

### 12.1 Layout Guidelines

A proper layout is critical for the operation of a switched-mode power supply (SMPS), even more at high switching frequencies. Therefore, the PCB layout of the TPS6211x devices demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

Provide low inductive and resistive paths for loops with high  $di/dt$ . Therefore, paths conducting the switched load current should be as short and wide as possible. The input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Provide low capacitive paths (with respect to all other nodes) for wires with high  $dv/dt$ . Therefore, keep the SW node small. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and LBI need to be connected with short wires and not nearby high  $dv/dt$  signals (that is, SW). The FB resistors, R1 and R2, and LBI resistors, R5 and R6, should be kept close to the IC and connect directly to those pins and AGND. The 1- $\mu$ F capacitor on VINA should connect directly from VINA to AGND.

All grounds (GND, AGND, and PGND) are directly connected to the exposed thermal pad. The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

See [Figure 22](#) for the recommended layout of the TPS6211x.

## 12.2 Layout Example

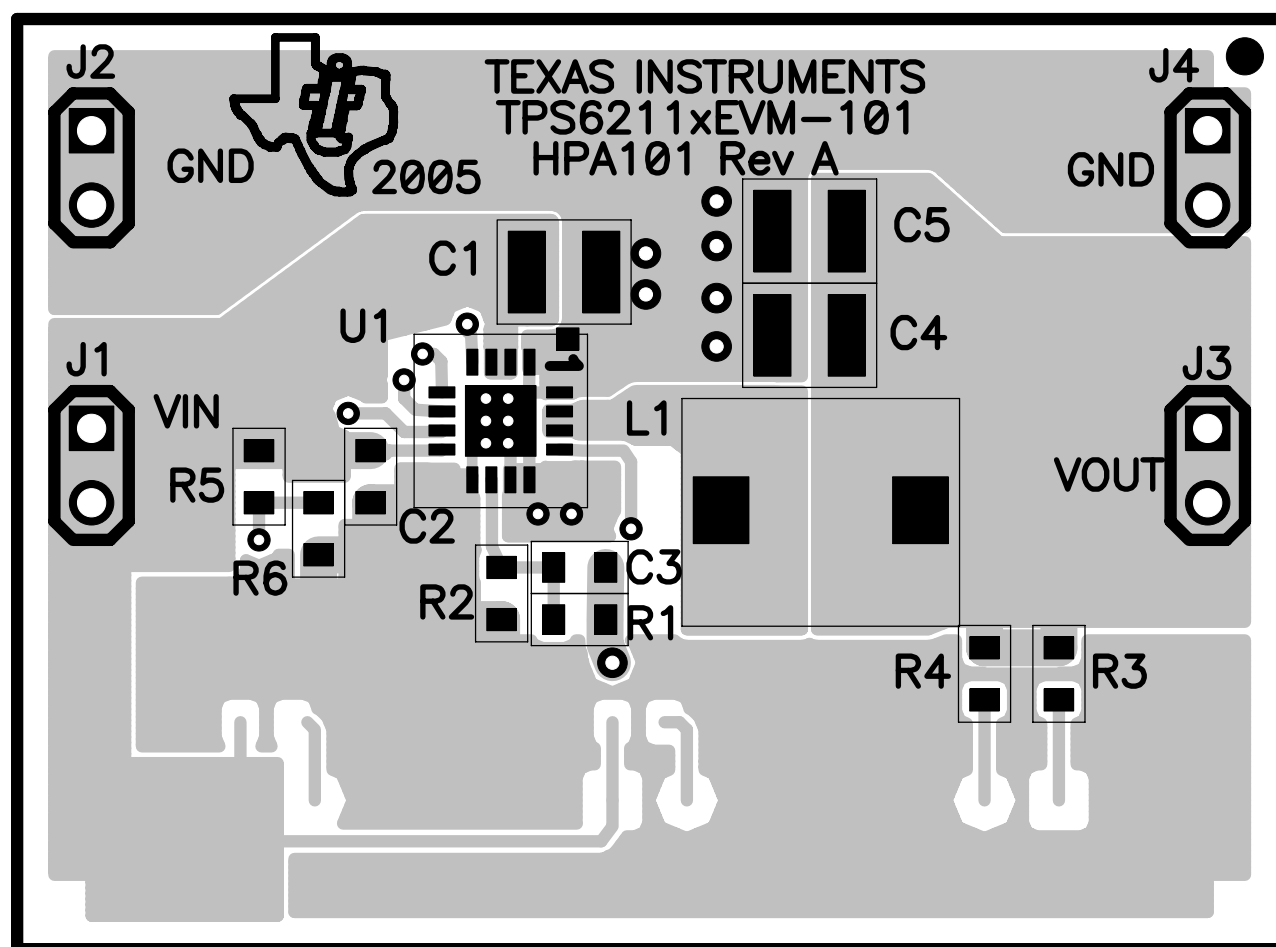


Figure 22. Recommended Layout



## 13 Device and Documentation Support

### 13.1 Device Support

*TPS6211x Driving EN and SYNC Pins*, [SLVA295](#)

*Adding Hysteresis to Low-Battery Input on the TPS62113*, [SLVA373](#)

#### 13.1.1 Third-Party Products Disclaimer

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### 13.2 Related Links

[Table 7](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 7. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS62110 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS62111 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS62112 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS62113 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS62110RSAR     | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62110            | <a href="#">Samples</a> |
| TPS62110RSARG4   | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62110            | <a href="#">Samples</a> |
| TPS62110RSAT     | ACTIVE        | QFN          | RSA             | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62110            | <a href="#">Samples</a> |
| TPS62110RSATG4   | ACTIVE        | QFN          | RSA             | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62110            | <a href="#">Samples</a> |
| TPS62111RSAR     | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62111            | <a href="#">Samples</a> |
| TPS62111RSARG4   | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62111            | <a href="#">Samples</a> |
| TPS62111RSAT     | ACTIVE        | QFN          | RSA             | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62111            | <a href="#">Samples</a> |
| TPS62112RSAR     | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62112            | <a href="#">Samples</a> |
| TPS62112RSARG4   | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62112            | <a href="#">Samples</a> |
| TPS62112RSAT     | ACTIVE        | QFN          | RSA             | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62112            | <a href="#">Samples</a> |
| TPS62113RSAR     | ACTIVE        | QFN          | RSA             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62113            | <a href="#">Samples</a> |
| TPS62113RSAT     | ACTIVE        | QFN          | RSA             | 16   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | TPS<br>62113            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS62110, TPS62111, TPS62112 :**

● Automotive : [TPS62110-Q1](#)

● Enhanced Product : [TPS62110-EP](#), [TPS62111-EP](#), [TPS62112-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62110RSAR | QFN          | RSA             | 16   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62110RSAT | QFN          | RSA             | 16   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62111RSAR | QFN          | RSA             | 16   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62111RSAT | QFN          | RSA             | 16   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62112RSAR | QFN          | RSA             | 16   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62112RSAT | QFN          | RSA             | 16   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62113RSAR | QFN          | RSA             | 16   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS62113RSAT | QFN          | RSA             | 16   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

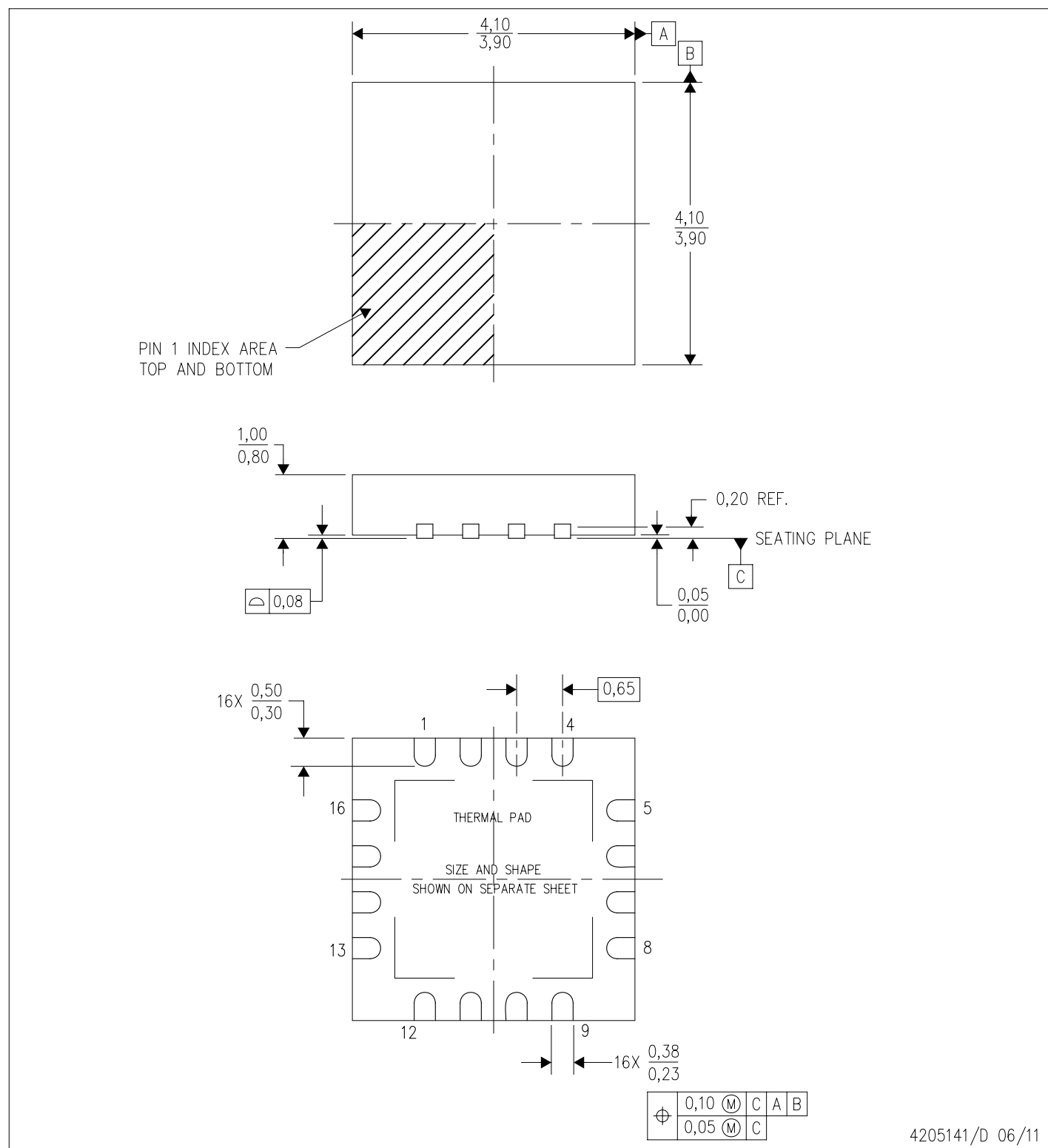


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62110RSAR | QFN          | RSA             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS62110RSAT | QFN          | RSA             | 16   | 250  | 210.0       | 185.0      | 35.0        |
| TPS62111RSAR | QFN          | RSA             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS62111RSAT | QFN          | RSA             | 16   | 250  | 210.0       | 185.0      | 35.0        |
| TPS62112RSAR | QFN          | RSA             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS62112RSAT | QFN          | RSA             | 16   | 250  | 210.0       | 185.0      | 35.0        |
| TPS62113RSAR | QFN          | RSA             | 16   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS62113RSAT | QFN          | RSA             | 16   | 250  | 210.0       | 185.0      | 35.0        |

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

RSA (S-PVQFN-N16)

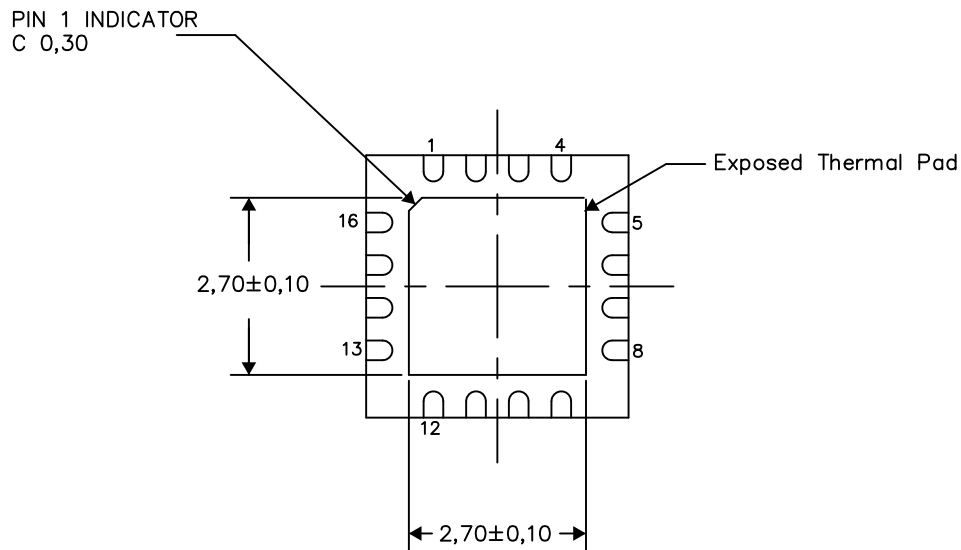
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

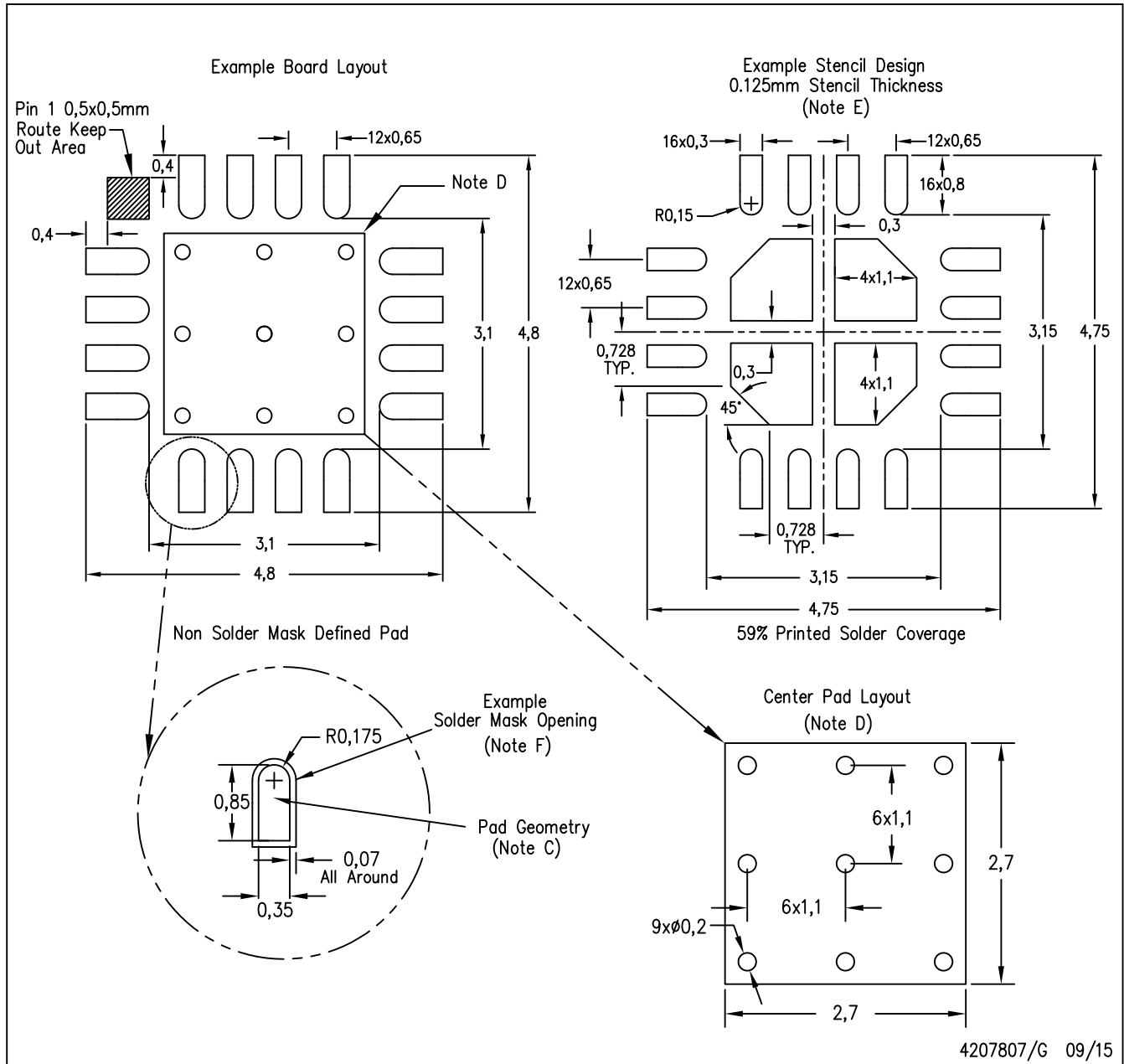
4206364-2/0 09/15

## NOTES:

A. All linear dimensions are in millimeters

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.



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