8-Input Data Selector/Multiplexer

MC74HC151A

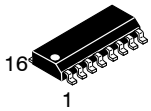
The MC74HC151A is identical in pinout to the LS151. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Strobe pin must be at a low level for the selected data to appear at the outputs. If Strobe is high, the Y output is forced to a low level and the $\overline{Y}$ output is forced to a high level.

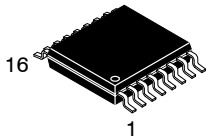
The HC151A is similar in function to the HC251 which has 3−state outputs.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



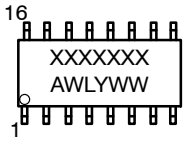
SOIC−16
D SUFFIX
CASE 751B

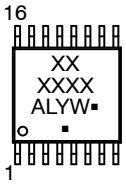


TSSOP−16
DT SUFFIX
CASE 948F

QFN16
MN SUFFIX
CASE 485AW

MARKING DIAGRAMS





A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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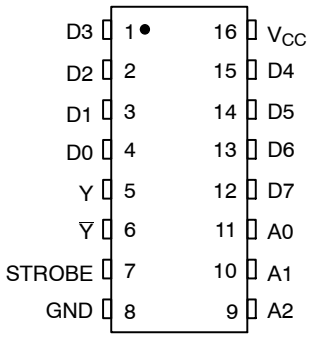

Figure 1. Pin Assignment

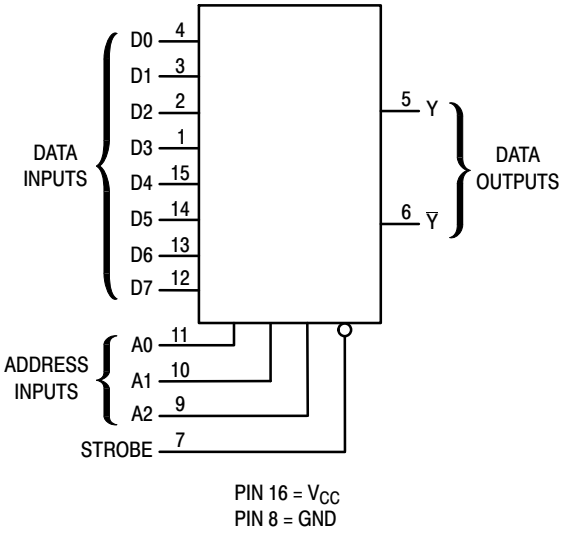

Figure 2. Logic Diagram

FUNCTION TABLE

Inputs				Outputs	
A2	**A1**	**A0**	**Strobe**	**Y**	**$\overline{Y}$**
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1, …, D7 = the level of the respective D input.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +6.5	V
V_{IN}	DC Input Voltage		–0.5 to V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature		–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		±150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC–16 QFN16 TSSOP–16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC–16 QFN16 TSSOP–16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm–by–114 mm, 2–ounce copper trace no air flow per JESD51–7.
2. HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free–Air Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit –55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} – 0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		$\|I_{OUT}\|$ ≤ 2.4 mA $\|I_{OUT}\|$ ≤ 4.0 mA $\|I_{OUT}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Minimum Low–Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		$\|I_{OUT}\|$ ≤ 2.4 mA $\|I_{OUT}\|$ ≤ 4.0 mA $\|I_{OUT}\|$ ≤ 5.2 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN} = V_{CC} or GND	6.0	8.0	80	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} V	Guaranteed Limit –55 to 25°C	≤ 85°C	≤ 125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Y (Figures 3 and 4)	2.0	170	215	255	ns
		3.0	TBD	TBD	TBD	
		4.5	34	43	51	
		6.0	29	37	43	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to $\overline{Y}$ (Figures 3 and 4)	2.0	185	230	280	ns
		3.0	TBD	TBD	TBD	
		4.5	37	46	56	
		6.0	31	39	48	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y (Figures 3 and 4)	2.0	185	230	280	ns
		3.0	TBD	TBD	TBD	
		4.5	37	46	56	
		6.0	31	39	48	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to $\overline{Y}$ (Figures 3 and 4)	2.0	205	255	310	ns
		3.0	TBD	TBD	TBD	
		4.5	41	51	62	
		6.0	35	43	53	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, STROBE to Y or $\overline{Y}$ (Figures 3 and 4)	2.0	125	155	190	ns
		3.0	TBD	TBD	TBD	
		4.5	25	31	38	
		6.0	21	26	32	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0	75	95	110	ns
		3.0	30	40	55	
		4.5	15	19	22	
		6.0	13	16	19	
C_{IN}	Maximum Input Capacitance	–	10	10	10	pF

			Typical @ 25°C	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	36	pF

4. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$.

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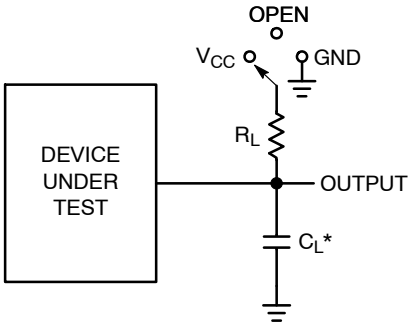
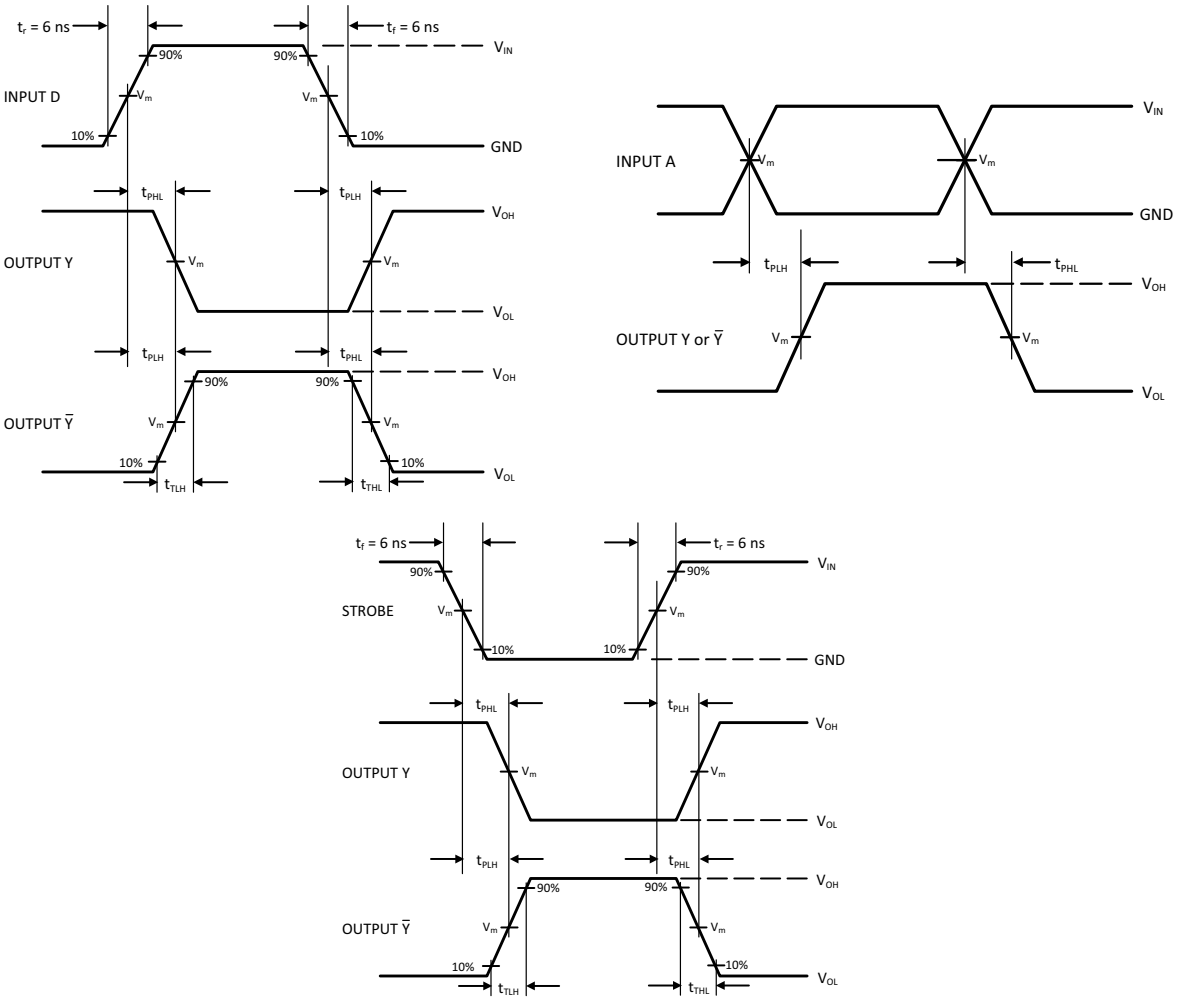


*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 3. Test Circuit



Device	V_{IN}, V	V_m, V
MC74HC151A	V_{CC}	50% x V_{CC}

Figure 4. Switching Waveforms

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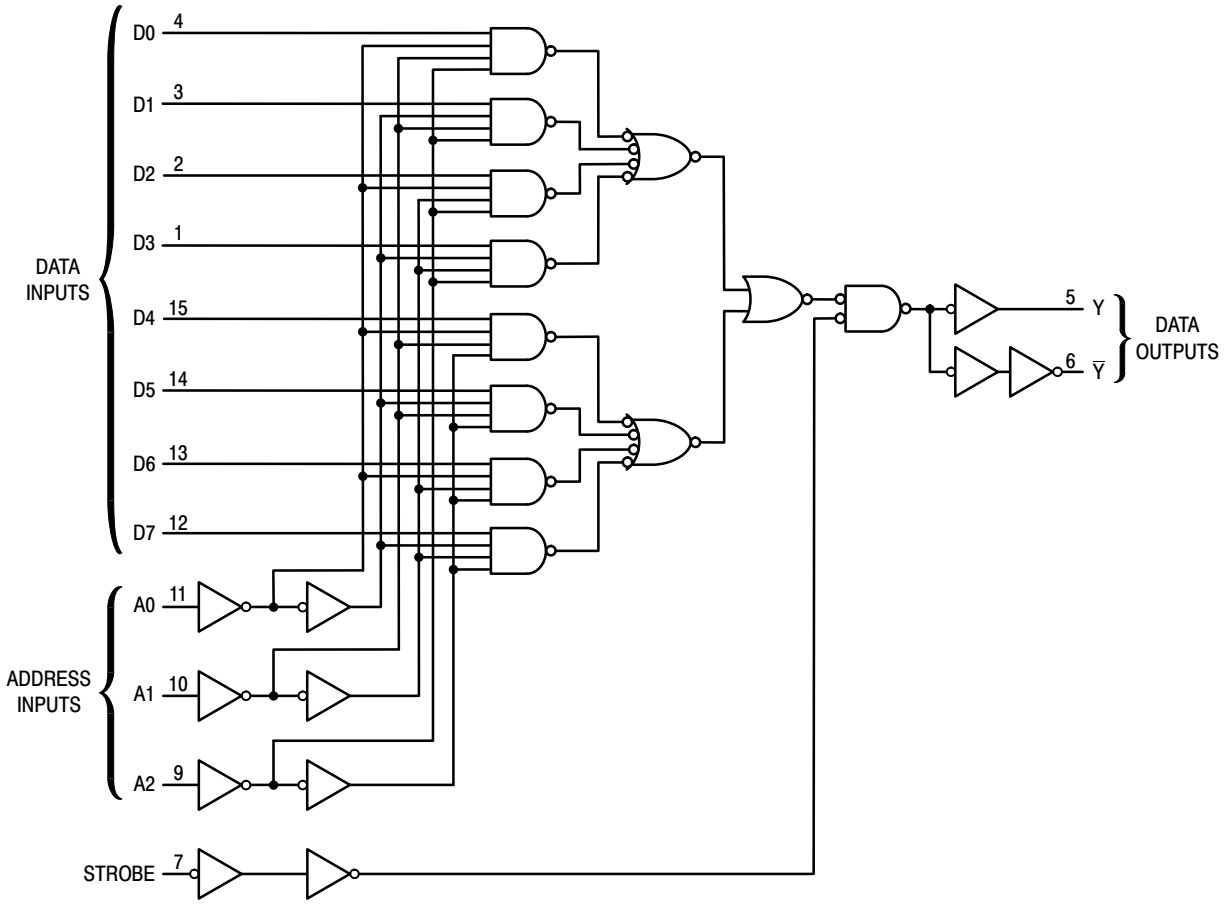

Figure 5. Expanded Logic Diagram

PIN DESCRIPTIONS

INPUTS

D0, D1, … , D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)

Data inputs. Data on any one of these eight binary inputs may be selected to appear on the output.

CONTROL INPUTS

A0, A1, A2 (Pins 11, 10, 9)

Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

Strobe (Pin 7)

Strobe. This input pin must be at a low level for the selected data to appear at the outputs. If the Strobe pin is high, the Y output is forced to a low level and the $\overline{Y}$ output is forced to a high level.

OUTPUTS

Y, $\overline{Y}$ (Pins 5, 6)

Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ($\overline{Y}$ output) forms.

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ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74HC151ADR2G	SOIC−16	HC151AG	1000 / Tape & Reel
MC74HC151ADR2G−Q*	SOIC−16	HC151AG	1000 / Tape & Reel
MC74HC151ADTG	TSSOP−16	HC 151A	75 Units / Rail
MC74HC151ADTR2G	TSSOP−16	HC 151A	2500 / Tape & Reel
MC74HC151ADTR2G−Q*	TSSOP−16	HC 151A	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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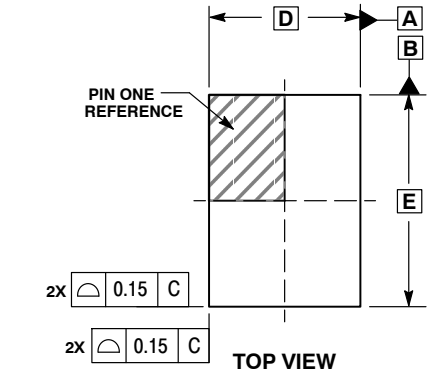
PACKAGE DIMENSIONS

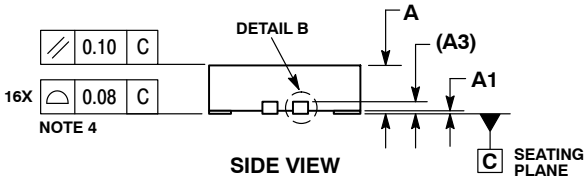
SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

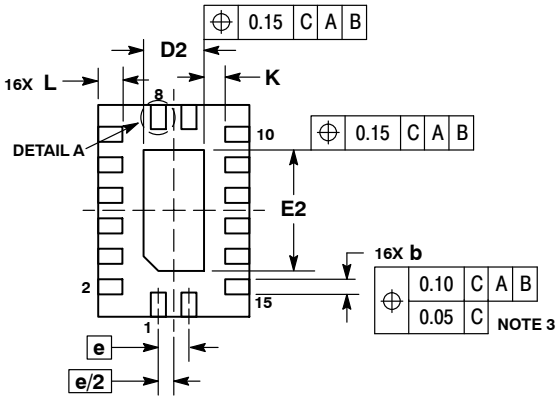
DATE 11 DEC 2008



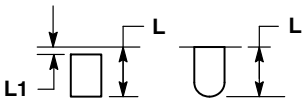
TOP VIEW



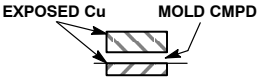
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

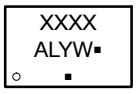


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

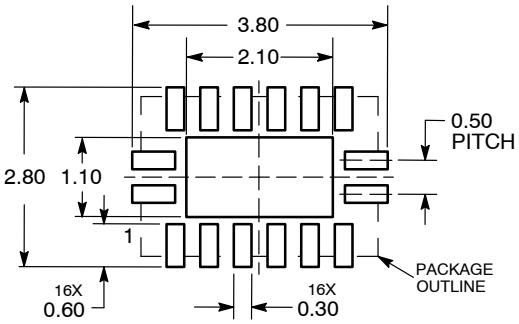


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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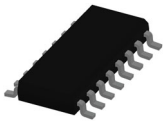
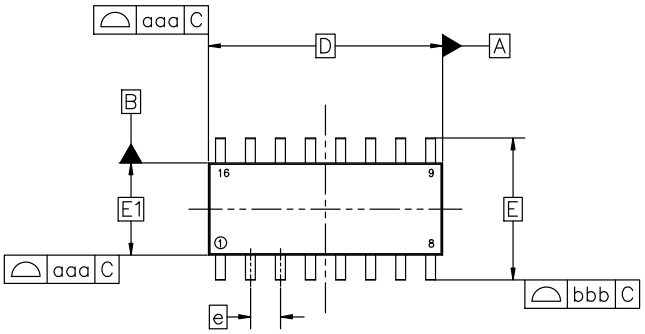


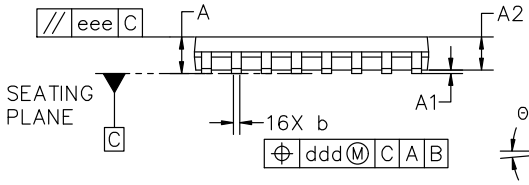
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

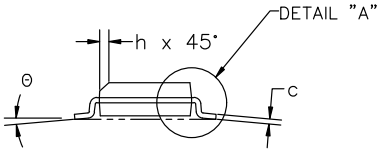
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

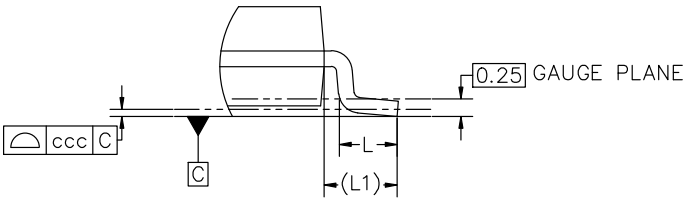


SIDE VIEW

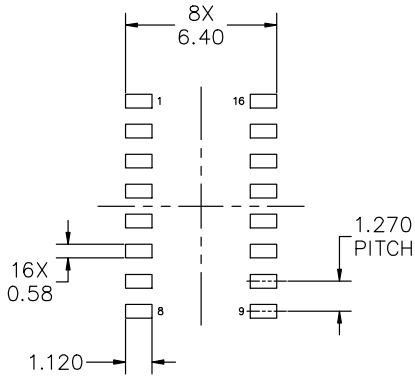


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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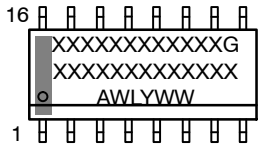
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**	**PAGE 2 OF 2**

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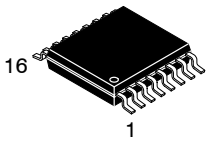
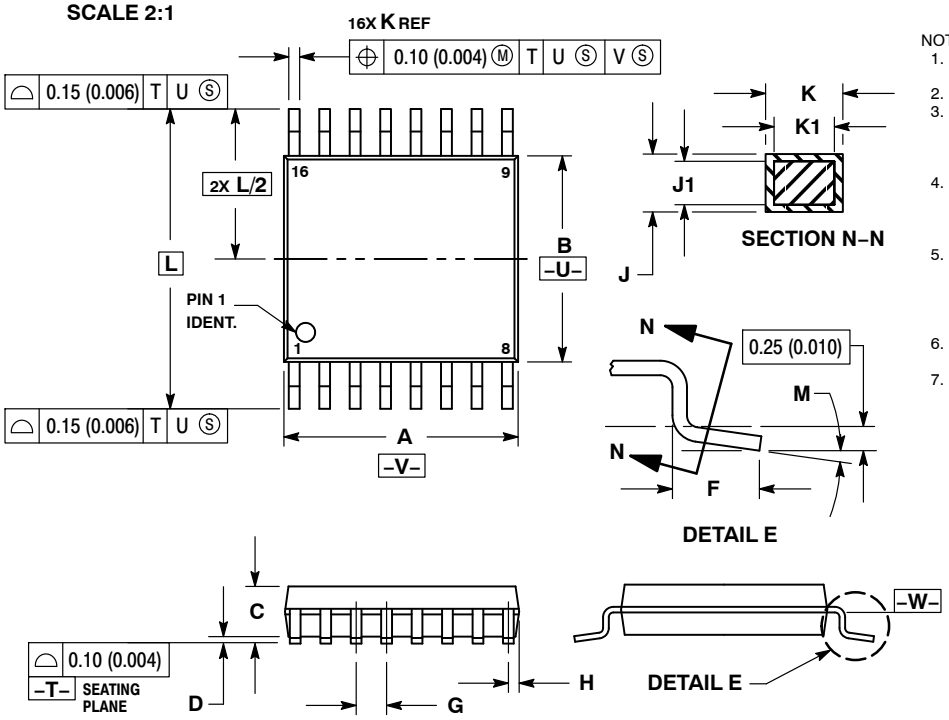


SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

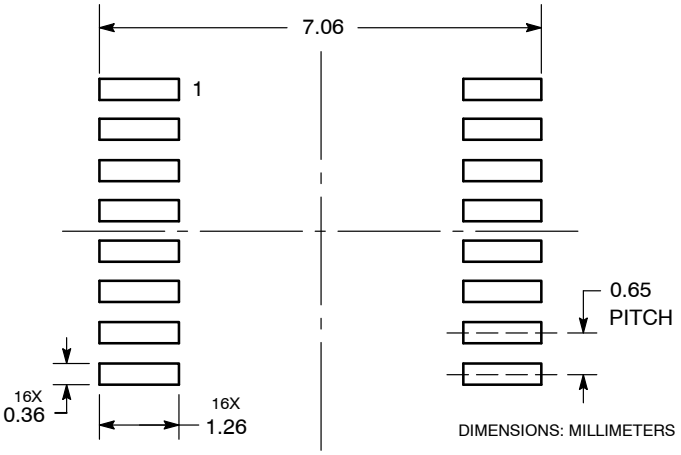
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

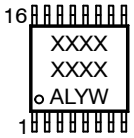
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

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DESCRIPTION:	TSSOP−16	PAGE 1 OF 1

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