1. Features and Benefits

- Motor driver
  - Driver for DC/BLDC/Stepper motor
  - Ron=0.8Ω typ. for 1 half-bridge + shunt
  - 2x NFET for each half-bridge
  - on-chip charge-pump for top-NFETs
  - V_{ds} protection for all NFETs
- Microcontroller:
  - MLX16-FX, application CPU
  - MLX4, communication CPU
  - 2x watch-dog
  - +50 input interrupt controller
  - Common purpose timer
- Memories split per CPU
  - MLX16-FX memories:
    - **64 kByte Flash with ECC**
    - 10 kByte ROM
    - **4 kByte RAM**
    - 512 Byte EEPROM
  - MLX4 memories:
    - 6 kByte ROM
    - 512 Byte RAM
- **Small QFN32,5x5 package**
- **Compatible with MLX81332 (32kB Flash)**
- **Automotive AEC-Q100 qualified**
- Periphery
  - Configurable RC-clock 12..32 MHz
  - 8x general purpose IO's, digital, analog, 1x high-voltage input, SPI, I2C-slave, UART
  - 5x 16-bit motor PWM timers
  - 2x 16-bit timers
  - 10-bit ADC with < 6 µs conversion time with multiple channels and different ADC references
  - Differential current sense amplifier
  - Temperature sensor, over-temperature detection
  - Over-current detection, over-voltage and under-voltage protection
- Voltage regulators
  - Internal voltage regulators, directly powered from 12V battery supply
  - Operating voltage Vs = 5.5V to 20V
  - Operation down to 3.5V with reduced analog characteristics, down to 3V without losing register content, down to 1.5V with intact RAM memory
  - Low standby current consumption of typ 25µA (max 50 µA) in sleep mode
  - Wake-up possible via LIN, external pins or internal wake-up timer
- Bus interface
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant LIN slave

2. Application Examples

- Small Stepper/BLDC flap or valve, up to 1A per phase
- Small DC flap or valve, or single-coil fan, up to 1.4A

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3. Ordering Information

Order Code	Temp. Range	Package	Delivery	Remark
MLX81334 LLW-AMT-001-RE	-40 - 150 °C	QFN32_WF 5x5	Reel	DC/BLDC/Stepper with 8x IO

Table 1 – Ordering information

4. Family Concept

	MLX81330	MLX81332	MLX81334
MCU Memory	32 KB Flash + 14 KB ROM	32 KB Flash + 16 KB ROM	**64 KB Flash** **+ 16 KB ROM**
MCU EEPROM	64x 8 Byte	64x 8 Byte	**64x 8 Byte**
MCU RAM	2.5 KB	2.5 KB	**4.5 KB**
Driver	4x Driver on-chip typ. 3Ω Halfbridge	4x Driver on-chip typ. 0.8Ω Halfbridge	**4x Driver on-chip** **typ. 0.8Ω Halfbridge**
IO pins (analog, digital)	3x LV + 1x HV/LV	7x LV + 1x HV/LV	**7x LV + 1x HV/LV**
Motor current sense	Low side, On-chip	Low side, On-chip	**Low side,** **On-chip**
Sensor interface (3V/5V supply)	analog, pwm, spi, sent, I^2C	analog, pwm, spi, sent, I^2C, uart	**analog, pwm, spi,** **sent, I^2C, uart**
Sensorless support (hw + sw)	Yes	Yes	**Yes**
LIN auto-address support (AA)	Yes	Yes	**Yes**
Maximum IC Temperature (with validated mission profile)	T_j = 175°C	Tj = 175°C	**Tj = 175°C**
Package	QFN24, 4x4 SO8-ep	QFN24, 4x4 SO8-ep	**QFN32, 5x5**

Table 2 – Famiy Overview

5. Revision history

Version	Date	Description
1.0	15/11/2021	Initial MLX81334 product abstract
2.0	03/04/2023	Product abstract update for launch

Table 3 – Revision history

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7. IC Block diagram

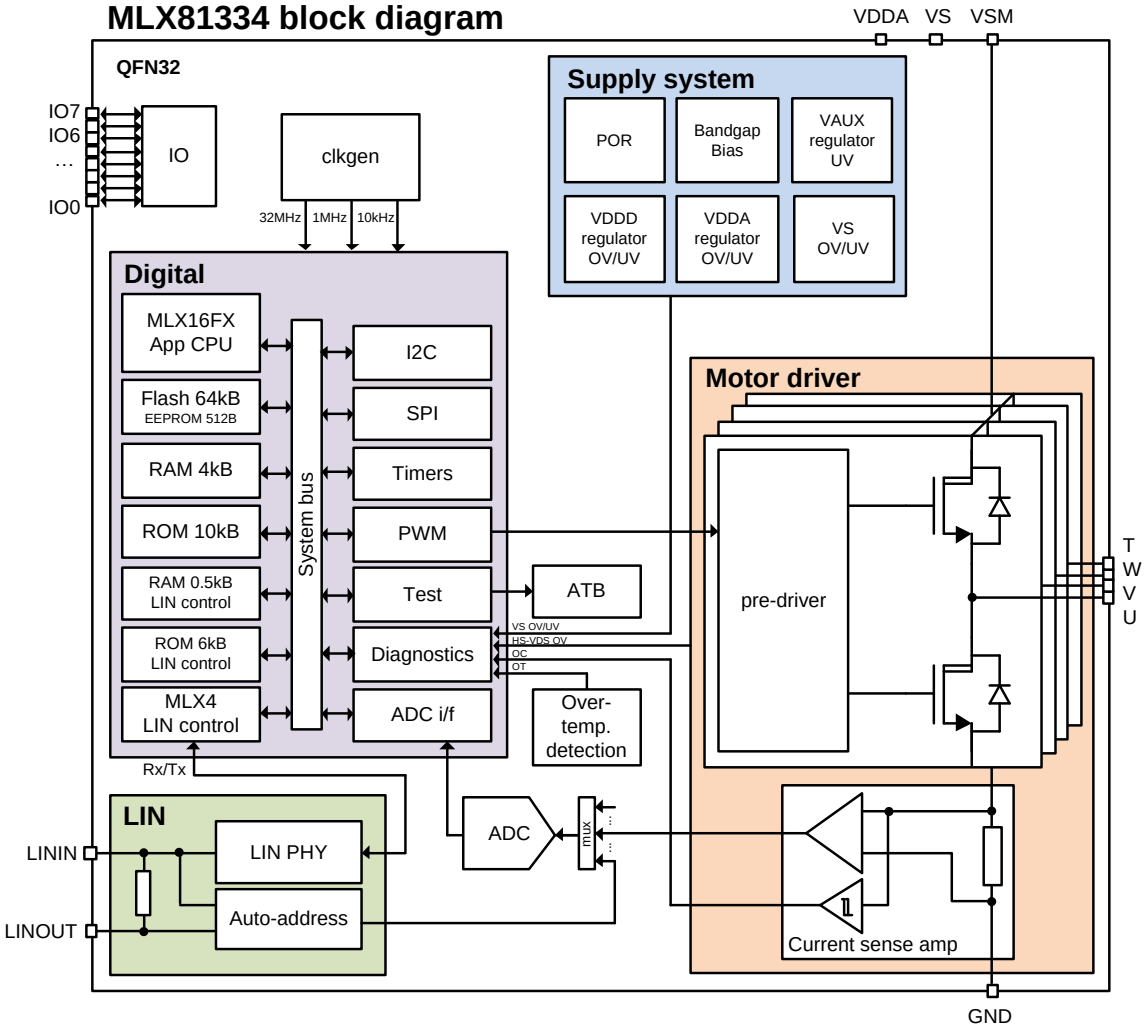
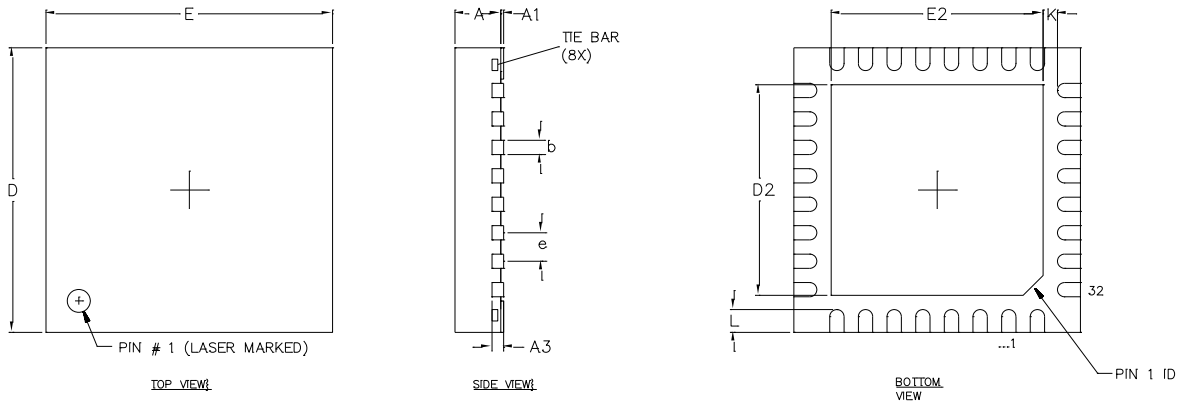


Figure 1 – IC Block diagram

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8. Technical description

8.1. Package data QFN32



COMMON DIMENSIONS AND TOLERANCES

SYMBOL	ALL DIMENSION ARE IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
L	0.30	0.40	0.50
K	0.20	---	---
b	0.18	0.25	0.30
e		0.50 BSC	

NOTE :
1. EXPOSED TIE BAR SHOULD BE KEPT FREE FROM SOLDER.
2. SIDE WALL IMMERSION TIN PLATING MIN 1um THICK.

Figure 2 – Package data QFN32

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8.3. Package Pin-out

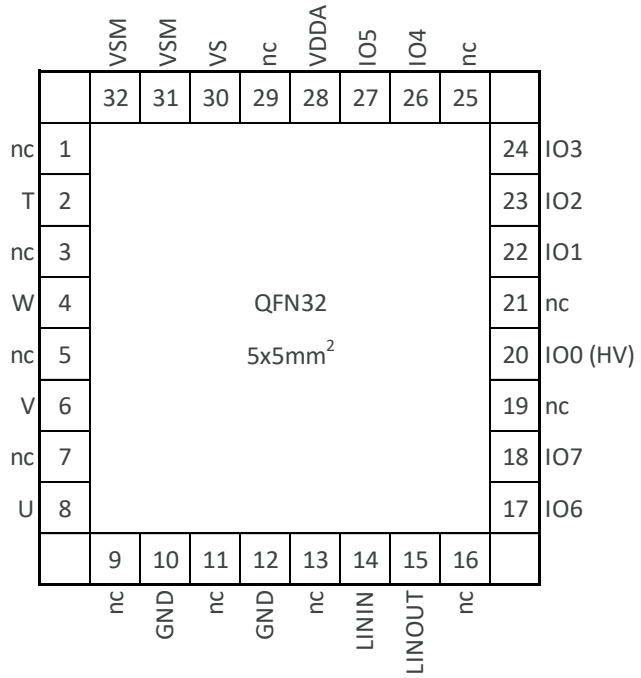


Figure 3 – Pin-out diagram QFN32

#	Pin name	Description	Comment
QFN32, 5x5mm		**All pins accessible**	**-0xx variant**
1	nc		
2	T	T-phase	
3	nc		
4	W	W-phase	
5	nc		
6	V	V-phase	
7	nc		
8	U	U-phase	
9	nc		
10	GND	Ground	
11	nc		
12	GND	Ground	
13	nc		

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#	Pin name	Description	Comment
QFN32, 5x5mm		**All pins accessible**	**-0xx variant**
14	LIN-IN	LIN input	
15	LIN-OUT	LIN output (for auto-addressing)	
16	nc		
17	IO6	LVIO + test input for development	
18	IO7	LVIO + test output for development	
19	nc		
20	IO0	LVIO + HVI (high-voltage input)	
21	nc		
22	IO1	LVIO	
23	IO2	LVIO	
24	IO3	LVIO	
25	nc		
26	IO4	LVIO	
27	IO5	LVIO	
28	VDDA	3.3V analog supply voltage	
29	nc		
30	VS	Supply voltage for MCU	
31	VSM	Supply voltage for motor driver	
32	VSM	Supply voltage for motor driver	

Table 4 – Pin-out description for QFN32

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8.4. Package Marking

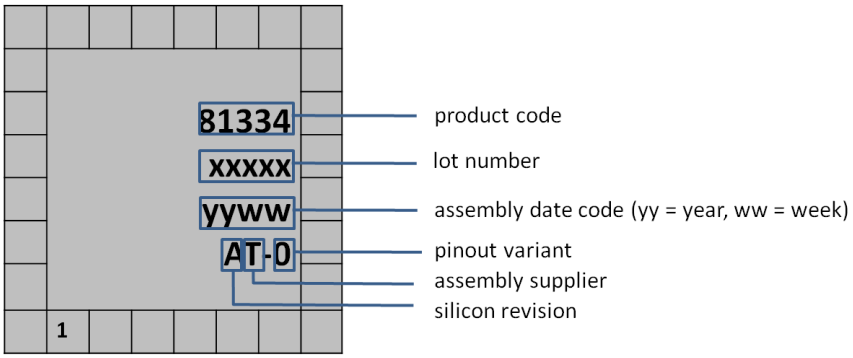


Figure 4 – Package Marking QFN32

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9. Typical application schematic

In the following schematic examples, external components are indicated that may be needed to protect the IC against EMC / ESD pulses. Depending on ECU conditioned power, overvoltage and reverse polarity discretes may not be needed. Capacitor discretes or capacitor values will depend on specific OEM ESD/EMC requirements

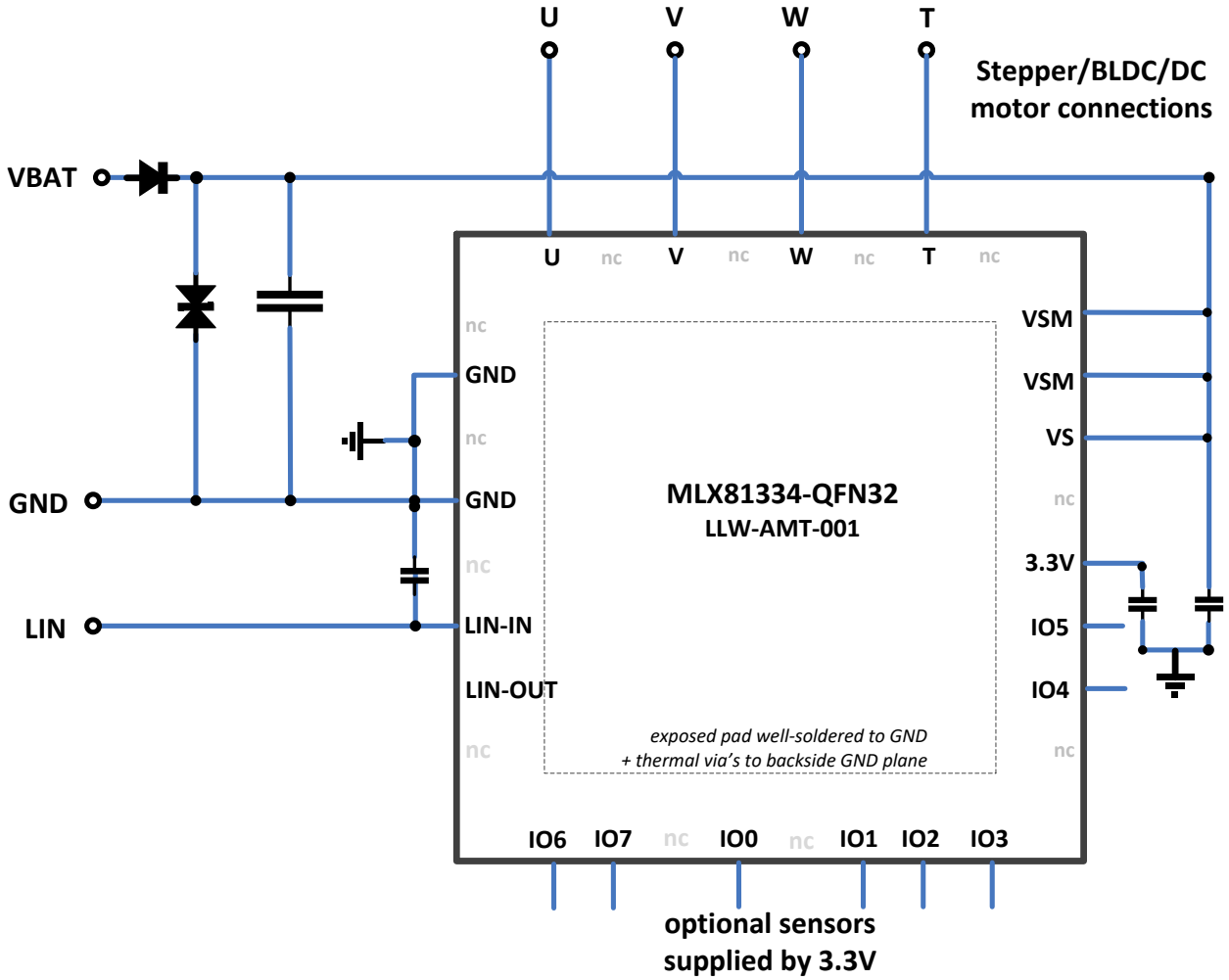


Figure 5 – Typical motor schematic with MLX81334 in QFN32

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10. Electrical characteristics

10.1. Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	VS, VSM	-0.3		28	V	
Supply voltage	VS, VSM	-0.3		40	V	t < 500ms
Supply voltage transient	VS.tr1	-100			V	ISO 7637-2 pulse 1 [1]
Supply voltage transient	VS.tr2			75	V	ISO 7637-2 pulse 2 [1]
Supply voltage transient	VS.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [1]
Output voltage	VDDA	-0.3		5.5	V	
LIN bus voltage	VLIN	-40			V	Referenced to VS
LIN bus voltage	VLIN			40	V	Referenced to GND
LIN bus voltage transient	VLIN.tr1	-30			V	ISO 7637-3 DCC slow – [2]
LIN bus voltage transient	VLIN.tr2			30	V	ISO 7637-3 DCC slow + [2]
LIN bus voltage transient	VLIN.tr3	-150		100	V	ISO 7637-2 pulses 3a, 3b [2]
Analog HV voltage	VAN_HV	-0.3		VS+0.3	V	IO0 (HV input mode) U, V, W, T
Analog LV voltage	VAN_LV	-0.3		VDDA+0.3	V	IO0...7
Digital input voltage	VIN_DIG	-0.3		VDDA+0.3	V	IO0…7
Digital output voltage	VOUT_DIG	-0.3		VDDA+0.3	V	IO0...7
ESD HBM capability	ESD_HBM	-2		2	kV	All pins except LININ, LINOUT
ESD HBM capability	ESD_HBM_LIN	-6		6	kV	Pins LININ, LINOUT
ESD CDM capability	ESD_CDM	-500		500	V	All pins
Junction temperature	TJ	-55		175	ºC	

Table 5 – Absolute maximum ratings

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and blocking capacitor.
[2] ISO 7637 test pulses are applied to LIN via a coupling capacitance of 1nF.

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10.2. Operating range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage	V_S, VSM	6.5	12	20	V	Driver full performance
Supply voltage	V_S, VSM	5.5		6.5	V	Driver reduced performance [1]
Supply voltage	V_S	4		20	V	Analog full performance
Supply voltage	V_S	3.5		4	V	Analog reduced performance [2]
Supply voltage	V_S	3		20	V	Digital functional
Supply voltage	V_S	1.5		20	V	SRAM content valid
Junction temperature	T_J	-40		175	ºC	Limited time at Tj=175 ºC [3]

Table 6 – Operating range

[1] Motor driver is functional at reduced performance (higher bridge resistance, reduced accuracy of current sense amplifier)
[2] 3.3V regulator is functional at reduced performance (lower current capability)
[3] Extended temperature range with Tj=175 ºC is only allowed for a limited time, customer's mission profile has to be agreed by Melexis as an obligatory part of the Part Submission Warrant (PSW).

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10.3. Electrical specifications

10.3.1. Current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Normal working current	INOM		10	15	mA	
Sleep mode current	ISLEEP		25	50	µA	VS=13V
Stop mode current	ISTOP		250	500	µA	
Holding current	IHOLD		5	7	mA	

Table 7 – Electrical specifications : current consumption

10.3.2. Supply system

10.3.2.1. VDDA 3.3V regulator (5V option, external C: 0 … 220nF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
3.3V analog supply voltage (default)	VDDA	3.2	3.3	3.4	V	Bandgap and VDDA regulator trimmed
3.3V current capability	IVDDA	20			mA	VS >= 4V
3.3V external current capability	IVDDA_EXT	0		15	mA	VS >= 4V
3.3V under-voltage detection threshold	VTH_UV_VDDA	2.75	2.85	2.95	V	VDDA ramping down
3.3V under-voltage detection hysteresis	VHY_UV_VDDA	0.1	0.15		V	
5V option (SWITCH_VDDA_TO_5V=1)						
5V analog supply voltage (option)	VDDA	4.85	5	5.15	V	Bandgap and VDDA regulator trimmed
5V current capability	IVDDA	20			mA	VS >= 6V
5V external current capability	IVDDA_EXT	0		15	mA	VS >= 6V
5V under-voltage detection threshold	VTH_UV_VDDA	3.95	4.1	4.25	V	VDDA ramping down
5V under-voltage detection hysteresis	VHY_UV_VDDA	0.1	0.15		V	

Table 8 – Electrical specifications : VDDA regulator

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10.3.2.2. VDDD 1.8V regulator

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
1.8V digital supply voltage	VDDD	1.8	1.875	1.95	V	Bandgap and VDDD regulator trimmed
1.8V current capability	IVDDD	15			mA	

Table 9 – Electrical specifications : VDDD regulator

10.3.2.3. VS under-voltage and over-voltage detection

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VS under-voltage detection threshold	VTH_UV_VS	3.5	4	4.5	V	PRUV_VS=0
VS under-voltage detection threshold	VTH_UV_VS	4.5	5	5.5	V	PRUV_VS=1
VS under-voltage detection threshold	VTH_UV_VS	5.5	6	6.5	V	PRUV_VS=2
VS under-voltage detection threshold	VTH_UV_VS	6.5	7	7.5	V	PRUV_VS=3
VS under-voltage detection threshold	VTH_UV_VS	7.5	8	8.5	V	PRUV_VS=4
VS under-voltage detection threshold	VTH_UV_VS	8.5	9	9.5	V	PRUV_VS=5
VS under-voltage detection hysteresis	VHY_UV_VS	0.1	0.5	1	V	
VS over-voltage detection threshold	VTH_OV_VS	20	22	24	V	PROV_VS=0
VS over-voltage detection threshold	VTH_OV_VS	22	24	26	V	PROV_VS=1
VS over-voltage detection threshold	VTH_OV_VS	38	40	42	V	PROV_VS=2
VS over-voltage detection hysteresis	VHY_OV_VS	1	2	3	V	

Table 10 – Electrical specifications : VS over- and under-voltage detection

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10.3.2.4. Wake-up circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Wake-up filter time IO pins	TFILT_WU_IO	15		80	µs	
Wake-up filter time LIN pin	TFILT_WU_LIN	28		125	µs	
Wake-up time internal timer	TWU_INT		n/a			WUI=00 (no wake-up)
Wake-up time internal timer	TWU_INT		4096 / FOSC_10K			WUI=01 (~0.4 s)
Wake-up time internal timer	TWU_INT		8192 / FOSC_10K			WUI=10 (~0.8 s)
Wake-up time internal timer	TWU_INT		16384 / FOSC_10K			WUI=11 (~1.6 s)

Table 11 – Electrical specifications : wake-up circuit

10.3.2.5. Bandgap

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Bandgap voltage	VBG	1.15	1.185	1.22	V	Trimmed
Bandgap voltage temperature coeff.	TC_VBG			180	ppm/K	

Table 12 – Electrical specifications : bandgap

10.3.3. Clock generation

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency 1MHz oscillator	FOSC_1M	-5%	1	+5%	MHz	Trimmed
Frequency 32MHz oscillator	FOSC_32M	-5%	32	+5%	MHz	Trimmed
Frequency 10kHz oscillator	FOSC_10K	5	10	20	kHz	
Timing accuracy	TIMING_ACC	-1.5%		1.5%	%	Timing accuracy after sw correction using EEPROM calibration values

Table 13 – Electrical specifications : clock generation

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10.3.4. Motor driver module

10.3.4.1. Charge Pump clock

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Charge pump clock frequency	FOSC_CP	51	60	69	MHz	Trimmed
Charge pump clock frequency	FOSC_CP	71	82	93	MHz	Trimmed (default)

Table 14 – Electrical specifications : driver clock

10.3.4.2. Output stage

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Half-bridge phase current	IHB			1.0	A_{pk}	During normal operation
Half-bridge phase current	IHB			0.7	A_{rms}	During normal operation
Half-bridge phase boost current	IHB			1.3	A	< 1s, ambient temperature -40°C…85°C [1]
2x half-bridge phase boost current	IHB			1.8	A	< 1s, ambient temperature -40°C…85°C, 2 phases in parallel [1]
Half-bridge resistance	RHB		0.8	1.6	Ω	TopFET + BottomFet + Shunt
Duty cycle range of PWM output	DC_OUT	2		98	%	For switching PWM (0% or 100% can be set as well) PWM frequency = 20kHz
Duty cycle of PWM output	DC_OUT	1		3	%	PWM duty cycle setting = 2% PWM frequency = 20kHz
Duty cycle of PWM output	DC_OUT	97		99	%	PWM duty cycle setting = 98% PWM frequency = 20kHz
FET over-current detection threshold	ITH_DS_HS	1.6	2.2	2.8	A	
FET over-current detection hysteresis	IHY_DS		0.1		A	

Table 15 – Electrical specifications : output stage

[1] Time between boost cycles is 2x boost time

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10.3.4.3. Current sense amplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Sense resistor	RCS		0.1	0.2	Ω	
Input range	ICS	-2		2	A	Current sensing range
Input range	ICS			4	A	High-end range extension for over-current detection
Over-current detection threshold	ITH_OC	-2		4	A	Adjustable through 8bit DAC [1]
Over-current detection threshold accuracy	ITH_OC	-10		10	%	OCD threshold = 2A
Over-current settling time	TSET_TH_OC			10	µs	Settling time after adjustment
Gain	GCS	0.38	0.4	0.42	V/A	Trimmed and calibrated
Offset	VCSO	1.215	1.25	1.285	V	Trimmed and calibrated

Table 16 – Electrical specifications : current sense amplifier

[1] 8bit signed DAC, step size = 23.4mA, value for code 0x00 = 800mA

10.3.5. VSM supply sensor

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Voltage range for ADC measurement				28	V	Measurement of VSM/21
VSM filter cut-off frequency				4	kHz	

Table 17 – Electrical specifications : VSM supply sensor

10.3.6. Over-temperature detection

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
OTD threshold	TTH_OT	175	185	195	ºC	Temperature ramping up
OTD threshold	TTH_OT	150	160	170	ºC	Temperature ramping down
OTD hysteresis	THY_OT	10	25		ºC	

Table 18 – Electrical specifications : over-temperature detection

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10.3.7. ADC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Reference voltage	VREFADC		VDDA		V	
Reference voltage	VREFADC	2.45	2.5	2.55	V	Trimmed and calibrated
Reference voltage	VREFADC	1.47	1.5	1.53	V	Trimmed and calibrated
Reference voltage	VREFADC	0.735	0.75	0.765	V	Trimmed and calibrated
Resolution			10		bit	
Conversion time	TCONV			6	µs	
DNL		-1		1	LSB	
INL		-3		3	LSB	
ADC LV channel (with 1/1.36 divider) accuracy [1]		-45		45	mV	0V – 3.3V input, calibrated acc. calibration document
ADC HV channel (with 1/21 divider) accuracy		-0.30		0.30	V	<5V input, calibrated acc. calibration document
ADC HV channel (with 1/21 divider) accuracy		-0.60		0.60	V	<20V input, calibrated acc. calibration document
ADC VSMF channel (with 1/21 divider) accuracy		-0.20		0.20	V	<5V input, calibrated acc. calibration document
ADC VSMF channel (with 1/21 divider) accuracy		-0.30		0.30	V	<20V input, calibrated acc. calibration document
ADC temperature channel accuracy		-10		10	ºC	Calibrated acc. calibration document
ADC channel select		0		25		See datasheet

Table 19 – Electrical specifications : ADC

[1] VS >= 4.7V for IO0 ADC LV channel

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10.3.8. IO

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input threshold level L → H				2.4	V	
Input threshold level H → L		1			V	[1]
Input hysteresis		0.1			V	
Output voltage L, IO1…7				0.4	V	ILOAD = 2mA
Output voltage L, IO0				0.5	V	ILOAD = 2mA
Output voltage H, IO1…7		VDDA - 0.4V			V	ILOAD = 2mA
Output voltage H, IO0		VDDA - 0.5V			V	ILOAD = 2mA, VS > 5.5V
Input voltage range for high-voltage ADC measurement		0		28	V	IO0 Measurement of IO0/21
Input voltage range for low-voltage ADC measurement		0		VDDA	V	IO0...7 Measurement of IOx/1.36
I2C SDA hold time (vs SCL)		0	35	70	ns	IO0 pin, SDAFILT_IO=00, setting for Fast-mode Plus
I2C SDA hold time (vs SCL)		180	260	340	ns	IO0 pin, SDAFILT_IO=01
I2C SDA hold time (vs SCL)		240	330	420	ns	IO0 pin, SDAFILT_IO=10
I2C SDA hold time (vs SCL)		360	500	640	ns	IO0 pin, SDAFILT_IO=11, setting for Standard-mode and Fast-mode

Table 20 – Electrical specifications : IO

[1] If IO0 is used as a global pin, then a series resistor of min. 800Ω / max. 10kΩ needs to be applied.

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10.3.9. LIN

10.3.9.1. LIN transceiver - static

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Transmitter internal capacitance [1]	CLIN		30	40	pF	Response on 14V pulse via 1K
Bus short circuit current	IBUS_LIM	40	100	200	mA	VLIN = VS = 27V, VTxD = 0V
Pull up resistance bus, untrimmed	RSLAVE	20	35	60	kΩ	VDISTERM = 0
Pull up current bus, sleep mode	ISLAVE_SLEEP	-50	-20	-5	µA	VLIN = 0V, VSBY = VAUX, VEN =0
Dominant input leakage current including pull up resistor	IBUS_PAS_dom	-600			µA	VLIN =0V, VS =12V, VTxD = VDDD, VDISTERM = 0 VEN = VDDD, VSBY = 0
Recessive input leakage current	IBUS_PAS_rec		0.25	1	µA	VEN = VDDD, VSBY = 0, VTxD = VDDD, VLIN > VS
Bus reverse current loss of battery [2]	IBUS_NO_BAT		0.25	1	µA	VS = 0V, 0V < VLIN < 27V
Bus current during loss of ground [2]	IBUS_NO_GND	-100		1	µA	VS = VGND = 12V, 0 < VLIN < 27V
Transmitter dominant output voltage [2]	VolBUS	0		0.2×VS	V	Rload = 500Ω
Transmitter recessive output voltage [2]	VohBUS	0.8×VS		1×VS	V	VEN = VDDD, VSBY = 0, VTxD = VDDD or sleep mode
Receiver dominant voltage	VBUSdom			0.4×VS	V	
Receiver recessive voltage	VBUSrec	0.6×VS			V	
Center point of receiver threshold	VBUS_CNT	0.475×VS	0.5×VS	0.525×VS	V	VBUS_cnt = (Vth_dom+ Vth_rec)/2
Receiver hysteresis	VHYS			0.175×VS	V	VHYS = (Vth_rec –Vth_dom)

Table 21 – Electrical specifications : LIN transceiver – static

[1] No production test, guaranteed by design and qualification
[2] In accordance to SAE J2602

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10.3.9.2. LIN transceiver – dynamic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Propagation delay receiver [1]	trx_pdf			6	µs	CRxD = 25pF, falling edge
Propagation delay receiver [1]	trx_pdr			6	µs	CRxD = 25pF, rising edge
Propagation delay receiver symmetry	trx_sym	-2		2	µs	Calculate trx_pdf – trx_pdr
Receiver debounce time [2]	trx_deb	0.5		4	µs	LIN rising & falling edge
LIN duty cycle 1 [2] [3] [5]	D1	0.396				20kbps operation, normal mode Vs = 7 to 18V
LIN duty cycle 2 [2] [3] [5]	D2			0.581		20kbps operation, normal mode Vs = 7 to 18V
LIN duty cycle 3 [2] [3] [5]	D3	0.417				10.4kbs operation, low speed mode Vs = 7 to 18V
LIN duty cycle 4 [2] [3] [5]	D4			0.590		10.4kbs operation, low speed mode Vs = 7 to 18V
tREC(MAX) – tDOM(MIN) [4] [5]	Δt3			15.9	µs	10.4kbs operation, low speed mode
tDOM(MAX) – tREC(MIN) [4] [5]	Δt4			17.28	µs	10.4kbs operation, low speed mode
Slew rate on pin LIN normal mode, untrimmed			1.7		V/ µs	dV/dt between duty cycle measurement points, Vs=12V
Slew rate on pin LIN low speed mode, untrimmed			0.85		V/ µs	dV/dt between duty cycle measurement points, Vs=12V
TxD dominant timeout [6]	ttxd_to		15		ms	Normal mode, vTxD = 0V

Table 22 – Electrical specifications : LIN transceiver – dynamic

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See Figure 6
[3] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal master termination disabled
[4] In accordance to SAE J2602, see Figure 7

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[5] For supply voltage ranges Vs=5.5…7V and Vs=18…27V parametric deviations are possible (target specification is w/o deviations & ppK>2.0)
[6] Parameter in relation to internal signal TxD

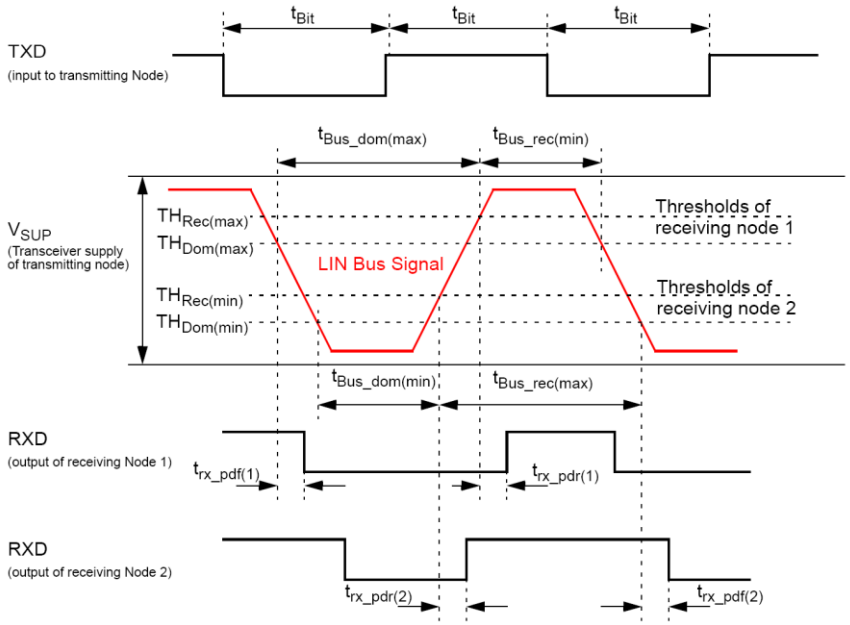


Figure 6 – LIN timing diagram (reference LIN2.1 specification)

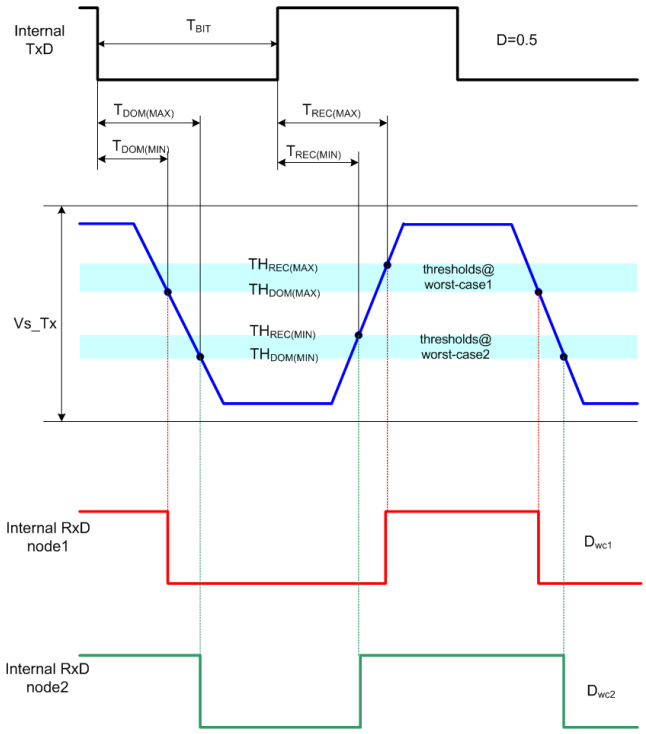


Figure 7 – LIN timing diagram, relation between propagation delay and duty cycle (reference SAE J2602 specification)

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