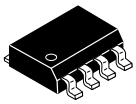
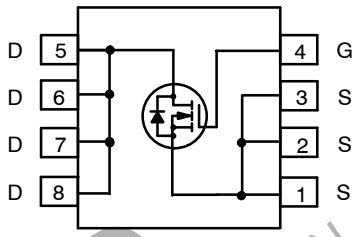
# MOSFET – N-Channel, POWERTRENCH®

## 40 V, 7.6 A, 29 mΩ

# FDS8449, FDS8449-G



SOIC8
CASE 751EB



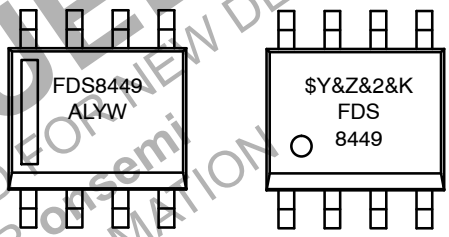

### General Description

These N−Channel MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize on−state resistance and yet maintain superior switching performance.

### Features

- 7.6 A, 40 V $R_{DS(on)}$ = 29 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(on)}$ = 36 mΩ @ $V_{GS}$ = 4.5 V
- High Power Handling Capability in a Widely Used Surface Mount Package
- Pb−Free, Halide Free and RoHS Compliant

### MARKING DIAGRAM




FDS8449 FDS8449−G

| | |
|---|---|
| FDS8449 | = Specific Device Code |
| A | = Assembly Site |
| L | = Wafer Lot Number |
| YW | = Assembly Start Week |
| $Y | = **onsemi** Logo |
| &Z | = Assembly Plant Code |
| &2 | = 2−Digit Code Format |
| &K | = 2−Digits Lot Run Traceability Code |

### ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | 40 | V |
| $V_{GSS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>– Continuous (Note 1a)<br>– Pulsed | <br>7.6<br>50 | A |
| $P_D$ | Power Dissipation for Single Operation<br>(Note 1a)<br>(Note 1b) | <br>2.5<br>1 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 125 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 25 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDS8449 | SOIC8 (Pb−Free/ Halide Free) | 2500 / Tape & Reel |
| FDS8449−G | SOIC8 (Pb−Free/ Halide Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** $T_A$ = 25°C unless otherwise noted.

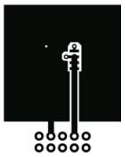
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAIN−SOURCE AVALANCHE RATINGS** (Note 3) | | | | | | |
| $E_{AS}$ | Drain to Source Avalanche Energy | $V_{DD}$ = 40 V, $I_D$ = 7.3 A, L = 1 mH | – | – | 27 | mJ |
| $I_{AS}$ | Drain to Source Avalanche Current | | – | 7.3 | – | A |
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 40 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | 34 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate−Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | −5 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On−Resistance | $I_D$ = 7.6 A, $V_{GS}$ = 10 V, | – | 21 | 29 | mΩ |
| | | $I_D$ = 6.8 A, $V_{GS}$ = 4.5 V | – | 26 | 36 | |
| | | $I_D$ = 7.6 A, $V_{GS}$ = 10 V, $T_J$ = 125°C | – | 29 | 43 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 7.6 A | – | 21 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 760 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 100 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 60 | – | |
| $R_G$ | Gate Resistance | f = 1.0 MHz | – | 1.2 | – | Ω |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GS}$ = 6 Ω | – | 9 | 18 | ns |
| $t_r$ | Turn−On Rise Time | | – | 5 | 10 | |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 23 | 17 | |
| $t_f$ | Turn−Off Fall Time | | – | 3 | 6 | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 20 V, $I_D$ = 7.6 A, $V_{GS}$ = 5 V | – | 7.7 | 11 | nC |
| $Q_{gs}$ | Gate−Source Charge | | – | 2.4 | – | |
| $Q_{gd}$ | Gate−Drain Charge | | – | 2.8 | – | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | – | 0.76 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 7.6 A, $d_{IF}/d_t$ = 100 A/μs | – | 17 | – | ns |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | – | 7 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 $in^2$ pad of 2 oz. copper.



b) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. BV(avalanche) Single−Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.



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## TYPICAL CHARACTERISTICS

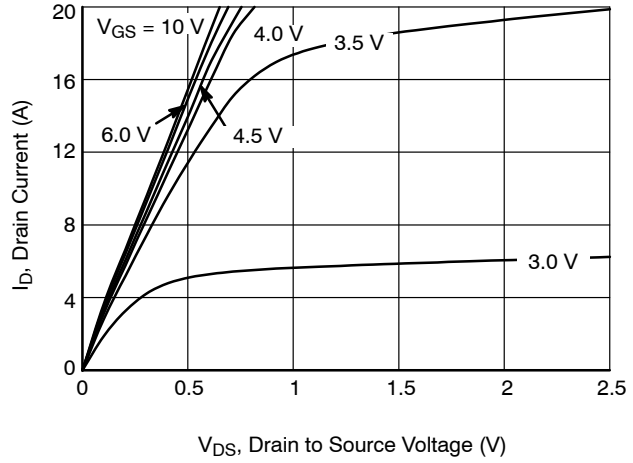



**Figure 1. On Region Characteristics**

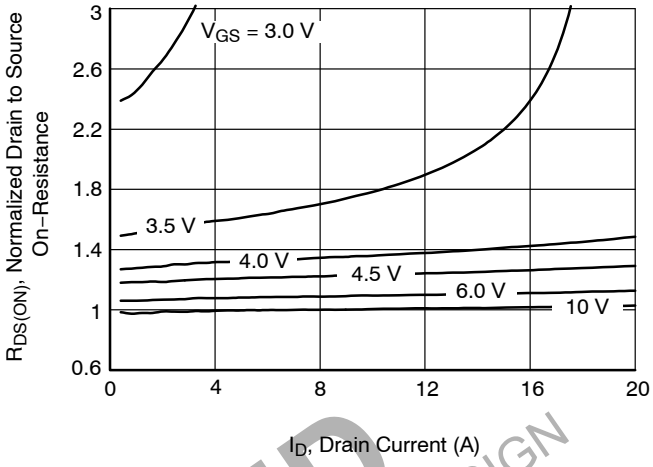



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

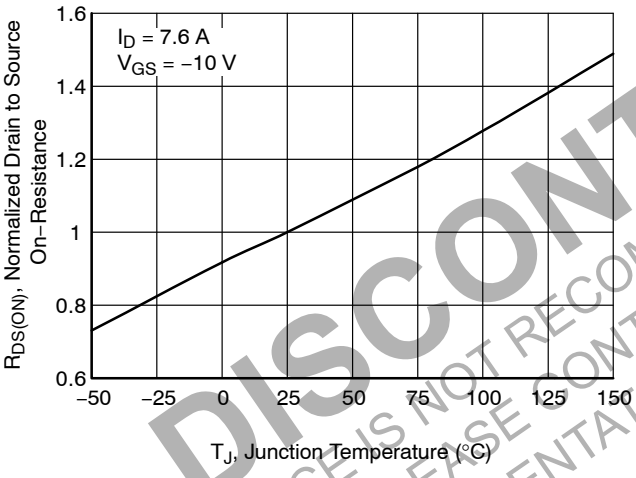



**Figure 3. On−Resistance Variation with Temperature**

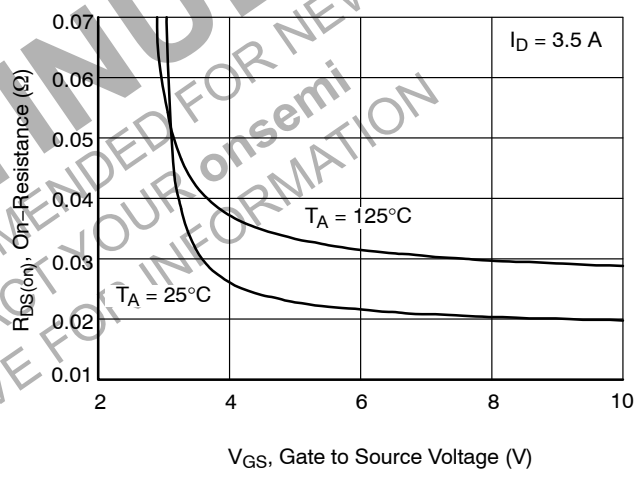



**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**

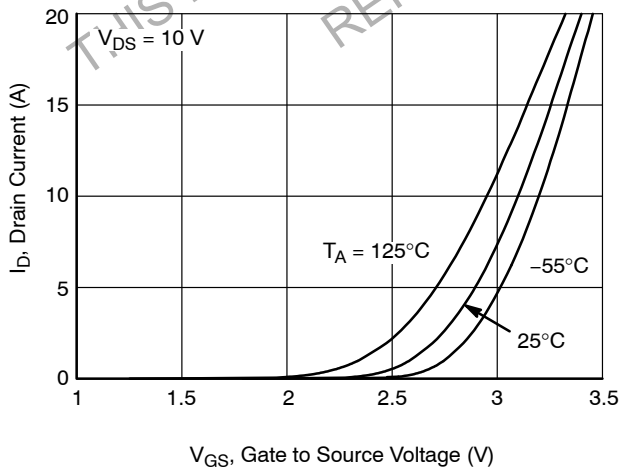



**Figure 5. Transfer Characteristics**

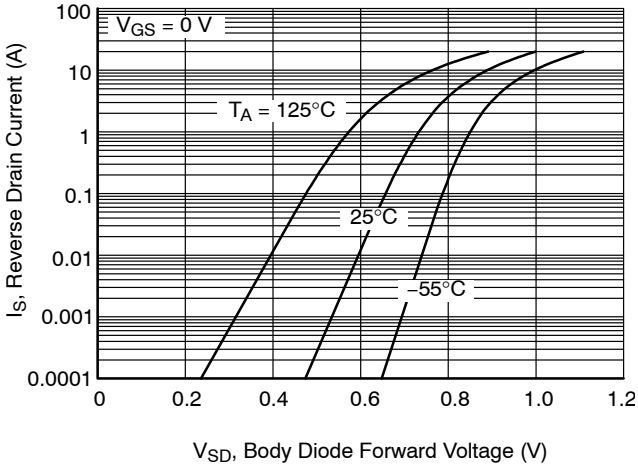



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

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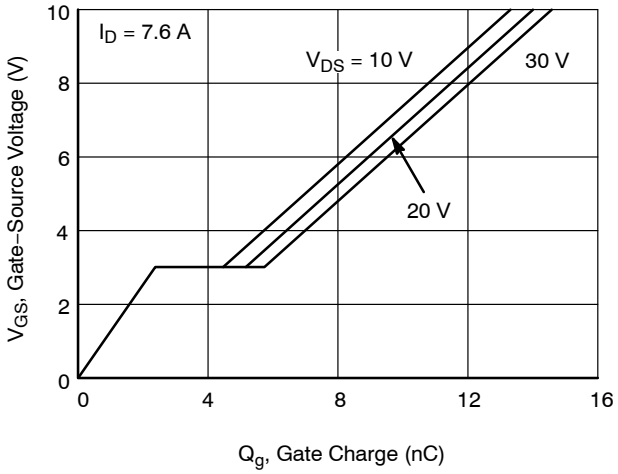



**Figure 7. Gate Charge Characteristics**

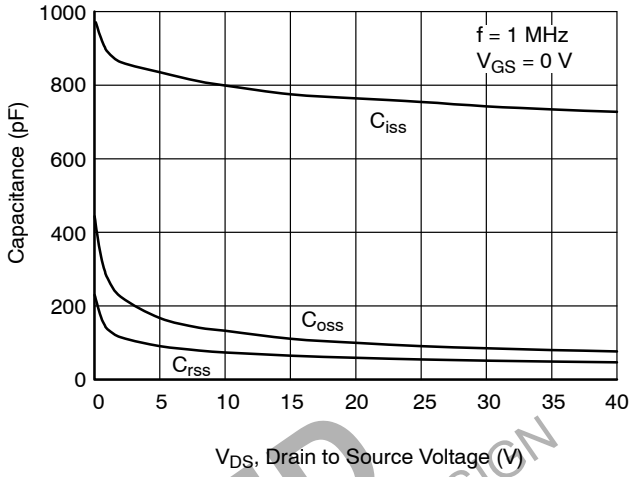



**Figure 8. Capacitance Characteristics**

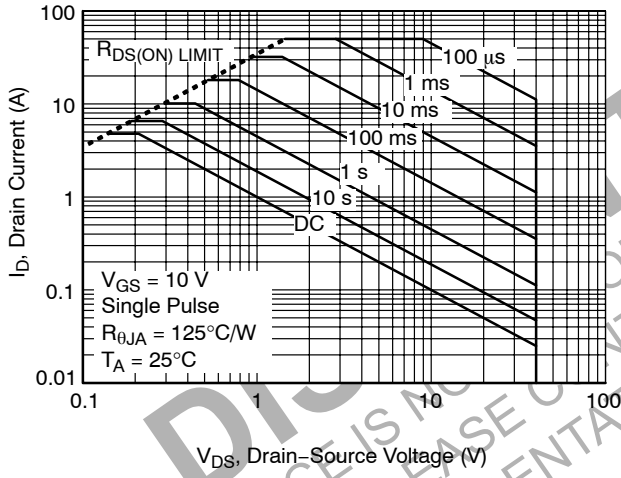



**Figure 9. Maximum Safe Operating Area**

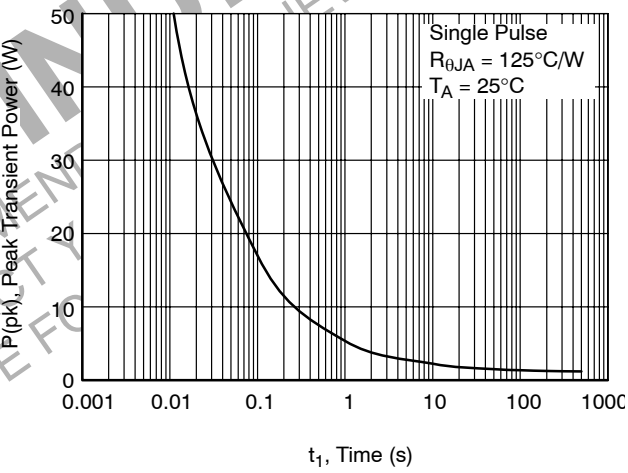



**Figure 10. Single Pulse Maximum Power Dissipation**

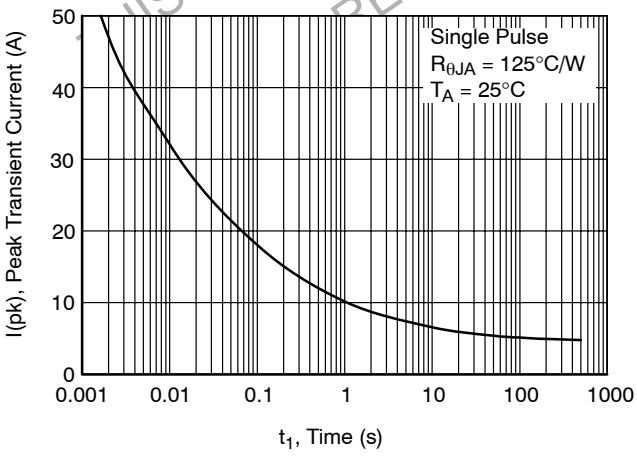



**Figure 11. Single Pulse Maximum Peak Current**

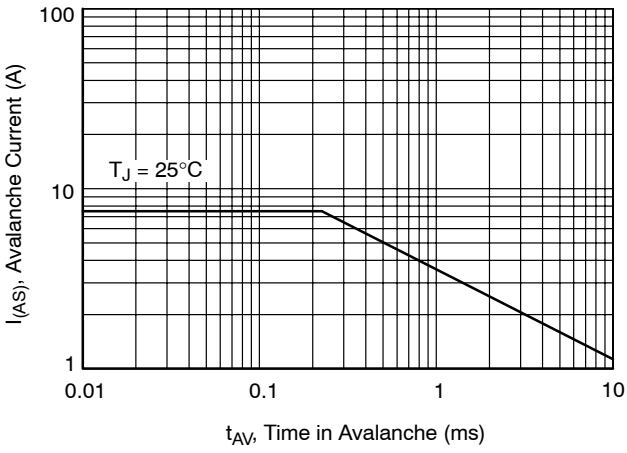



**Figure 12. Unclamped Inductive Switching Capability**

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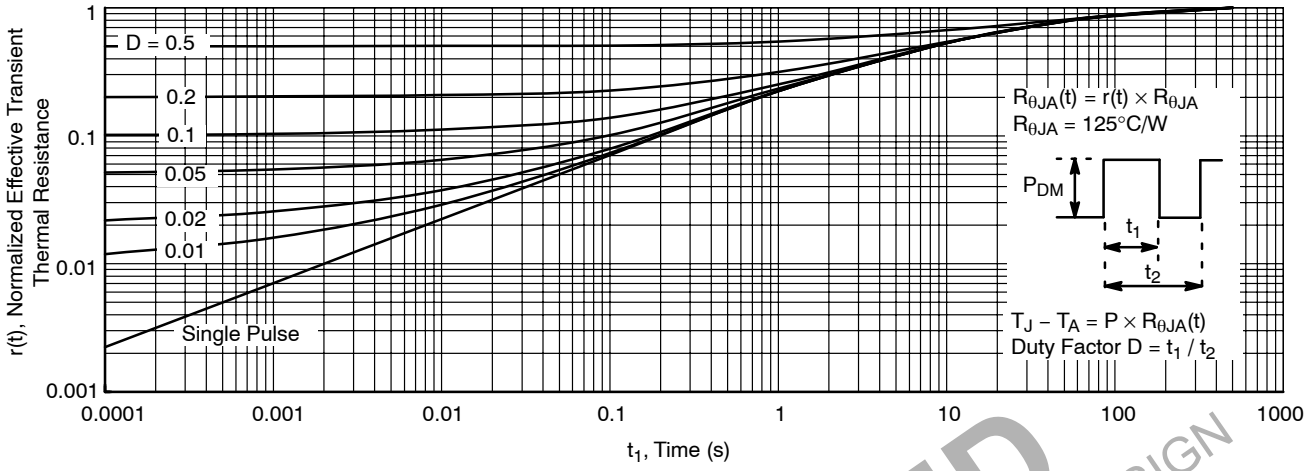



**Figure 13. Transient Thermal Response Curve**

NOTE: Transient thermal response will change depending on the circuit board design.

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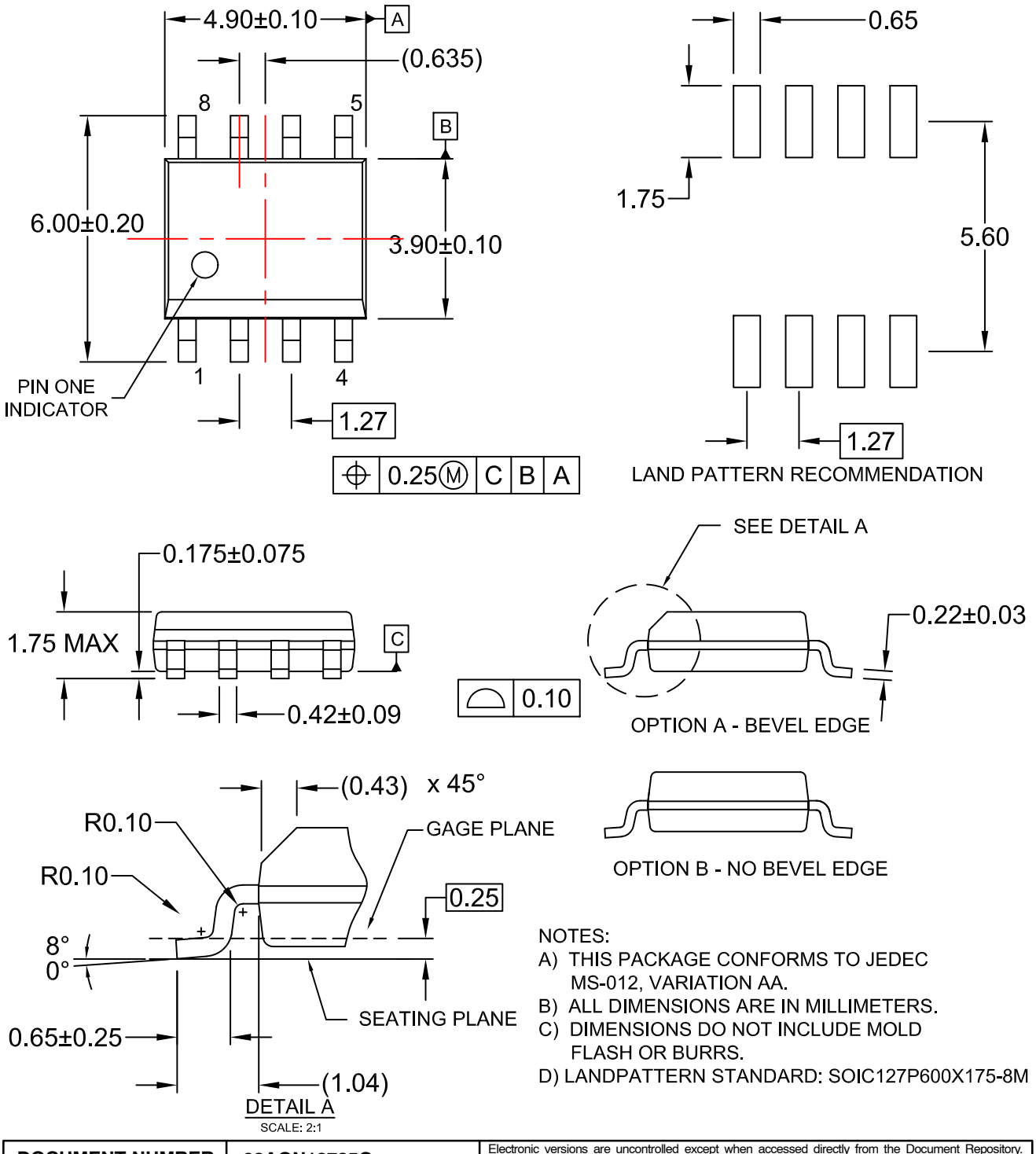
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**SOIC8**
CASE 751EB
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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