Data Sheet

AD8411A

−2 V to 70 V Wide Input Voltage Range, 2.7 MHz High Bandwidth, Current-Sense Amplifier with PWM Rejection and Gain 50 V/V

FEATURES

- 2.7 MHz small signal, −3 dB bandwidth
- In-package Trim Core (DigiTrim™)
  - Precision without chopping and/or auto-zero
  - Typical ±0.26 µV/°C offset drift
  - Maximum ±200 µV voltage-offset over temperature range
  - Typical DC CMRR: 142 dB
  - Typical AC CMRR at 50 kHz: 96 dB
- Wide common-mode input voltage range
  - −2 V to +70 V, continuous operation
  - −20 V to +85 V, continuous survival
- Initial gain: 50 V/V
- Wide operating temperature range:
  - AD8411AWB: −40°C to +125°C
  - AD8411AWH: −40°C to +150°C
- Bidirectional operation
- 2.9 V to 5.5 V power-supply operating range
- Available in 8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP packages
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- In-phase or high-side current sensing in
  - BLDC motors, low-inductance motors
  - Bidirectional 48 V to 12 V DC-DC converters
  - Solenoid controls
  - Power rail monitoring
- Low-side current sensing
- Datacenter power supply unit (PSU) and battery backup unit (BBU)

TYPICAL APPLICATION CIRCUIT

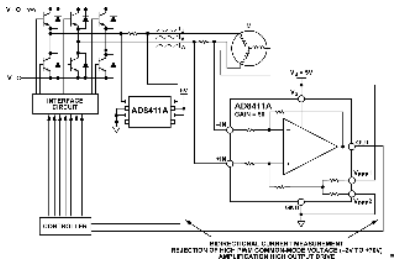

Figure 1. AD8411A in BLDC Motor Control Application

GENERAL DESCRIPTION

The AD8411A[1] is a high-voltage, high-bandwidth current-sense amplifier. The device features an initial gain of 50 V/V, with a 2.7 MHz bandwidth with a maximum ±0.15% gain error over the entire temperature range. The buffered output voltage directly interfaces with any typical converter. The AD8411A has a minimum DC common-mode rejection ratio (CMRR) of 123 dB from −2 V to +70 V. The AD8411A performs bidirectional current measurements across a shunt resistor in various industrial and automotive applications.

The AD8411A offers breakthrough performance throughout the −40°C to +150°C temperature range. The device features an in-package trim core, which leads to a typical offset drift of ±0.26 µV/°C (based on the box method, see *Figure 57*) throughout the operating temperature range and the common-mode voltage range without the need for chopping and auto-zero clocks (which could lead to intermodulation in the application). The device includes circuitry to achieve a wide input common-mode range and balanced input bias currents, regardless of input differential voltage or common-mode voltage, and circuitry to achieve ultra-low CMRR drift. The device also includes circuitry to enable output accuracy in the presence of pulse-width modulation (PWM) type input common-mode voltages. The AD8411A is available in 8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP packages.

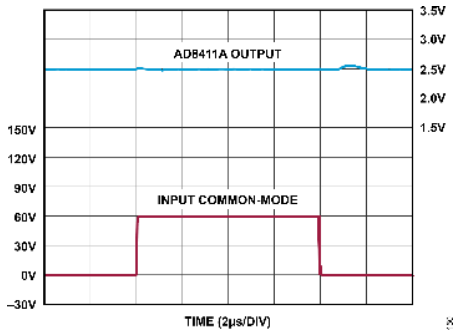

Figure 2. Input Common-Mode Step Response (0 V to 60 V), VS = 5 V, Inputs Shorted

[1] Protected by U.S. patent numbers 10,312,865 and 10,587,228

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FUNCTIONAL BLOCK DIAGRAM

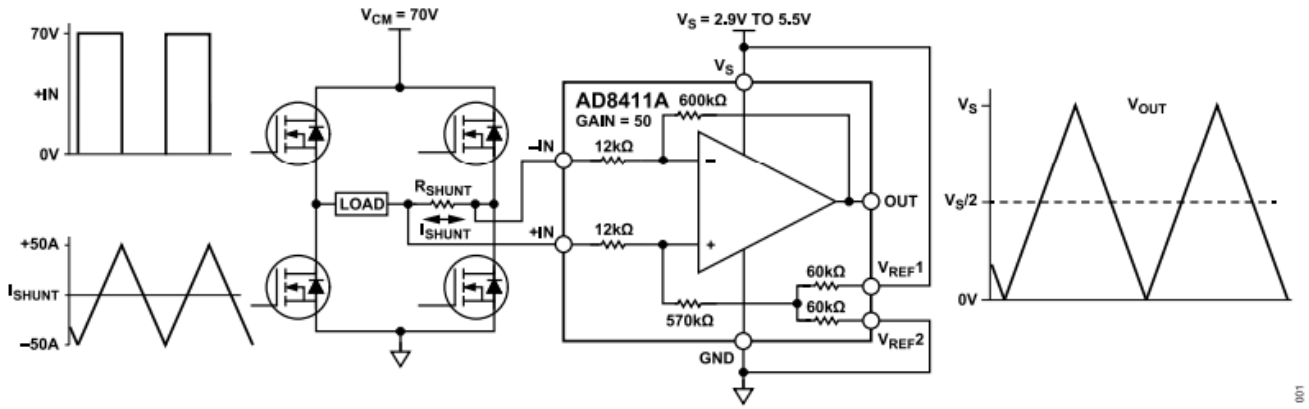

Figure 3. Functional Block Diagram

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REVISION HISTORY

REVISION	DATE	DESCRIPTION	PAGES CHANGED
D	4/26	Updated General Description, Features	1
		Updated Electrical Characteristics table (Table 1)	6–8
		Updated Absolute Maximum Ratings (Table 2)	9
		Updated Pin Descriptions titles (Tables 7 and 8)	11, 12
		Rearranged Typical Performance Characteristics 28–30	16, 17
C	2/25	Updated Electrical Characteristics table	4
		Updated Equation 2	23
B	10/24	Updated General Description, Features, Applications	1
		Updated Electrical Characteristics table	6–8
		Added Thermal Resistance (Table 3)	9
		Added ESD Ratings tables (Table 4, Table 5, and Table 6)	10
		Added 10-Lead MSOP Pin Configuration (Figure 5), Pin Descriptions (Table 8)	12
		Added Note 2	12
		Rearranged Typical Performance Characteristics 6-47	13–19
		Updated Figure 58	26
		Added Pinout Option Engineered for FMEA section	33
		Updated Outline Dimensions (Figure 69)	36
		Updated Ordering Guide, Evaluation Boards	37
A	7/2023	Changes to Data Sheet Title	1
		Changes to Features Section	1
		Changes to General Description Section	1
		Changes to Table 3	6
		Added Table 4, Renumbered Sequentially	6
		Changes to Typical Performance Characteristics Section	8
		Added Figure 11, Renumbered Sequentially	9
		Added Current Sense Layout Guidelines Section	16
		Added Choosing a Shunt Resistor Section	16
		Added Shunt Resistor Connection Section, Figure 48, and Figure 49	16
		Changes to Box Method Section	19
		Changes to Bowtie Method Section	19
		Updated Outline Dimensions	24
		Changes to Ordering Guide	24
		Changes to Evaluation Boards	24
		Added Automotive Products Section	24
0	4/23	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

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(T_A = −40°C to +125°C (operating temperature range) for the AD8411AWB, T_A = −40°C to +150°C (operating temperature range) for the AD8411AWH, supply voltage (V_S) = 5 V, ground (GND) = 0 V, input common-mode voltage (V_{CM}) = -IN, +IN =12 V, and V_{REF}^1 = V_{REF}^2 = 2.5 V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN						
Initial	A_V			50		V/V
Initial Error Over Temperature	A_{V_ERROR}	Specified temperature range			0.15	%
Initial Gain vs. Temperature					±6	ppm/°C
VOLTAGE-OFFSET (Referred to input (RTI))						
Over Temperature	V_{OS}	Specified temperature range[1]			±200	µV
Offset Drift	V_{OS_TC}	Box method (See *Figure 57*)		±0.26	±0.75	µV/°C
		Bowtie method (-40°C to 25°C) (see *Figure 58*)			±2.03	µV/°C
		Bowtie method (25°C to 125°C) (see *Figure 58*)			±1.65	µV/°C
INPUT						
Total Input-Bias Current[2]	I_B	+IN = −IN = 0 V, V_S = V_{REF}^1 = 5 V, V_{REF}^2 = 0 V	−11.0			µA
Total Input-Bias Current[2]	I_B	+IN = −IN = 12 V, V_S = V_{REF}^1 = V_{REF}^2 = 0 V, T_A = 25°C		44		µA
Total Input-Bias Current[2]	I_B	+IN = −IN = 12 V, V_S = V_{REF}^1 = 5 V, V_{REF}^2 = 0 V			350	µA
Total Input-Bias Current[2]	I_B	+IN = −IN = 48 V, V_S = V_{REF}^1 = V_{REF}^2 = 0 V, T_A = 25°C		178		µA
Total Input-Bias Current[2]	I_B	+IN = −IN = 48 V, V_S = V_{REF}^1 = 5 V, V_{REF}^2 = 0 V			484	µA
Input Offset Current	I_{OS}	+IN = −IN = 0 V			1.0	µA
		+IN = −IN = 12 V			2.5	µA
		+IN = −IN = 48 V			2.7	µA
Input Voltage Range	IVR	Common mode, continuous	−2		+70	V
Common-Mode Rejection Ratio	CMRR	Specified temperature range, DC, V_{CM} = −2 V to +70 V	123	142		dB

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(T_A = −40°C to +125°C (operating temperature range) for the AD8411AWB, T_A = −40°C to +150°C (operating temperature range) for the AD8411AWH, supply voltage (V_S) = 5 V, ground (GND) = 0 V, input common-mode voltage (V_{CM}) = -IN, +IN =12 V, and V_{REF}^1 = V_{REF}^2 = 2.5 V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		T_A = 25°C, frequency = 10 kHz		110		dB
		T_A = 25°C, frequency = 50 kHz		96		dB
OUTPUT						
Voltage Swing to GND (OUT - GND)		Load resistance (R_L) = 10 kΩ			5	mV
Voltage Swing to V_S (V_S - OUT)		Load resistance (R_L) = 10 kΩ			16	mV
Output Resistance	R_{OUT}	T_A = 25°C		0.2		Ω
Maximum Capacitive-Load	C_{Load}	No continuous oscillation, T_A = 25°C		4.7		nF
DYNAMIC RESPONSE						
Small Signal, −3 dB Bandwidth	f_{-3dB}	T_A = 25°C		2.7		MHz
Slew Rate	SR	T_A = 25°C		10		V/µs
NOISE						
0.1 Hz to 10 Hz (RTI)	$V_{N, p-p}$	T_A = 25°C		7.5		µV p-p
Spectral Density, 1 kHz (RTI)	V_N	T_A = 25°C		40		nV/√Hz
Spectral Density, 10 kHz (RTI)	V_N	T_A = 25°C		30		nV/√Hz
OFFSET ADJUSTMENT						
Ratiometric Accuracy[3]		V_{REF} pins divider to supply	0.499		0.501	V/V
Accuracy, Referred to the Output (RTO)		V_{REF} error when using an external reference of 2.5 V applied to V_{REF}^1 and V_{REF}^2 in parallel			±1	mV/V
$V_{REF}^{1,2}$ Input Voltage Range			GND		V_S	V
$V_{REF}^{1,2}$ Divider Resistor Values				60		kΩ
POWER SUPPLY						
Operating Voltage Range	V_S		2.9		5.5	V

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(T_A = −40°C to +125°C (operating temperature range) for the AD8411AWB, T_A = −40°C to +150°C (operating temperature range) for the AD8411AWH, supply voltage (V_S) = 5 V, ground (GND) = 0 V, input common-mode voltage (V_{CM}) = -IN, +IN =12 V, and V_{REF}^1 = V_{REF}^2 = 2.5 V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_q	Output voltage (V_{OUT}) = 2.5 V DC, T_A = 25°C		7.8		mA
		V_{OUT} = 2.5 V DC			10.8	mA
Power Supply Rejection Ratio	PSRR	V_S from 3 V to 5 V, Specified temperature range	84	120		dB
TEMPERATURE RANGE						
For Specified Performance		Operating temperature range (AD8411AWB)	−40		+125	°C
		Operating temperature range (AD8411AWH)	−40		+150	°C

1 Guaranteed by test and characterization

2 To see input bias current per pin, see *Figure 15* and *Figure 16*.

3 The offset adjustment is ratiometric to the power supply when V_{REF}^1 and V_{REF}^2 are used as dividers between the supplies.

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage (V_S to GND)	6V
Input Voltage Range, Continuous Common-Mode (+IN to GND)	−20V to +85V
Input Voltage Range, Continuous Common-Mode (−IN to GND)	−20V to +85V
Input Voltage Range, Differential (+IN to −IN)	± 20V
V_{REF}[1], V_{REF}[2]	GND − 0.3 V to V_S + 0.3 V
Reverse Supply Voltage	0.3V
Operating Temperature Range	
AD8411AWB	−40°C to +125°C
AD8411AWH	−40°C to +150°C
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit Duration	Indefinite

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JB} is the junction-to-board thermal resistance. θ_{JCT} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	θ_{JCT}	Unit
R-8	142.8	140.6	64.01	°C/W
RM-8	152	120.6	59.7	°C/W
RM-10	172.6	144.2	33.3	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board for θ_{JA}, JEDEC 2S2P thermal impedance with ring style cold plate attached to PCB for θ_{JB}, and a JEDEC 1S0P thermal test board for θ_{JCT}. See JEDEC JESD-51.

Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

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Field-induced robotic charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD8411A

Table 4. AD8411A, 8-Lead SOIC_N

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1000	C3

Table 5. AD8411A, 8-Lead MSOP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

Table 6. AD8411A, 10-Lead MSOP

ESD Model	Withstand Threshold (V)	Class
FICDM	±1000	C3

ESD Caution

	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 4. 8-Lead MSOP and 8-Lead SOIC Pin Configuration

8-Lead Pin Descriptions

Table 7. Pin Descriptions

PIN	NAME	DESCRIPTION
1	-IN	Negative Input.
2	GND	Ground.
3	V_{REF}[2]	Reference Input 2.
4	NC	No Connect.[1]
5	OUT	Output.
6	V_S	Supply Voltage.
7	V_{REF}[1]	Reference Input 1.
8	+IN	Positive Input.

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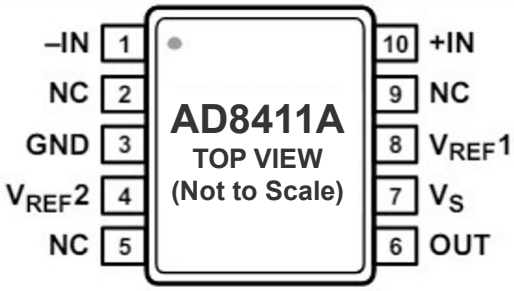

Figure 5. 10-Lead MSOP Pin Configuration

10-Lead Pin Descriptions

Table 8. Pin Descriptions

PIN	NAME	DESCRIPTION
1	-IN	Negative Input.
2	NC	No Connect.[2]
3	GND	Ground.
4	V_{REF}[2]	Reference Input 2.
5	NC	No Connect.[1]
6	OUT	Output.
7	V_S	Supply Voltage.
8	V_{REF}[1]	Reference Input 1.
9	NC	No Connect.[2]
10	+IN	Positive Input.

[1] This NC pin is connected internally to the die. It can be left floating or tied to GND.

[2] This NC pin is not connected internally and is used for FMEA requirement to isolate the voltages at the input pins. It should be left floating.

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TYPICAL PERFORMANCE CHARACTERISTICS

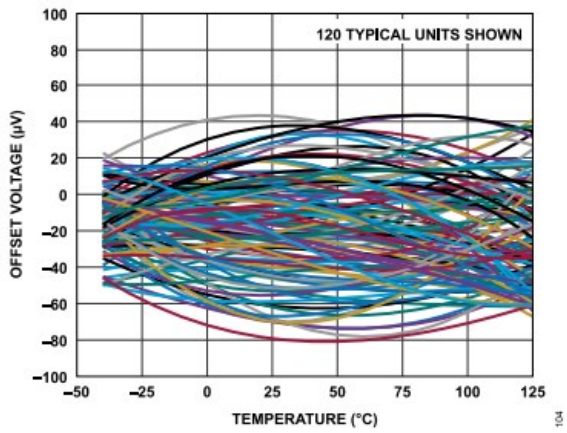

Figure 6. Offset Voltage vs. Temperature

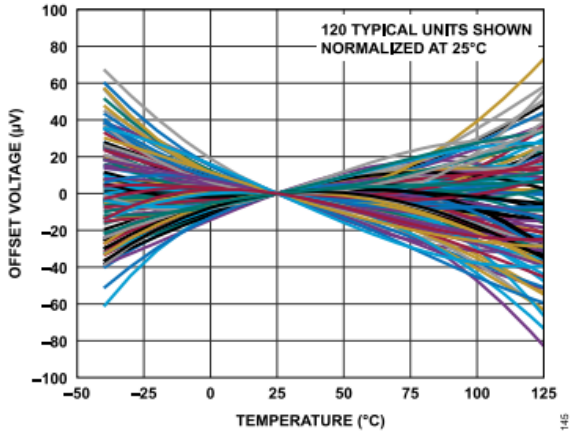

Figure 7. Offset Voltage vs. Temperature, Normalized at 25°C

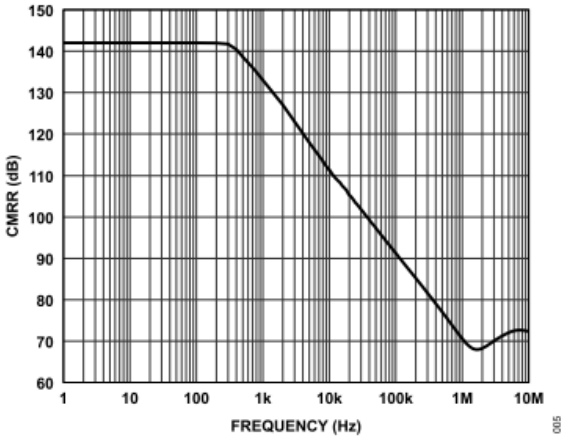

Figure 8. CMRR vs. Frequency

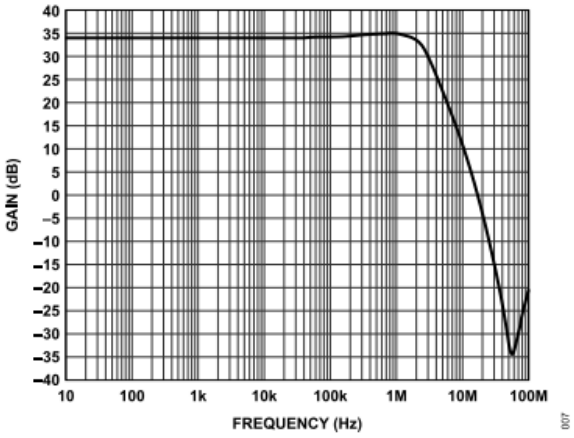

Figure 9. Typical Small Signal Bandwidth, V_{OUT} = 200 mV p-p

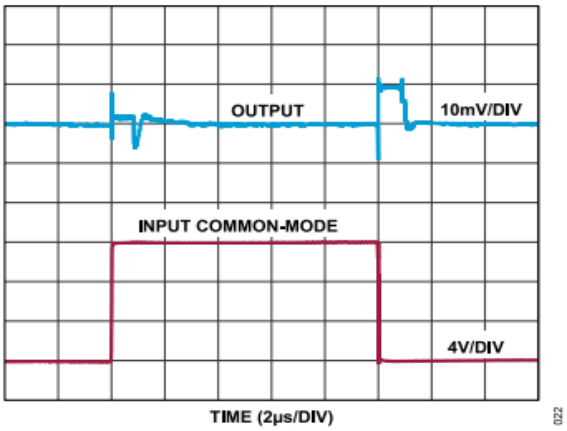

Figure 10. Input Common-Mode Step Response (0 V to 12 V), V_S = 5 V, Inputs Shorted

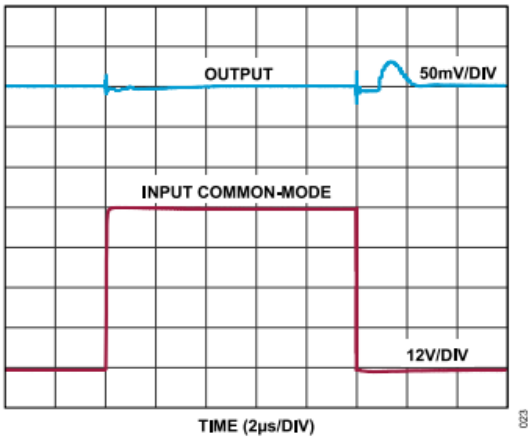

Figure 11. Input Common-Mode Step Response (0 V to 48 V), V_S = 5 V, Inputs Shorted

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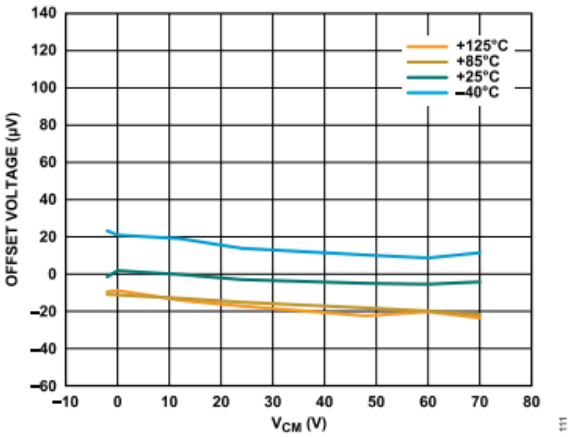

Figure 12. Offset Voltage vs. Common-Mode Voltage

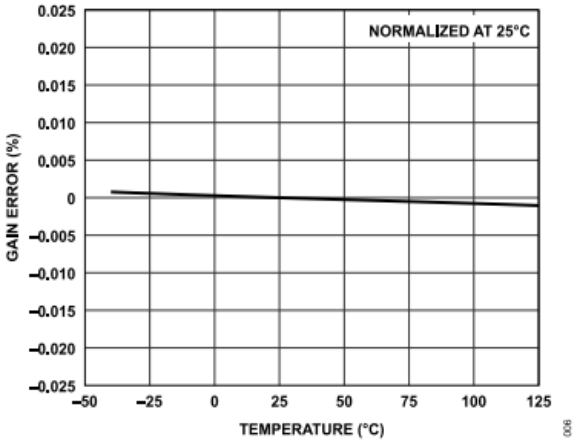

Figure 13. Gain Error vs. Temperature

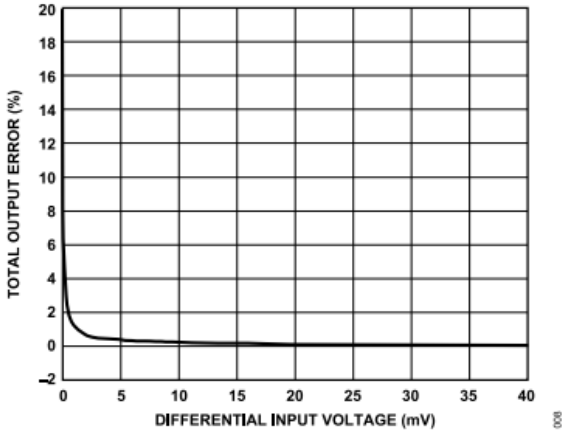

Figure 14. Total Output Error vs. Differential Input Voltage

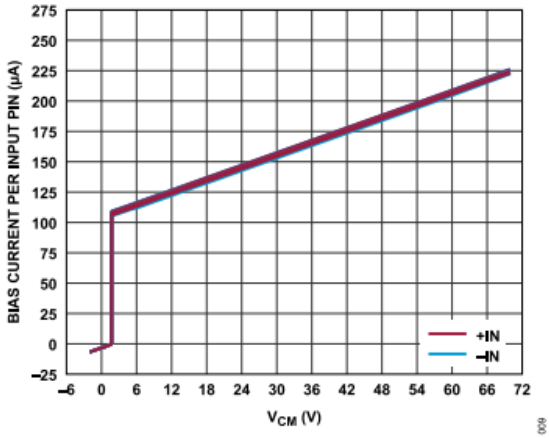

Figure 15. Bias Current Per Input Pin vs. VCM, V_S = 5 V

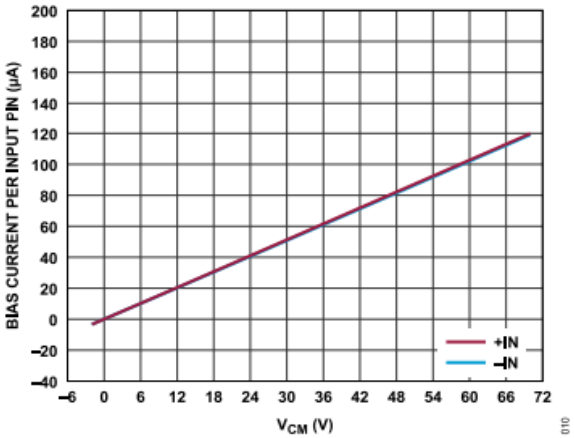

Figure 16. Bias Current Per Input Pin vs. VCM, V_S = 0 V, R_L = 10 kΩ

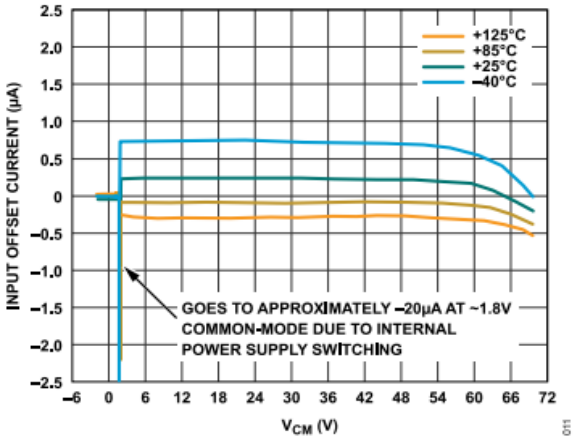

Figure 17. Input Offset Current vs. VCM at Various Temperatures

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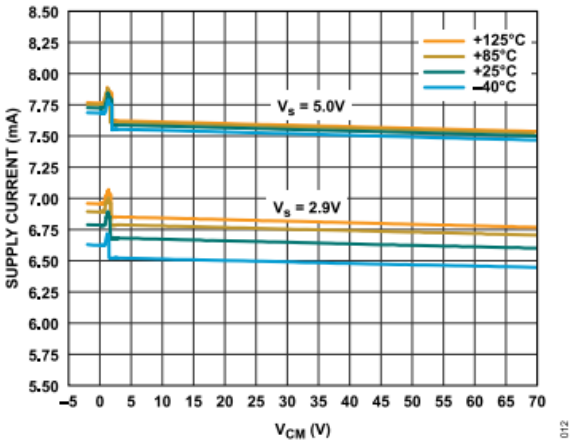

Figure 18. Supply Current vs. Input VCM at Various Temperatures and Supply Voltages

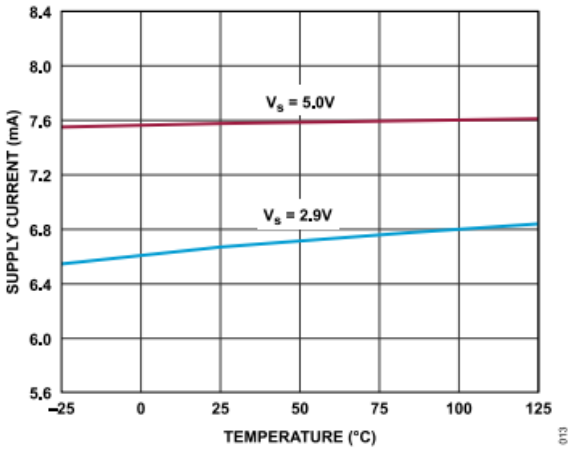

Figure 19. Supply Current vs. Temperature at Various Supply Voltages

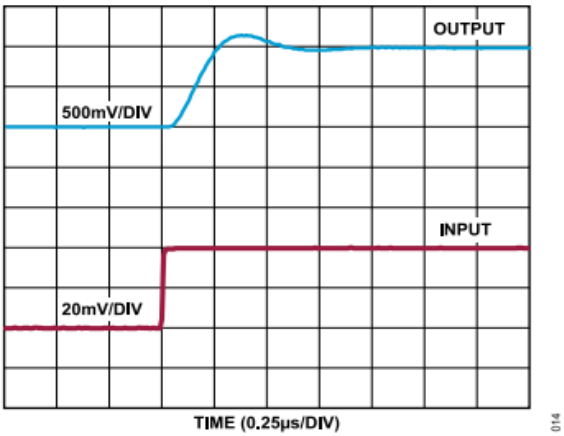

Figure 20. Rise Time, V_S = 2.9 V

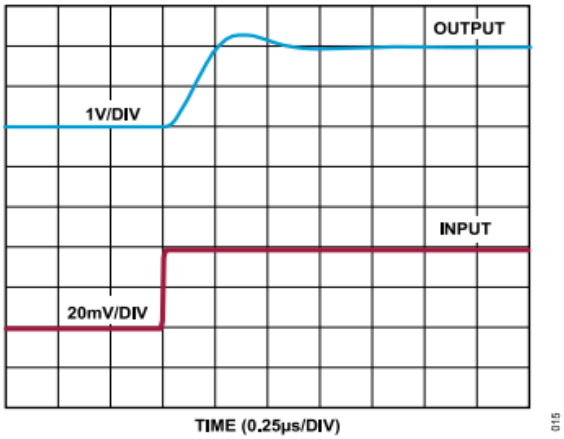

Figure 21. Rise Time, V_S = 5 V

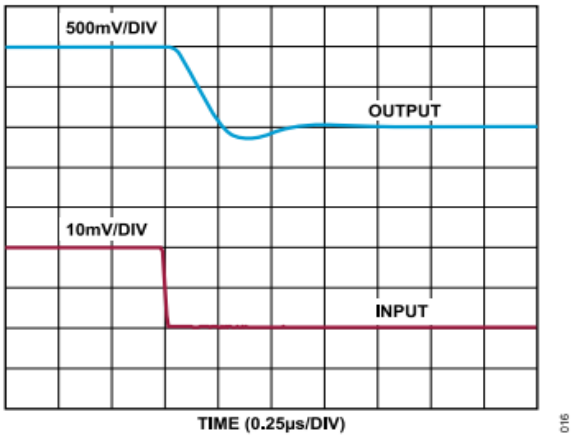

Figure 22. Fall Time, V_S = 2.9 V

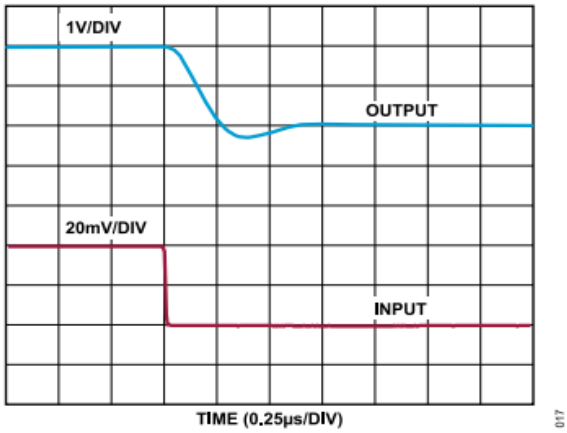

Figure 23. Fall Time, V_S = 5 V

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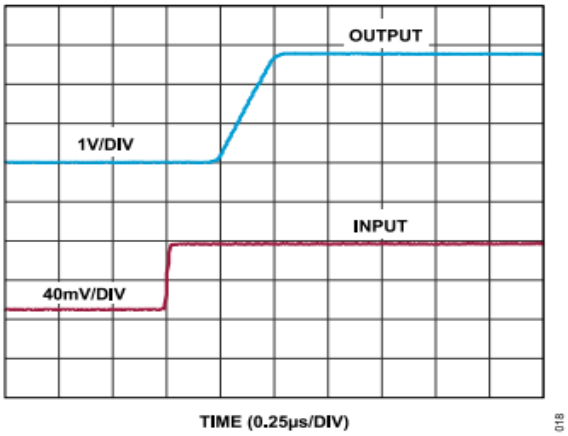

Figure 24. Differential Overload Recovery, Rising, V_S = 2.9 V

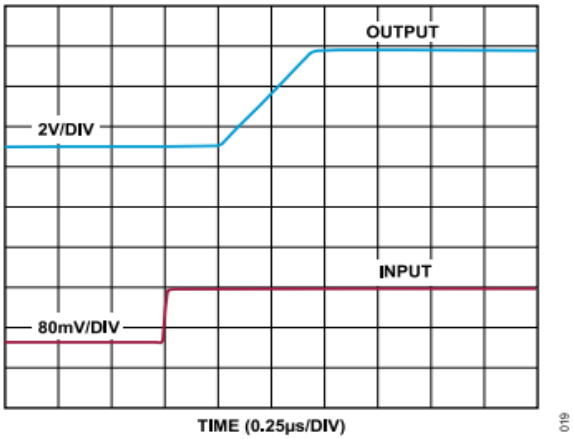

Figure 25. Differential Overload Recovery, Rising, V_S = 5 V

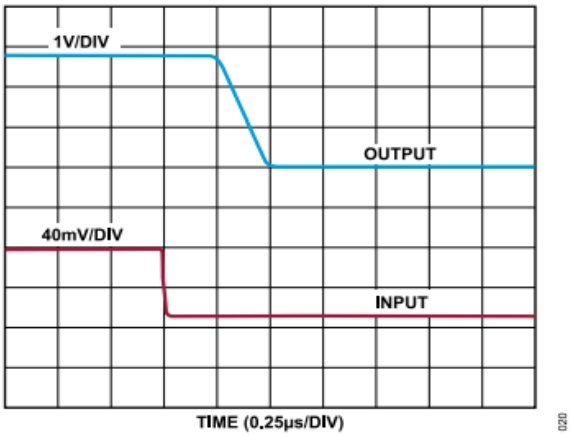

Figure 26. Differential Overload Recovery, Falling, V_S = 2.9 V

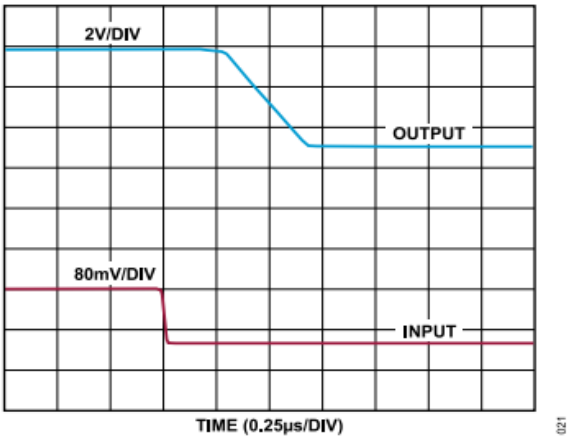

Figure 27. Differential Overload Recovery, Falling, V_S = 5 V

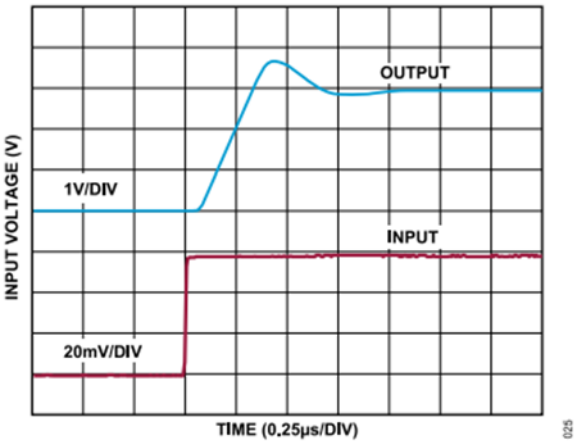

Figure 28. Large Signal Response, Rising, V_S = 5 V

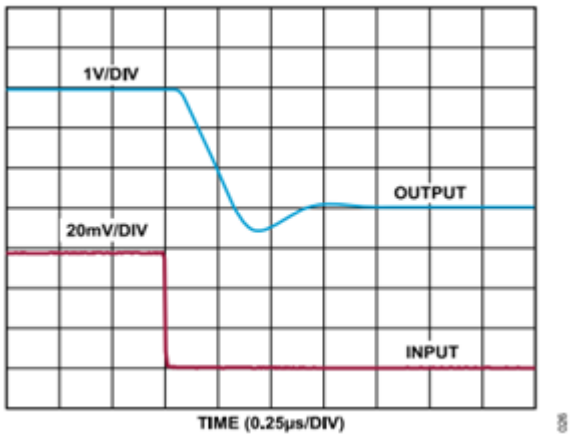

Figure 29. Large Signal Response, Falling, V_S = 5 V

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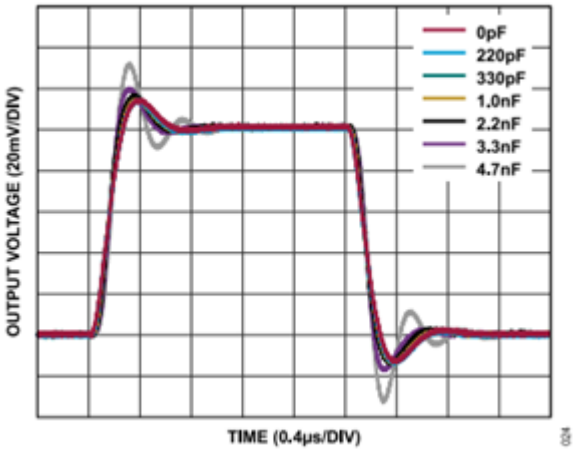

Figure 30. Small Signal Response for Various Capacitive Loads

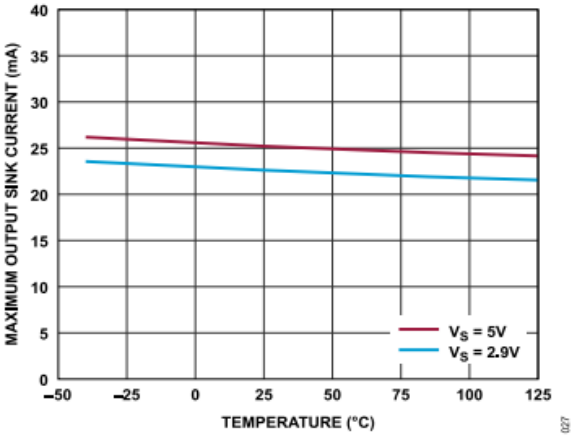

Figure 31. Maximum Output Sink Current vs. Temperature at Various Supply Voltages

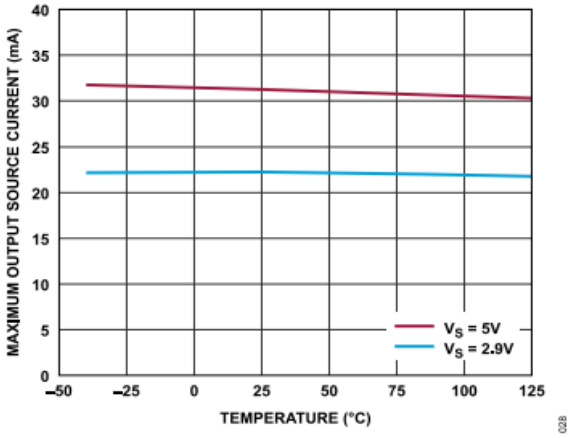

Figure 32. Maximum Output Source Current vs. Temperature at Various Supply Voltages

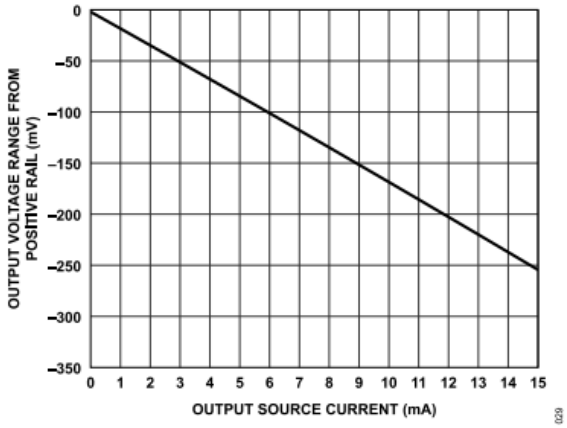

Figure 33. Output Voltage Range from Positive Rail vs. Output Source Current

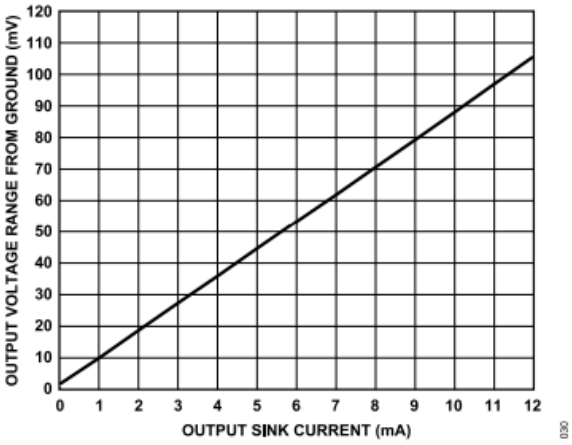

Figure 34. Output Voltage Range from Ground vs. Output Sink Current

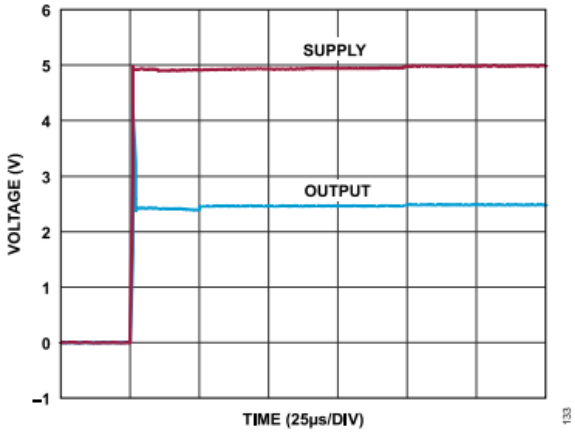

Figure 35. Start-Up Response

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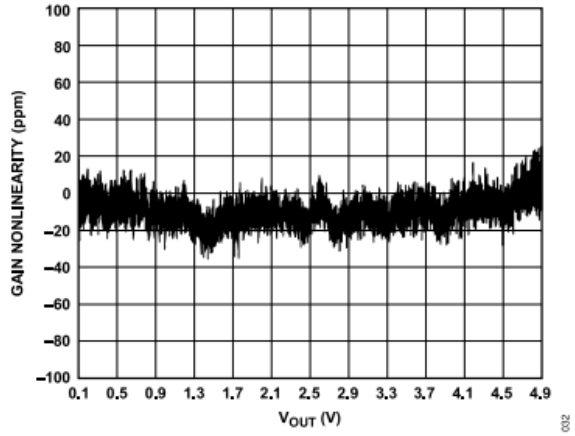

Figure 36. Gain Nonlinearity vs. Output Voltage, V_S = 5 V

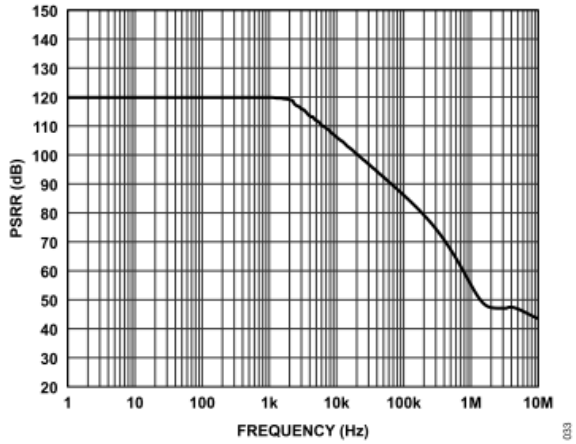

Figure 37. PSRR vs. Frequency

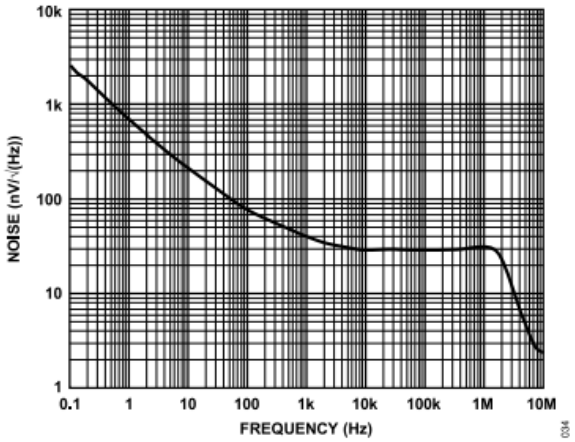

Figure 38. Spectral Density, RTI

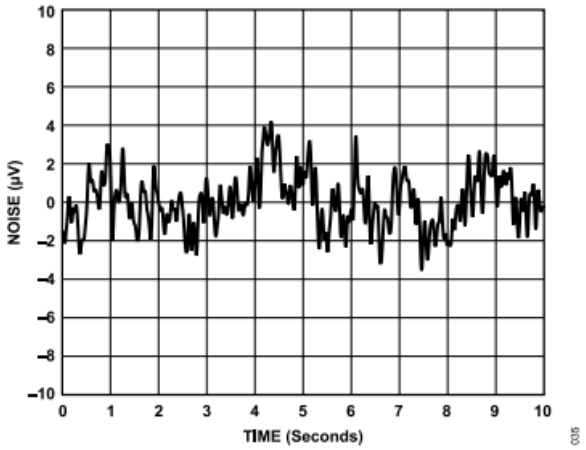

Figure 39. 0.1 Hz to 10 Hz Noise, RTI

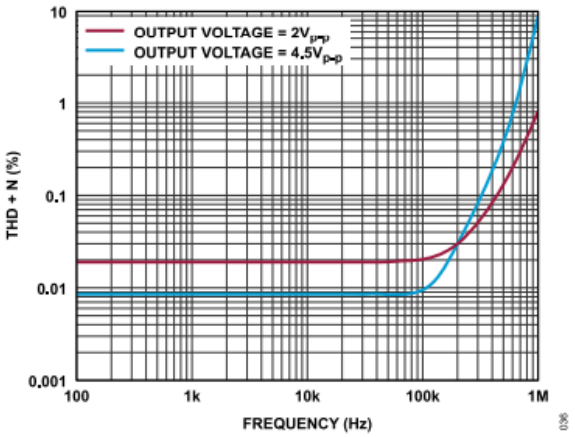

Figure 40. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

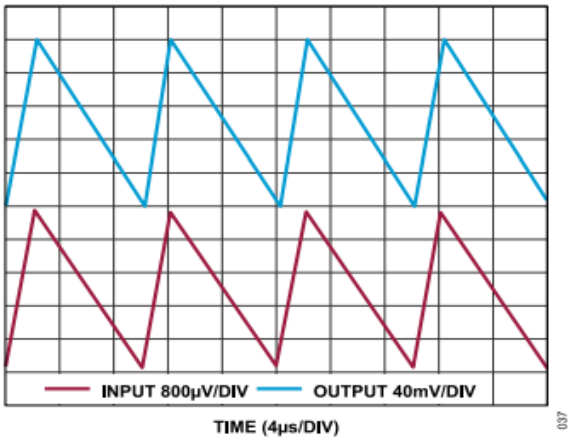

Figure 41. Output Response for 100 kHz, 20% Duty-Cycle, Sawtooth Waveform, Input Voltage(V_{IN}) = 4mVp-p

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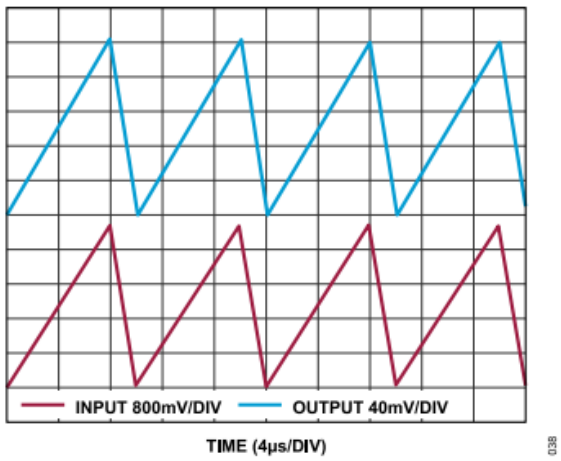

Figure 42. Output Response for 100 kHz, 80% Duty-Cycle, Sawtooth Waveform, Input Voltage(V_{IN}) = 4mVp-p

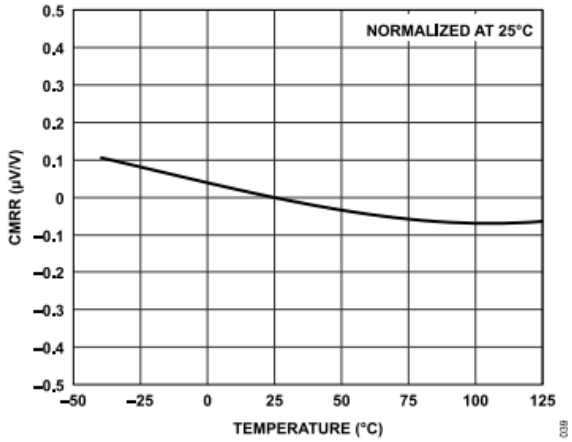

Figure 43. CMRR vs. Temperature

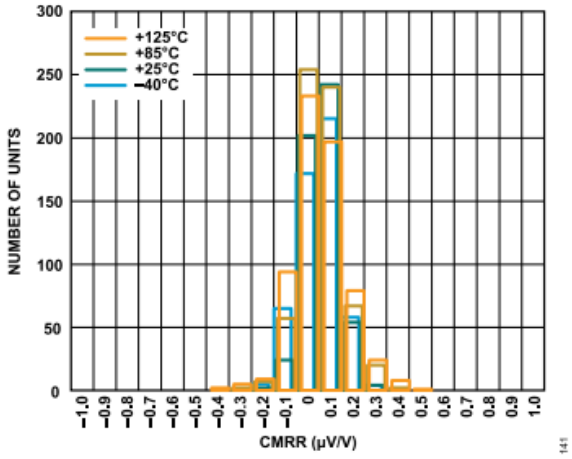

Figure 44. CMRR Distribution

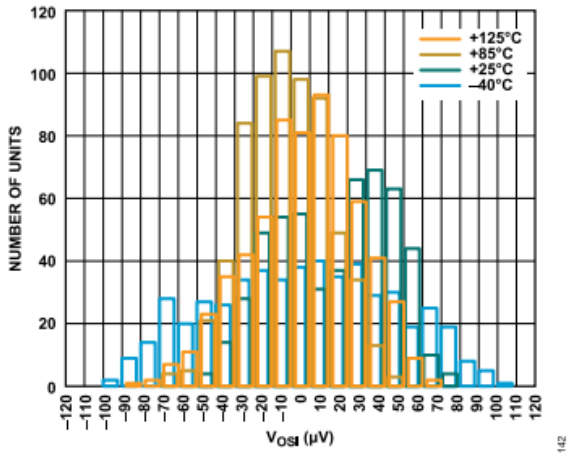

Figure 45. Offset Voltage (VOS) Distribution, RTO

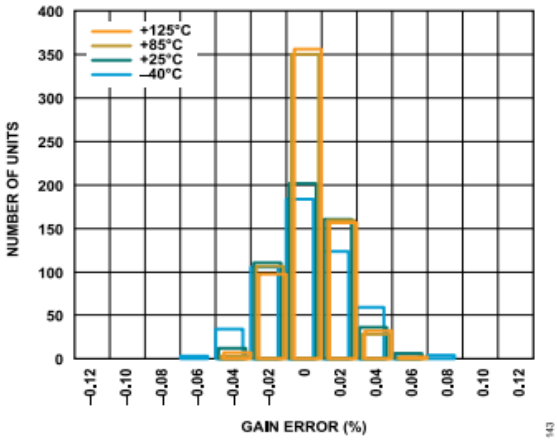

Figure 46. Gain Error Distribution

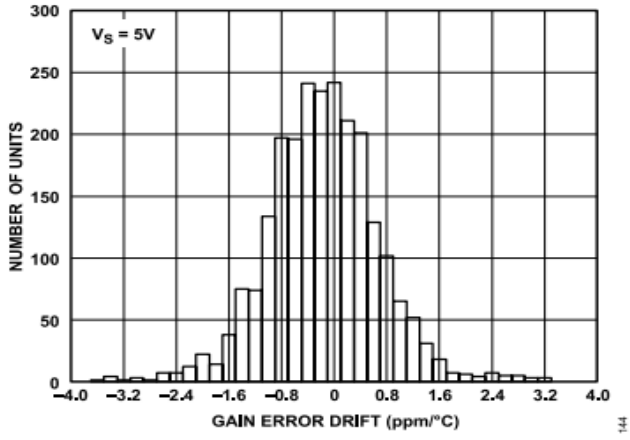

Figure 47. Gain Error Drift Distribution

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THEORY OF OPERATION

The AD8411A is a wide input voltage range, high bandwidth current-sense amplifier with PWM rejection that uses a unique architecture to accurately amplify the small differential current shunt voltages in the presence of rapidly changing common-mode voltages.

In typical applications, the AD8411A measures the current by amplifying the voltage across a shunt resistor connected to the inputs by a gain of 50 V/V (see *Figure 48*).

The AD8411A design provides excellent common-mode rejection, even with PWM common-mode inputs that can change at fast rates, such as 1 V/ns. The AD8411A has internal deglitch circuitry that helps to reduce the negative effects (such as the amplitude and settling time) of the output response in the presence of common-mode PWM input signals typically found in the applications for current-sense amplifiers. When there is a large common-mode transient at the input of the AD8411A, the output of the AD8411A is held at the last value for about 1 µs. This allows the change in the amplitude of the output of the AD8411A after a VCM step to remain low and undisturbed. After the typical 1 µs deglitch time, the output begins to settle to the appropriate value based on the differential voltage across the shunt resistor at the inputs (see *Figure 10* and *Figure 11).*

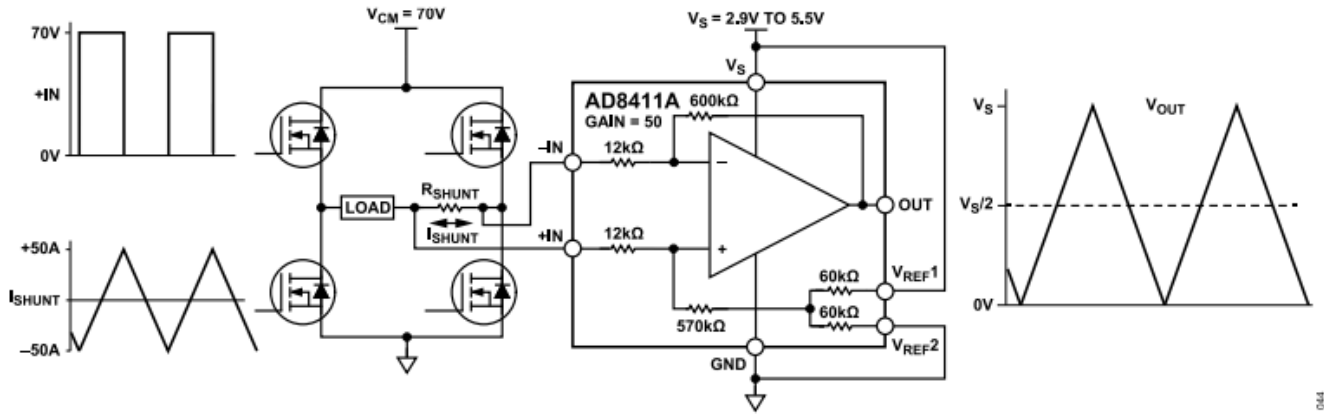

Figure 48. Typical Application

The AD8411A features an in-package trim core, which leads to a typical offset drift of ±0.26 µV/°C throughout the operating temperature range and the common-mode voltage range without the need for chopping and autozero clocks (which can lead to intermodulation in the application). This architecture does not compromise bandwidth, which is typically rated at 2.7 MHz.

The reference input pins, $V_{REF}{}^1$ and $V_{REF}{}^2$, are connected through 60 kΩ resistors to the positive input of the main amplifier, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1 V/V from the reference pins to the output when the reference pins are used in parallel. When the reference pins are used to divide the supply, the gain is 0.5 V/V.

The AD8411A offers breakthrough performance without compromising the robust application needs typical of solenoid control, motor control, or DC-DC converters. The ability to reject PWM input common-mode voltages, and the DigiTrim™ architecture providing low offset and offset drift, allows the AD8411A to deliver total accuracy for these demanding applications.

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CURRENT-SENSE LAYOUT GUIDELINES

Choosing a Shunt Resistor

There are different factors to consider in selecting the appropriate shunt resistor, including the resistor value, size, cost, tolerance, power dissipation, and thermal drift.

Commonly, the resistor value is selected based upon the desired maximum differential voltage generated at the highest expected current, while considering the power loss budget. Another consideration is to ensure the output is maximized at full-scale current, taking full advantage of the available system dynamic range. Choosing the shunt resistor, R_{SHUNT}, value is often a compromise between these two considerations.

$$R_{SHUNT} = V_{DIFF, MAX}/I_{MAX} \qquad (1)$$

The shunt resistor tolerance directly affects the accuracy of the overall gain error of the current measurement. The AD8411A is specified to have a maximum gain error of 0.15% over the specified temperature range from −40°C to +125°C. For optimal performance, select a 0.1% shunt resistor (or with lower tolerance) that does not introduce more gain error than the AD8411A.

The power dissipation in the shunt resistor is calculated using the equation: $P = I^2R$. Thus, a higher resistance results in higher power dissipation. Power dissipation in the shunt resistor leads to self heating, resulting in an increase in the temperature of the shunt resistor. Any change in shunt resistor temperature due to self heating can result in a nonlinear error. Selecting a shunt resistor with a low temperature coefficient minimizes any self heating of the shunt and minimizes any thermal nonlinearities.

The thermal drift of the voltage developed across the shunt resistor varies in relationship to the power dissipated by the resistor.

Shunt Resistor Connection

The shunt resistor, R_{SHUNT}, is connected between the input pins of the current-sense amplifier, which is shown in *Figure 49.* Typically, the shunt resistor has very low resistance. Thus, it is recommended to use a Kelvin (4-wire) connection on the shunt to achieve high-accuracy current-sense measurement. A proper Kelvin connection avoids sensing across any parasitic PCB trace resistance.

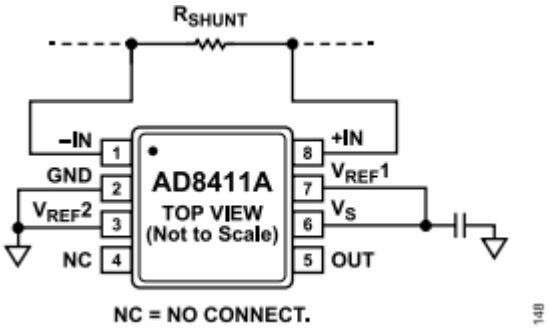

Figure 49. Shunt Resistor Layout

There are different ways to make the Kelvin connection to the R_{SHUNT} resistor. *Figure 50* shows a test board of five different layouts to verify which is the best layout to optimize high-current sensing accuracy. Based on the Analog Dialogue article, "**Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low Value Shunt Resistors**" (Volume 46, June 2012), the sense points must be considered by placing them at the outer extremity of the resistor. The article shows that it was experimentally determined that the layouts with the lowest errors are Style C and Style D. Layout Style C is preferred because component placement tolerance issues are less likely to arise.

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Without a Kelvin connection, measuring across the top pad (i.e., across the main high-current pad) of footprint E in *Figure 50*, there is about a 22.8% error. Therefore, it is better to use a Kelvin connection when using a low-value R_{SHUNT} to obtain more accurate current-sense measurements.

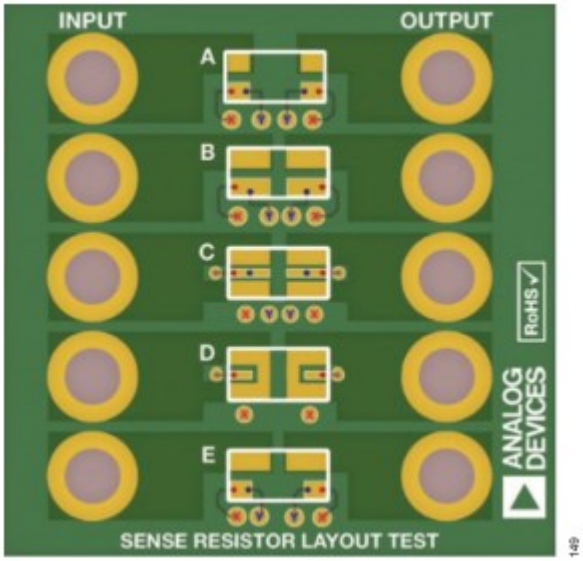

Figure 50. Sample R_{SHUNT} Layout Board

OUTPUT OFFSET ADJUSTMENT

The output of the AD8411A can be adjusted for unidirectional or bidirectional operation.

Unidirectional Operation

Unidirectional operation allows the AD8411A to measure currents through a resistive shunt in one direction. The basic modes for unidirectional operation are ground referenced output mode and V_S referenced output mode. For unidirectional operation, the output can be set at the negative rail (near ground) or at the positive rail (near V_S) when the differential input is 0 V. The output moves to the opposite rail when a correct polarity differential input voltage is applied. The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to decrease the output. If the output is set at ground, the polarity must be positive to increase the output.

Ground Referenced Output Mode

When using the AD8411A in ground referenced output mode, both referenced inputs are connected to the GND pin, which causes the output to sit at the negative rail when there are zero differential volts at the input (see *Figure 51*).

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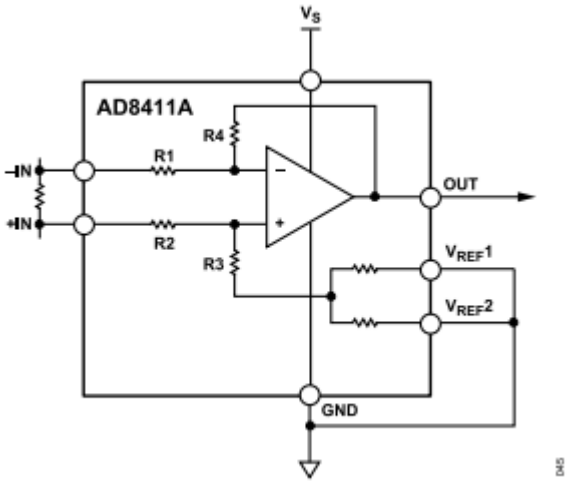

Figure 51. Ground Referenced Output

V_S Referenced Output Mode

V_S referenced output mode is set when both reference pins are tied to the positive supply. This mode is typically used when the diagnostic scheme requires the detection of the amplifier and the wiring before power is applied to the load (see *Figure 52*).

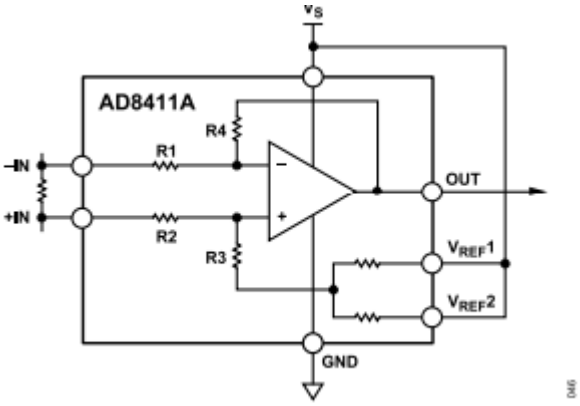

Figure 52. V_S Referenced Output

Bidirectional Operation

The bidirectional operation allows the AD8411A to measure the currents through a resistive shunt in two directions.

In this case, the output is set anywhere within the output range. Typically, the output is set at half-scale for an equal range in both directions. In some cases, however, the output is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

Adjusting the output is accomplished by applying DC voltage to the reference inputs. $V_{REF}{}^1$ and $V_{REF}{}^2$ are connected to internal resistors that connect to an internal node. There is no operational difference between the reference pins.

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External Referenced Output

Tie V_{REF}^1 and V_{REF}^2 together and to a reference to produce an output equal to the reference voltage when there is no differential input (see *Figure 53*). The output decreases with respect to the reference voltage when the input is negative, relative to the −IN pin, and increases when the input is positive, relative to the −IN pin.

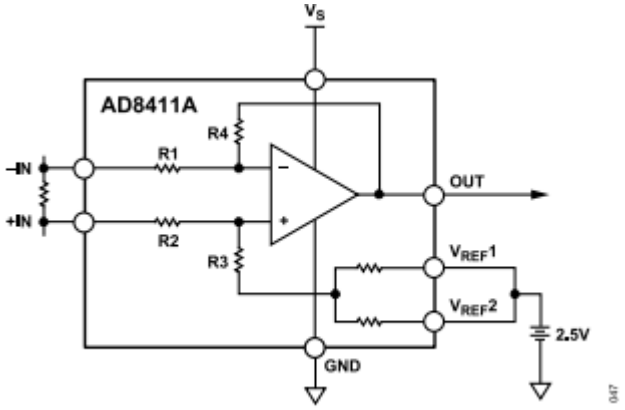

Figure 53. External Referenced Output

Splitting the Supply

By tying one reference pin to the V_S pin and the other reference pin to the GND pin, the output is set at half of the supply when there is no differential input (see *Figure 54*). The benefit of this configuration is that an external reference is not required to offset the output for bidirectional current measurement. Tying one reference pin to the V_S pin and the other reference pin to the GND pin creates a midscale offset that is ratiometric to the supply, which means that if the supply increases or decreases, the output remains at half the supply. For example, if the supply is 5.0 V, the output is at half-scale or 2.5 V. If the supply increases by 10% (to 5.5 V), the output increases to 2.75 V.

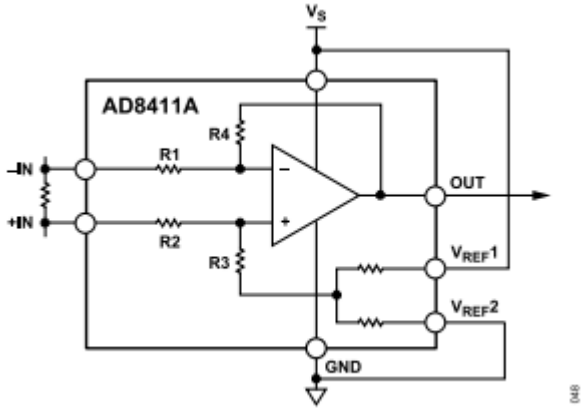

Figure 54. Split Supply

Splitting an External Reference

Use the internal reference resistors to divide an external reference by 2 with an accuracy of approximately 0.5%. Split an external reference by connecting one V_{REF}^X pin to the GND pin and the other V_{REF}^X pin to the reference voltage (see *Figure 55*).

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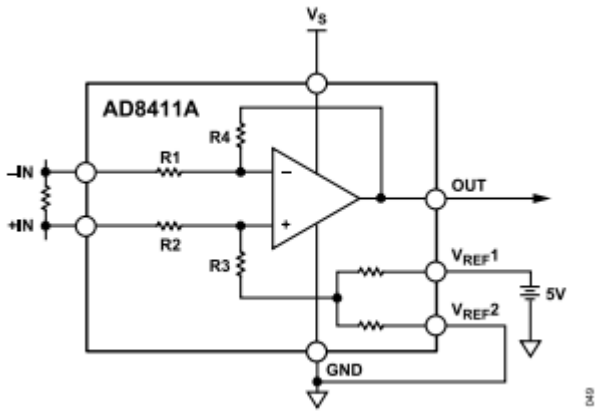

Figure 55. Split External Reference

OFFSET VOLTAGE TERMINOLOGY

BOX METHOD

The AD8411A features an in-package trim core, which leads to a typical offset drift of ±0.26 µV/°C (using the box method) throughout the operating temperature range and the common-mode voltage range. This architecture does not compromise bandwidth, but the offset voltage drift signatures for the AD8411A vary part to part as shown in *Figure 56*. After observing the minimum and maximum value for V_{OS} over the full temperature range from −40°C to 125°C, the V_{OS} in µV/°C is calculated for each part using the box method.

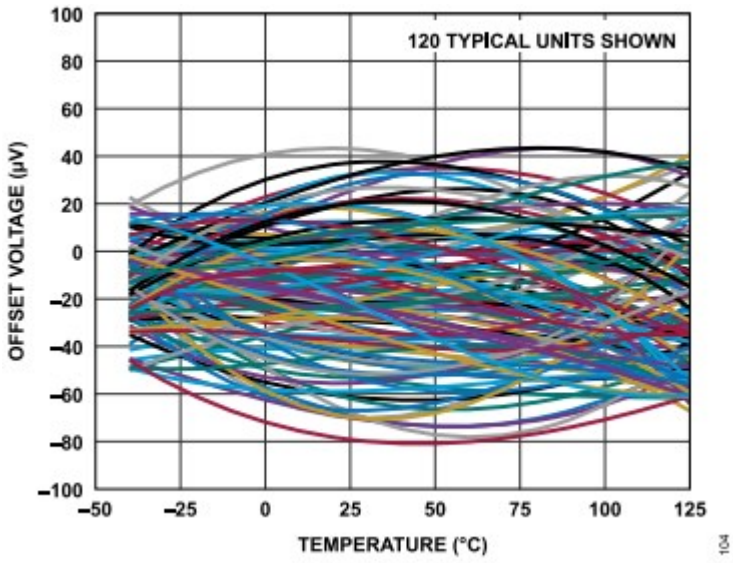

Figure 56. Offset Voltage vs. Temperature

A visual representation of this box method calculation and the mean value for the V_{OS} drift using the box method is shown in *Figure 57*. Based on the mean (typ) value of ±0.26 µV/°C and the standard deviation of the box method drift of the 120 parts from *Figure 56*, a user can calculate a value (see Equation 2) for a guarantee V_{OS} drift by characterization, ±0.75 µV/°C.

$$\pm \text{MAX}(\text{ABS}(\text{MEAN} + 5 \times (\text{STANDARD DEVIATION}))) \quad (2)$$

This is valid over the −40°C to 125°C temperature range.

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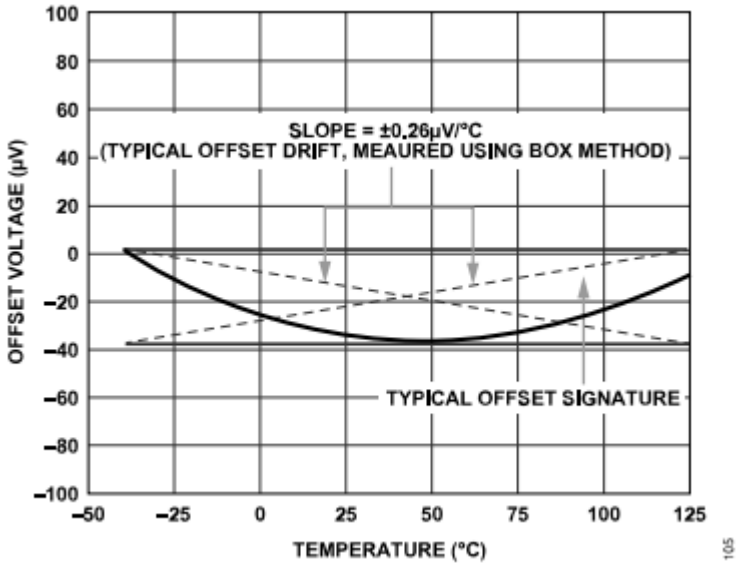

Figure 57.Box Method

BOWTIE METHOD

Typically, in the applications where the AD8411A is used, a calibration is done at 25°C. If a single point calibration at 25°C is done on the 120 parts as shown in *Figure 56*, this creates a plot shown in *Figure 58*. For each part, the slope of the line from 25°C to −40°C is calculated and the slope from 25°C to 125°C for each part is calculated. The mean and standard deviation for the slope of all the parts from 25°C to −40°C is then calculated. The V_{OS} max drift of ±2.03 µV/°C using the bowtie method is then calculated using Equation 2. The mean and standard deviation for the slope of all the parts from 25°C to 125°C is then calculated. The V_{OS} max drift of ±1.65 µV/°C using the bowtie method is then calculated using Equation 2. The red lines in *Figure 58* represent the worst-case V_{OS} drift slopes using the bowtie method that a user can guarantee through characterization. Calibrating at 25°C allows the max V_{OS} over the full temp range to be reduced to ~±165 µV, as opposed to the ±200 µV listed in the **Specifications** section as the max V_{OS} over temperature (with no calibration).

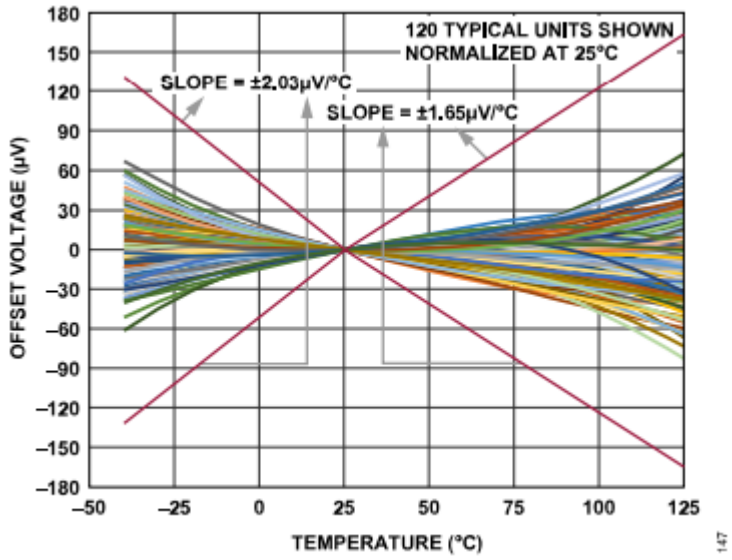

Figure 58. Bowtie Method

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APPLICATIONS INFORMATION

Motor Control

3-Phase Motor Control

The AD8411A is ideally suited for monitoring current in 3-phase motor applications such as brushless DC motors.

The 2.7 MHz typical bandwidth of the AD8411A provides instantaneous current monitoring. Additionally, the typical low offset drift of ±0.26 µV/°C means that the measurement error between the two motor phases is at a minimum over temperature. The AD8411A rejects PWM input common-mode voltages in the −2 V to +70 V range. Monitoring the current on the motor phase allows sampling of the current at any point and provides diagnostic information, such as a short to ground and battery. The DigiTrim™ architecture used in the AD8411A provides precision specifications without the need for chopping and/or auto-zeroing. The DigiTrim™ architecture of the AD8411A avoids the potential for intermodulation distortion, which is observed when using amplifiers with chopping/auto-zero architectures. For the typical phase current measurement setup with the AD8411A, see *Figure 59*.

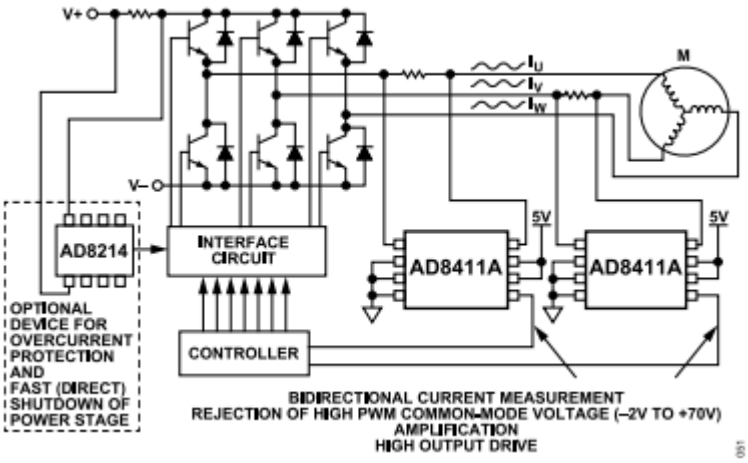

Figure 59. 3-Phase Motor Control

H-Bridge Motor Control

Another typical application for the AD8411A is to form part of the control loop in H-bridge motor control. In this case, place the shunt resistor in the middle of the H-bridge to accurately measure current in both directions by using the shunt available at the motor (see *Figure 60*). Using an amplifier and shunt in this location is a more accurate solution than a ground-referenced op amp because ground is not typically a stable reference voltage in this type of application. The instability of the ground reference causes inaccuracies in the measurements that can be made with a simple ground referenced op amp. The AD8411A measures current in both directions as the H-bridge switches and the motor changes direction. The output of the AD8411A is configured in an external referenced bidirectional mode (see the **Bidirectional Operation** section).

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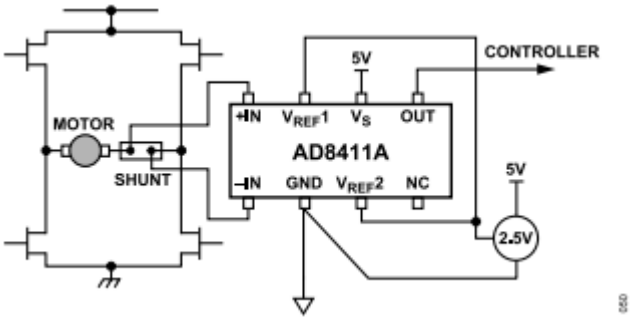

Figure 60. H-Bridge Motor Control

Solenoid Control

High-Side Current Sense with a Low-Side Switch

In the case of a high-side current sense with a low-side switch, the PWM control switch is ground referenced. Connect an inductive load (solenoid) to a power supply and place a resistive shunt between the switch and the load (see *Figure 61*). An advantage of placing the shunt on the high side is that the entire current, including the recirculation current, is measurable because the shunt remains in the loop when the switch is off. In addition, diagnostics are enhanced because shorts to ground are detected with the shunt on the high side.

In this circuit configuration, when the switch is closed, the common-mode voltage decreases to near the negative rail. When the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.

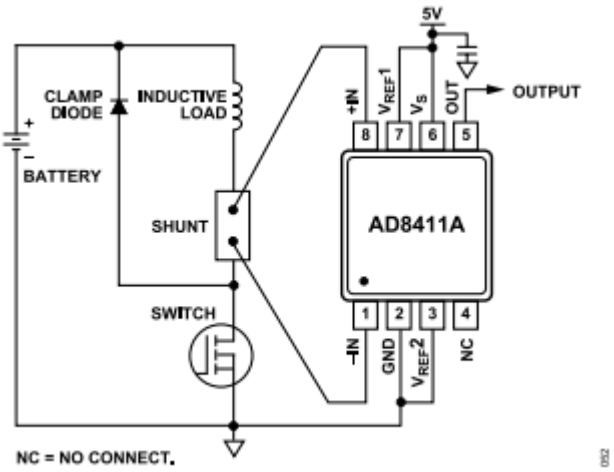

Figure 61. Low-Side Switch

High-Side Current Sense with a High-Side Switch

The high-side current sense with a high-side switch configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion due to constant battery draw (see *Figure 62*). In this case, both the switch and the shunt are on the high side. When the switch is off, the battery is removed from the load, which prevents damage from potential shorts to ground while still allowing the recirculating current to be measured and to provide diagnostics. Removing the power supply from the load for the majority of the time that the switch is open minimizes the corrosive effects that can be caused by the differential voltage between the load and ground.

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When using a high-side switch, the battery voltage is connected to the load when the switch is closed, causing the common-mode voltage to increase to the same value as the battery voltage. In this case, when the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

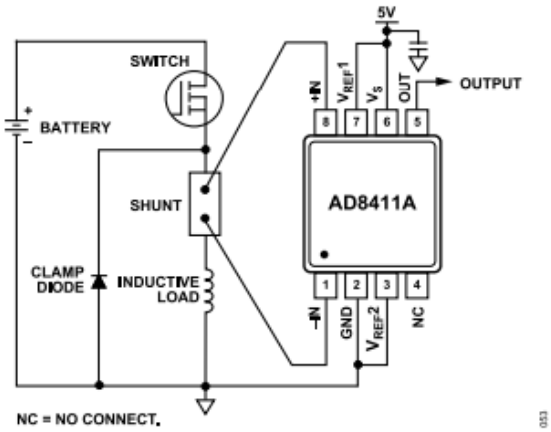

Figure 62. High-Side Switch

High Rail Current Sensing

In the high rail current-sensing configuration, the shunt resistor is referenced to the battery. High voltage is present at the inputs of the current-sense amplifier. When the shunt is battery referenced, the AD8411A produces a linear ground-referenced analog output. Additionally, the AD8214 provides an overcurrent detection signal in <100 ns (see *Figure 63*). This feature is useful in high-current systems where fast shutdown in overcurrent conditions is essential.

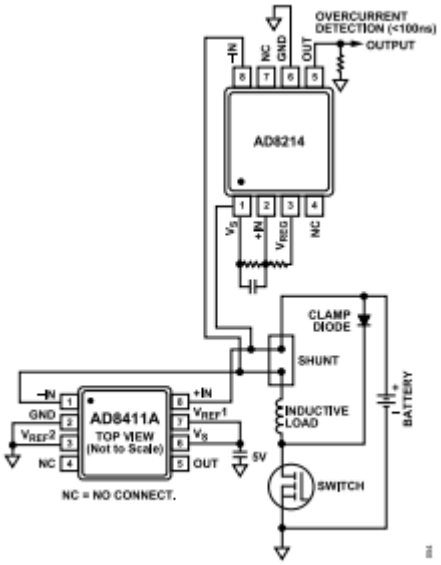

Figure 63.High Rail Current Sensing

Input Filter

In typical applications, such as motor control and solenoid current sensing, filtering at the input of the AD8411A can be beneficial in reducing differential noise, as well as transients and current ripples flowing through the input shunt

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resistor. Also, it is recommended to filter at the input of the AD8411A to further reduce the electromagnetic interference (EMI). The EMI specifications vary depending on the application. Filter at the input if the output cannot be filtered because filtering at the output changes the low output impedance seen by the components attached to the output of the AD8411A. The +IN and −IN pins of the AD8411A have balanced input-bias currents. The input series resistors, R1 and R2 in *Figure 64*, must be the same measured value not to add large offset voltage on the output of the device as a result of R1 and R2. It is recommended to keep R1 and R2 at or below 100 Ω. In *Figure 64*, C1 and C3 must be the same value.

For example, at 48 V common mode, when using a 10 Ω resistor for R1 and R2, the estimated maximum error that is seen on the input of the AD8411A ($V_{ErrorRTI}$) due to the R1 and R2 resistors in the input filter is:

$$V_{ErrorRTI} = 10\ \Omega \times 2.7\ \mu A = 27\ \mu V \quad (3)$$

Where 2.7 µA is the maximum input offset current at 48 V input common mode, as listed in *Table 1*.

The EMI filter has two different bandwidths, common-mode and differential. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the two inputs of the amplifier, +IN and −IN.

The −3 dB differential bandwidth for the filter is:

$$BW_{DIFF} = \frac{1}{2\pi \times R1 \times ((2 \times C2) + C1)} \quad (4)$$

The common-mode bandwidth defines what a common-mode RF signal sees between GND and the +IN and −IN of the amplifier tied together.

The −3 dB common-mode bandwidth for the filter is:

$$BW_{CM} = \frac{1}{2\pi \times R1 \times C1} \quad (5)$$

Keep the resistor values to a 1% tolerance and the filter capacitors to a 5% tolerance to assist with reducing AC common-mode rejection (CMR) errors. Choose C2 to be at least 10x larger than C1 or C3 to reduce AC CMR errors, which are caused by component mismatching.

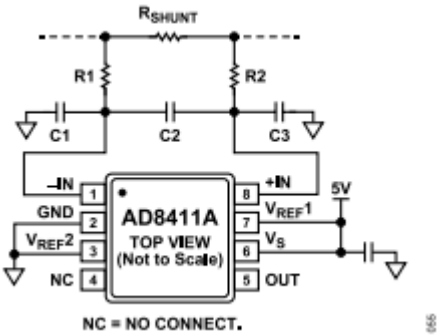

Figure 64.Input Filter

Overcurrent Detection

In several current-sensing applications, it is required to quickly detect when the current exceeds a certain threshold in the presence of a fault condition for safety concerns. As mentioned in the **High Rail Current Sensing** section, the

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AD8214 can be used for overcurrent detection in high-current systems where fast shutdown in overcurrent conditions is essential.

Another common practice for overcurrent detection in current-sense applications is to use a comparator on the output of the current-sense amplifier. *Figure 65* and *Figure 66* show typical configurations for monitoring current and using a comparator for overcurrent detection in unidirectional current and bidirectional currents, respectively.

Choose the values of R1 and R2 in *Figure 65* and *Figure 66* to set the threshold voltage at which the overcurrent detection trips. For example, for the bidirectional overcurrent detection configuration shown in *Figure 66* if the shunt resistance (R_{SHUNT}) is 10 mΩ, and it is required to trip the overcurrent detection at ±3 A, use Equation 6, Equation 7, and Equation 8 to find the R1 value after choosing an arbitrary value for R2. Choose, R2 = 4800 Ω, and V_S = 5 V.

Threshold voltage (V_{THR}) is the voltage that the output of the AD8411A must reach to trip the overcurrent detection. If it is required that the overcurrent detection trips at 3 A, then:

$$V_{THR} = 3\ A \times R_{SHUNT} \times 50\ V/V + 2.5\ V \quad (6)$$

The 2.5 V is added because the references are set up in split supply mode, then:

$$V_{THR} = 3\ A \times 10\ m\Omega \times 50\ V/V + 2.5\ V = 4\ V \quad (7)$$

After V_{THR} is known, use the following Equation 8 to find R1:

$$R1 = \frac{R2(V_S - V_{THR})}{V_{THR}} = \frac{4800\Omega \times (5V - 4V)}{4V} \quad (8)$$

For the second ADCMP601, keep the same values for R1 and R2. Attach the V_N pin to the output of the AD8411A, attach R2 to the 5 V supply, attach R1 to ground, and attach the V_P pin to the connection between R2 and R1 to allow negative overcurrent detection (as shown in *Figure 66*).

Therefore, when the output of the AD8411A reaches as shown in Equation 9, then the output of the ADCMP601 used for negative overcurrent detection trips high.

$$(2.5\ V - 3\ A \times 10\ m\Omega \times 50\ V/V) = 1\ V \quad (9)$$

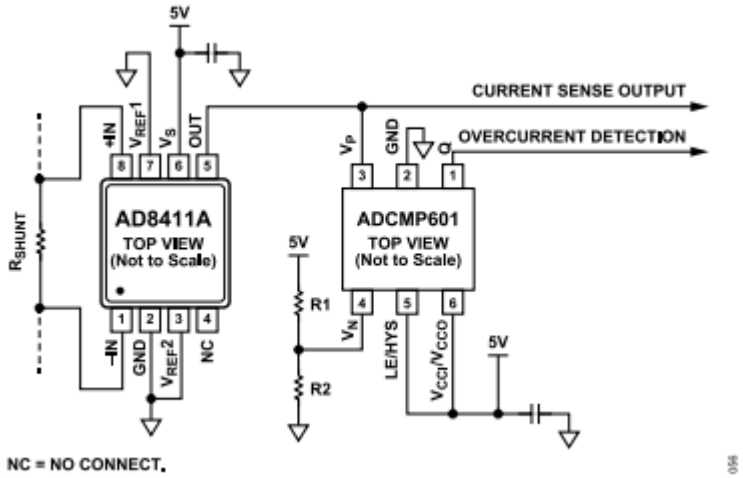

Figure 65. Unidirectional Overcurrent Detection

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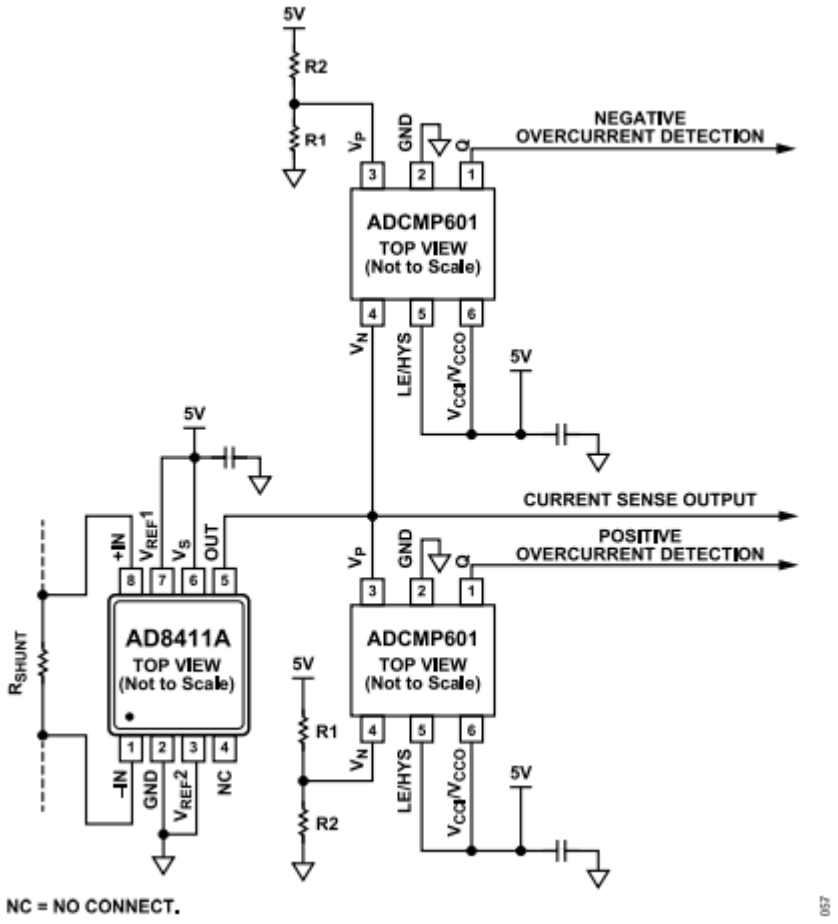

Figure 66. Bidirectional Overcurrent Detection

Pinout Option Engineered for FMEA

The AD8411A is available in a 10-lead MSOP pinout option engineered for FMEA. This FMEA tolerant pinout is designed to meet stringent requirements and to conditionally survive single faults that are a result of common printed circuit board (PCB) defects, as described in *Table 9* and *Table 10*. NC pins are inserted between -IN and GND, as well as between +IN and V_{REF}^1. These NC pins effectively isolate the voltages at the input pins, which may range from -2 V to +70 V, from adjacent pins that prevent the occurrence of unrecoverable faults.

Table 9. Behavior as a Result of Adjacent Pin to Pin Shorts

Pin Number	Adjacent Pins Shorted	Behavior
1, 2	−IN and NC	The circuit behaves normally.
2, 3	NC and GND	The circuit behaves normally.
3, 4	GND and V_{REF}^2	The operating range of V_{REF}^2 is from GND to V_S. Therefore, shorting V_{REF}^2 to GND does not represent a fault. For example, if the 10-lead MSOP AD8411A reference pins are configured to split the supply with V_{REF}^2 tied to GND, the circuit behaves normally. A system error occurs, however, if V_{REF}^2 is tied either to V_S or to a different external reference

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		because GND is shorted to V_S or to the external reference voltage on the PCB.
4, 5	V_{REF}^2 and NC	The circuit behaves normally.
5, 6	OUT and VS	OUT approaches V_S voltage.
6, 7	V_S and V_{REF}^1	The operating range of V_{REF}^1 is from GND to V_S. Therefore, shorting V_{REF}^1 to V_S does not represent a fault. For example, if the 10-lead MSOP AD8411A reference pins are configured to split the supply with V_{REF}^1 tied to V_S, the circuit behaves normally. A system error occurs, however, if V_{REF}^1 is tied either to GND or to a different external reference because V_S is shorted to GND or to the external reference voltage on the PCB.
8, 9	V_{REF}^1 and NC	The circuit behaves normally.
9, 10	NC and +IN	The circuit behaves normally.

Table 10. Behavior as a Result of Open Pin, Split Supply Setup (V_{REF}^1 to V_S and V_{REF}^2 to GND), V_S = 5 V, −IN = +IN = 12 V

Pin Number	Pin Opened	Behavior
1	-IN	OUT is undetermined, but is limited between GND and V_S.
2	NC	The circuit behaves normally.
3	GND	The output voltage range is limited to 0.7 V to V_S and the device receives the ground through an ESD diode on V_{REF}^2.
4	V_{REF}^2	OUT approaches V_S.
5	NC	The circuit behaves normally.
6	OUT	No OUT signal.
7	V_S	The device is powered through an ESD diode between the V_{REF}^1 pin and V_S pin. The output voltage range is limited to GND to V_S − 0.7 V.
8	V_{REF}^1	OUT approaches GND.
9	NC	The circuit behaves normally.
10	+IN	OUT is undetermined, but is limited between GND and V_S.

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OUTLINE DIMENSIONS

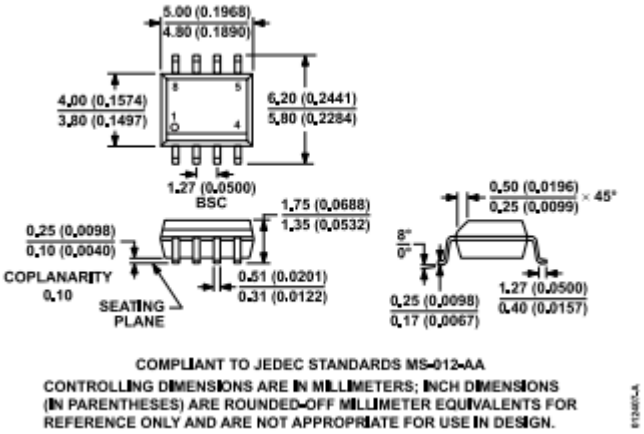

Figure 67. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8) Dimensions Shown in millimeters and (inches)

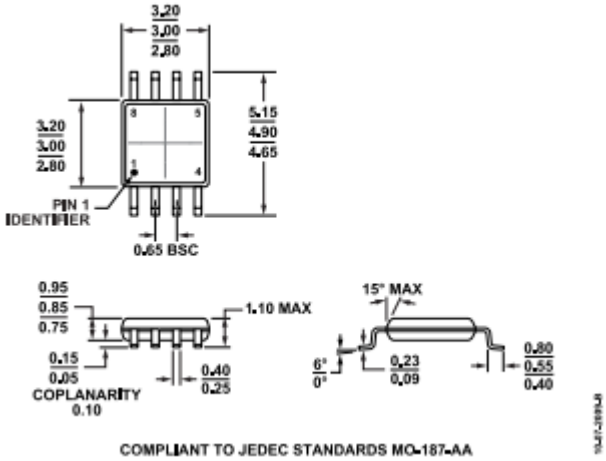

Figure 68. 8-Lead Mini Small Outline Package [MSOP] Narrow Body (RM-8) Dimensions Shown in millimeters and (inches)

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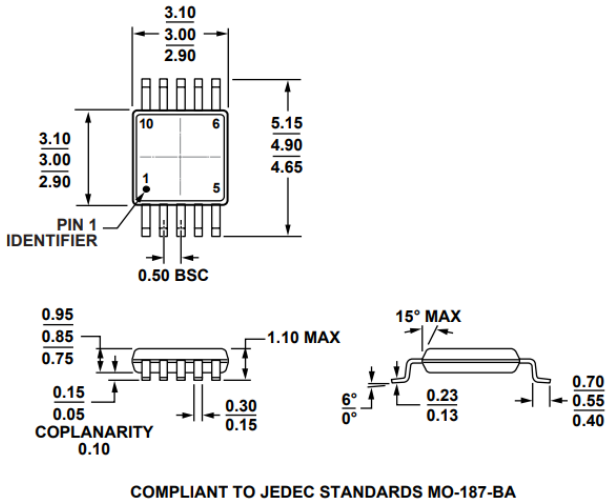

Figure 69. 10-Lead Mini Small Outline Package [MSOP] Narrow Body (RM-10) Dimensions Shown in millimeters and (inches)

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ORDERING GUIDE

Table 11. Ordering Guide

Model[1,2]	Temperature Range	Package Description	Package Quantity	Package Option	Marking Code
AD8411AWBRZ	−40°C to +125°C	8-Lead SOIC_N		R-8	
AD8411AWBRZ-RL	−40°C to +125°C	8-Lead SOIC_N	Reel, 2500	R-8	
AD8411AWBRMZ	−40°C to +125°C	8-Lead MSOP		RM-8	A55
AD8411AWBRMZ-RL	−40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A55
AD8411AWHRMZ	−40°C to +125°C	8-Lead MSOP		RM-8	A56
AD8411AWHRMZ-RL	−40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A56
AD8411AWBRMZ-10	−40°C to +125°C	10-Lead MSOP		RM-10	A5P
AD8411AWBRMZ-10RL	−40°C to +125°C	10-Lead MSOP	Reel, 3000	RM-10	A5P

1 Z = RoHS-compliant part.

2 W = Qualified for automotive applications.

EVALUATION BOARDS

Model[1]	Description
AD8411AR-EVALZ	Evaluation Board for 8-Lead Standard Small Outline Package [SOIC_N]
AD8411ARM-EVALZ	Evaluation Board for 8-Lead Mini Small Outline Package [MSOP]
AD8411ARM-10-EVALZ	Evaluation Board for 10-Lead Mini Small Outline Package [MSOP]

1 Z = RoHS-compliant part.

Automotive Products

The AD8411A models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the **Specifications** section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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