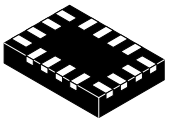
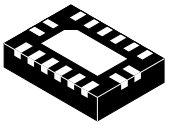
Low-Voltage Dual-Supply 4-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

FXL4TD245



UQFN16 1.80x2.60x0.50, 0.40P
CASE 523BF



WQFN16 3.5x2.5, 0.5P
CASE 510CC

General Description

The FXL4TD245 is a configurable 4-bit dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6 V to as low as 1.1 V. The A port tracks the V_{CCA} level, and the B port tracks the V_{CCB} level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

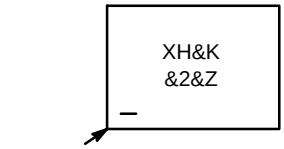
The device remains in 3-STATE until both V_{CC}s reach active levels allowing either V_{CC} to be powered-up first. Internal power down control circuits place the device in 3-STATE if either V_{CC} is removed.

The Transmit/Receive ($T/\overline{R}$) inputs independently determine the direction of data through each of the four bits. The $\overline{OE}$ input, when HIGH, disables both the A and B Ports by placing them in a 3-STATE condition. The FXL4TD245 is designed so that the control pins ($T/\overline{R}$ and $\overline{OE}$) are supplied by V_{CCA}.

Features

- Bi-directional Interface between Any 2 Levels from 1.1 V to 3.6 V
- Fully Configurable: Inputs Track V_{CC} Level
- Non-preferential Power-up Sequencing; either V_{CC} May be Powered-up First
- Outputs Remain in 3-STATE until Active V_{CC} Level is Reached
- Outputs Switch to 3-STATE if Either V_{CC} is at GND
- Power-off Protection
- Control Inputs ($T/\overline{R}_n$, $\overline{OE}$) Levels are Referenced to V_{CCA} Voltage
- Packaged in 16-terminal DQFN (2.5 mm x 3.5 mm) and 16-terminal MicroMLP (1.8 mm x 2.6 mm)
- ESD Protections Exceeds:
  - 4 kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8 kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1 kV CDM ESD (per ESD STM 5.3)
  - 200 V MM ESD (per JESD22-A115 & ESD STM5.2)
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

MARKING DIAGRAM



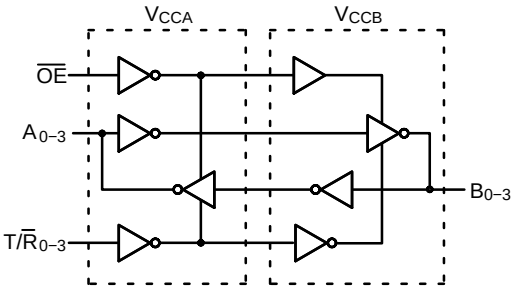
Pin#1 Identifier
UQFN16 (MicroMLP) (Top View)



WQFN16 (DQFN) (Top View)

4TD245, XH = Specific Device Code
&Z = Assembly Plant Code
&2 = 2-Digit Date Code
&K = 2-Digits Lot Run Traceability Code

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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Connection Diagrams

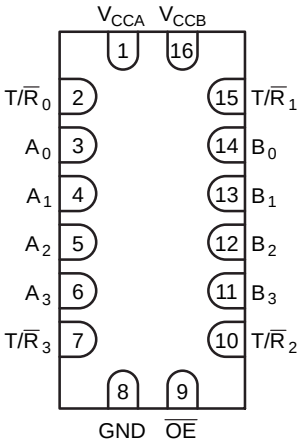


Figure 1. DQFN Pad Assignments (Top Through View)

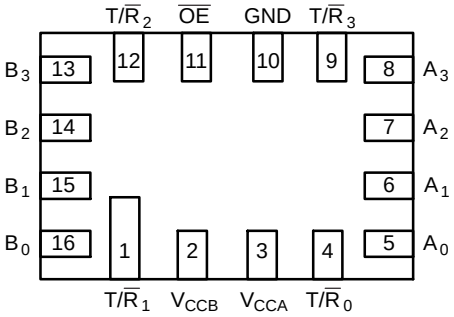


Figure 2. MicroMLP Pad Assignments (Top Through View)

PIN ASSIGNMENT

DQFN Pin #	μMLP Pin #	Terminal Name	Description
1	3	V_{CCA}	Side A Power Supply
2	4	$T/\overline{R}_0$	Transmit/Receive Input
3–6	5–8	A_0–A_3	Side A Inputs or 3-STATE Outputs
7	9	T/R_3	Transmit/Receive Input
8	10	GND	Ground
9	11	$\overline{OE}$	Output Enable Input
10	12	$T/\overline{R}_2$	Transmit/Receive Input
11–14	13–16	B_3–B_0	Side B Inputs or 3-STATE Outputs
15	1	$T/\overline{R}_1$	Transmit/Receive Input
16	2	V_{CCB}	Side B Power Supply

TRUTH TABLE

Inputs					Outputs
$\overline{OE}$	$T/\overline{R}_0$	$T/\overline{R}_1$	$T/\overline{R}_2$	$T/\overline{R}_3$	
L	L	X	X	X	B0 Data to A0 Output
L	H	X	X	X	A0 Data to B0 Output
L	X	L	X	X	B1 Data to A1 Output
L	X	H	X	X	A1 Data to B1 Output
L	X	X	L	X	B2 Data to A2 Output
L	X	X	H	X	A2 Data to B2 Output
L	X	X	X	L	B3 Data to A3 Output
L	X	X	X	H	A3 Data to B3 Output
H	X	X	X	X	3-State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a HIGH-Impedance state. The control inputs ($T/\overline{R}_n$ and $\overline{OE}$) are designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the $\overline{OE}$ driver.

The recommended power-up sequence is the following:

1. Apply power to either V_{CC}.
2. Apply power to the $T/\overline{R}_n$ inputs (Logic HIGH for A-to-B operation; Logic LOW for B-to-A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1.
3. Apply power to other V_{CC}.
4. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power-down sequence is the following:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rating
V_{CCA} to V_{CCB}	Supply Voltage		−0.5 V to +4.6 V
V_I	DC Input Voltage	I/O Port A	−0.5 V to +4.6 V
		I/O Port B	−0.5 V to +4.6 V
		Control Inputs (T/$\overline{R}_n$, $\overline{OE}$)	−0.5 V to +4.6 V
V_O	Output Voltage (Note 1)	Outputs 3-STATE	−0.5 V to +4.6 V
		Outputs Active (A_n)	−0.5 V to V_{CCA} + 0.5 V
		Outputs Active (B_n)	−0.5 V to V_{CCB} + 0.5 V
I_{IK}	DC Input Diode Current	V_I < 0 V	−50 mA
I_{OK}	DC Output Diode Current	V_O < 0 V	−50 mA
		V_O > V_{CC}	+50 mA
I_{OH}/I_{OL}	DC Output Source/Sink Current		−50 mA / +50 mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin		±100 mA
T_{STG}	Storage Temperature Range		−65 °C to +150 °C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. I_O Absolute Maximum Rating must be observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Conditions		Value
V_{CCA} or V_{CCB}	Power Supply Operating			1.1 V to 3.6 V
	Input Voltage	Port A		0.0 to 3.6 V
		Port B		0.0 to 3.6 V
		Control Inputs (T/$\overline{R}_n$, $\overline{OE}$)		0.0 to V_{CCA}
	Output Current in I_{OH}/I_{OL}	V_{CC}	3.0 V to 3.6 V	±24 mA
			2.3 V to 2.7 V	±18 mA
			1.65 V to 1.95 V	±6 mA
			1.40 V to 1.65 V	±2 mA
			1.1 V to 1.4 V	±0.5 mA
T_A	Free Air Operating Temperature			−40 to +85 °C
$\Delta V/\Delta t$	Minimum Input Edge Rate	$V_{CCA/B}$ = 1.1 V to 3.6 V		10 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. All unused inputs and I/O pins must be held at V_{CCI} or GND.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
V_{IH}	High Level Input Voltage (Note 3)	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0	–	V
			2.3–2.7		1.6	–	
			1.65–2.3		0.65 x V_{CCI}	–	
			1.4–1.65		0.65 x V_{CCI}	–	
			1.1–1.4		0.9 x V_{CCI}	–	
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	2.0	–	
			2.3–2.7		1.6	–	
			1.65–2.3		0.65 x V_{CCA}	–	
			1.4–1.65		0.65 x V_{CCA}	–	
			1.1–1.4		0.9 x V_{CCA}	–	
V_{IL}	Low Level Input Voltage (Note 3)	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	–	0.8	V
			2.3–2.7		–	0.7	
			1.65–2.3		–	0.35 x V_{CCI}	
			1.4–1.65		–	0.35 x V_{CCI}	
			1.1–1.4		–	0.1 x V_{CCI}	
		Control Pins $\overline{OE}$, T/$\overline{R}_n$ (Referenced to V_{CCA})	2.7–3.6	1.1–3.6	–	0.8	
			2.3–2.7		–	0.7	
			1.65–2.3		–	0.35 x V_{CCA}	
			1.4–1.65		–	0.35 x V_{CCA}	
			1.1–1.4		–	0.1 x V_{CCA}	
V_{OH}	High Level Output Voltage (Note 4)	I_{OH} = −100 μA	1.1–3.6	1.1–3.6	V_{CC0}–0.2	–	V
		I_{OH} = −12 mA	2.7	2.7	2.2	–	
		I_{OH} = −18 mA	3.0	3.0	2.4	–	
		I_{OH} = −24 mA	3.0	3.0	2.2	–	
		I_{OH} = −6 mA	2.3	2.3	2.0	–	
		I_{OH} = −12 mA	2.3	2.3	1.8	–	
		I_{OH} = −18 mA	2.3	2.3	1.7	–	
		I_{OH} = −6 mA	1.65	1.65	1.25	–	
		I_{OH} = −2 mA	1.4	1.4	1.05	–	
		I_{OH} = −0.5 mA	1.1	1.1	0.75 x V_{CC0}	–	
V_{OL}	Low Level Output Voltage (Note 4)	I_{OL} = 100 μA	1.1–3.6	1.1–3.6	–	0.2	V
		I_{OL} = 12 mA	2.7	2.7	–	0.4	
		I_{OL} = 18 mA	3.0	3.0	–	0.4	
		I_{OL} = 24 mA	3.0	3.0	–	0.55	
		I_{OL} =12 mA	2.3	2.3	–	0.4	
		I_{OL} = 18 mA	2.3	2.3	–	0.6	
		I_{OL} = 6 mA	1.65	1.65	–	0.3	
		I_{OL} = 2 mA	1.4	1.4	–	0.35	
		I_{OL} = 0.5 mA	1.1	1.1	–	0.3 x V_{CC0}	
I_I	Input Leakage Current. Control Pins	V_I = V_{CCA} or GND	1.1–3.6	3.6	–	±1.0	μA

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DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
I_{OFF}	Power Off Leakage Current	A_n, V_I or V_O = 0 V to 3.6 V	0	3.6	−	±10.0	μA
		B_n, V_I or V_O = 0 V to 3.6 V	3.6	0	−	±10.0	
I_{OZ}	3-STATE Output Leakage (Note 5) $0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	A_n, B_n, $\overline{OE} = V_{IH}$	3.6	3.6	−	±10.0	μA
		B_n, $\overline{OE}$ = Don't Care	0	3.6	−	+10.0	
		A_n, $\overline{OE}$ = Don't Care	3.6	0	−	+10.0	
$I_{CCA/B}$	Quiescent Supply Current (Note 6)	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6	−	20.0	μA
I_{CCZ}	Quiescent Supply Current (Note 6)	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6	−	20.0	μA
I_{CCA}	Quiescent Supply Current	$V_I = V_{CCA}$ or GND; $I_O = 0$	0	1.1–3.6	−	−10.0	μA
		$V_I = V_{CCA}$ or GND; $I_O = 0$	1.1–3.6	0	−	10.0	μA
I_{CCB}	Quiescent Supply Current	$V_I = V_{CCB}$ or GND; $I_O = 0$	1.1–3.6	0	−	−10.0	μA
		$V_I = V_{CCB}$ or GND; $I_O = 0$	0	1.1–3.6	−	10.0	μA
$\Delta I_{CCA/B}$	Increase in I_{CC} per Input; Other Inputs at V_{CC} or GND	V_{IH} = 3.0	3.6	3.6	−	500	μA

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. Don't care = Any valid logic level.
6. Reflects current per supply, V_{CCA} or V_{CCB}.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = −40 °C to +85 °C										Unit
		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		V_{CCB} = 1.4 V to 1.6 V		V_{CCB} = 1.1 V to 1.3 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Typ	
V_{CCA} = 3.0 V to 3.6 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	1.4	22.0	ns
	Propagation Delay B to A	0.2	3.5	0.2	3.8	0.3	4.0	0.5	4.3	0.8	13.0	
t_{PZH}, t_{PZL}	Output Enable OE to B	0.5	4.0	0.7	4.4	1.0	5.9	1.0	6.4	1.5	17.0	ns
	Output Enable OE to A	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	
t_{PHZ}, t_{PLZ}	Output Disable OE to B	0.2	3.8	0.2	4.0	0.7	4.8	1.5	6.2	2.0	17.0	ns
	Output Disable OE to A	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	0.2	3.7	
V_{CCA} = 2.3 V to 2.7 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	1.4	22.0	ns
	Propagation Delay B to A	0.3	3.9	0.4	4.2	0.5	4.5	0.5	4.8	1.0	7.0	
t_{PZH}, t_{PZL}	Output Enable OE to B	0.6	4.2	0.8	4.6	1.0	6.0	1.0	6.8	1.5	17.0	ns
	Output Enable OE to A	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	
t_{PHZ}, t_{PLZ}	Output Disable OE to B	0.2	4.1	0.2	4.3	0.7	4.8	1.5	6.7	2.0	17.0	ns
	Output Disable OE to A	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
V_{CCA} = 1.65 V to 1.95 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.3	4.0	0.5	4.5	0.8	5.7	0.9	7.1	1.5	22.0	ns
	Propagation Delay B to A	0.5	5.4	0.5	5.6	0.8	5.7	1.0	6.0	1.2	8.0	
t_{PZH}, t_{PZL}	Output Enable OE to B	0.6	5.2	0.8	5.4	1.2	6.9	1.2	7.2	1.5	18.0	ns
	Output Enable OE to A	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	
t_{PHZ}, t_{PLZ}	Output Disable OE to B	0.2	5.1	0.2	5.2	0.8	5.2	1.5	7.0	2.0	17.0	ns
	Output Disable OE to A	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	
V_{CCA} = 1.4 V to 1.6 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.5	4.3	0.5	4.8	1.0	6.0	1.0	7.3	1.5	22.0	ns
	Propagation Delay B to A	0.6	6.8	0.8	6.9	0.9	7.1	1.0	7.3	1.3	9.5	
t_{PZH}, t_{PZL}	Output Enable OE to B	1.1	7.5	1.1	7.6	1.3	7.7	1.4	7.9	2.0	20.0	ns
	Output Enable OE to A	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	
t_{PHZ}, t_{PLZ}	Output Disable OE to B	0.4	6.1	0.4	6.2	0.9	6.2	1.5	7.5	2.0	18.0	ns
	Output Disable OE to A	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	
V_{CCA} = 1.1 V to 1.3 V												
t_{PLH}, t_{PHL}	Propagation Delay A to B	0.8	13.0	1.0	7.0	1.2	8.0	1.3	9.5	2.0	24.0	ns
	Propagation Delay B to A	1.4	22.0	1.4	22.0	1.5	22.0	1.5	22.0	2.0	24.0	
t_{PZH}, t_{PZL}	Output Enable OE to B	1.0	12.0	1.0	9.0	2.0	10.0	2.0	11.0	2.0	24.0	ns
	Output Enable OE to A	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	2.0	22.0	
t_{PHZ}, t_{PLZ}	Output Disable OE to B	1.0	15.0	0.7	7.0	1.0	8.0	2.0	10.0	2.0	20.0	ns
	Output Disable OE to A	2.0	15.0	2.0	12.0	2.0	12.0	2.0	12.0	2.0	12.0	

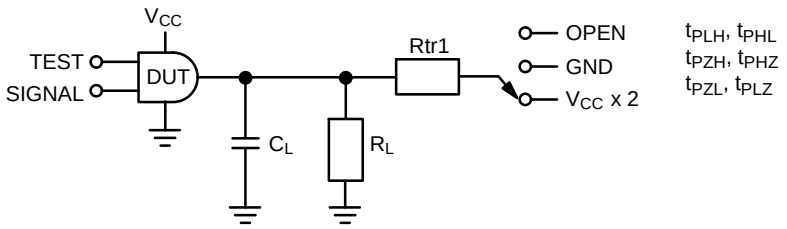
CAPACITANCE

Symbol	Parameter	Conditions	T_A = +25 °C	Unit
			Typical	
C_{IN}	Input Capacitance Control Pins ($\overline{OE}$, T/$\overline{R}$)	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	4.0	pF
$C_{I/O}$	Input/Output Capacitance A_n, B_n Ports	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CC}, F = 10 MHz	20.0	pF

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AC LOADINGS AND WAVEFORMS

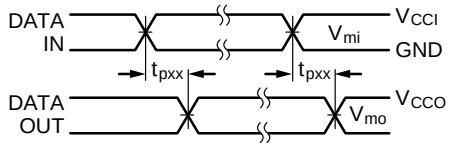


Test	Switch
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	V_{CCO} x 2 at V_{CCO} = 3.3 ±0.3 V, 2.5 V ±0.2 V, 1.8 V ±0.15 V, 1.5 V ±0.1 V, 1.2 V ±0.1 V
t_{PHZ}, t_{PZH}	GND

Figure 3. AC Test Circuit

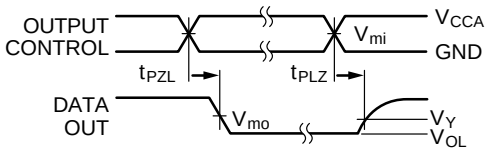
AC LOAD TABLE

V_{CCO}	C_L	R_L	Rtr1
1.2 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.5 V ±0.1 V	15 pF	2 kΩ	2 kΩ
1.8 V ±0.15 V	15 pF	2 kΩ	2 kΩ
2.5 V ±0.2 V	15 pF	2 kΩ	2 kΩ
3.3 V ±0.3 V	15 pF	2 kΩ	2 kΩ



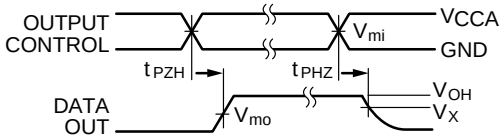
Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 4. Waveform for Inverting and Non-Inverting Functions



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 5. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic



Input $t_R = t_F$ = 2.0 ns, 10% to 90%
Input $t_R = t_F$ = 2.5 ns, 10% to 90%, @ V_I = 3.0 V to 3.6 V only

Figure 6. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}				
	3.3 V ±0.3 V	2.5 V ±0.2 V	1.8 V ±0.15 V	1.5 V ±0.1 V	1.2 V ±0.1 V
V_{mi}	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2	V_{CCI} / 2
V_{mo}	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2	V_{CCO} / 2
V_X	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V	V_{OH} − 0.1 V	V_{OH} − 0.1 V
V_Y	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V	V_{OL} + 0.1 V	V_{OL} + 0.1 V

7. For V_{mi}: V_{CCI} = V_{CCA} for Control Pins T/$\overline{R}$ and $\overline{OE}$ or V_{CCA} / 2.

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ORDERING INFORMATION

Order Number	Package Number	Package Description	Shipping†
FXL4TD245BQX	MLP016E	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5 mm x 3.5 mm (Pb-Free, Halide Free)	3000 / Tape & Reel
FXL4TD245UMX	UMLP16A	16-Terminal Quad, Ultrathin, Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm, 0.4 mm Pitch (Pb-Free, Halide Free)	5000 / Tape & Reel

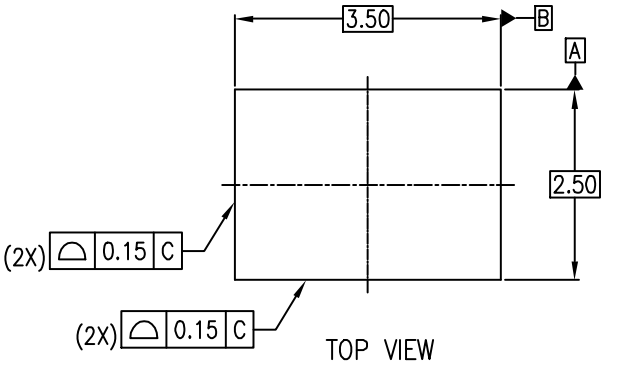
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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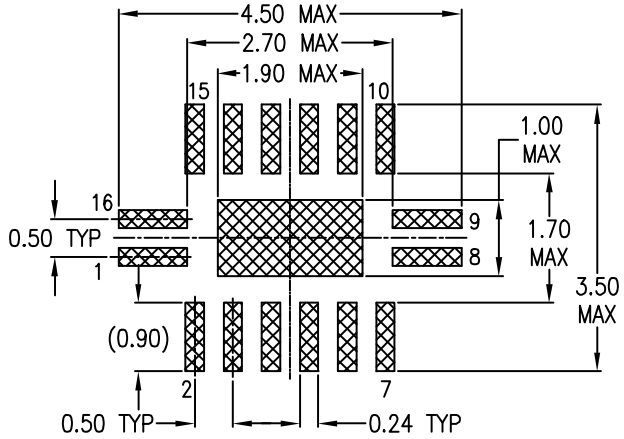
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WQFN16 3.5x2.5, 0.5P
CASE 510CC
ISSUE O

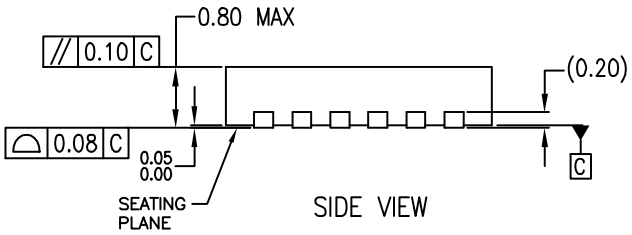
DATE 31 AUG 2016



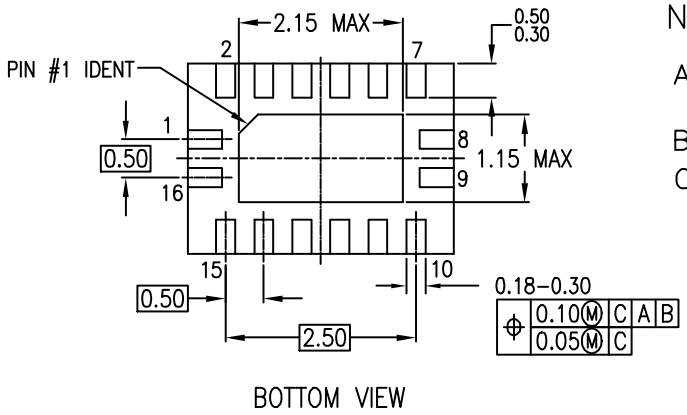
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

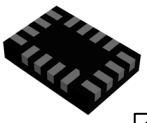
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A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AB
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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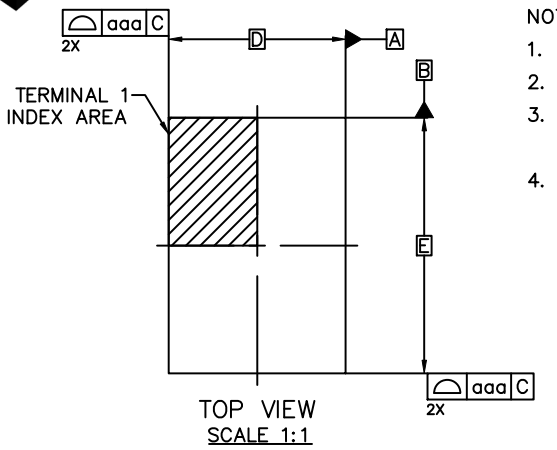
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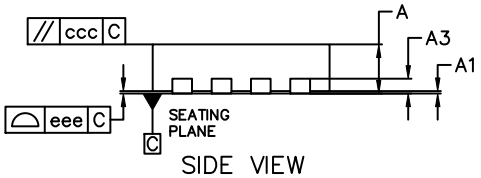


UQFN−16 1.80x2.60x0.50, 0.40P
CASE 523BF
ISSUE B

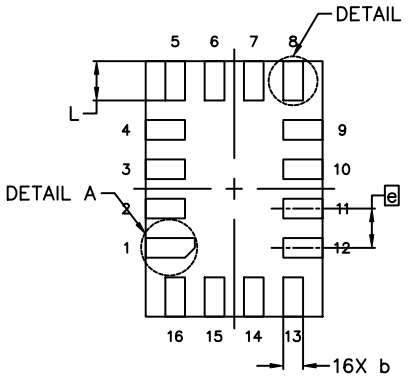
DATE 18 JUN 2026



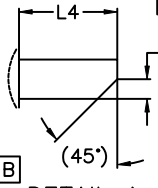
TOP VIEW
SCALE 1:1



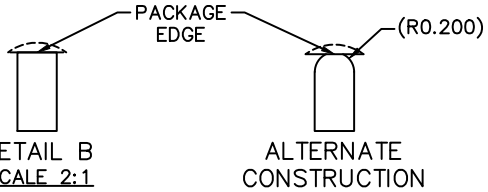
SIDE VIEW
SCALE 1:1



BOTTOM VIEW
SCALE 1:1



DETAIL A
SCALE 2:1



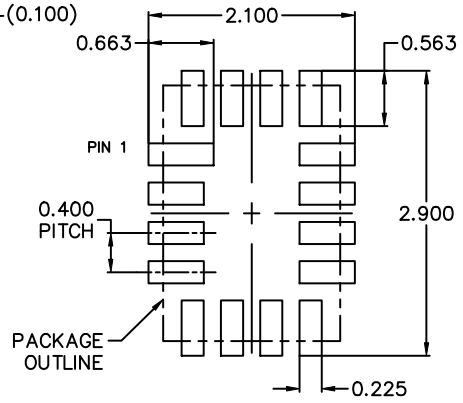
DETAIL B
SCALE 2:1

ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS, DEGREES IN ANGLE.
3. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
4. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.450	0.500	0.550
A1	0.000	0.025	0.050
A3	0.100	0.150	0.200
b	0.150	0.200	0.250
D	1.800 BSC		
E	2.600 BSC		
e	0.400 BSC		
L	0.350	0.400	0.450
L4	0.450	0.500	0.550
TOLERANCES FOR FEATURE CONTROL FRAME			
aaa	0.050		
bbb	0.100		
ccc	0.100		
ddd	0.050		
eee	0.050		



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