QCN9074 2.4/5/6 GHz 4 x 4 MIMO 802.11ax/ac/a/b/g/n WLAN AP RFIC

Data Sheet

80-Y9000-1 Rev. D

Qualcomm Technologies, Inc.

Device description

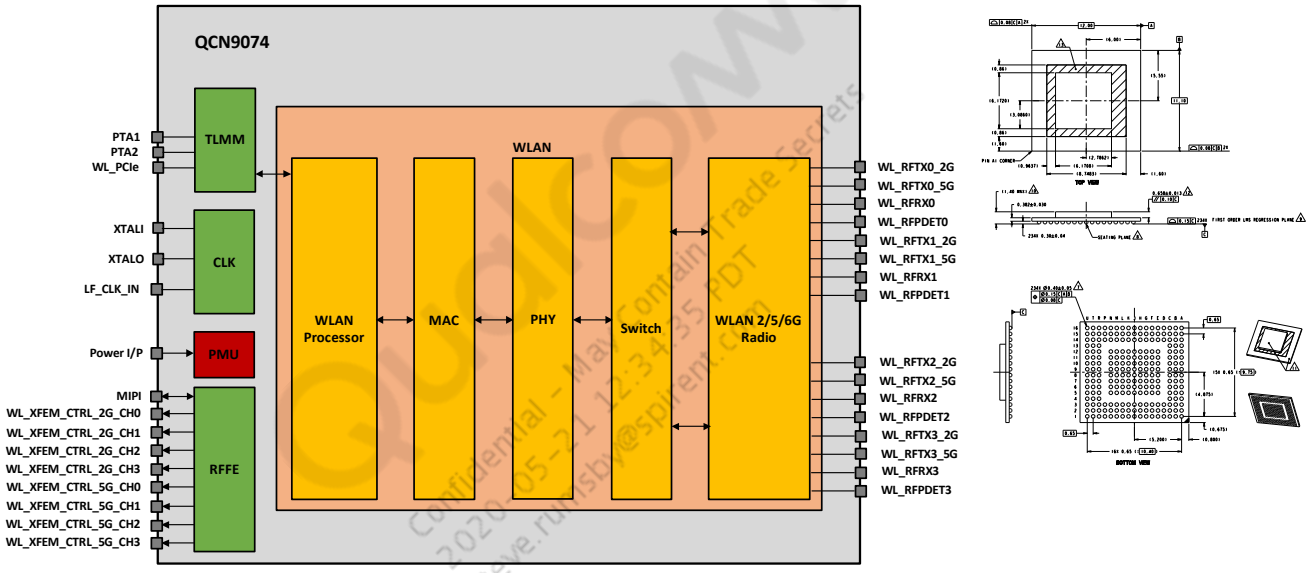
QCN9074 is an 802.11ax Wi-Fi 6E PCIe radio for Enterprise Access Points and Campus deployments.

QCN9074 with Qualcomm® 802.11ax technology is a highly integrated wireless local area network (WLAN) system-on-chip (SoC) for 2.4/5/6 GHz IEEE802.11ax/ac/n/g/b/a applications. QCN9074 performs AP and STA functionality with 4x4 MIMO and 4 spatial streams. The QCN9074 is a dual-synthesizer WLAN radio with native 160 MHz support.

Key features

- 4x4/160 MHz 11ax PCIe Radio
- Tri-band: 2.4 GHz, 5 GHz, 6 GHz full band support
- Dual Lane PCIe-g3
- PCI Express 3.0 dual-lane interface
- Four interfaces to external 2.4 GHz PAs
- Four interfaces to external PAs operating in the range from 4.9 GHz to 7.125 GHz
- Package: 11.1x 12 FCBGA, 0.65mm ball pitch

QCN9074 high-level block diagram and 234 MSP package outline



Although certain pin signal names are denoted as 5G, they apply equally well for both 5 GHz and 6 GHz.

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1 Introduction

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The QCN9074 chipset implements half-duplex OFDM, CCK, and DSSS PHY, and complies with IEEE 802.11a/b/g/n/ac/ax. In 5 GHz and 6 GHz bands, the maximum PHY rate of 4804 Mbps is achieved in 802.11ax 4x4/160 MHz native operation. In 2.4 GHz bands, a maximum PHY rate of 573.5 Mbps for 20 MHz and 1147 Mbps for 40 MHz is supported. Additional features include IEEE802.11ax and IEEE802.11ac explicit transmit beamforming (TxBF), DL/UL multi-user MIMO (MU-MIMO) up to 4 users, DL/UL multi user OFDMA up to 37 users, Dynamic Bandwidth Switching, agile DFS and agile spectrum analysis, where designated chain #3 scans another channel than the serving channel during listen receive intervals, Maximum Likelihood (ML) decoding, Low-Density Parity Check (LDPC), Maximum Ratio Combining (MRC), Space Time Block Code (STBC). The QCN9074 also supports the following protocols: IEEE802.11d/h/i/j/k/r/u/v/w/x.

The QCN9074 chipset supports up to four simultaneous spatial streams integrating four Tx and four Rx chains for high throughput and extended coverage. Tx chains combine PHY in-phase (I) and quadrature (Q) signals, convert them to the desired RF radio frequency. External power amplifiers (PAs) increase the signal strength to the desired EIRP. Rx chains receive from antennas through external LNAs. The frequency synthesizer supports 1-MHz steps to match frequencies defined by IEEE 802.11a/b/g/n/ac/ax specifications. The QCN9074 supports frame data transfer to and from the host using a 1 or 2 lane PCIe gen3 interface that supports interrupt generation and status reporting. Other external interfaces include EEPROM, GPIO, UART, PTA, and MCI interfaces for radio coexistence management.

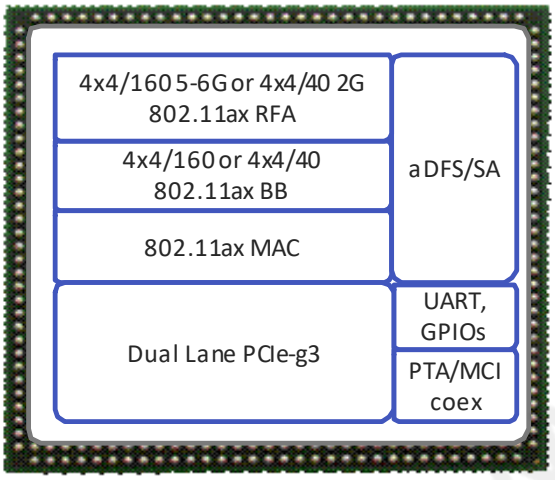


Figure 1-1 QCN9074 high-level block diagram

1.1 Features

NOTE: The features listed in this document show the chip hardware capability. Supported software features can be found in software documentation.

General

- 4x4/160 MHz 11ax PCIe Radio
- Tri-band: 2.4 GHz, 5 GHz, 6 GHz full band support
- Package: 11.1 x 12 FCBGA, 0.65mm ball pitch

WLAN

- Dual-synthesizer WLAN radio up to 160MHz bandwidth support
- Supports 5/10 MHz in 4.9 GHz (Public Safety band)
- Supports 20/40 MHz in 2.4 GHz
- Supports 20/40/80/160 MHz in 5 GHz
- Supports 20/40/80/160 MHz in 6 GHz
- DL/UL MU-MIMO, up to 4 users per PPDU
- DL/UL MU-OFDMA, up to 37 users per PPDU
- TxBF, MU-MIMO, MU-OFDMA/TxBF, ML, STBC
- Agile DFS (dynamic switching between 4 and 3+1)
- Agile Spectral Analysis (aSA) for all bands (dynamic switching between 4 and 3+1)
- PTA (3-wire) and WCI (2-wire) coexistence
- Supports up to 1024 QAM (4SS) and 4096 QAM(2SS)

- Data rates of up to 4804 Mbps in 802.11ax 160 MHz channels using reduced (short) guard interval (GI)
- Data rates of up to 573.5 Mbps for 20 MHz and 1147 Mbps for 40 MHz channel in 2.4 GHz mode using short GI
- Multi-user multiple input multiple output (MU-MIMO) for 802.11ac/ax
- 802.11 ac/ax explicit transmit beamforming (TxBF)
- 802.11 ac/ax beamformee for STA mode
- Spatial reuse through BSS color, OBSS-PD, SRG and SRP
- TCP and UDP checksum offload
- Dynamic bandwidth switching
- Maximum likelihood (ML) decoding
- Supports low-density parity check (LDPC), maximal ratio combining (MRC), Space Time Block Code (STBC)
- AMSDU and AMPDU frame aggregation

  A-MSDU: No limit on the number of MSDUs aggregated, only limited by maximum A-MSDU size, which is approx. 11kB
  A-MPDU: Maximum. 256 MPDU per PPDU
- 802.11e-compatible bursting
- Digital Pre-Distortion (DPD)
- Locationing (RSSI and RTT-based, 802.11REVmc compliant)
- Supports monitor mode

Supported Standards

- IEEE 802.11a/b/g/n/ac/ax
- IEEE 802.11d, e, h, i, j, k, r, u, v timestamp, and w

CPU/Memory

- Integrated CPU with SRAM memory
- On-chip OTP memory

RF Interfaces

- Four interfaces to external 2.4 GHz PAs
- Four interfaces to external PAs operating in the range from 4.9 GHz to 7.125 GHz
- Four interfaces to external LNAs for all bands
- Four PDET interfaces for Front End feedback control signals
- RFSAT and BBSAT; RFSAT improves AACI and ACI performance and BBSAT enables quick AGC
- MIPI interface for Front End Control

Security

- AES-CCMP at 128/256 bits
- AES-GCMP at 128/256 bits
- WEP, TKIP hardware encryption
- WAPI hardware encryption

- WPA/WPA2-Personal/WPA2-Enterprise and WPA3 Personal
- FIPS ECB

Interfaces

- PCI Express 3.0 dual-lane interface
- I^{2}C EEPROM support
- GPIOs
- JTAG for debugging and boundary scan
- UART

Power Supply

- QCN9074 power rails are supplied by an external PMIC.
- The PMIC will make sure that all of the rails are up before releasing QCN9074 from reset.
- QCN9074 SoC consists of two power rails, a WLAN_CX rail (for digital logic), and a WLAN_MX rail (for memories).
- The WLAN Always On rail shares the WLAN_MX rail.
- The WLAN_CX and WLAN_MX rails move together through different power modes, though with different voltages.
- The WLAN_MX rail is generally at a higher voltage than the WLAN_CX rail.

1.2 Functional specification

Figure 1-2 illustrates the QCN9074 functional block diagram.

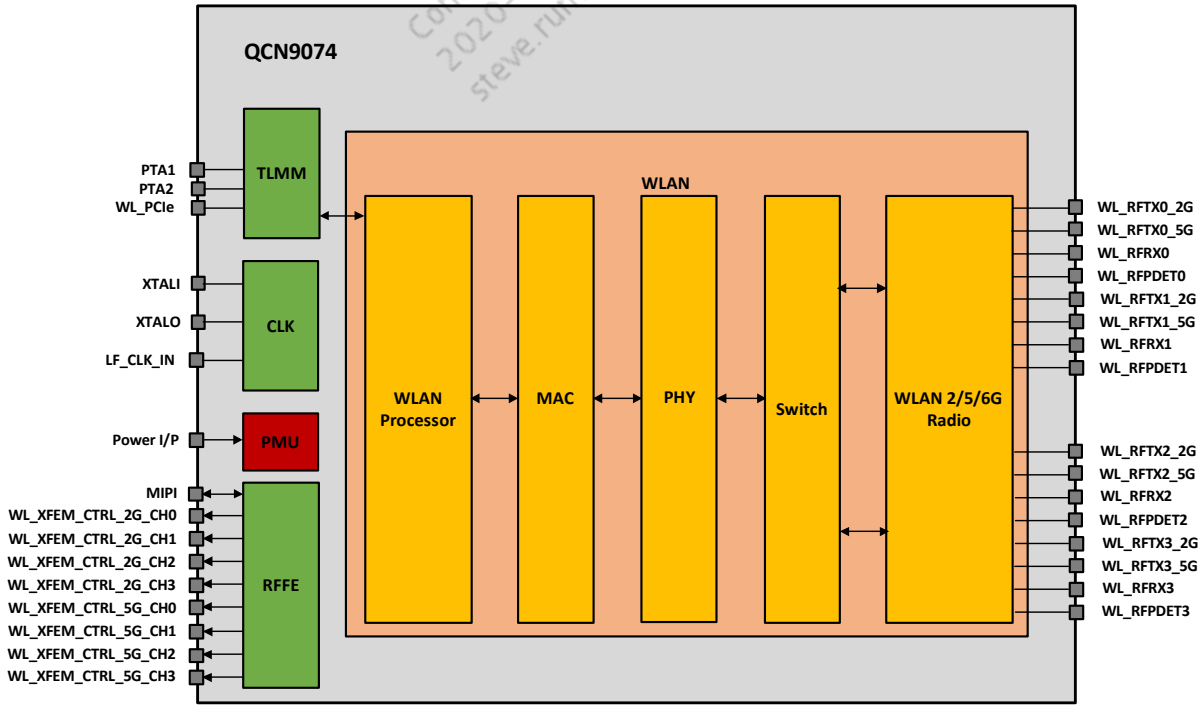


Figure 1-2 QCN9074 functional block diagram [1]

1.3 Acronyms

Table 1-1 defines terms and acronyms commonly used throughout this document.

Table 1-1 Terms and acronyms

Term	Definition
n-QAM	n-state quadrature amplitude modulation, where n=2,4,16,64,256,1024,4096
AEC	Automotive Electronics Council
ADC	Analog-to-digital converter
BER	Bit error rate
BLE	Bluetooth Low Energy
bps	Bits per second
BT	Bluetooth
CCK	Complementary Code Keying
DAC	Digital-to-analog converter
DSSS	Direct-sequence spread spectrum
EDR	Enhanced data rate
EIA	Electronic Industries Alliance
FCCSP	Flip-chip Chip Scale Package
FIPS L2	Federal Information Protection System Level 2
GI	Guard Interval
GPIO	General-purpose input/output
JESD	JEDEC standards
LNA	Low Noise Amplifier
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface
MCI	Memory Card Interface
MSL	Moisture Sensitivity Level (for PCBs)
PA	Power amplifier
PM	Power management
PTA	Packet traffic assistance
PPDU	PLCP Protocol Data Unit
QCN	Qualcomm connectivity network
RH	Relative humidity
RoHS	Restriction of Hazardous Substances
SnPB	Tin-Lead (for solder)

1. Although certain pin signal names are denoted as 5G, they apply equally well for both 5 GHz and 6 GHz.

Table 1-1 Terms and acronyms (cont.)

Term	Definition
SS	Spatial Stream
UART	Universal asynchronous receiver transmitter
WLAN	Wireless local area network

1.4 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, SDC1_DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Nonobvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input signal (CMOS)
DO	Digital output signal (CMOS)
GND	Ground
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
PU	Contains an internal pull-down device
PD	Contains an internal pull-up device
NP	Contains no internal pull

2.2 Pin assignments

2.2.1 Pin map

The QCN9074 uses the 234 MSP package. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

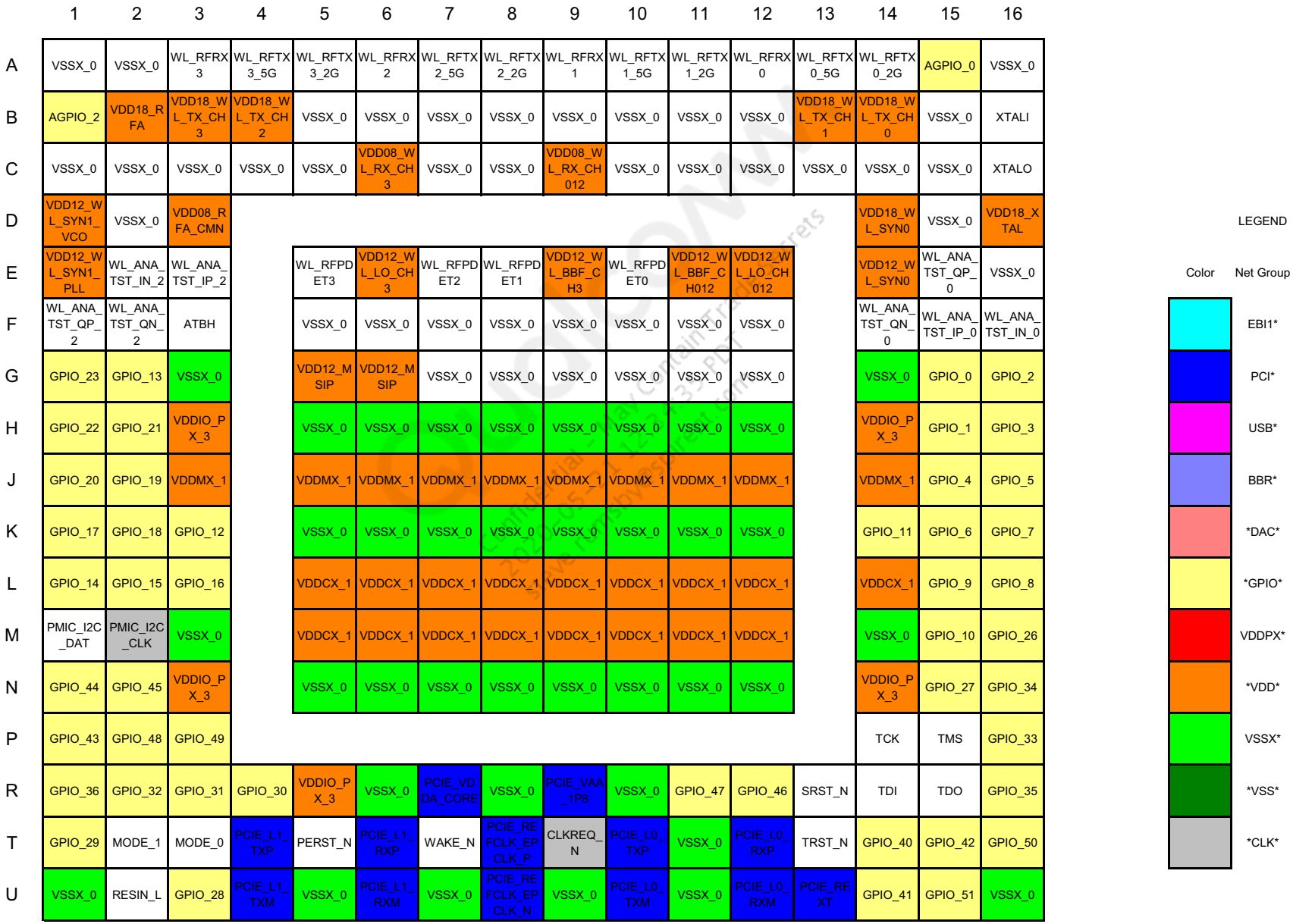


Figure 2-1 Top view of QCN9074 pin assignments (from above, through package)

2.2.2 Pin descriptions

Descriptions of pins are presented in the following tables, organized by functional group:

Table 2-2 Pin descriptions—interface and control signals

Pad #	Pad name	Configurable function	PU/PD	I/O pad	Functional description
G15	GPIO_0	WL_XFEM_CTRL_2G_CH0_0_GPIO	PD	B	WLAN RF 2.4 GHz chain 0 front-end control signal
H15	GPIO_1	WL_XFEM_CTRL_2G_CH0_1_GPIO	PD	B	
G16	GPIO_2	WL_XFEM_CTRL_2G_CH0_2_GPIO	PD	B	
H16	GPIO_3	WL_XFEM_CTRL_5G_CH0_0_GPIO	PD	B	WLAN RF 5/6 GHz chain 0 front-end control signal
J15	GPIO_4	WL_XFEM_CTRL_5G_CH0_1_GPIO	PD	B	
J16	GPIO_5	WL_XFEM_CTRL_5G_CH0_2_GPIO	PD	B	
K15	GPIO_6	WL_XFEM_CTRL_2G_CH1_0_GPIO	PD	B	WLAN RF 2.4 GHz chain 1 front-end control signal
K16	GPIO_7	WL_XFEM_CTRL_2G_CH1_1_GPIO	PD	B	
L16	GPIO_8	WL_XFEM_CTRL_2G_CH1_2_GPIO	PD	B	
L15	GPIO_9	WL_XFEM_CTRL_5G_CH1_0_GPIO	PD	B	WLAN RF 5/6 GHz chain1 front-end control signal
M15	GPIO_10	WL_XFEM_CTRL_5G_CH1_1_GPIO	PD	B	
K14	GPIO_11	WL_XFEM_CTRL_5G_CH1_2_GPIO	PD	B	
K3	GPIO_12	WL_XFEM_CTRL_2G_CH2_0_GPIO	PD	B	WLAN RF 2.4 GHz chain 2 front-end control signal
G2	GPIO_13	WL_XFEM_CTRL_2G_CH2_1_GPIO	PD	B	
L1	GPIO_14	WL_XFEM_CTRL_2G_CH2_2_GPIO	PD	B	
L2	GPIO_15	WL_XFEM_CTRL_5G_CH2_0_GPIO	PD	B	WLAN RF 5/6 GHz chain 2 front-end control signal
L3	GPIO_16	WL_XFEM_CTRL_5G_CH2_1_GPIO	PD	B	
K1	GPIO_17	WL_XFEM_CTRL_5G_CH2_2_GPIO	PD	B	
K2	GPIO_18	WL_XFEM_CTRL_2G_CH3_0_GPIO	PD	B	WLAN RF 2.4 GHz chain 3 front-end control signal
J2	GPIO_19	WL_XFEM_CTRL_2G_CH3_1_GPIO	PD	B	
J1	GPIO_20	WL_XFEM_CTRL_2G_CH3_2_GPIO	PD	B	
H2	GPIO_21	WL_XFEM_CTRL_5G_CH3_0_GPIO	PD	B	WLAN RF 5/6 GHz chain 3 front-end control signal
H1	GPIO_22	WL_XFEM_CTRL_5G_CH3_1_GPIO	PD	B	
G1	GPIO_23	WL_XFEM_CTRL_5G_CH3_2_GPIO	PD	B	
M2	GPIO_24	WL_I2C_SCL_0_MAPPING	PU	B	I^2C master bus. The maximum clock rate is 400 kHz.

Table 2-2 Pin descriptions—interface and control signals (cont.)

Pad #	Pad name	Configurable function	PU/PD	I/O pad	Functional description
M1	GPIO_25	WL_I2C_SDA_0_MAPPING	PU	B	I^2C master bus. It is an open drain signal and requires an external pull-up resistor if used.
M16	GPIO_26	SW0	PD	B	Software GPIO
N15	GPIO_27	LED_0	PU	O	LED interface 0 for RFA debug
U3	GPIO_28	REF_CLK_SEL	PD	O	Reference clock selection
T1	GPIO_29	WMAC0_ANTENNA_INFO0_ MAPPING	PD	O	WMAC antenna info 0 mapping
R4	GPIO_30	WMAC0_ANTENNA_INFO1_ MAPPING	PD	O	WMAC antenna info 1 mapping
R3	GPIO_31	SW1	PD	O	Software GPIO
R2	GPIO_32	SW2	PD	O	Software GPIO
P16	GPIO_33	EEPROM_I2C_SCL	PU	B	EEPROM I^2C master mode interface clock
N16	GPIO_34	EEPROM_I2C_SDA	PU	B	EEPROM I^2C master mode interface data
R16	GPIO_35	SW_LED_1	PD	O	LED interface 1
R1	GPIO_36	SW4	PD	O	Software GPIO
T5	GPIO_37	WL_PCIE_RST_N	PD	I	WLAN PCIe reset signal is an input signal.
T7	GPIO_38	WL_PCIE_WAKE_N	PU	B	WLAN PCIe wake-up signal is an output signal. It is an open-drain signal that requires an external 10 KΩ pull-up resistor.
T9	GPIO_39	WL_PCIE_CLKREQ_N	PU	B	WLAN PCIe clock request signal is a bidirectional signal. It is an open-drain signal that requires an external 10 KΩ pull-up resistor.
T14	GPIO_40	PTA1_BT_ACTIVE_MAPPING	PD	I	Wi-Fi coexistence with Bluetooth active signal PTA 1
U14	GPIO_41	PTA1_BT_PRIORITY_MAPPING	PD	I	Wi-Fi coexistence with Bluetooth priority signal PTA 1
T15	GPIO_42	PTA1_WL_ACTIVE_MAPPING	PD	O	WLAN active signal PTA 1
P1	GPIO_43	SW5	PD	O	Software GPIO, PTA2 Bluetooth Active
N1	GPIO_44	SW6	PD	O	Software GPIO, PTA2 Bluetooth Priority
N2	GPIO_45	SW7	PD	O	Software GPIO, PTA2 WL Active
R12	GPIO_46	WCI2_UART_RXD	PU	O	Wireless coexistence interface (WCI) UART asynchronous.
R11	GPIO_47	WCI2_UART_TXD	PU	I	Wireless coexistence interface (WCI) UART asynchronous; WSI data.

Table 2-2 Pin descriptions—interface and control signals (cont.)

Pad #	Pad name	Configurable function	PU/PD	I/O pad	Functional description
P2	GPIO_48	DBG_UART_TXD_MAPPING	PU	O	Debug UART TxD
P3	GPIO_49	DBG_UART_RXD_MAPPING	PU	I	Debug UART RxD
T16	GPIO_50	WR_PROTECT	PD	O	Write protection
U15	GPIO_51	LF_CLK_IN	PD	I	An external 32.768 KHz sleep clock input pin. The PCB design can use either external sleep clock (32.768 KHz) or internal sleep clock (32 KHz), but external sleep clock provides better sleep clock accuracy. A pull-down resistor is required if LF_CLK_IN is not used. WSI clock.
U8	WL_PCIE_REFCLK_EPCLK_N		–	I	WLAN PCIe reference clock input differential signals
T8	WL_PCIE_REFCLK_EPCLK_P		–	I	
T10	WL_PCIE_L0_TXM		–	O	WLAN PCIe L0 transmit output differential signals
U10	WL_PCIE_L0_TXP		–	O	
U12	WL_PCIE_L0_RXM		–	I	WLAN PCIe L0 receive input differential signals
T12	WL_PCIE_L0_RXP		–	I	
U4	WL_PCIE_L1_TXM		–	O	WLAN PCIe L1 transmit output differential signals
T4	WL_PCIE_L1_TXP		–	O	
U6	WL_PCIE_L1_RXM		–	I	WLAN PCIe L1 receive input differential signals
T6	WL_PCIE_L1_RXP		–	I	
B16	XTALI		–	I	Crystal input. It can be used as TCXO input with DC block capacitor. V_{pp} must be less than 1.3 V.
C16	XTALO		–	O	Crystal output. V_{pp} must be less than 1.3 V.

Table 2-3 Pin descriptions—RF signals

Pad #	Pad name	I/O pad	Functional description
A12	WL_RFRX0	RF	WLAN RF 2.4/5/6 GHz chain 0 receiver LNA input
A9	WL_RFRX1	RF	WLAN RF 2.4/5/6 GHz chain 1 receiver LNA input
A6	WL_RFRX2	RF	WLAN RF 2.4/5/6 GHz chain 2 receiver LNA input
A3	WL_RFRX3	RF	WLAN RF 2.4/5/6 GHz chain 3 receiver LNA input
A14	WL_RFTX0_2G	RF	WLAN RF 2.4 GHz chain 0 transmitter DA output
A13	WL_RFTX0_5G	RF	WLAN RF 5/6 GHz chain 0 transmitter DA output
A11	WL_RFTX1_2G	RF	WLAN RF 2.4 GHz chain 1 transmitter DA output
A10	WL_RFTX1_5G	RF	WLAN RF 5/6 GHz chain 1 transmitter DA output
A8	WL_RFTX2_2G	RF	WLAN RF 2.4 GHz chain 2 transmitter DA output
A7	WL_RFTX2_5G	RF	WLAN RF 5/6 GHz chain 2 transmitter DA output
A5	WL_RFTX3_2G	RF	WLAN RF 2.4 GHz chain 3 transmitter DA output
A4	WL_RFTX3_5G	RF	WLAN RF 5/6 GHz chain 3 transmitter DA output
E10	WL_RFPDET0	RF	WLAN RF 2.4 GHz/5/6 GHz chain 0 PDET input
E8	WL_RFPDET1	RF	WLAN RF 2.4 GHz/5/6 GHz chain 1 PDET input
E7	WL_RFPDET2	RF	WLAN RF 2.4 GHz/5/6 GHz chain 2 PDET input
E5	WL_RFPDET3	RF	WLAN RF 2.4 GHz/5/6 GHz chain 3 PDET input

Table 2-4 Pin descriptions—power signals

Pad #	Pad name	I/O pad	Functional description
PMU: PMU for digital and digital power supply input pins			
L5	VDDCX_1	I	WLAN digital power supply input from VDD08_PMU_WLCX
L6	VDDCX_1	I	
L7	VDDCX_1	I	
L8	VDDCX_1	I	
L9	VDDCX_1	I	
L10	VDDCX_1	I	
L11	VDDCX_1	I	
L12	VDDCX_1	I	
L14	VDDCX_1	I	
M5	VDDCX_1	I	
M6	VDDCX_1	I	
M7	VDDCX_1	I	
M8	VDDCX_1	I	
M9	VDDCX_1	I	
M10	VDDCX_1	I	
M11	VDDCX_1	I	
M12	VDDCX_1	I	
PMU: PMU for memory and memory power supply input pins			
J3	VDDMX_1	I	WLAN memory power supply input
J5	VDDMX_1	I	
J6	VDDMX_1	I	
J7	VDDMX_1	I	
J8	VDDMX_1	I	
J9	VDDMX_1	I	
J10	VDDMX_1	I	
J11	VDDMX_1	I	
J12	VDDMX_1	I	
J14	VDDMX_1	I	
PMU: PCIe			
R9	PCIE_VAA_1P8	I	PCIe 1.8 V power supply input from VDD18_IO
R7	PCIE_VDDA_CORE	I	VDD08 power supply input for PCIe core logic from VDD18_IO
U13	PCIE_REXT	A	External resistor pin for PCIe PHY bias generation
VDDIO power supply input			
H3	VDDIO_PX_3	I	VDDIO 1.8 V power supply input on left side

Table 2-4 Pin descriptions—power signals (cont.)

Pad #	Pad name	I/O pad	Functional description
H14	VDDIO_PX_3	I	VDDIO 1.8 V power supply input at bottom
N3	VDDIO_PX_3	I	VDDIO 1.8 V power supply input on right side
N14	VDDIO_PX_3	I	VDDIO 1.8 V power supply input
R5	VDDIO_PX_3	I	VDDIO 1.8 V power supply input
PMU: RFA VDD08 PMU and power supply pins			
C9	VDD08_WL_RX_CH012	I	0.8 V supply for WLAN Rx
C6	VDD08_WL_RX_CH3	I	
D3	VDD08_RFA_CMN	I	0.8 V supply for RFA digital
PMU: RFA VDD012 PMU and power supply pins			
G5	VDD12_MSIP	I	1. 2V supply for WLAN mixed signal
G6	VDD12_MSIP	I	
E11	VDD12_WL_BBF_CH012	I	1.2 V supply for WLAN analog
E9	VDD12_WL_BBF_CH3	I	
E6	VDD12_WL_LO_CH3	I	1.2 V supply for WLAN LO
E12	VDD12_WL_LO_CH012	I	
E14	VDD12_WL_SYN0	I	1.2 V supply for WLAN Synth
E1	VDD12_WL_SYN1_PLL	I	
D1	VDD12_WL_SYN1_VCO	I	
PMU: RFA VDD18 PMU and power supply pins			
B3	VDD18_WL_TX_CH3	I	1.8 V supply for WLAN Tx
B4	VDD18_WL_TX_CH2	I	
B13	VDD18_WL_TX_CH1	I	
B14	VDD18_WL_TX_CH0	I	
D14	VDD18_WL_SYN_0	I	1.8 V supply for WLAN Synth
B2	VDD18_RFA	I	1.8 V supply for WLAN RFA
D16	VDD18_XTAL	I	VDD18 crystal power supply input

Table 2-5 Pin descriptions—NC signals

Pad #	Pad name	I/O pad	Functional description
T3	MODE_0	–	No connect
T2	MODE_1	–	No connect
R13	SRST_N	–	JTAG signal, no connect
P14	TCK	–	JTAG signal, no connect
R14	TDI	–	JTAG signal, no connect
R15	TDO	–	JTAG signal, no connect
P15	TMS	–	JTAG signal, no connect
T13	TRST_N	–	JTAG signal, no connect
U2	RESIN_L	–	Fundamental reset input. Pull up to 1.8 V with a 10K resistor. A power-up sequence is required at cold start. Control this reset input and release it 100 ms after the last voltage in the sequence has reached its threshold level. It is expected that the PMIC chip drive this signal.
F3	ATBH	–	Ground
A15	AGPIO_0	–	No connect
B1	AGPIO_2	–	No connect
F16	WL_ANA_TST_IN_0	O	No connect
E2	WL_ANA_TST_IN_2	O	No connect
F15	WL_ANA_TST_IP_0	O	No connect
E3	WL_ANA_TST_IP_2	O	No connect
F14	WL_ANA_TST_QN_0	O	No connect
F2	WL_ANA_TST_QN_2	O	No connect
E15	WL_ANA_TST_QP_0	O	No connect
F1	WL_ANA_TST_QP_2	O	No connect

Table 2-6 Pin descriptions—Ground signals

Pad #	Pad name	Functional description
A1	RF_GND	Ground
A2	RF_GND	Ground
A16	RF_GND	Ground
B5	RF_GND	Ground
B6	RF_GND	Ground
B7	RF_GND	Ground
B8	RF_GND	Ground
B9	RF_GND	Ground
B10	RF_GND	Ground
B11	RF_GND	Ground
B12	RF_GND	Ground
B15	RF_GND	Ground
C1	RF_GND	Ground
C2	RF_GND	Ground
C3	RF_GND	Ground
C4	RF_GND	Ground
C5	RF_GND	Ground
C7	RF_GND	Ground
C8	RF_GND	Ground
C10	RF_GND	Ground
C11	RF_GND	Ground
C12	RF_GND	Ground
C13	RF_GND	Ground
C14	RF_GND	Ground
C15	RF_GND	Ground
D2	RF_GND	Ground
D15	RF_GND	Ground
E16	RF_GND	Ground
F5	RF_GND	Ground
F6	RF_GND	Ground
F7	RF_GND	Ground
F8	RF_GND	Ground
F9	RF_GND	Ground
F10	RF_GND	Ground
F11	RF_GND	Ground

Table 2-6 Pin descriptions—Ground signals (cont.)

Pad #	Pad name	Functional description
F12	RF_GND	Ground
G12	RF_GND	Ground
G7	VSSX_0	Ground
G8	VSSX_0	Ground
G9	VSSX_0	Ground
G10	VSSX_0	Ground
G11	VSSX_0	Ground
G3	VSSX_0	Ground
G14	VSSX_0	Ground
H5	VSSX_0	Ground
H6	VSSX_0	Ground
H7	VSSX_0	Ground
H8	VSSX_0	Ground
H9	VSSX_0	Ground
H10	VSSX_0	Ground
H11	VSSX_0	Ground
H12	VSSX_0	Ground
K5	VSSX_0	Ground
K6	VSSX_0	Ground
K7	VSSX_0	Ground
K8	VSSX_0	Ground
K9	VSSX_0	Ground
K10	VSSX_0	Ground
K11	VSSX_0	Ground
K12	VSSX_0	Ground
M3	VSSX_0	Ground
M14	VSSX_0	Ground
N5	VSSX_0	Ground
N6	VSSX_0	Ground
N7	VSSX_0	Ground
N8	VSSX_0	Ground
N9	VSSX_0	Ground
N10	VSSX_0	Ground
N11	VSSX_0	Ground
N12	VSSX_0	Ground
R6	VSSX_0	Ground

Table 2-6 Pin descriptions—Ground signals (cont.)

Pad #	Pad name	Functional description
R8	VSSX_0	Ground
R10	VSSX_0	Ground
T11	VSSX_0	Ground
U1	VSSX_0	Ground
U5	VSSX_0	Ground
U7	VSSX_0	Ground
U9	VSSX_0	Ground
U11	VSSX_0	Ground
U16	VSSX_0	Ground

3 Electrical characteristics

3.1 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1 summarizes the absolute maximum ratings for the QCN9074.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 3-1 Absolute maximum ratings

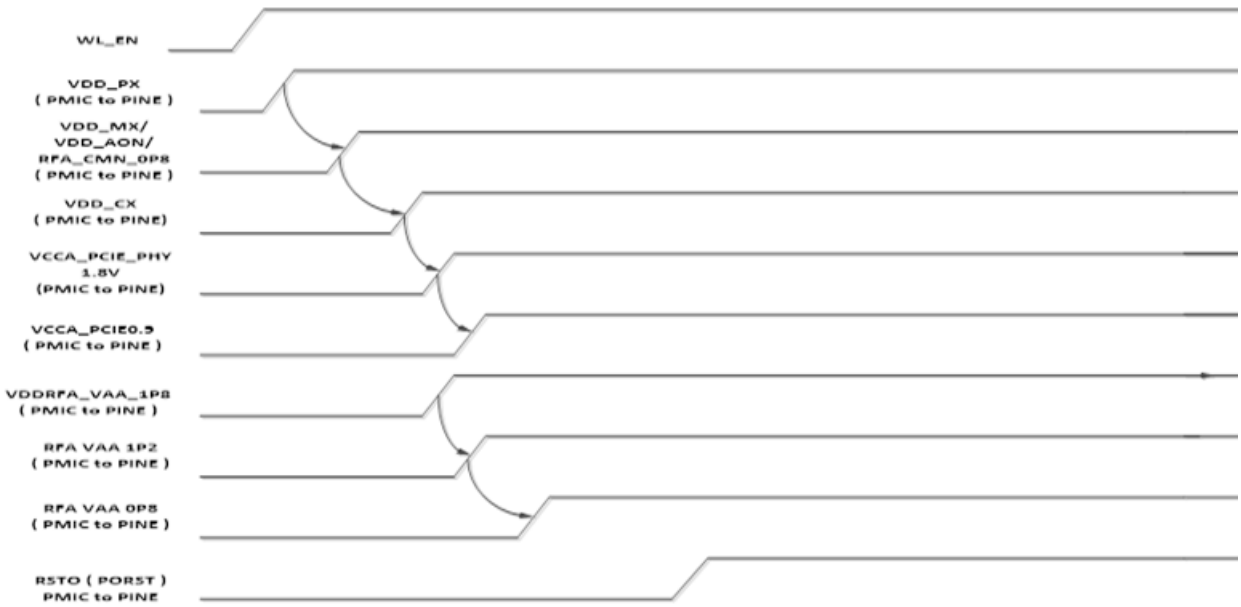
Pad #	Parameter		Min	Max	Unit
Power-supply voltages					
B2	VDD18_RFA	High voltage analog supply		2.05	V
E11 E9	VDD12_WL_BBF_CH012 VDD12_WL_BBF_CH3	Medium voltage analog supply	-0.3	1.46	V
G5 G6	VDD12_MSIP VDD12_MSIP	Medium voltage analog supply		1.46	
D3	VDD08_RFA_CMN	Low voltage analog supply		1.05	
R9 R7	PCIE_VAA_1P8 PCIE_VDDA_CORE	High voltage supply Analog and digital supply	-0.3	2.05 1.05	V
L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, M5, M6, M7, M8, M9, M10, M11, M12	VDDCX_1	Core digital supply	-0.3	1.178	V
J3, J5, J6, J7, J8, J9, J10, J11, J12, J14	VDDMX_1	Core digital supply			
H14 N3 N14 R5	VDDIO_PX_3 VDDIO_PX_3 VDDIO_PX_3 VDDIO_PX_3	I/O supply	-0.3	2.05	V

3.2 Operating conditions

Table 3-2 Operating conditions

Pad #	Parameter		Min	Typ	Max	Unit
Power-supply voltages						
L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, M5, M6, M7, M8, M9, M10, M11, M12	VDDCX_1	Core digital supply	0.71		0.87	V
J3, J5, J6, J7, J8, J9, J10, J11, J12, J14	VDDMX_1	Core digital supply	0.85		0.92	V
B2	VDD18_RFA	High voltage analog supply	1.71	1.8	1.89	V
E11 E9	VDD12_WL_BBF_CH012 VDD12_WL_BBF_CH3	Medium voltage analog supply	1.14	1.2	1.26	V
G5 G6	VDD12_MSIP VDD12_MSIP	Medium voltage analog supply	1.14	1.2	1.26	V
D3	VDD08_RFA_CMN	High voltage analog supply	0.81	0.85	0.89	V
H14 N3 N14 R5	VDDIO_PX_3 VDDIO_PX_3 VDDIO_PX_3 VDDIO_PX_3	I/O supply	1.71	1.8	1.89	V

3.3 Powerup sequence timing



3.4 Digital logic characteristics

Table 3-3 Digital logic characteristics

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage (hihys_en=HIGH)	–	0.7 x VDDIO	–	VDDIO + 0.3	V
V_{IL}	Low-level input (hihys_en=HIGH)	–	-0.3	–	0.3 x VDDIO	V
V_{IH}	High-level input voltage (hihys_en=LOW)	–	0.65 x VDDIO	–	VDDIO + 0.3	V
V_{IL}	Low-level input (hihys_en=LOW)	–	-0.3	–	0.35 x VDDIO	V
V_{SHYS}	Schmitt hysteresis (hihys_en=HIGH)	–	300	-	–	mV
V_{SHYS}	Schmitt hysteresis (hihys_en=LOW)	–	100	-	–	mV
I_{IH}	Input high leakage current	V_IN = VDDIO max	–	–	1.0	µA
I_{IL}	Input low leakage current	V_IN = 0 V; supply = VIO max	-1.0	–	–	µA
V_{OH}	High-level output voltage, CMOS	–	VDDIO-0.45	–	VDDIO	V
V_{OL}	Low-level output voltage, CMOS	–	0.0	–	0.45	V
I_{OH}	High-level output current	–	2	–	–	mA
I_{OL}	Low-level output current	–	–	–	-16	mA
C_{IN}	Input capacitance 2	–	–	–	TBD	pF

3.5 Clock requirements

QCN9074 supports a crystal as the reference clock. When using a crystal, a 96 MHz crystal must be used. The clock requirements for the external clock and crystal are listed in the following tables.

3.5.1 96 MHz crystal requirement

Table 3-4 96 MHz crystal requirement

Description	Min	Typ	Max	Unit
Operating frequency	–	96	–	MHz
Frequency stability	-20	–	20	PPM
Equivalent series resistance	8	–	20	Ohm

Table 3-4 96 MHz crystal requirement

Description	Min	Typ	Max	Unit
Drive level	0.01	100	400	µW
Load capacitance		9.9		pF

3.5.2 External sleep clock timing

Figure 3-1 and Table 3-5 show the sleep clock input requirements.

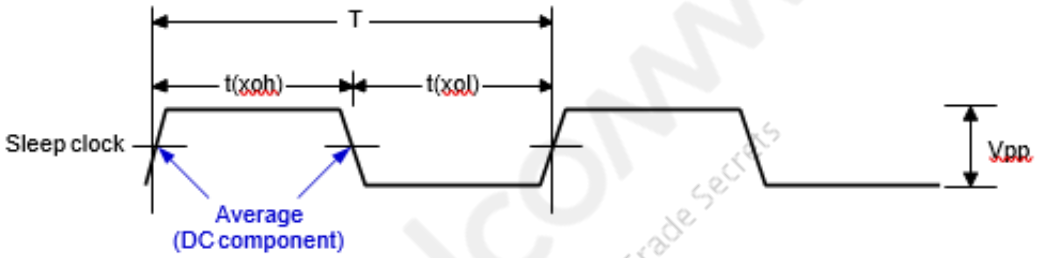


Figure 3-1 External sleep clock

Table 3-5 External sleep clock timing

Parameter		Comments	Min	Typ	Max	Units
$t_{(xoh)}$	Sleep-clock logic high	–	4.58	–	25.94	µs
$t_{(xol)}$	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.5208	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.7645	–	kHz
V_{pp}	Peak-to-peak voltage	–	–	1.8	–	V

3.6 PCIe interface

The QCN9074 supports PCIe Gen 3 interface for WLAN.

3.7 WLAN RF characteristics

This section describes the WLAN Rx and Tx RF characteristics.

3.7.1 Rx characteristics

Table 3-6 Rx characteristics for 2.4 GHz operation

Parameter	Min	Nom	Max	Units	Comments
Receive input frequency range	2400	—	2496	MHz	
Maximum power gain		60		dB	
Gain control range		60		dB	Excluding the front-end module
Rx gain step		1		dB	
NF		4.5		dB	At maximum power gain
Maximum operational LNA input power			-10	dBm	
Recommended signal source impedance		50		Ω	Chip Rx input

Table 3-7 Rx characteristics for 5 GHz operation

Parameter	Min	Nom	Max	Units	Comments
Receive input frequency range	4900	—	5925	MHz	Might observe lower performance for channels with f <5180MHz and f > 5825 MHz
Maximum power gain		60		dB	
Gain control range		60		dB	Excluding the front-end module
Rx gain step		1		dB	
NF		5.0		dB	At maximum power gain
Maximum operational LNA input power			-20	dBm	
Recommended signal source impedance		50		Ω	Chip Rx input

Table 3-8 Rx characteristics for 6 GHz operation

Parameter	Min	Nom	Max	Units	Comments
Receive input frequency range	5925	—	7250	MHz	Might observe lower performance for channels with f <5180MHz and f > 5825 MHz
Maximum power gain		60		dB	
Gain control range		60		dB	Excluding the front-end module

Table 3-8 Rx characteristics for 6 GHz operation (cont.)

Parameter	Min	Nom	Max	Units	Comments
Rx gain step		1		dB	
NF		5.5		dB	At maximum power gain
Maximum operational LNA input power			-20	dBm	
Recommended signal source impedance		50		Ω	Chip Rx input

3.7.2 Tx characteristics

Table 3-9 Tx characteristics for 2.4 GHz operation at chip output with external PA

Parameter	Min	Nom	Max	Units	Comments	
Transmit output frequency range	2400	—	2496	MHz		
Mask compliant output power - MCS0		-3		dBm	HE20/40[1]	
HO-EVM without DPD[2]	**Tx Power (dBm)**					
		-40		dB	MCS8	802.11ax, HE20
		-40			MCS9	802.11ax, HE40
		-44			MCS11	802.11ax, HE20/40
		-44			MCS13	802.11ax, HE20/40
Tx gain step[3]		1		dB		
Accuracy of power control loop		±1		dB	See Note[4]	
Recommended load Z		50		Ω	Chip Tx output	

1. Measured with reference board
2. Simulated at the chip output
3. Guaranteed by design
4. Manufacturing calibration required

Table 3-10 Tx characteristics for 5 GHz operation at chip output with external PA

Parameter	Min	Nom	Max	Units	Comments
Transmit output frequency range	4900	—	5925	MHz	Might observe lower EVM performance for channels with f <5180MHz and f > 5825 MHz
Mask compliant output power - MCS0		-3		dBm	HE20/40/80/160[1]

Table 3-10 Tx characteristics for 5 GHz operation at chip output with external PA (cont.)

Parameter	Min	Nom	Max	Units	Comments	
HO-EVM without DPD[2]		**Tx Power (dBm)**				
		-40		dB	MCS8	802.11ax, HE20
		-40			MCS9	802.11ax, HE40
		-43.5			MCS11	802.11ax, HE20/40/80/160
		-43.5			MCS13	802.11ax, HE20/40/80/160
Tx gain step[3]		1		dB		
Accuracy of power control loop		±1		dB	See Note[4]	
Recommended load Z		50		Ω	Chip Tx output	

1. Measured with reference board
2. Simulated at the chip output
3. Guaranteed by design
4. Manufacturing calibration required

Table 3-11 Tx characteristics for 6 GHz operation at chip output with external PA

Parameter	Min	Nom	Max	Units		Comments
Transmit output frequency range	5925	—	7250	MHz	Might observe lower EVM performance for channels with f > 7125 MHz	
Mask compliant output power - MCS0		-2		dBm	HE20/40/80/160[1]	
HO-EVM without DPD[2]		**Tx Power (dBm)**				
		-40		dB	MCS8	802.11ax, HE20
		-40			MCS9	802.11ax, HE40
		-43			MCS11	802.11ax, HE20/40/80/160
		-43			MCS13	802.11ax, HE20/40/80/160
Tx gain step[3]		1		dB		
Accuracy of power control loop		±1		dB	See Note[4]	
Recommended PA single-ended load impedance		50		Ω	Chip Tx output	

1. Measured with reference board
2. Simulated at the chip output
3. Guaranteed by design
4. Manufacturing calibration required

4 Mechanical information

NOTE The information in this chapter is preliminary and subject to change without notice.

4.1 Device physical dimensions

The QCN9074 device is available in the 234 MSP package that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 234 MSP outline drawing is shown in Figure 4-1 and Figure 4-2.

NOTE Click the following link to download *Package Outline Drawing, MSP234, 12.0 x 11.1 x 12.0 mm, D600, S382* (NT90-YD077-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-YD077-1

After successfully logging in, the document is downloaded.

NOTE Make this document a favorite to be notified of any changes.

Use the package coordinate file (.txt) for the correct ball location.

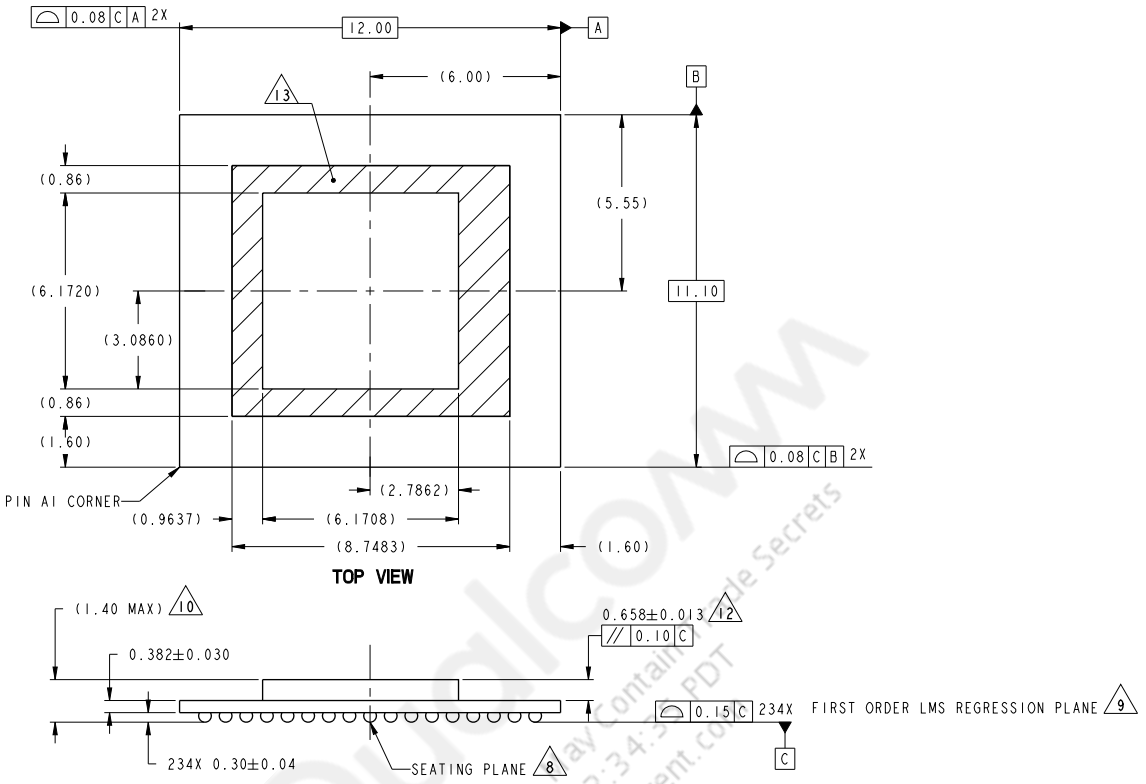


Figure 4-1 234 MSP outline drawing—Top view

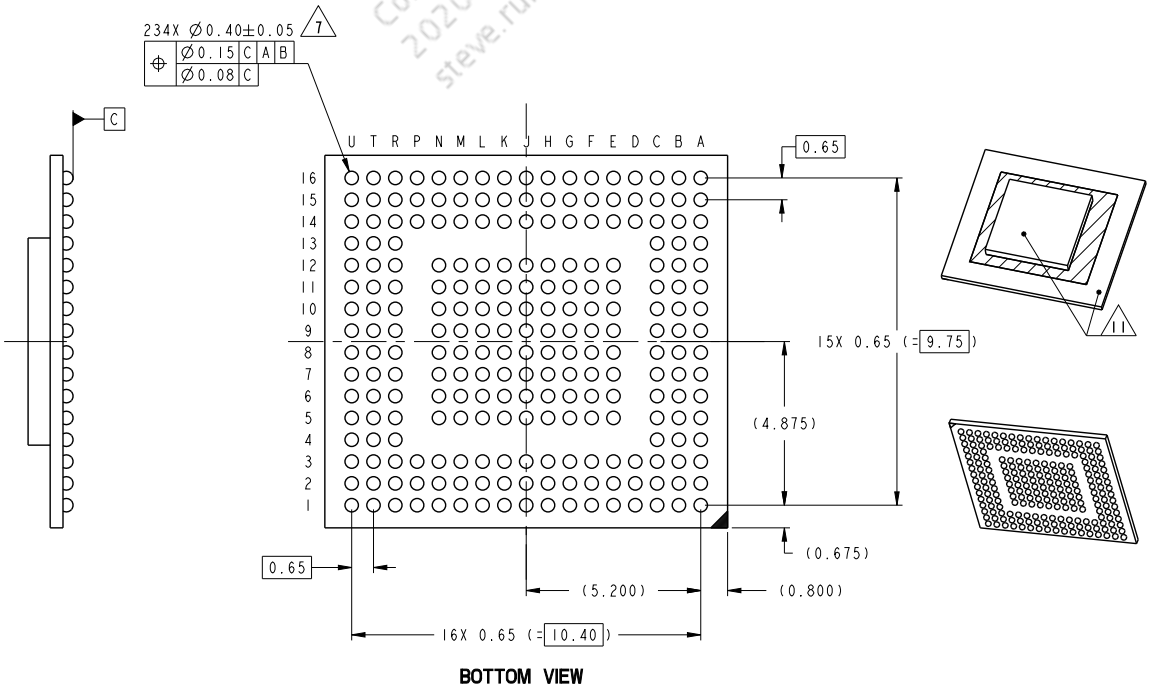


Figure 4-2 234 MSP outline drawing—Bottom view

4.2 Part marking

This device can be ordered using the identification code shown in Section 4.3.

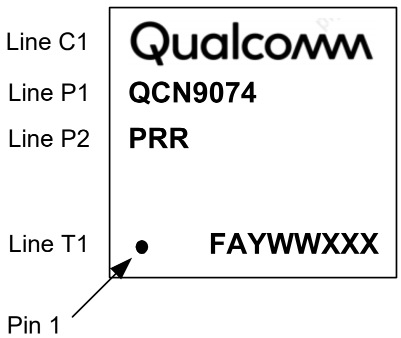


Figure 4-3 Device marking (top view)

Table 4-1 QCN9074 NSP part configuration marking

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	QCN9074	Qualcomm product name
P2	PRR	P = product configuration code RR = product revision code
T1	FAYWWXXX	F = supply source code ■ F = J (Samsung) A = assembly site code ■ A= E (ASE Taiwan) ■ A= K (SPIL Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
Pin 1	●	Ball A1 identifier

4.3 Device ordering information

This device can be ordered using the ordering number shown in Table 4-2. Figure 4-4 explains how the device can be identified.

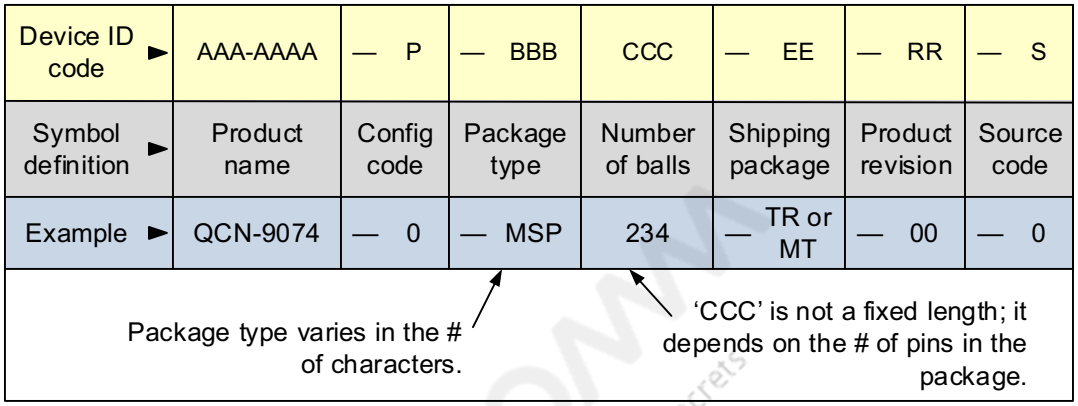


Figure 4-4 Device identification

Table 4-2 Ordering information

Product part number	Ordering number	PRR	Date code	Product type	Temperature
QCN9074	QCN-9074-0-MSP234-MT-00-0	000	2006	ES	Commercial
	QCN-9074-0-MSP234-TR-00-0	000	2006	ES	Commercial

NOTE TR – tape and reel, MT – matrix tray

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-3.

Table 4-3 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; QCN9074 rating
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The QCN9074 devices are classified as MSL3; the qualification temperature is 250ºC.*** This qualification temperature (250°C) should not be confused with the peak temperature within the recommended solder reflow profile.

During device qualification, QTI follows the latest revision IPC/JEDEC J-STD-020 standard to determine the IC's moisture-sensitivity level (MSL).

- Devices which qualify as MSL 1 are deemed not moisture sensitive
- All other devices MSL 2 through MSL 6 are deemed to be moisture sensitive.
- Moisture sensitive devices are dry baked and dry packed in accordance with IPC/JEDEC JSTD-033

To ensure proper SMT assembly, procedures must follow the MSL and maximum reflow temperature specified on the shipping bag labels or barcode labels accompanying all QCN9074 IC shipments.

Additional MSL information is included in *ASIC Packing Methods and Materials Specification* (80-VK055-1).

4.5 Thermal characteristics

Table 4-4 Device thermal resistance

Parameter		Comment	Typical	Unit
θ_{JA}	Junction-to-Ambient	■ JEDEC JESD51-2A ■ JEDEC JESD51-5	26.262	°C/W
θ_{JB}	Junction-to-Board	■ JEDEC JESD51-7 ■ JEDEC JESD51-8	13.834	°C/W
θ_{JC}	Junction-to-Case	■ JEDEC JESD51-7 ■ JEDEC JESD51-8	0.170	°C/W
Ψ_{JT}	Junction-to-Top	■ JEDEC JESD51-2A[1]	0.071	°C/W

1. Use Ψ_{JT} to calculate junction temperature from temperature measured at center of case top; Tj = Tc + (Ψ_{JT} * power)

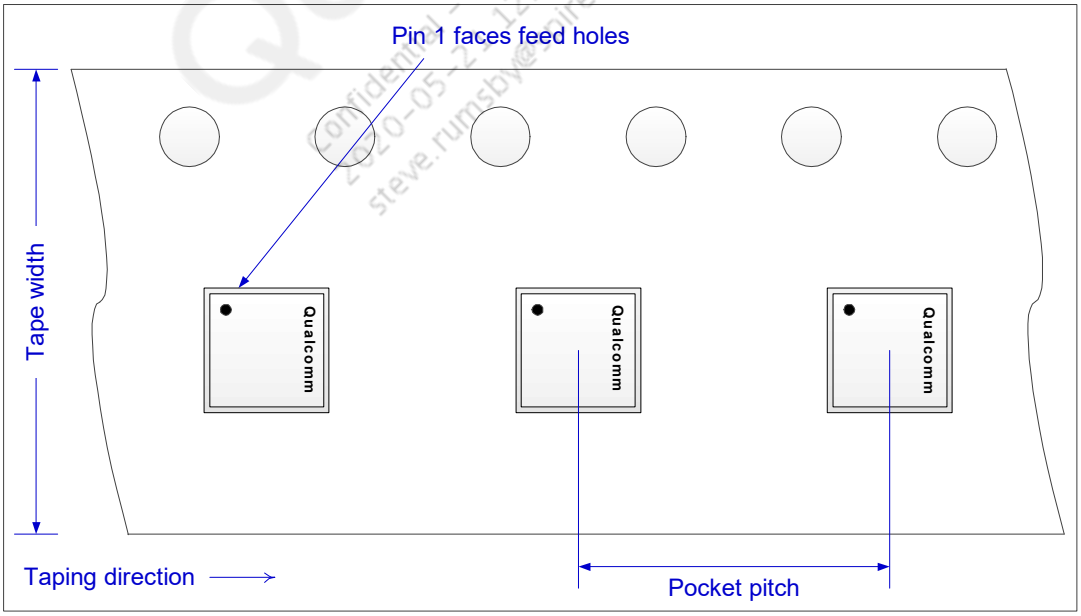
5 Carrier, storage, and handling information

5.1 Carrier

The QCN9074 package can be shipped in either matrix tray and/or tape-and-reel carriers. Carriers shall be in accordance with the IC package carrier requirements in Qualcomm documents, 80-V3652-10 (carrier tape system) and 80-V3652-11 (matrix tray system).

5.1.1 Tape and reel information

All QCT tape carrier tape systems conform to EIA-481 standards. A simplified sketch of the QCN9074 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed: Single	Reel diameter: 330 mm	Tape width: 24 mm
Units per reel: 1000 (TR)	Hub diameter: 178 mm	Pocket pitch: 16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

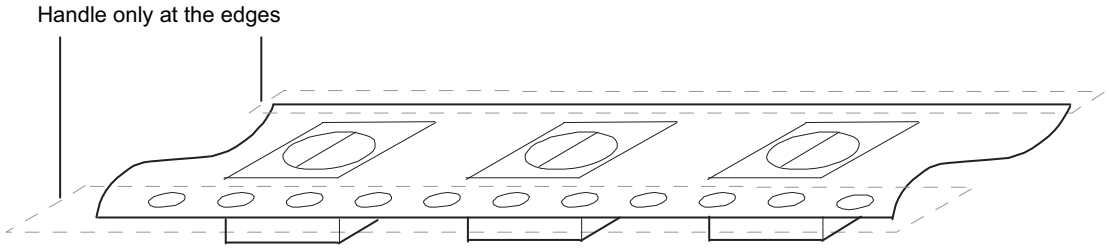
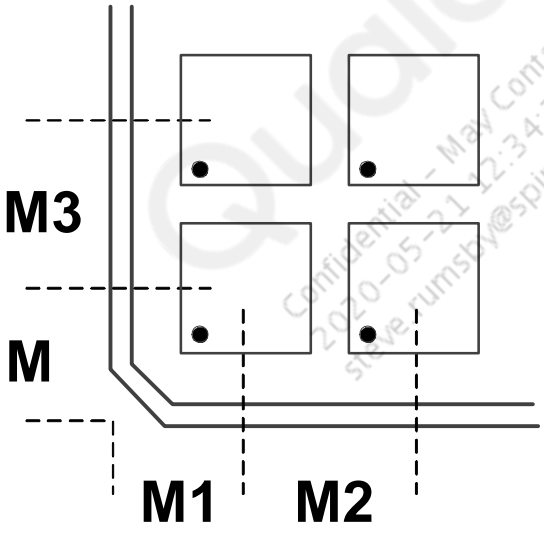


Figure 5-2 Tape handling

5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards. Each tray of the QCN9074 contains up to 8x19 (152) devices. See Figure 5-3 for matrix-tray key attributes and dimensions.



Key Dimensions	
Units per tray	8 x 19 (152)
M	11.95 mm
M1	12.15 mm
M2	16.15 mm
M3	16.00 mm
Standard bundle	10+1 trays (1520 units)

Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Storage

5.2.1 Bag storage conditions

The packages described in this document must be stored in a nitrogen-purged, sealed moisture barrier antistatic bag. The Qualcomm-calculated shelf life in a sealed moisture bag is 30 months at < 40°C and < 90% relative humidity (RH). Qualcomm recommends the following shipping and storage conditions for the FCBGA reel inside the sealed bag:

- Relative humidity between 15% and 70%
- Temperature - Room temperature lower than 30°C
- Atmosphere - A nitrogen dry cabinet is highly preferred

Devices should not be baked in tapes and reels at the temperatures described in this section, or at any other temperatures.

5.2.2 Out-of-bag duration

After unpacking, the package must be soldered to the PCB within the factory floor life according to the MSL rating when factory conditions are < 30°C and < 60% RH, as specified in the IPC/JEDEC-STD-033 standard.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented as follows:

NOTE: To eliminate damage to the silicon die due to improper handling, the following recommendations should be followed:

- Do not use tweezers, because that may cause damage to the silicon die. Qualcomm Technologies recommends using a vacuum tip to handle the device.
- Carefully select a pickup tool to avoid any damage during the SMT process.
- Do not make contact with the device while reworking or tuning components that are in close proximity to the device.

5.3.1 Baking

It is **not necessary** to bake the QCN9074 if the conditions specified in Section 5.2 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the QCN9074 if any condition specified in Section 5.2 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.4 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.5 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details

6 PCB mounting guidelines

Guidelines for mounting the QCN9074 device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

6.1 RoHS compliance

The QCN9074 device is externally lead-free and RoHS-compliant. Qualcomm defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, see the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 SMT parameters

This section describes board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.3.1 Land pad and stencil design

Qualcomm recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil-pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability. Review the land pattern and stencil pattern design recommendations as a guide for characterization:

PCB Land and Stencil Design Guide (LS90-NG134-1).

6.3.2 Reflow profile

Reflow profile conditions typically used by Qualcomm for lead-free systems are listed in Table 6-1 and are shown in Figure 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Dry-out and flux activation	150 to 190°C	60 to 120sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C. This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.3.3.

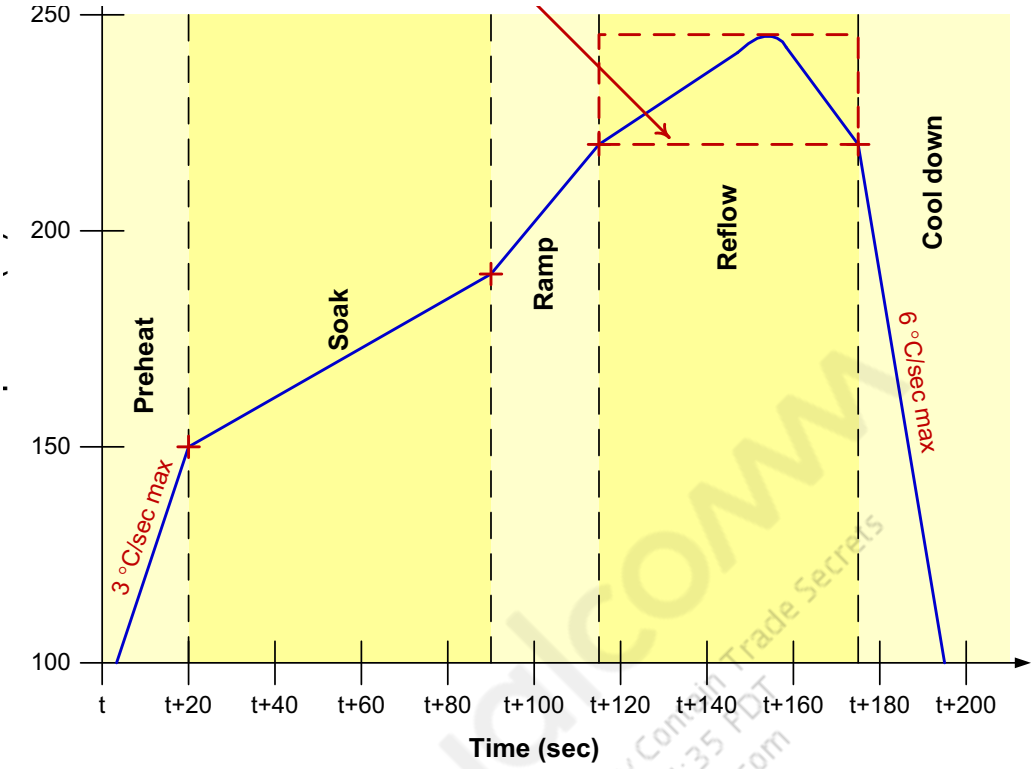


Figure 6-1 Typical SMT reflow profile

6.3.3 SMT peak package-body temperature

During a production board's reflow process, the temperature seen by the package must be controlled. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more). Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the Qualcomm recommended limits must not be exceeded.

6.3.4 SMT process verification

Qualcomm recommends verification of the SMT process prior to high-volume board assembly, including:

- Electrical continuity
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume

6.4 Board-level reliability

Qualcomm conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

For board-level reliability data, refer to *Board-Level Reliability DRQFN/mQFN* (BR80-NT096-1).

7 Part reliability

7.1 Reliability qualifications summary

This information will be included in future revisions of this document.

7.2 Qualification sample description

- Device name: QCN9074
- Package type: MSP234
- Package body size: 12.0 mm x 11.1 mm x 1.4 mm
- Lead count: 570
- Lead pitch: 0.65 mm

Revision history

Revision	Date	Description
A	February 19, 2020	Initial release
B	February 25, 2020	■ Section 2.2, Pin assignments: Updated pad # for GPIO_42, and pad names for U6 and T6 ■ Section 3.1, Absolute maximum ratings and Section 3.2, Operating conditions: Added the pad # column and updated the power supply pin names
C	April 2020	■ Section 2.2, Pin assignments: Updated description for pad # U2 ■ Section 4.5, Thermal characteristics: Updated the device thermal resistance values
D	May 2020	■ Section 7.2, Qualification sample description: Updated the package body size

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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