REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Added CAGE number 1FN41 and 34335 to the drawing as approved sources of supply. Added vendor CAGE number 18324 to device types 01ZX, 02ZX, and 03ZX, with changes to margin test methods A and B. Added device type 07 to the drawing for vendor CAGE number 65579 with changes to table I. Deleted figure 5 and table III. Also, deleted program method column from 6.6. Editorial changes throughout.	89-10-30	M. A. Frye
D	Added provisions for the addition of QD certified parts to drawing. Updated boilerplate. Added CAGE OC7V7 as supplier. - glg	00-06-23	Raymond Monnin
E	Corrected marking paragraph 3.5, updated boilerplate paragraphs. ksr	05-03-28	Raymond Monnin
F	Boilerplate update, part of 5 year review. ksr	11-03-03	Charles F. Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	F	F	F	F	F	F	F	F	F	F	F	F		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Sandra Rooney

CHECKED BY
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APPROVED BY
N A. Hauck

DRAWING APPROVAL DATE
10 January 1986

REVISION LEVEL
F

DLA LAND AND MARITIME

COLUMBUS, OHIO 43218-3990

http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 8K x 8 UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**85102**
SHEET	1 OF 12	

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

85102	01	Y	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	27C64-25	8K x 8-bit CMOS UVEPROM	250 ns
02	27C64-35	8K x 8-bit CMOS UVEPROM	350 ns
03	27C64-20	8K x 8-bit CMOS UVEPROM	200 ns
04	27C64-90	8K x 8-bit CMOS UVEPROM	90 ns
05	27C64-12	8K x 8-bit CMOS UVEPROM	120 ns
06	27C64-15	8K x 8-bit CMOS UVEPROM	150 ns
07	57C64-70	8K x 8-bit CMOS UVEPROM	70 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
Y	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Z	CQCC1-N32	32	rectangular chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Storage temperature range ..... -65°C to +150°C
All input or output voltages with respect to ground ..... -2.0 V dc to +7.0 V dc 2/
Voltage on A_9 with respect to ground ..... -2.0 V dc to +13.5 V dc 2/
V_{PP} supply voltage with respect to ground during programming ..... -2.0 V dc to +14.0 V dc 2/
Maximum power dissipation (P_D): 3/
  Device types 01 and 03 ..... 170 mW
  Device type 02 ..... 140 mW
  Device types 04, 05, 06, and 07 ..... 550 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}):
  Cases Y and Z ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C
Data Retention ..... 10 years, minimum

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Minimum dc input voltage is -0.5 V dc, during transitions, the inputs may undershoot to -2.0 V dc for periods less than 20 ns.

3/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Case operating temperature range (T_C) ..... -55°C to +125°C
Input low voltage ±10% supply (V_{IL}) ..... -0.5 V dc to +0.8 V dc
Input high voltage ±10% supply (V_{IH}) ..... 2.0 V dc to V_{CC} +0.5 V dc
Supply voltage range (V_{CC}) ..... 4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth table shall be as specified on figure 2.

3.2.2.1 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input load current	I_{LI}	V_{IN} = 5.5 V or GND 1/	1, 2, 3	All	-10	10	µA
Output leakage current	I_{LO}	V_{OUT} = 5.5 V or GND	1, 2, 3	All	-10	10	µA
Operating current, TTL inputs 2/	I_{CC} TTL	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ 0_0-0_7 = 0 mA f = 5 MHz min	1, 2, 3	04 01, 03 02 05 06 07		75 30 25 65 60 65	mA
Operating current 3/	I_{CC} CMOS	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$ 0_0-0_7 = 0 mA f = 5 MHz min	1, 2, 3	04 01,02, 03 05 06 07		60 10 55 50 70	mA
Standby current, TTL inputs 2/	I_{SB} TTL	$\overline{OE} = \overline{CE} = V_{IH}$ f = 0 MHz 0_0-0_7 = disabled	1, 2, 3	01,02, 03 04,05, 06 07		1 2 15	mA
Standby current, CMOS inputs 4/	I_{SB} CMOS	$\overline{OE} = \overline{CE} = V_{IH}$ f = 0 MHz 0_0-0_7 = disabled	1, 2, 3	01,02, 03 04,05, 06 07		140 200 500	µA
V_{PP} read current 5/	I_{PP}	$V_{PP} = V_{CC}$	1, 2, 3	All		100	µA
Input low voltage ±10% supply 6/	V_{IL}	$V_{PP} = V_{CC}$	1, 2, 3	All	-0.5	0.8	V
Input high voltage ±10% supply 6/	V_{IH}	$V_{PP} = V_{CC}$	1, 2, 3	All	2.0	V_{CC} +0.5	V
Output low voltage	V_{OL}	V_{IL} = 0.8 V, V_{IH} = 2.0 V I_{OL} = 2.1 mA	1, 2, 3	01-06 07		0.45 0.4	V
Output high voltage	V_{OH}	V_{IL} = 0.8 V, V_{IH} = 2.0 V I_{OH} = -400 µA	1, 2, 3	All	2.4		V
Output short-circuit current	I_{OS} 6/		1, 2, 3	All		100	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
V_{PP} read voltage 7/	V_{PP}		1, 2, 3	All	V_{CC} -0.7	V_{CC}	V
Input capacitance	C_{IN}	V_{IN} = 0 V, See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, See 4.3.1c	4	All		12	
Functional tests		See 4.3.1e	7, 8	All			
Address to output delay 8/ 9/	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	04		90	ns
				01		250	
				02		350	
				03		200	
				05		120	
				06		150	
				07		70	
$\overline{CE}$ to output delay 8/ 9/	t_{CE}	$\overline{OE}$ = V_{IL}	9, 10, 11	04		90	ns
				01		250	
				02		350	
				03		200	
				05		120	
				06		150	
				07		70	
$\overline{OE}$ to output delay 8/ 9/	t_{OE}	$\overline{CE}$ = V_{IL}	9, 10, 11	04, 07		30	ns
				01		100	
				02		120	
				03		75	
				05		35	
				06		45	
$\overline{OE}$ high to output float 8/ 9/	t_{DF} 6/	$\overline{CE}$ = V_{IL}	9, 10, 11	04, 07	0	25	ns
				01, 03	0	55	
				02	0	105	
				05	0	35	
				06		40	
Output hold from $\overline{addresses}$, CE or OE whichever occurred first 8/ 9/	t_{OH} 6/	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	01-06	0		ns
				07	10		

1/ Pins not tested are all at GND and 5.5 V respectively.
2/ TTL inputs: Specify V_{IL} and V_{IH} levels.
3/ CMOS inputs: GND $\pm$0.2 V to V_{CC} $\pm$0.2 V.
4/ CE = V_{CC} $\pm$0.2 V. All other inputs can have any value within specified limits.
5/ Maximum active power usage is the sum of $I_{PP} + I_{CC}$.
6/ If not tested, shall be guaranteed to the limits specified in table I.
7/ V_{PP} may be connected directly to V_{CC} except during programming.
8/ Outputs shall be loaded in accordance with figure 3.
9/ See figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A. For Class Q product built in accordance with A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified by the manufacturer.

3.10.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified by the manufacturer.

3.10.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device Types	All		
Case Outlines	Y		Z
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	V_{PP}	1	NC
2	A12	2	V_{PP}
3	A7	3	A12
4	A6	4	A7
5	A5	5	A6
6	A4	6	A5
7	A3	7	A4
8	A2	8	A3
9	A1	9	A2
10	A0	10	A1
11	O0	11	A0
12	O1	12	NC
13	O2	13	O0
14	V_{SS}	14	O1
15	O3	15	O2
16	O4	16	V_{SS}
17	O5	17	NC
18	O6	18	O3
19	O7	19	O4
20	$\overline{CE}$	20	O5
21	A10	21	O6
22	$\overline{OE}$	22	O7
23	A11	23	$\overline{CE}$
24	A9	24	A10
25	A8	25	$\overline{OE}$
26	NC	26	NC
27	$\overline{PGM}$	27	A11
28	V_{CC}	28	A9
29	- - -	29	A8
30	- - -	30	NC
31	- - -	31	$\overline{PGM}$
32	- - -	32	V_{CC}

FIGURE 1. Terminal connections.

Read modes (see notes 1 and 2)

Mode Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0 V $\pm$0.5 V.

FIGURE 2. Truth table.

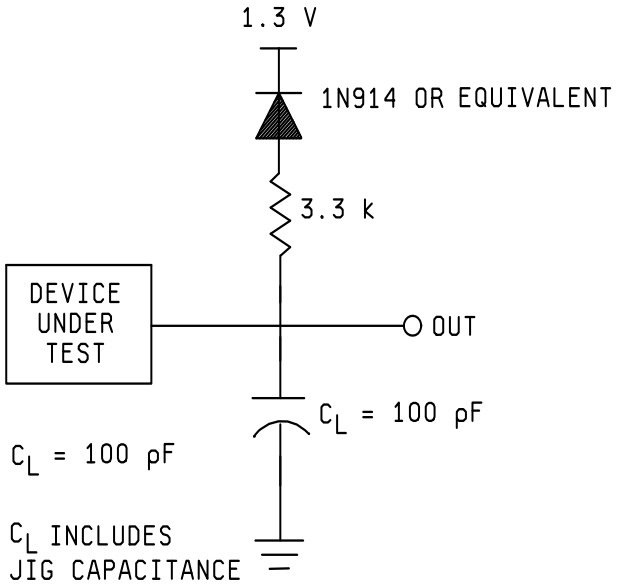
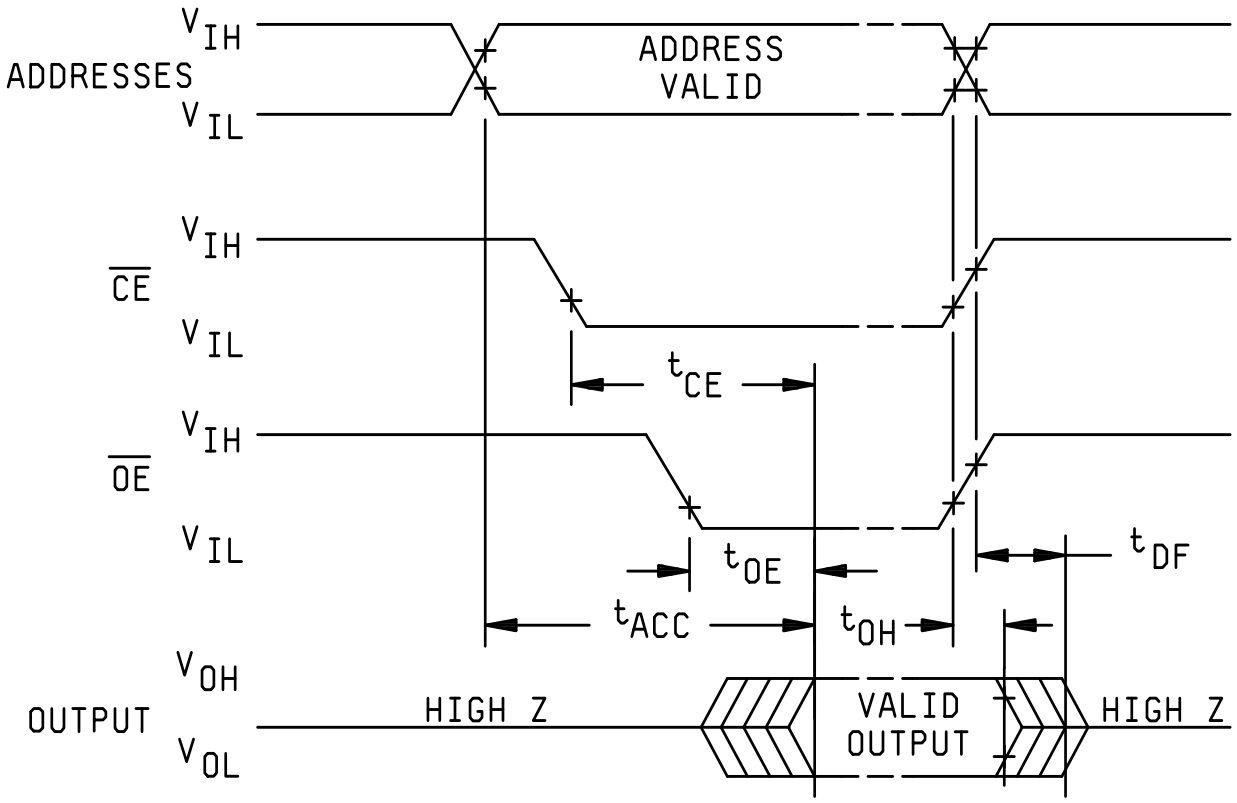


FIGURE 3. Output loading.



NOTES:

1. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
3. AC characteristics tested at V_{IH} = 2.4 V and V_{IL} = 0.45 V, timing measurement made at 2.0 V and 0.8 V levels.

FIGURE 4. Timing waveform.

TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8A, 10

* PDA applies to subgroups 1 and 7. Any or all subgroups may be combined when using a high speed tester.

1/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

2/ For all electrical tests, the device shall be programmed to the pattern specified in 4.3.1(d).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups C and D testing).

e. Subgroup 7 and 8 shall include verification of the pattern specified in 4.3.1(d).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone 614-692-0540.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-03-03

Approved sources of supply for SMD 85102 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8510201YA	0C7V7	QP27C64-25/YA
	3/	MD27C64-25/B
	3/	MD27C64-25/BYA
	3/	NMC2764Q25/883
	3/	27C64A/BXA-25
	3/	WS27C64L-25DMB
8510201ZA	0C7V7	QP27C64-25/ZA
	3/	MR27C64-25/B
	3/	MR27C64-25/BZA
	3/	27C64A/BUA-25
	3/	WS27C64L-25CMB
8510202YA	0C7V7	QP27C64-35/YA
	3/	MD27C64-35/B
	3/	MD27C64-35/BYA
	3/	NMC2764Q35/883
	3/	27C64A/BXA-35
	3/	WS27C64L-35DMB
8510202ZA	0C7V7	QP27C64-35/ZA
	3/	MR27C64-35/B
	3/	MR27C64-35/BZA
	3/	27C64A/BUA-35
	3/	WS27C64L-35CMB
8510203YA	0C7V7	QP27C64-20/YA
	3/	MD27C64-20/B
	3/	MD27C64-20/BYA
	3/	NMC2764Q20/883
	3/	27C64A/BXA-20
	3/	WS27C64L-20DMB
8510203ZA	0C7V7	QP27C64-20/ZA
	3/	MR27C64-20/B
	3/	MR27C64-20/BZA
	3/	27C64A/BUA-20
	3/	WS27C64L-20CMB
8510204YA	0C7V7	QP27C64-90/YA
	3/	AT27HC64L-90DM/883
	3/	AM27C64-90/BXA
	3/	WS27C64L-90DMB

See footnote at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8510204ZA	0C7V7	QP27C64-90/ZA
	3/	AT27HC64L-90LM/883
	3/	AM27C64-90/BUA
	3/	WS27C64L-90CMB
8510205YA	0C7V7	QP27C64-12/YA
	3/	AM27C64-120/BXA
	3/	WS27C64L-12DMB
8510205ZA	0C7V7	QP27C64-12/ZA
	3/	AM27C64-120/BUA
	3/	WS27C64L-12CMB
8510206YA	0C7V7	QP27C64-15/YA
	3/	AM27C64-150/BXA
	3/	WS27C64L-15DMB
8510206ZA	0C7V7	QP27C64-15/ZA
	3/	AM27C64-150/BUA
	3/	WS27C64L-15CMB
8510207YA	0C7V7	QP57C64-70/YA
	3/	WS57C64F-70DMB
8510207ZA	0C7V7	QP57C64-70/ZA
	3/	WS57C64F-70CMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.