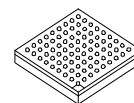




MCIMX6L



Package Information
Plastic Package
13 x 13 mm, 0.5 mm pitch

i.MX 6SoloLite Applications Processors for Consumer Products

Ordering Information

See [Table 1 on page 3](#)

1 Introduction

The i.MX 6SoloLite processor represents Freescale's latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processor features Freescale's advanced implementation of the a single ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. It includes 2D graphics processor and integrated power management. The processor provides a 32-bit DDR3-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6SoloLite processor is specifically useful for applications, such as:

- Color and monochrome eReaders
- Entry level tablets
- Barcode scanners

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The i.MX 6SoloLite processor features:

- **Applications processor**—The processor enhances the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- **Multilevel memory system**—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, and managed NAND, including eMMC up to rev 4.4.
- **Smart speed technology**—The processor has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- **Dynamic voltage and frequency scaling**—The processor improves the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- **Multimedia powerhouse**—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, and a programmable smart DMA (SDMA) controller.
- **Powerful graphics acceleration**—Each processor provides three independent, integrated graphics processing units: 2D BLit engine, a 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- **Interface flexibility**—The processor supports connections to a variety of interfaces: LCD controller, CMOS sensor interface (parallel), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Mbps Ethernet controller, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio).
- **Electronic Paper Display Controller**—The processor integrates EPD controller that supports E-INK color and monochrome with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh and 5-bit grayscale (32-levels per color channel). The processor also integrates an EPD controller that supports SiPix monochrome panels.
- **Advanced security**—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6SoloLite security reference manual. Contact your local Freescale representative for more information.
- **Integrated power management**—The processor integrates linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.
- **GPIO with interrupt capabilities**—The new GPIO pad design supports configurable dual voltage rails at 1.8V and 3.3V supplies. The pad is configurable to interface at either voltage level.

1.1 Ordering Information

Table 1 shows the orderable part numbers covered by this datasheet. **Table 1** does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in **Table 1**, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Orderable Part Numbers

Part Number ¹	Mask Set	Options	Speed Grade	Temperature (Tj)	Package ²
MCIMX6L8DVN10AA	N20G	With GPU, E-ink	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L7DVN10SA	N20G	With Sipix	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L3EVN10AA	N20G	With GPU	1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA
MCIMX6L2EVN10AA	N20G		1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA

¹ Part numbers with a PC prefix indicate non-production engineering parts.

² Case 2240 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

Figure 1 describes the part number nomenclature so that users can identify the characteristics of the specific part number they have (for example, Cores, Frequency, Temperature Grade, Fuse options, Silicon revision).

Ensure that you have the right datasheet for your specific part by checking the Temperature Grade (Junction) field and matching it to the right datasheet. If you have questions, see freescale.com/imx6series or contact your Freescale representative.

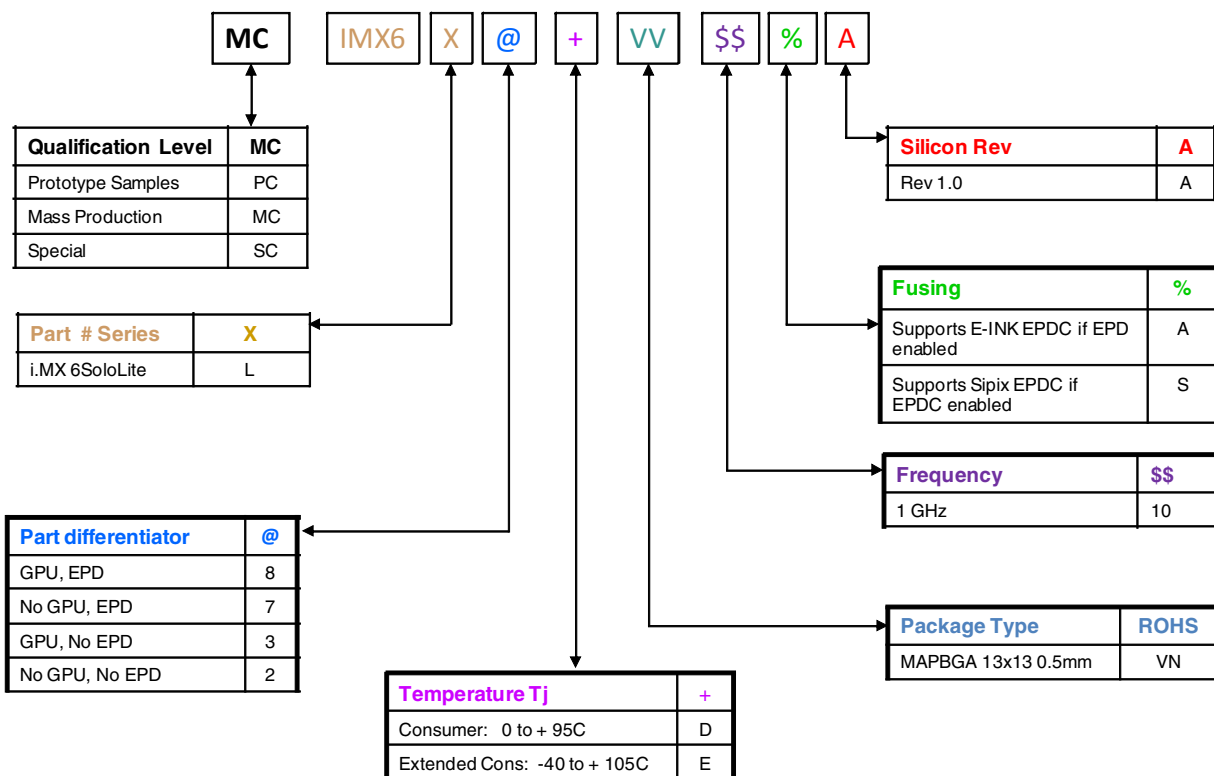


Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore CPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
 - 32 KByte L1 Instruction Cache
 - 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per [Table 9, "Operating Ranges," on page 21](#)
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (256 KByte)
- On-Chip Memory:
 - Boot ROM, including HAB (96 KB)
 - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
- External memory interfaces:
 - 16-bit, and 32-bit DDR3-800, and LPDDR2-800 channels
 - 16/32-bit NOR Flash.
 - 16/32-bit PSRAM, Cellular RAM (32 bits or less)

Each i.MX 6SoloLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total three interfaces are available.
 - LCD, 24bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz)

- EPDC, color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
- SPDC, color, and monochrome SiPix panels
- Camera sensors:
 - Parallel Camera port (up to 16 bit)
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
 - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
 - One USB 2.0 (480 Mbps) hosts:
 - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
 - Three I²S/SSI/AC97 supported
 - Five UARTs, up to 4.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Four eCSPI (Enhanced CSPI)
 - Three I²C, supporting 400 kbps
 - Ethernet Controller, 10/100 Mbps
 - Four Pulse Width Modulators (PWM)
 - System JTAG Controller (SJC)
 - GPIO with interrupt capabilities
 - 8x8 Key Pad Port (KPP)
 - Sony Philips Digital Interface (SPDIF), Rx and Tx
 - Two Watchdog timers (WDOG)
 - Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloLite processor uses dedicated HW accelerators to meet the targeted multimedia performance. The use of HW accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloLite processor incorporates the following hardware accelerators:

- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSES and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in [Table 1, "Orderable Part Numbers," on page 3](#). Functions, such as 2D hardware graphics acceleration, E-Ink or SiPix may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloLite processor system.

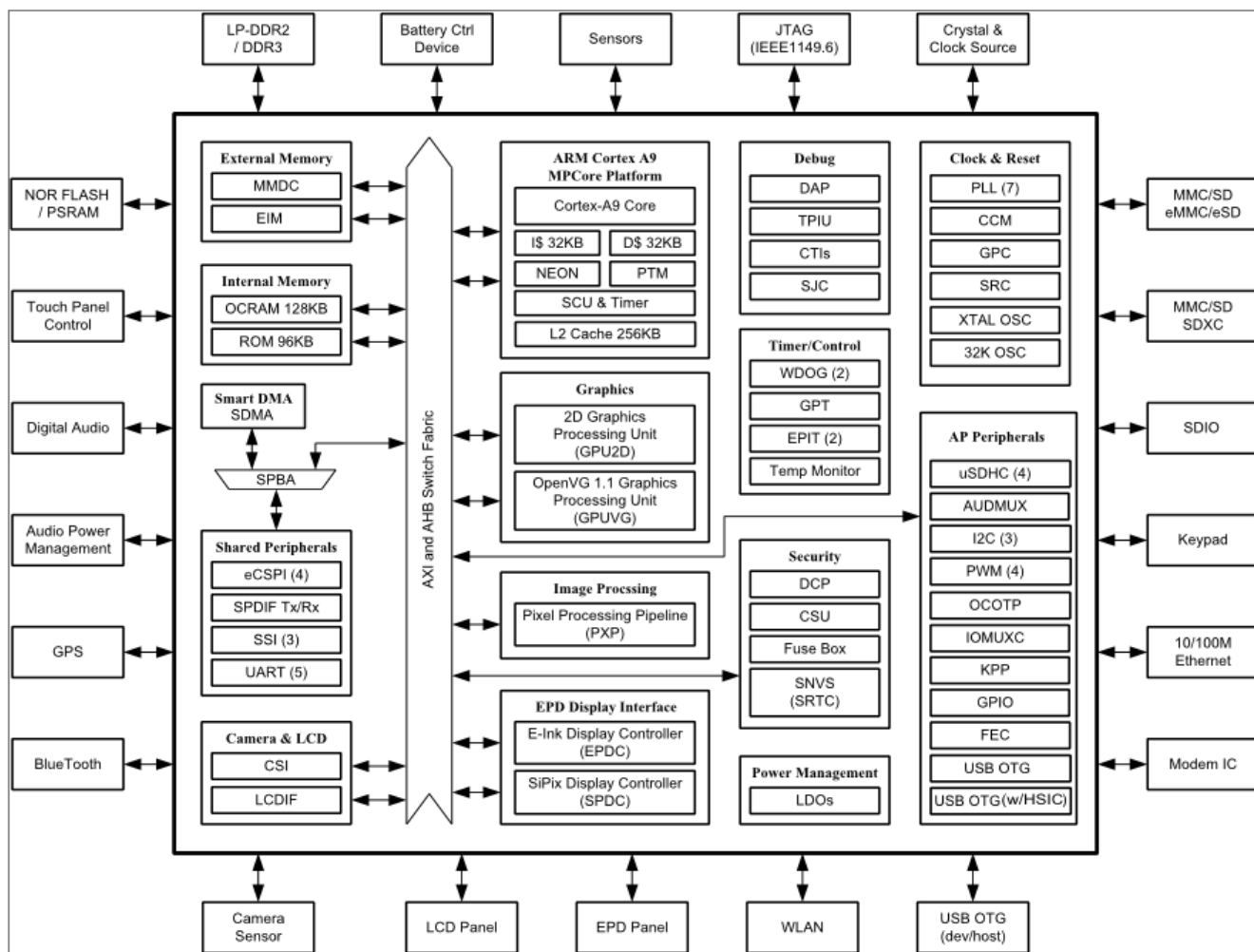


Figure 2. i.MX 6SoloLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcpy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tessellation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I ² C-1 I ² C-2 I ² C-3	I ² C Interface	Connectivity Peripherals	I ² C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSES). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD. either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Softwareitching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDC	Electrophoretic Display Controller	Peripherals	The SPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive SiPix™ EPD panels, supporting a wide variety of TFT backplanes.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • One Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: - Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. - Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. - Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 - Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: - Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset - All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SoloLite processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, “Package Information and Contact Assignments.” Signal descriptions are provided in the i.MX 6SoloLite reference manual.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: - To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. - To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the i.MX 6SoloLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximal clock out frequency range supported is 528 MHz. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLK1 input/output could be disabled (if not used). If unused, the CLK1_N/P pair may be left floating.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the $\pm$ 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SoloLite are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices).
GPANAIO	This signal is reserved for Freescale manufacturing use only. User must leave this connection floating.
JTAG_nnnn	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up. JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided. JTAG_MOD is referenced as SJC_MOD in the i.MX 6SoloLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to Software controllable power down). Long above ~5s connection to GND causes “forced” OFF.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤ 100 k Ω ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 M Ω). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μ W. An ESR (equivalent series resistance) of typically 80 Ω is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from $\sim 0.8 \times \text{NVCC_PLL_OUT}$ to ~ 0.2 V. This clock is used as a reference for USB, PCIe, and SATA, so there are strict frequency tolerance and jitter requirements. See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual, for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 k Ω pull-up
JTAG_TMS	Input	47 k Ω pull-up
JTAG_TDI	Input	47 k Ω pull-up
JTAG_TDO	3-state output	Keeper

Table 4. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-Chip Termination
JTAG_TRSTB	Input	47 k Ω pull-up
JTAG_MOD	Input	100 k Ω pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, ...	Topic appears ...
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 18
Operating Ranges	on page 21
External Clock Sources	on page 22
Maximal Supply Currents	on page 23
Low Power Mode Supply Currents	on page 24
USB PHY Current Consumption	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under [Table 7](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max ¹	Unit
Core supply voltages	VDD_ARM_IN VDD_SOC_IN VDD_PU_IN	-0.3	1.5	V
Internal supply voltages	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V _{in} /V _{out}	-0.5	OVDD ² +0.3	V
ESD Immunity (HBM)	Vesd_CDM	—	2000	V
ESD Immunity (CDM)	Vesd_CDM	—	500	V
Storage temperature range	T _{STORAGE}	-40	150	°C

¹ Exceeding maximum may result in breakdown, or reduction in IC life time, performance, and/or reliability.

² OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

[Table 8](#) provides the MAPBGA package thermal resistance data.

Table 8. Package Thermal Resistance Data

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient ¹ (natural convection)	Single layer board (1s)	R _{θJA}	51	°C/W
	Four layer board (2s2p)	R _{θJA}	28	°C/W

Table 8. Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient ¹ (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board ²	—	$R_{\theta JB}$	14	°C/W
Junction to Case ³ (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top ⁴	Natural Convection	Ψ_{JT}	2	°C/W

- ¹ Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
- ² Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
- ³ Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- ⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Figure 3 shows major power systems blocks and internal/external connections for the i.MX 6SoloLite processor.

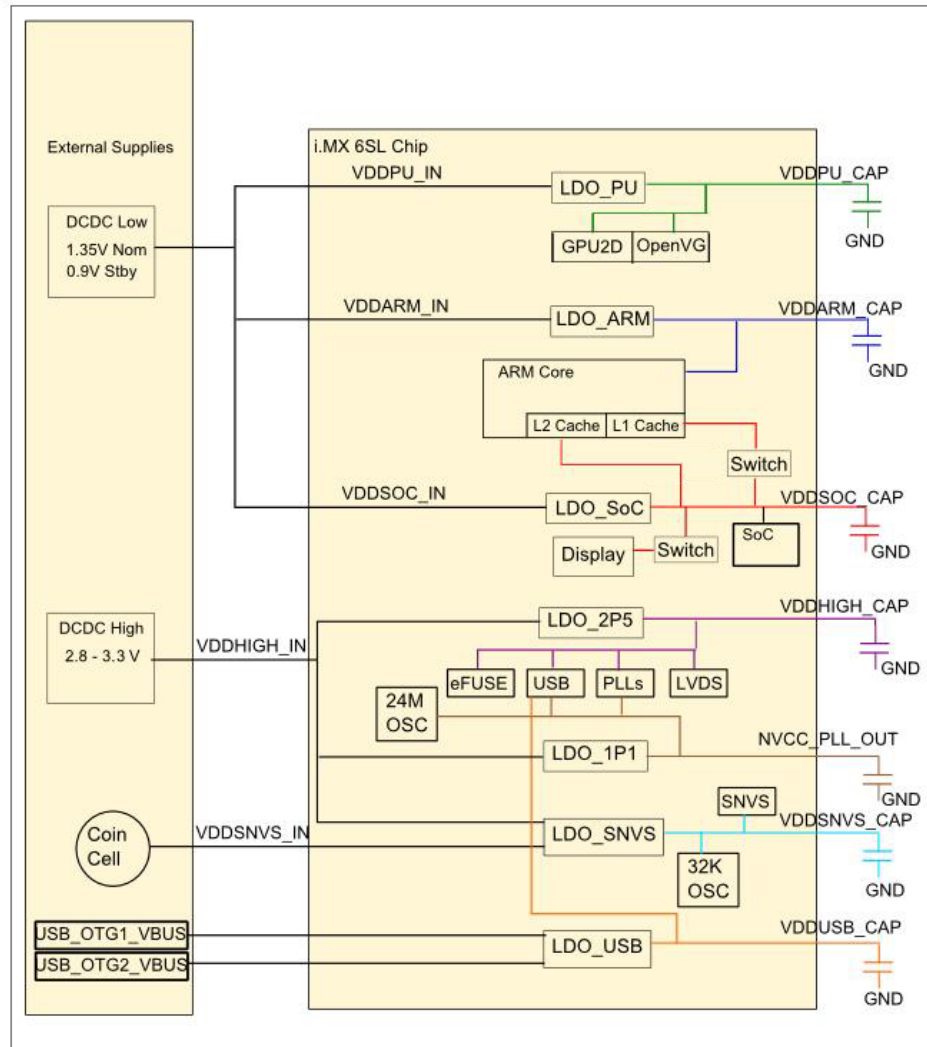


Figure 3. i.MX 6SoloLite SoC Power Block Diagram

Table 9 provides the operating ranges of the i.MX 6SoloLite processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375 ²		1.5	V	LDO output set at 1.250V minimum for operation up to 996MHz.
		1.275 ²		1.5	V	LDO output set at 1.150V minimum for operation up to 792MHz
		1.075 ²		1.5	V	LDO output set at 0.95V minimum for operation up to 396MHz
		1.075 ²		1.5	V	LDO output set at 0.950V minimum for operation up to 192MHz
		1.050 ²		1.5	V	LDO output set at 0.9250V minimum for operation up to 24MHz
	VDD_SOC_IN ³ VDD_PU_IN	1.275 ^{2,4}		1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250		1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 396 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 192MHz
		0.925		1.3	V	LDO bypassed for operation up to 24MHz
	VDD_SOC_IN ³ VDD_PU_IN	1.15 ⁴		1.3	V	
Standby/DSM Mode	VDD_ARM_IN	0.9		1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 24.
	VDD_SOC_IN VDD_PU_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN ⁵	2.8		3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN ⁵	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
GPIO supplies ⁶	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	
	NVCC_1P2V		1.2			
Junction temperature	T _J	0		95	°C	Consumer
Junction temperature	T _J	-40		105		Extended Consumer

¹ Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (V_{min} + the supply tolerance). This results in an optimized power/speed ratio.

² VDD_ARM_IN and VDDSOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

³ VDD_SOC_CAP and VDD_PU_CAP must be equal.

⁴ VDDSOC and VDDPU output voltage must be set to this rule: VDDARM-VDDSOC/PU<50mV

⁵ While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

⁶ All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTAL) and a high frequency (XTAL).

The RTC_XTAL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and Watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTAL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTAL Oscillator ^{1,2}	f _{ckil}	—	32.768 ³ /32.0	—	kHz
XTAL Oscillator ^{4,2}	f _{xtal}		24		MHz

¹ External oscillator or a crystal with internal oscillator amplifier.

² The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

³ Recommended nominal frequency 32.768 kHz.

⁴ External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in [Table 10](#) are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
 - Approximately 25 μ A more I_{dd} than crystal oscillator
 - Approximately $\pm 50\%$ tolerance
 - No external component required
 - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
 - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
 - Higher accuracy than ring oscillator
 - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in [Table 11](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6SoloLite Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30 ¹	mA
VDD_SNVS_IN	—	250 ²	μ A

Table 11. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
USB_OTG1_VBUS USB_OTG2_VBUS	—	25 ³	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	— ⁴	
NVCC33_IO	N=156	Use maximal IO Equation ⁵	
NVCC18_IO	N=156	Use maximal IO Equation ⁵	
MISC			
DRAM_VREF	—	1	mA

¹ The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

² The maximum VDD_SNVIS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVIS_IN can draw up to 1 mA, if available. VDD_SNVIS_CAP charge time will increase if less than 1 mA is available.

³ This is the maximum current per active USB physical interface.

⁴ The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

⁵ General equation for estimated, maximal power consumption of an IO power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical ¹	Unit
WAIT	- ARM, SoC, and PU LDOs are set to 1.225 V - HIGH LDO set to 2.5 V - Clocks are gated - DDR is in self refresh - PLLs are active in bypass (24 MHz) - Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW

Table 12. Stop Mode Current and Power Consumption (continued)

STOP_ON	- ARM LDO set to 0.9 V - SoC and PU LDOs set to 1.225 V - HIGH LDO set to 2.5 V - PLLs disabled - DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN (3.0 V)	4.5	
		Total	29.3	mW
STOP_OFF	- ARM LDO set to 0.9 V - SoC LDO set to 1.225 V - PU LDO is power gated - HIGH LDO set to 2.5 V - PLLs disabled - DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	0.1	
		VDD_HIGH_IN (3.0 V)	4.0	
		Total	25.9	mW
STANDBY	- ARM and PU LDOs are power gated - SoC LDO is in bypass - HIGH LDO is set to 2.5 V - PLLs are disabled - Low voltage - Well Bias ON - XTAL is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	1.0	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	3	
		Total	10.1	mW
Deep Sleep Mode (DSM)	- ARM and PU LDOs are power gated - SoC LDO is in bypass - HIGH LDO is set to 2.5 V - PLLs are disabled - Low voltage - Well Bias ON - XTAL and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	0.75	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	0.15	
		Total	1.3	mW

¹ The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. [Table 13](#) shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 μ A	1.7 μ A	<0.5 μ A

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDD_ARM_IN and VDD_SOC_IN are connected to different external supply sources, then VDD_ARM_IN supply must be turned ON together with VDD_SOC_IN supply or not delayed more than 1 ms.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6SoloLite reference manual for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

4.2.2 Power-Down Sequence

Table 14 shows the power down sequence orders. The two cases shown are, using the i.MX6 SoloLite internal supplies (non-bypass) and bypassing the internal LDO supplies.

Table 14. Power-Down Sequencing Order

Power Rail Name	Using all internal LDOs (non-bypass mode)	Internal LDOs Bypassed
VDD_SNVS_IN	7	9
VDD_HIGH_IN / NVCC33_IO	6	8
VDD_HIGH_CAP	6	7
NVCC18_IO	5	6
NVCC_PLL	6	5
NVCC_DRAM	4	4
VDD_ARM_IN	3	3
VDD_PU_IN	2	2
VDD_SOC_IN	1	1
USB_VBUS	N/A	N/A

NOTE

- VDD_ARM_IN, VDD_PU_IN, and VDD_SOC_IN can startup at the same. However, VDD_ARM_IN and VDD_PU_IN must be at their target values within 0.5 ms of VDD_SOC_IN.
- There are no special timing requirements for USB_VBUS.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 80, “13 x 13 mm Functional Contact Assignments,” on page 101.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6SoloLite reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see [Table 9](#) for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 15. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz

Table 15. Audio/Video PLL's Electrical Parameters (continued)

Parameter	Value
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μ s)

4.4.2 528 MHz PLL

Table 16. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μ s)

4.4.3 Ethernet PLL

Table 17. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μ s)

4.4.4 480 MHz PLL

Table 18. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles (15 μ s)

4.4.5 ARM PLL

Table 19. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz

Table 19. ARM PLL's Electrical Parameters (continued)

Parameter	Value
Reference clock	24 MHz
Lock time	<2250 reference cycles (50 μ s)

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. It also implements a power mux such that the oscillator can be powered from VDD1P1 or VDD_SOC. VDD_1P1 should be the cleaner supply and is the preferable choice, but if the oscillator is needed to run in "stop mode" then it is necessary to run from VDD_SOC, which is 0.9 V in stop mode.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, $R_s = (3.2 - 2.5) / 0.6 \text{ m} = 1.17 \text{ k}$

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc		32.768 kHz		This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption		4 μ A		The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μ A should be added to this value.
Bias resistor		14 M Ω		This is the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 k Ω		Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIIO)
- Single Voltage General Purpose I/O cell set (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

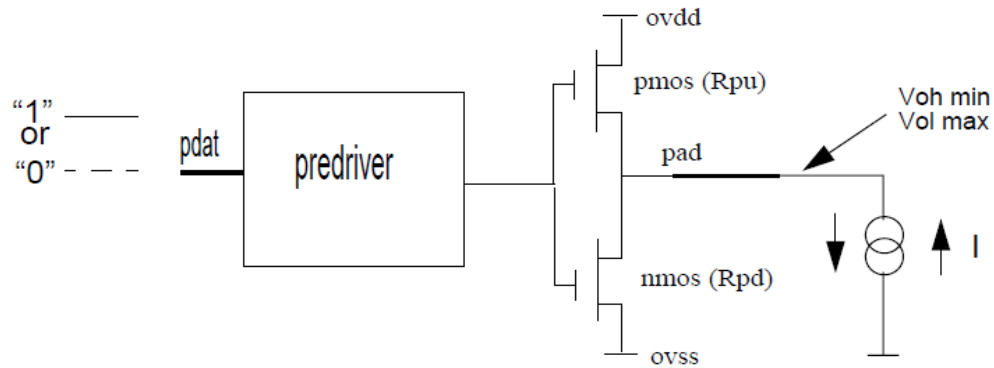


Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 Dual Voltage General Purpose IO cell set (DVGPIO) DC parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 21. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage ¹	Voh	Ioh = -0.1 mA (DSE ² = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD - 0.15	—	V
Low-level output voltage ¹	Vol	Iol = 0.1 mA (DSE ² = 001, 010) Iol = 1 mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage ^{1, 3}	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage ^{1, 3}	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+ ^{3, 4}	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT- ^{3, 4}	VT-	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	μA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	μA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	μA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	48 1	μA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	μA
Keeper circuit resistance	Rkeep	Vin = 0.3 × OVDD Vin = 0.7 × OVDD	105	205	kΩ

Table 21. DVGPI0 I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Sink current in Open Drain mode	Iskod	—	—	7	mA
Sink/source current in Push-Pull mode	Isspp	—	—	7	mA

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² DSE is the Drive Strength Field setting in the associated IOMUX control register.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.2 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 22. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage ¹	Voh	Ioh = -0.1 mA (DSE ² = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD - 0.15	—	V
Low-level output voltage ¹	Vol	Iol = 0.1 mA (DSE ² = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage ^{1, 3}	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage ^{1, 3}	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+ ^{3, 4}	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT- ^{3, 4}	VT-	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	μA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	μA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	μA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	48 1	μA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	μA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

Table 22. GPIO I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Sink current in Open Drain mode	Iskod	—	—	7	mA
Sink/source current in Push-Pull mode	Isspp	—	—	7	mA

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² DSE is the Drive Strength Field setting in the associated IOMUX control register.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The parameters in [Table 23](#) are guaranteed per the operating ranges in [Table 9](#), unless otherwise noted.

Table 23. LPDDR2 I/O DC Electrical Parameters¹

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9*OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1*OVDD	V
Input reference voltage	Vref		0.49*OVDD	0.51*OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)		0.26	See Note ²	
Differential Input Logic Low	Vil(diff)		See Note ²	-0.26	
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	μA
Pull-up/pull-down impedance Mismatch	MMpupd		-15	+15	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see [Table 27](#)).

4.6.3.2 DDR3 Mode I/O DC Parameters

The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 24 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

4.7 I/O AC Parameters

Table 24. DDR3 I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA Voh (DSE = 001)	0.8*OVDD ¹	—	V
		Ioh = -1 mA Voh (for all except DSE = 001)			
Low-level output voltage	Vol	Iol = 0.1 mA Vol (DSE = 001)	—	0.2*OVDD	V
		Iol = 1 mA Vol (for all except DSE = 001)			
Input reference voltage	Vref ²		0.49*OVDD	0.51*OVDD	
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	See Note ³	V
Differential input Logic Low	Vil(diff)	—	See Note ³	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	μA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance ⁴	Rkeep	—	105	175	kΩ

¹ OVDD – I/O power supply (1.425 V–1.575 V for DDR3)

² Vref – DDR3 external reference voltage

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 28).

⁴ Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Dual Voltage General Purpose I/O (DVGPIIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

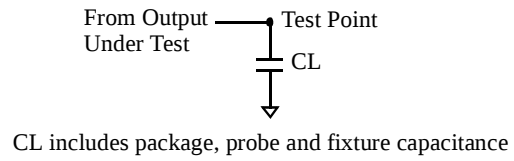


Figure 5. Load Circuit for Output

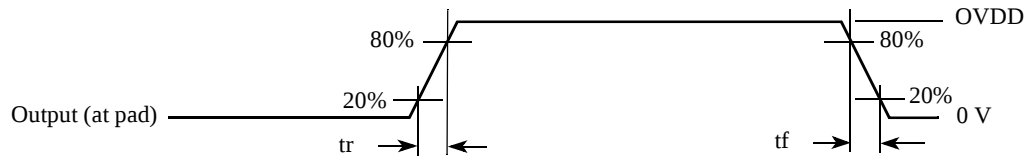


Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the [Table 25](#) and [Table 26](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 27 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 27. DDR I/O LPDDR2 Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage ²	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage ³	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω $\pm$ 30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω $\pm$ 30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t _{SKD}	clk = 400 MHz	—	—	0.1	ns

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage $V_{tr} - V_{cp}$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.

³ The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 28 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 28. DDR I/O DDR3 Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage ²	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage ³	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns

Table 28. DDR I/O DDR3 Mode AC Parameters¹ (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t _{SKD}	clk = 400 MHz	—	—	0.1	ns

¹ Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage |V_{tr}-V_{cpl}| required for switching, where V_{tr} is the “true” input signal and V_{cpl} is the “complementary” input signal. The Minimum value is equal to V_{ih}(ac) – V_{il}(ac).

³ The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

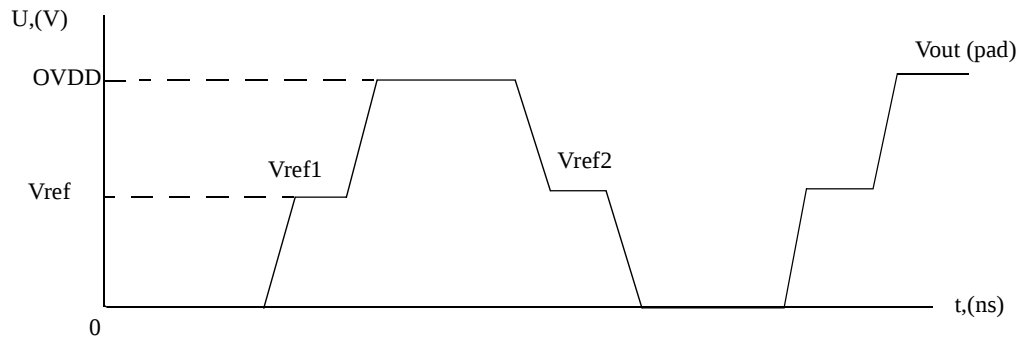
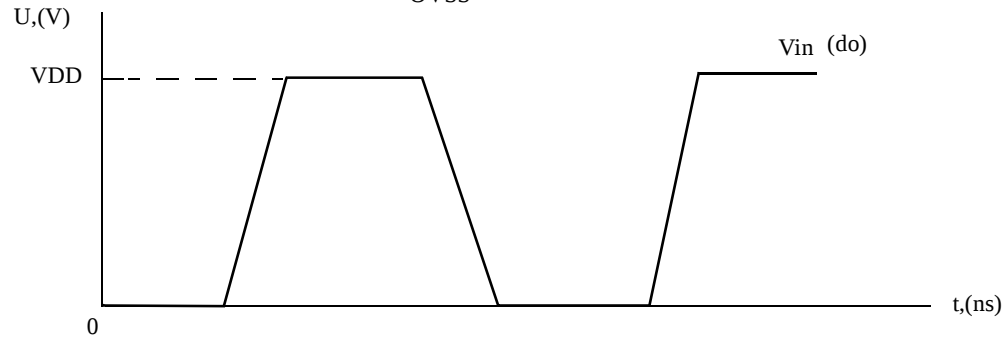
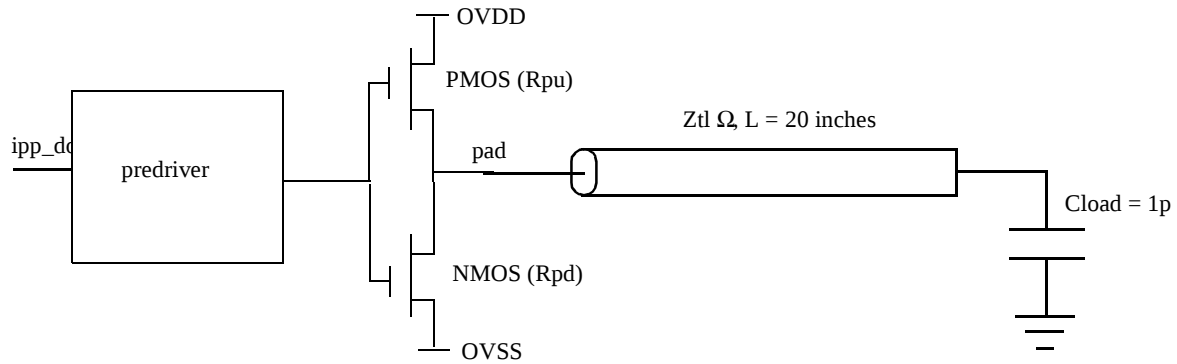
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloLite processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPI0)
- Single Voltage General Purpose I/O cell set (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see [Figure 7](#)).



$$R_{pu} = \frac{V_{ovdd} - V_{ref1}}{V_{ref1}} \times Z_{tl}$$

$$R_{pd} = \frac{V_{ref2}}{V_{ovdd} - V_{ref2}} \times Z_{tl}$$

Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 29 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 29. DVGPI Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	260	Ω
		010	130	
		011	90	
		100	60	
		101	50	
		110	40	
		111	33	

Table 30 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 30. DVGPI Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	150	Ω
		010	75	
		011	50	
		100	37	
		101	30	
		110	25	
		111	20	

4.8.2 Single Voltage GPIO Output Buffer Impedance

Table 31 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 31. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	150	Ω
		010	75	
		011	50	
		100	37	
		101	30	
		110	25	
		111	20	

4.8.3 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 32 shows DDR I/O output buffer impedance of i.MX 6SoloLite processor.

Table 32. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is $\pm 5\%$ (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloLite processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 33 lists the timing parameters.

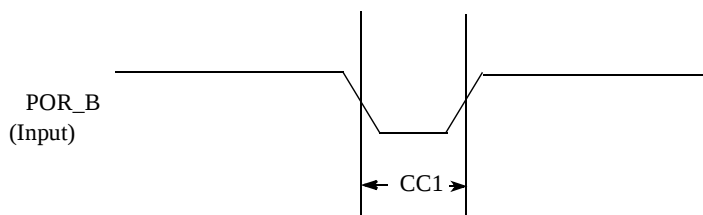


Figure 8. Reset Timing Diagram

Table 33. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope ≤ 5 ns)	1	—	XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 34 lists the timing parameters.

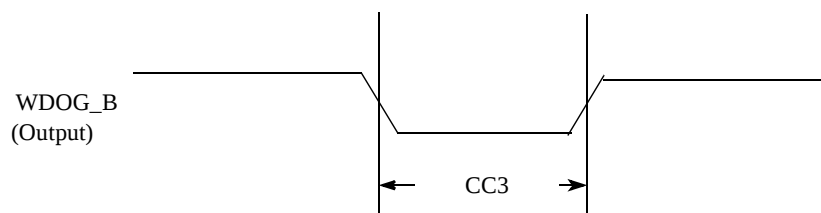


Figure 9. WDOG_B Timing Diagram

Table 34. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	XTALI cycle

NOTE

XTALI is approximately 32 kHz. XTALI cycle is one period or approximately 30 μ s.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 35 is a guide intended to help the user identify the signals in the EIM chapter of the i.MX 6SoloLite reference manual that are identical to those mentioned in this data sheet.

Table 35. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.9.3.2 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit, and 8-bit devices operating in address/data separate or multiplexed modes. Table 36 provides EIM interface pads allocation in different modes.

Table 36. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode			Multiplexed Address/Data mode	
	8 Bit		16 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001	MUM = 1, DSZ = 010	MUM = 1, DSZ = 011
A[15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]
A[25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_D [9:0]
D[7:0], EIM_EB0	EIM_D [7:0]	—	EIM_D [7:0]	EIM_DA_A [7:0]	EIM_DA_A [7:0]
D[15:8], EIM_EB1	—	EIM_D [15:8]	EIM_D [15:8]	EIM_DA_A [15:8]	EIM_DA_A [15:8]
D[23:16], EIM_EB2	—	—	—	—	EIM_D [7:0]
D[31:24], EIM_EB3	—	—	—	—	EIM_D [15:8]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6SoloLite reference manual.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 37 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

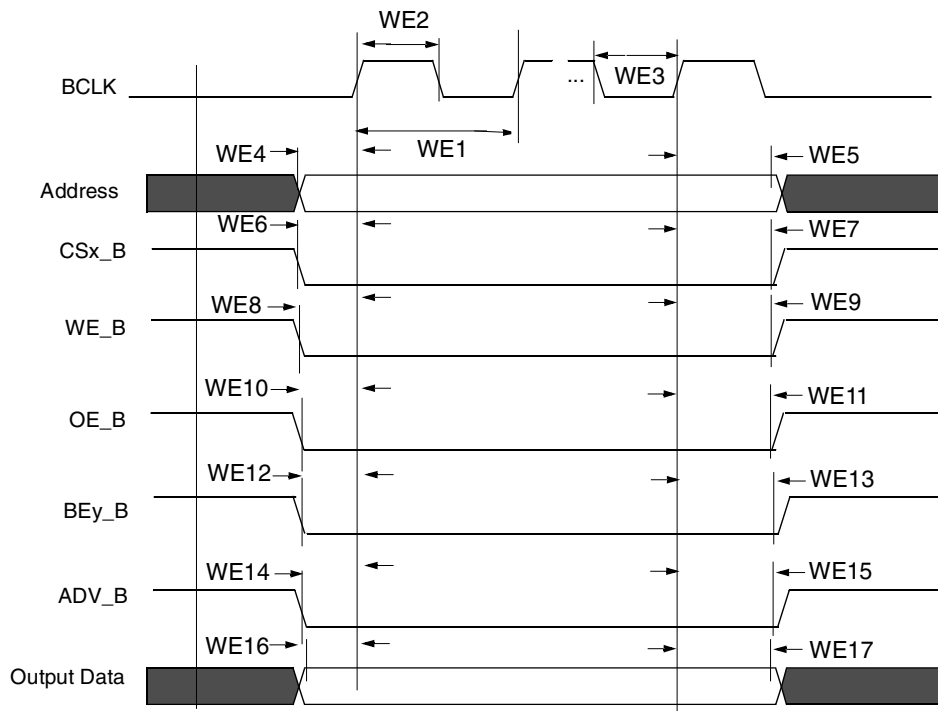


Figure 10. EIM Output Timing Diagram

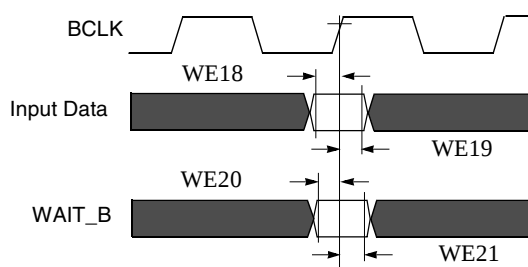


Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 37. EIM Bus Timing Parameters

ID	Parameter	Min ¹	Max ¹	Unit
WE1	BCLK cycle time ²	$t^*(k+1)$	—	ns
WE2	BCLK high level width	$0.4 * t^*(k+1)$	—	ns

Table 37. EIM Bus Timing Parameters (continued)

WE3	BCLK low level width	$0.4 \cdot t \cdot (k+1)$	—	ns
WE4	Clock rise to address valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE5	Clock rise to address invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE6	Clock rise to CSx_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE7	Clock rise to CSx_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE8	Clock rise to WE_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE9	Clock rise to WE_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE10	Clock rise to OE_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE11	Clock rise to OE_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE12	Clock rise to BEy_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE13	Clock rise to BEy_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE14	Clock rise to ADV_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE15	Clock rise to ADV_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE16	Clock rise to output data valid	—	$-(k+1) \cdot t/2 + 2.75$	ns
WE17	Clock rise to output data invalid	$(k+1) \cdot t/2 - 1.25$	—	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	WAIT_B setup time to clock rise	2	—	ns
WE21	WAIT_B hold time from clock rise	2	—	ns

¹ k represents BCD value² EIM maximum operating frequency is 93 MHz (t = 10.753 ns)

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

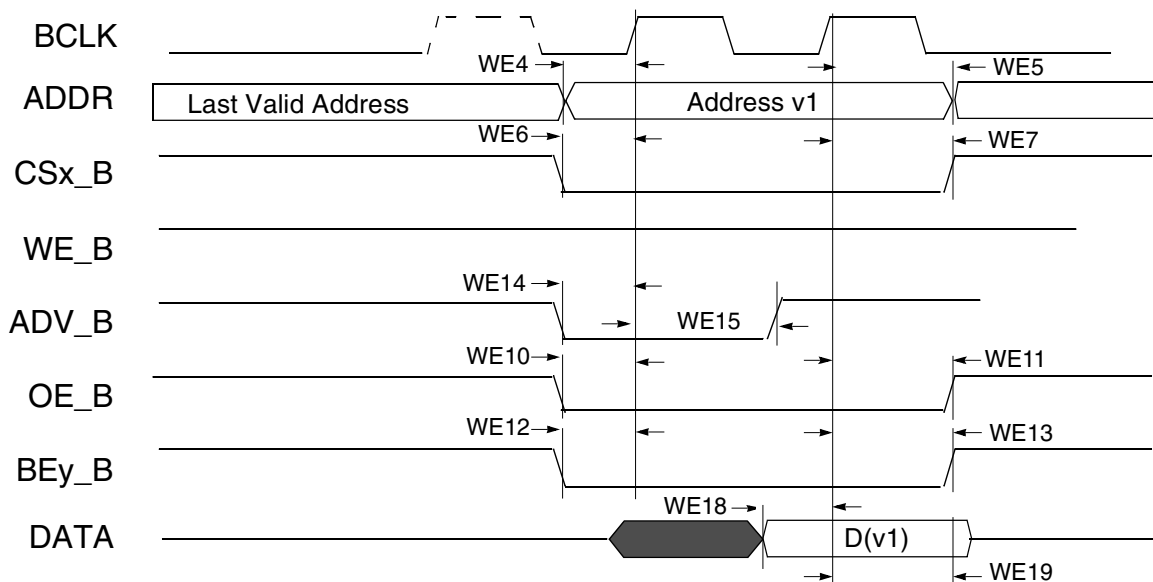


Figure 12. Synchronous Memory Read Access, WSC=1

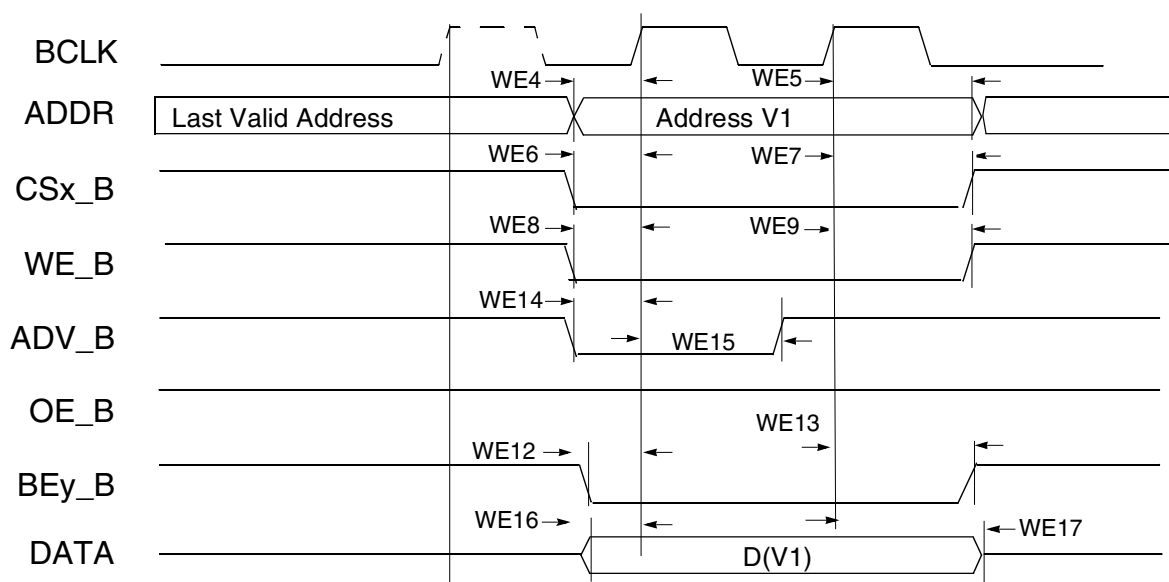


Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

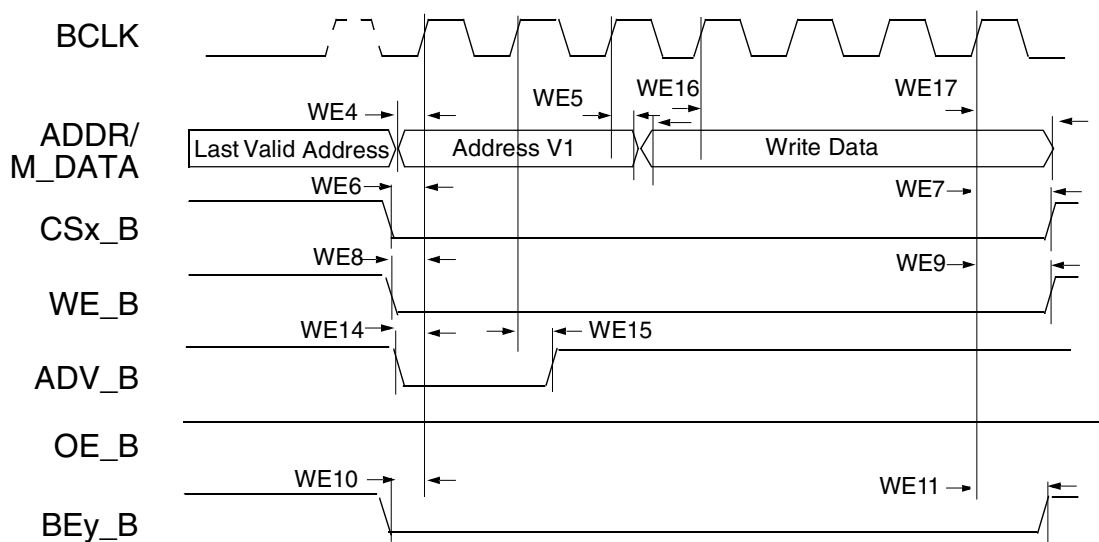


Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

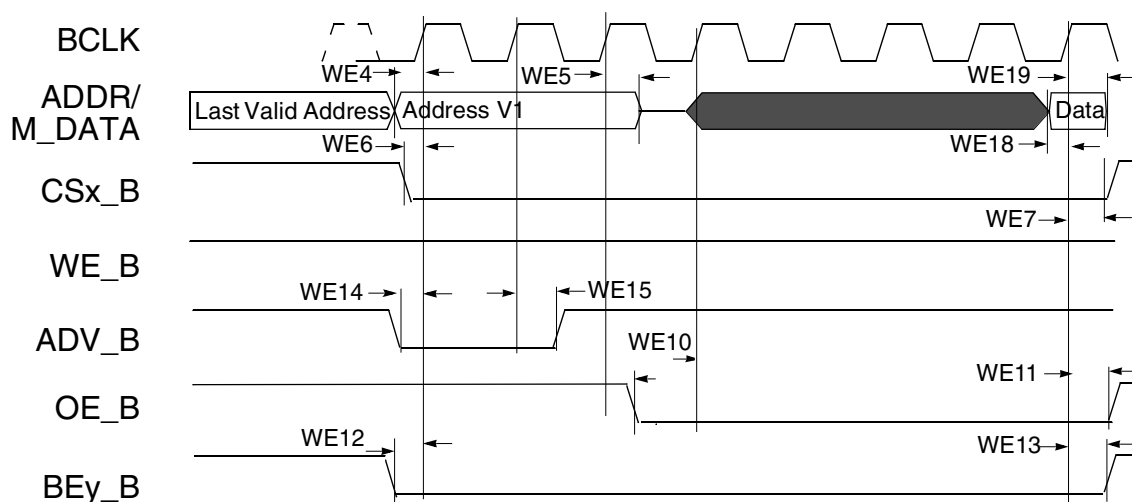


Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20, and Table 38 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6SoloLite reference manual for the EIM programming model.

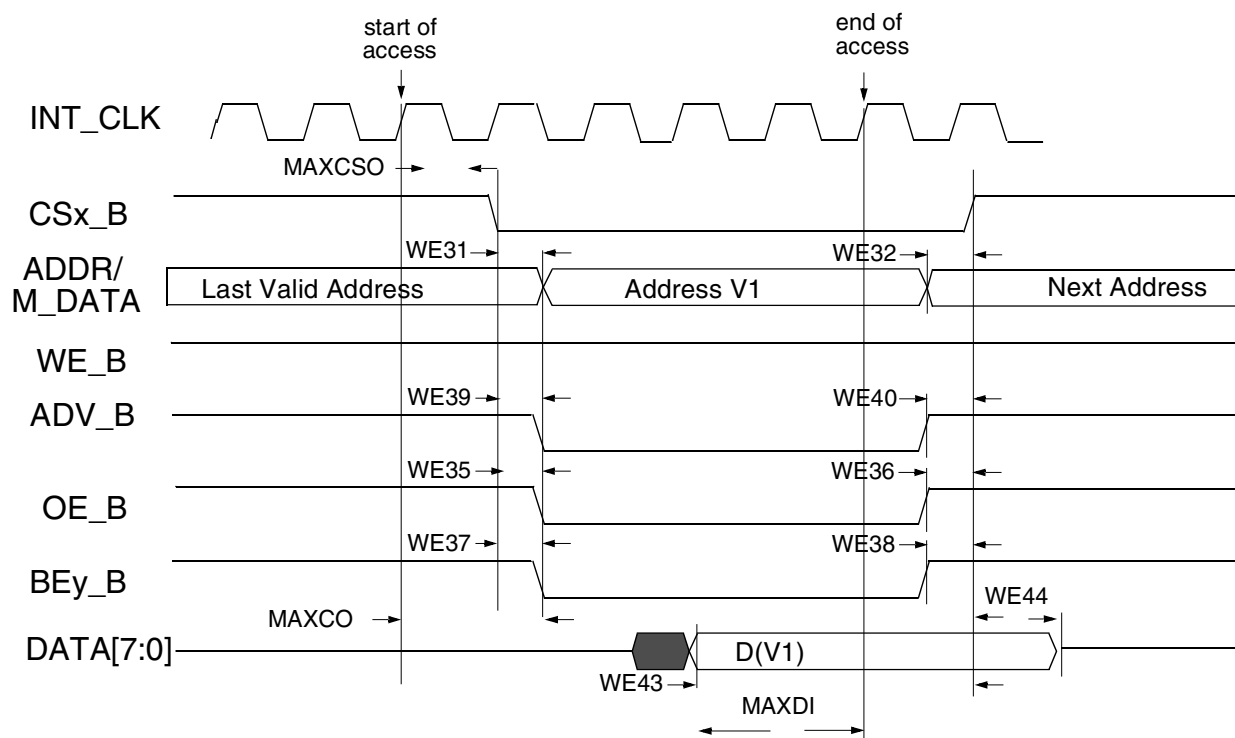


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

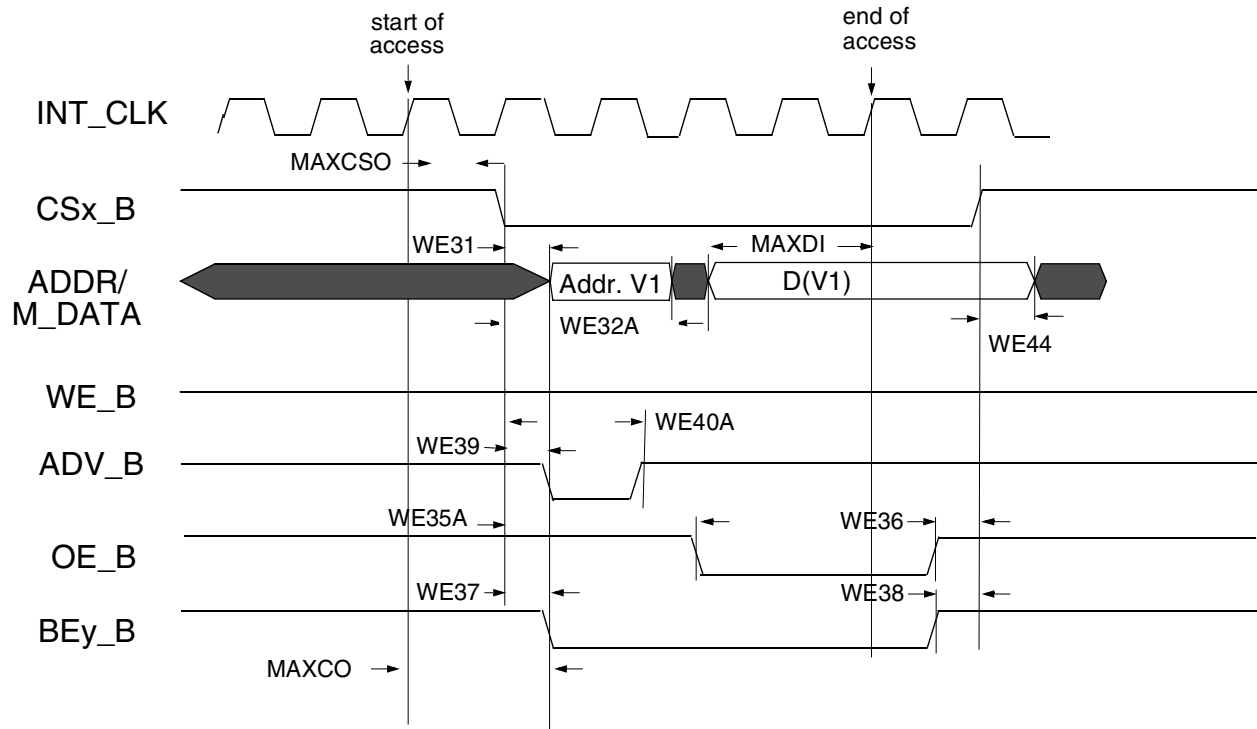


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

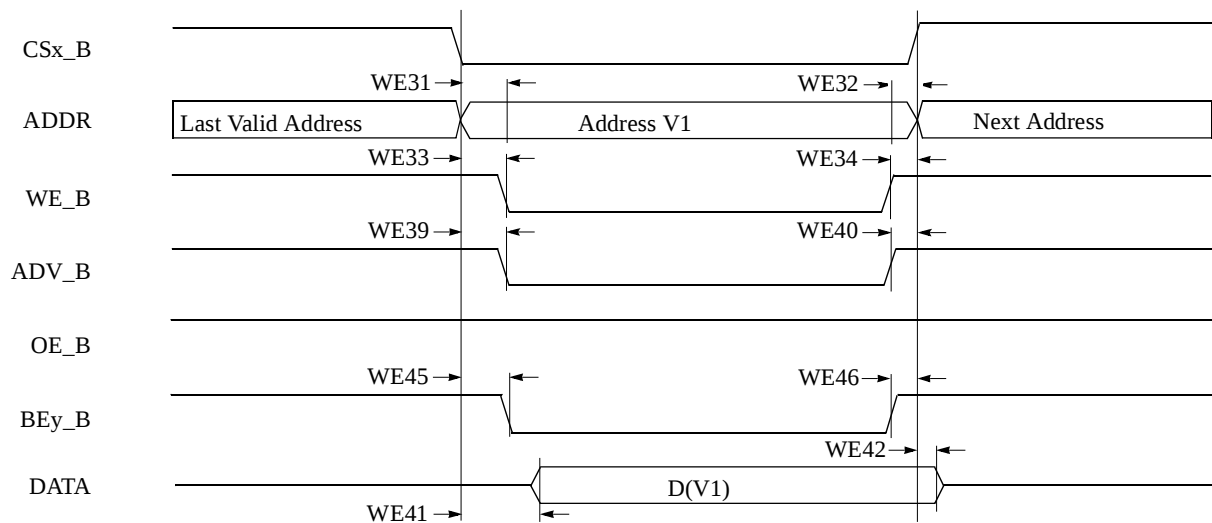
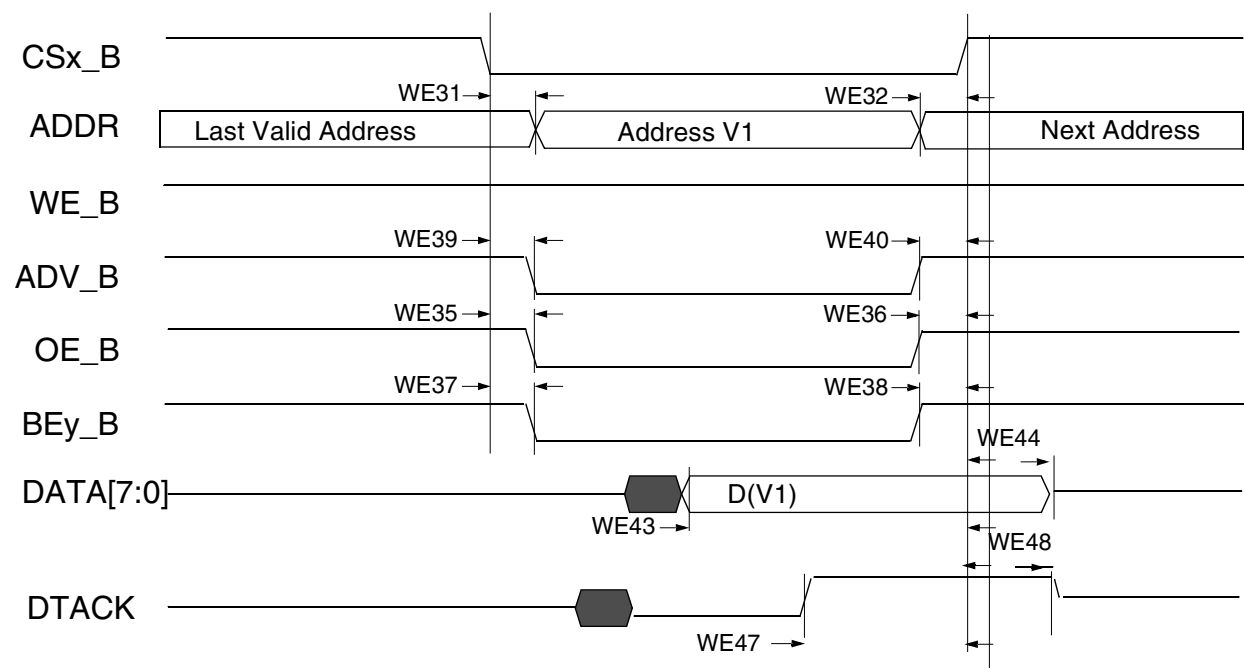
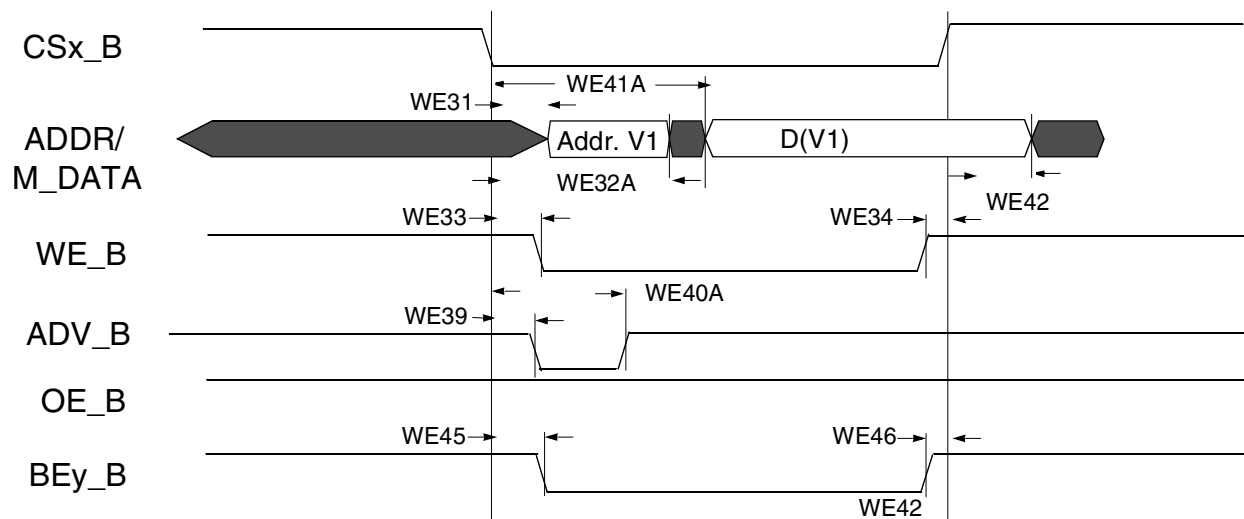


Figure 18. Asynchronous Memory Write Access



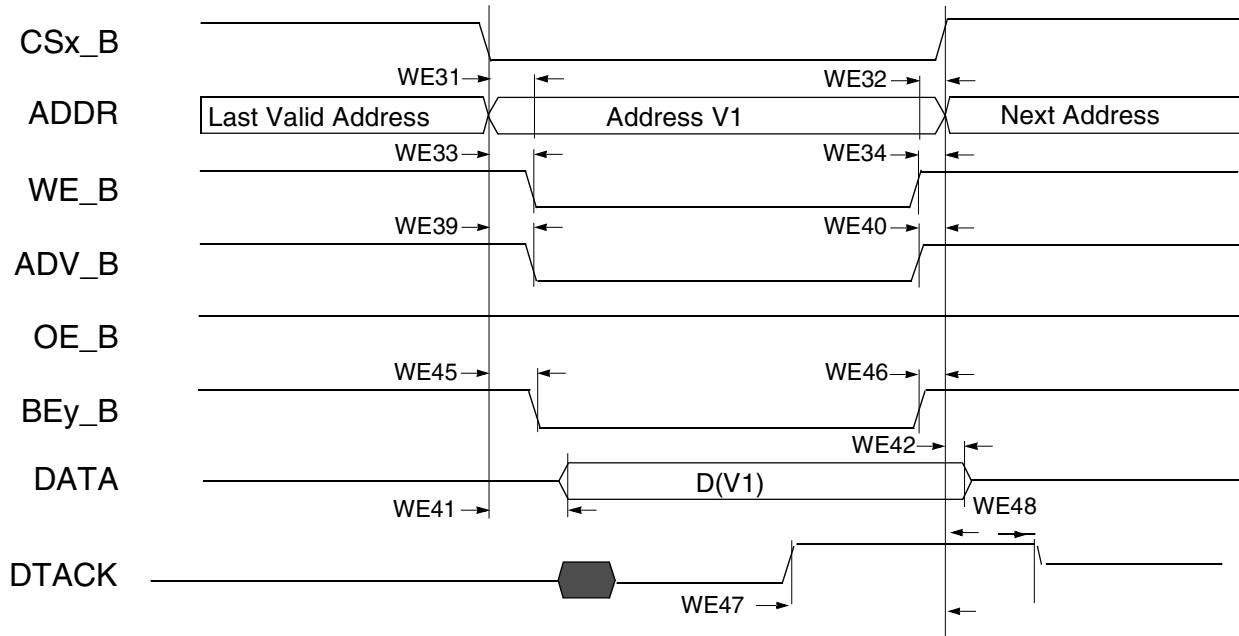


Figure 21. DTACK Write Access (DAP=0)

Table 38. EIM Asynchronous Timing Parameters Table Relative Chip Select

Reference Number	Parameter	Determination by Synchronous measured parameters ¹	Min	Max	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA ²	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN ³	—	3 - CSN	ns
WE32A(mixed A/D)	CSx_B valid to Address Invalid	$t^4 + WE4 - WE7 + (ADV_N + ADVA + 1 - CSA^2)$	-3 + (ADV_N + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN - CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	3 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA ⁵ - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	4 - (RBEN ⁶ - CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns

Table 38. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters ¹	Min	Max	Unit
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	$WE14 - WE6 + (ADV_N + ADVA + 1 - CSA)$	$-3 + (ADV_N + ADVA + 1 - CSA)$	$3 + (ADV_N + ADVA + 1 - CSA)$	ns
WE41	CSx_B Valid to Output Data Valid	$WE16 - WE6 - WCSA$	—	$3 - WCSA$	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	$WE16 - WE6 + (WADV_N + WADVA + ADH + 1 - WCSA)$	—	$3 + (WADV_N + WADVA + ADH + 1 - WCSA)$	ns
WE42	Output Data Invalid to CSx_B Invalid	$WE17 - WE7 - CSN$	—	$3 - CSN$	ns
MAXCO	Output maximum delay from internal driving ADDR/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	Data maximum delay from chip input data to its internal FF	6	—	—	ns
WE43	Input Data Valid to CSx_B Invalid	$MAXCO - MAXCSO + MAXDI$	$MAXCO - MAXCSO + MAXDI$	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	$WE12 - WE6 + (WBEA - CSA)$	—	$3 + (WBEA - CSA)$	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	$WE7 - WE13 + (WBEN - CSN)$	—	$-3 + (WBEN - CSN)$	ns
MAXDTI	DTACK maximum delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	ns
WE47	Dtack Active to CSx_B Invalid	$MAXCO - MAXCSO + MAXDTI$	$MAXCO - MAXCSO + MAXDTI$	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

² CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

³ CS Negation. This bit field determines when CS signal is negated during read/write cycles.

⁴ t is axi_clk cycle time.

⁵ BE Assertion. This bit field determines when BE signal is asserted during read cycles.

⁶ BE Negation. This bit field determines when BE signal is negated during read cycles.

4.9.4 DDR SDRAM Specific Parameters (DDR3 and LPDDR2)

4.9.4.1 DDR3 Parameters

Figure 22 shows the DDR3 basic timing diagram. The timing parameters for this diagram appear in Table 39.

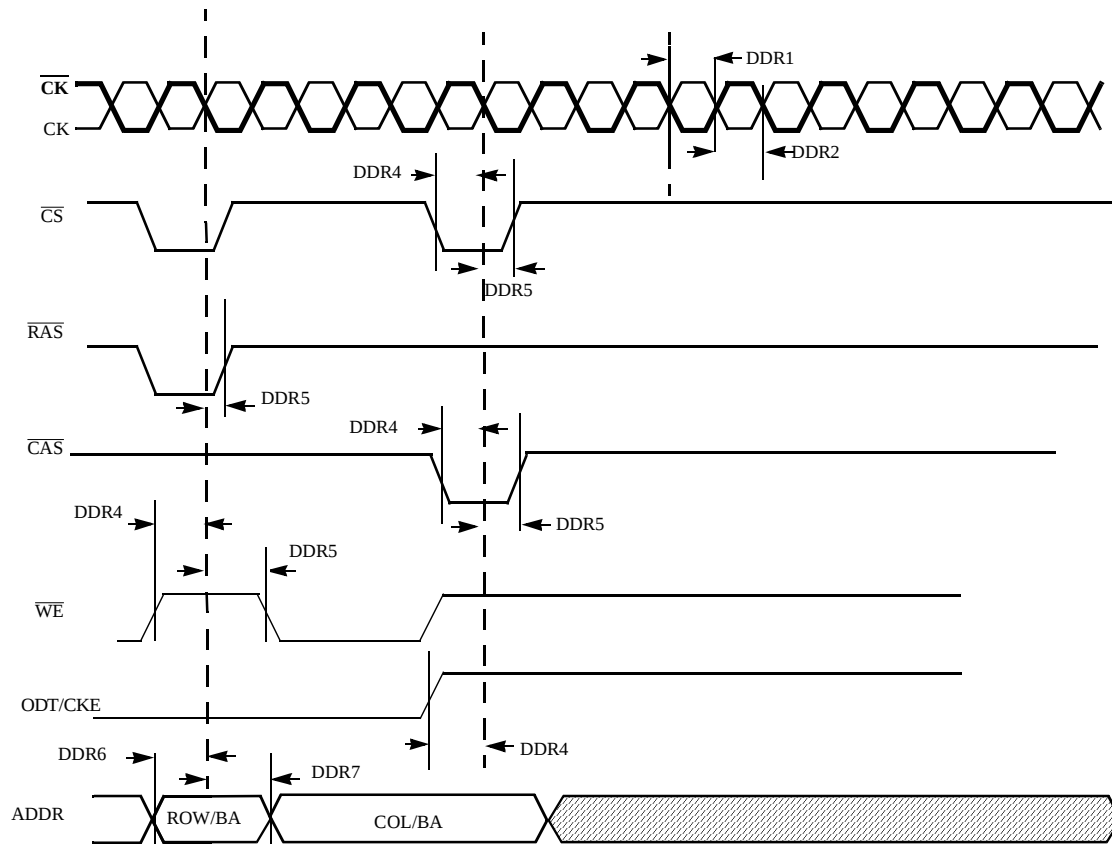


Figure 22. DDR3 Command and Address Timing Diagram

Table 39. DDR3 Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tck
DDR2	CK clock low-level width	tCL	0.47	0.53	tck
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	580	—	ps

Table 39. DDR3 Timing Parameter Table (continued)

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR6	Address output setup time	tIS	800	—	ps
DDR7	Address output hold time	tIH	580	—	ps

¹ All measurements are in reference to Vref level.

² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 23 shows the DDR3 write timing diagram. The timing parameters for this diagram appear in Table 40.

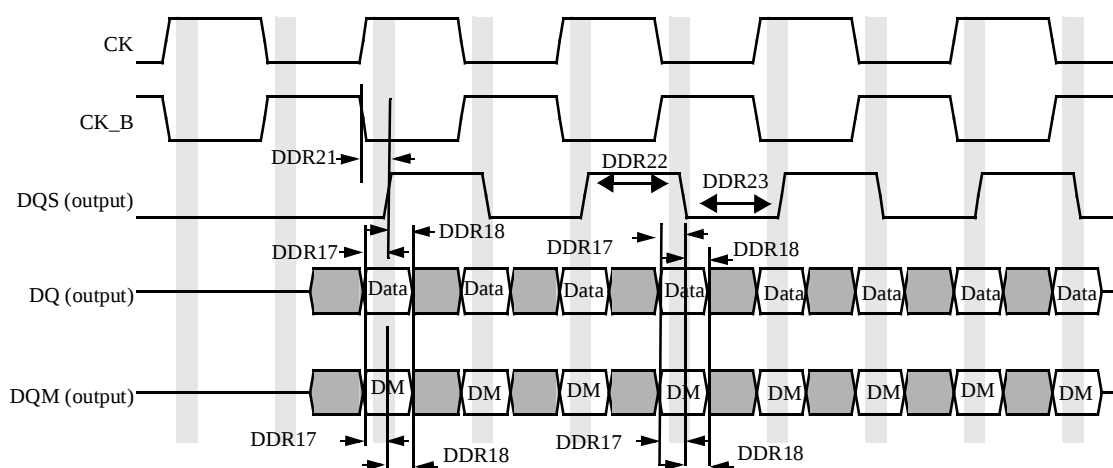


Figure 23. DDR3 Write Cycle

Table 40. DDR3 Write Cycle

ID	Parameter	Symbol	CK = 400MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR23	DQS low level width	tDQSL	0.45	0.55	tCK

¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to Vref level.

³ Measurements were taken using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 24 shows the DDR3 read timing diagram. The timing parameters for this diagram appear in Table 41.

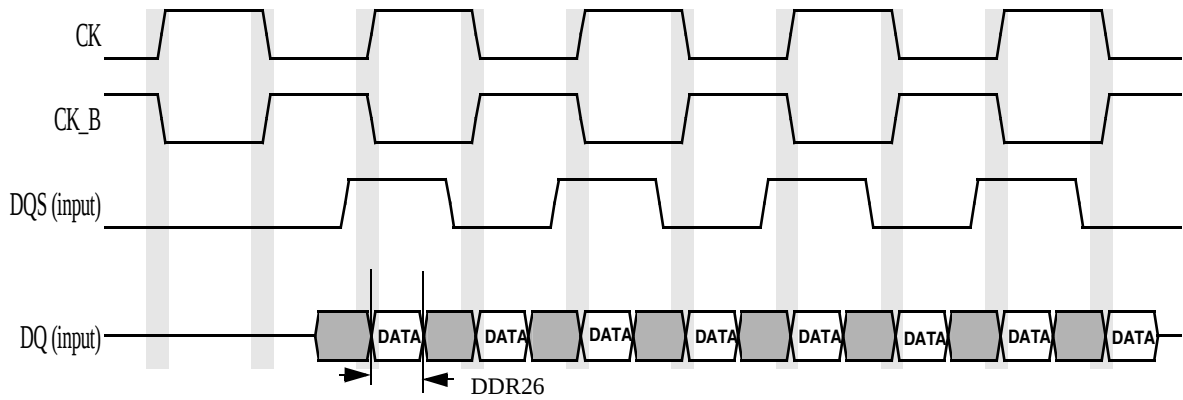


Figure 24. DDR3 Read Cycle

Table 41. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	—	450	—	ps

- ¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.
- ² All measurements are in reference to Vref level.
- ³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 42.

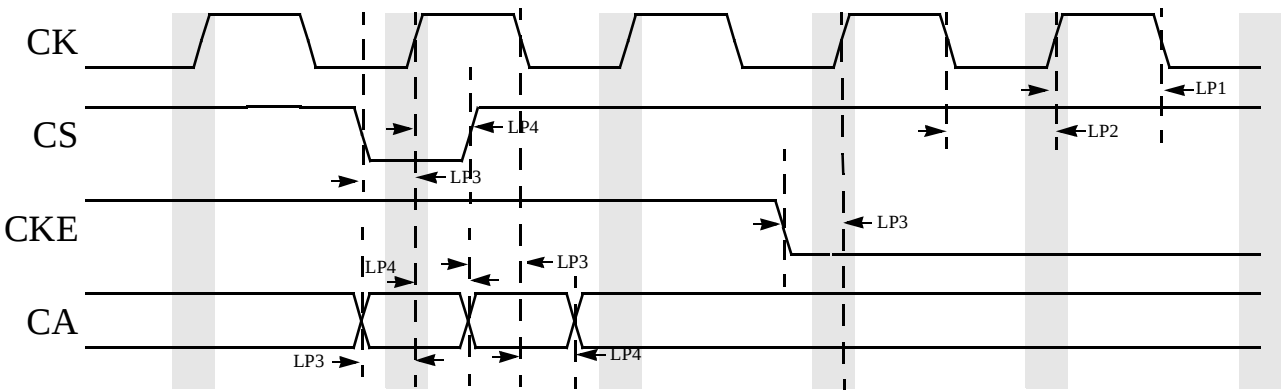


Figure 25. LPDDR2 Command and Address Timing Diagram

Table 42. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tck
LP2	SDRAM clock low-level width	tCL	0.45	0.55	tck
LP3	CS, CKE setup time	tIS	380	—	ps
LP4	CS, CKE hold time	tIH	380	—	ps
LP3	CA setup time	tIS	770	—	ps
LP4	CA hold time	tIH	770	—	ps

¹ All measurements are in reference to Vref level.
² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 26 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 43.

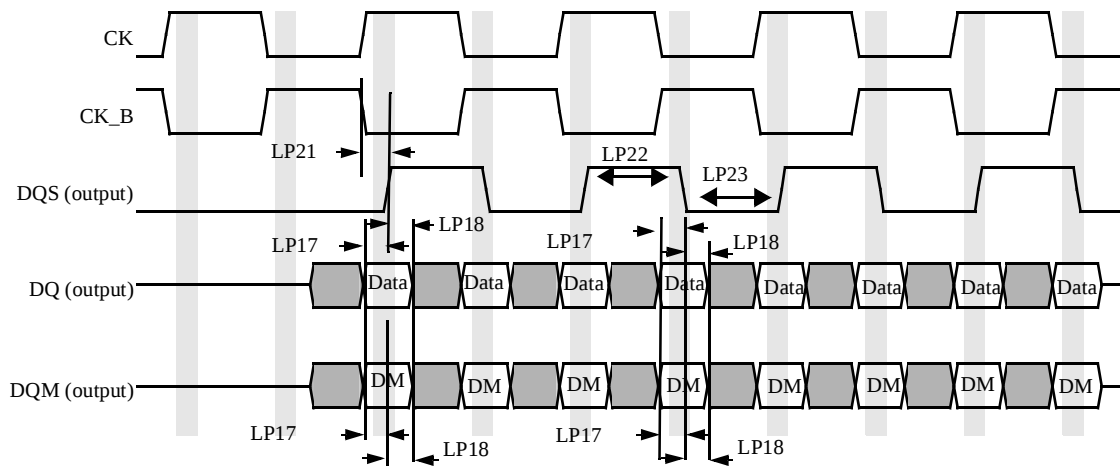


Figure 26. LPDDR2 Write Cycle

Table 43. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	t _{DS}	375	—	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	t _{DH}	375	—	ps
LP21	DQS latching rising transitions to associated clock edges	t _{DQSS}	-0.25	+0.25	tCK
LP22	DQS high level width	t _{DQSH}	0.4	-	tCK
LP23	DQS low level width	t _{DQSL}	0.4	-	tCK

¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to V_{ref} level.

³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 27 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 44.

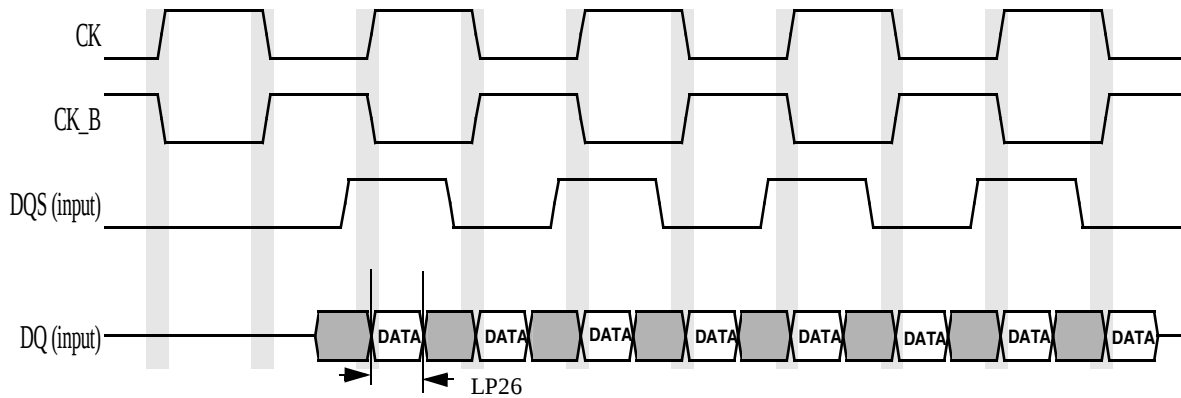


Figure 27. LPDDR2 Read Cycle

Table 44. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	270	—	ps

- ¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.
- ² All measurements are in reference to Vref level.
- ³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.10.2 CMOS Sensor Interface (CSI) Timing Parameters

4.10.2.0.1 Gated Clock Mode Timing

Figure 28 and Figure 29 shows the gated clock mode timings for CSI, and Table 45 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

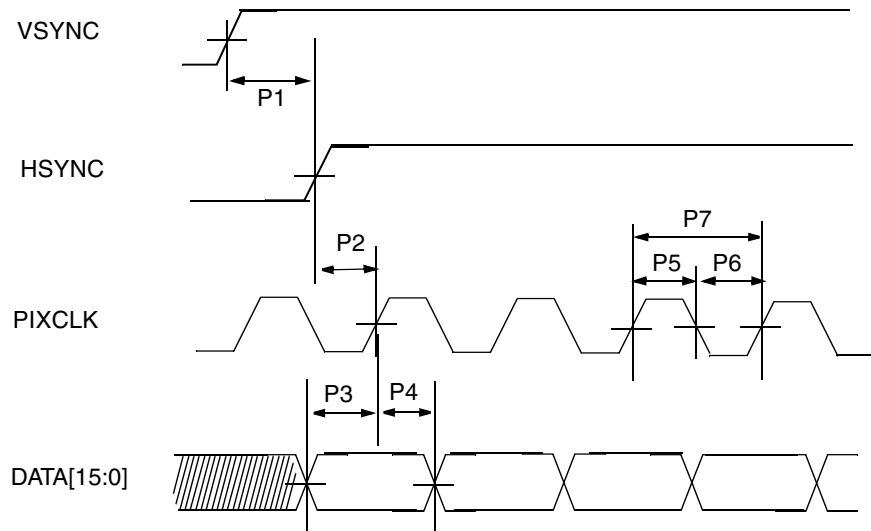


Figure 28. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

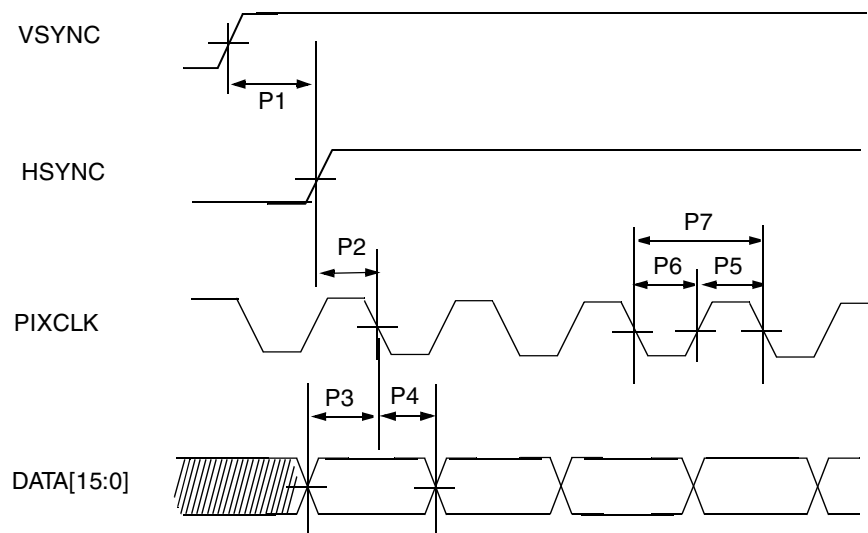


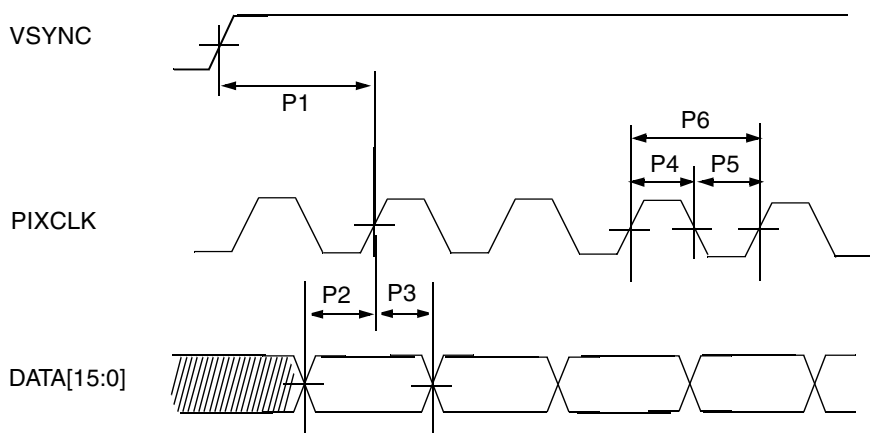
Figure 29. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to HSYNC time	tV2H	67.5	—	ns
P2	CSI HSYNC setup time	tHsu	2	—	ns
P3	CSI DATA setup time	tDsu	2.5	—	ns
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	10	—	ns
P6	CSI pixel clock low time	tCLKl	10	—	ns
P7	CSI pixel clock frequency	fCLK	—	66 ± 10%	MHz

4.10.2.0.2 Ungated Clock Mode Timing

Figure 30 shows the ungated clock mode timings of CSI, and Table 46 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the VSYNC and PIXCLK signals are used, and the HSYNC signal is ignored.

**Figure 30. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge****Table 46. CSI Ungated Clock Mode Timing Parameters**

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	2.5	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	10	—	ns
P5	CSI pixel clock low time	tCLKl	10	—	ns
P6	CSI pixel clock frequency	fCLK	—	66 ± 10%	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync(HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.10.3 ECSPi Timing Parameters

This section describes the timing parameters of the ECSPi block. The ECSPi has separate timing parameters for master and slave modes.

4.10.3.1 ECSPi Master Mode Timing

Figure 31 depicts the timing of ECSPi in master mode and Table 47 lists the ECSPi master mode timing characteristics.

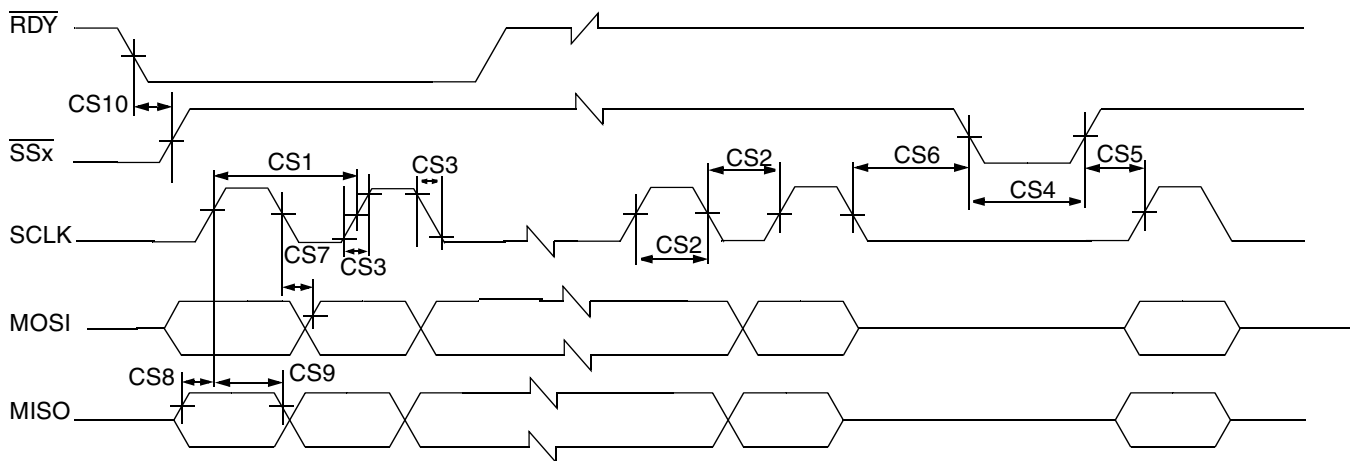


Figure 31. ECSPi Master Mode Timing Diagram

Table 47. ECSPi Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read	t_{clk}	46	—	ns
	• Slow group ¹		40		
	• Fast group ²		15		
CS2	SCLK Cycle Time–Write	t_{sw}	22	—	ns
	• Slow group ¹		20		
	• Fast group ²		7		
	SCLK High or Low Time–Read				
	• Slow group ¹				
	• Fast group ²				
	SCLK High or Low Time–Write				

Table 47. ECSPi Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS3	SCLK Rise or Fall ³	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 3	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period	—	ns
CS7	MOSI Propagation Delay ($C_{LOAD} = 20$ pF)	t_{PDmosi}	-0.5	2	ns
CS8	MISO Setup Time	t_{Smiso}	8.5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time ⁴	t_{SDRY}	5	—	ns

¹ ECSPi slow include:

ECSPi2/EPDC_SDLE, ECSPi3/EPDC_D9, ECSPi4/EPDC_D1

² ECSPi fast include:

ECSPi1/LCD_DAT1, ECSPi1/ECSPi1_MISO, ECSPi2/LCD_DAT10, ECSPi2/ECSPi2_MISO, ECSPi3/AUD_TXC,
ECSPi3/SD2_DAT1, ECSPi4/KEY_ROW1, ECSPi4/FEC_CRS_DV

³ See specific I/O AC parameters [Section 4.7, "I/O AC Parameters."](#)

⁴ SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.10.3.2 ECSPi Slave Mode Timing

Figure 32 depicts the timing of ECSPi in slave mode and Table 48 lists the ECSPi slave mode timing characteristics.

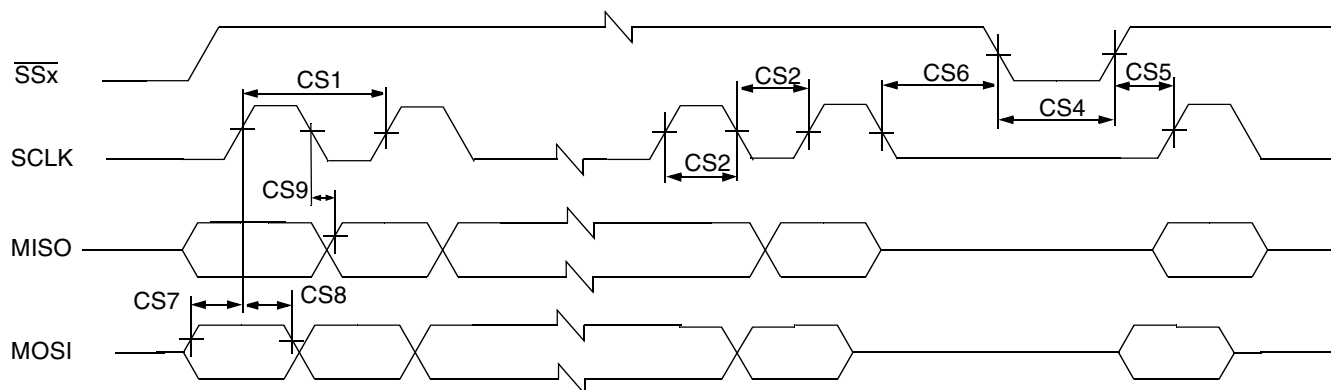


Figure 32. ECSPi Slave Mode Timing Diagram

Table 48. ECSPi Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time—Read SCLK Cycle Time—Write	t_{clk}	40 15	—	ns
CS2	SCLK High or Low Time—Read SCLK High or Low Time—Write	t_{SW}	20 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay ($C_{LOAD} = 20$ pF)	t_{PDmiso}	4	17	ns

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Data Rate) timing.

4.10.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 33 depicts the timing of SD/eMMC4.3, and Table 49 lists the SD/eMMC4.3 timing characteristics.

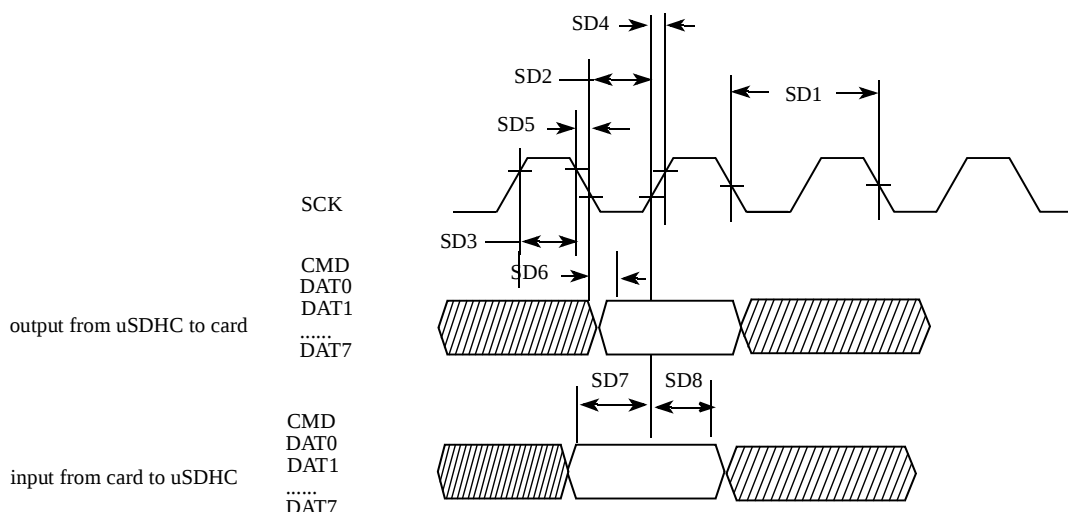


Figure 33. SD/eMMC4.3 Timing

Table 49. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}^1	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}^2	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}^3	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	-6.6	3.6	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					

Table 49. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time ⁴	t_{IH}	5.6	—	ns

¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

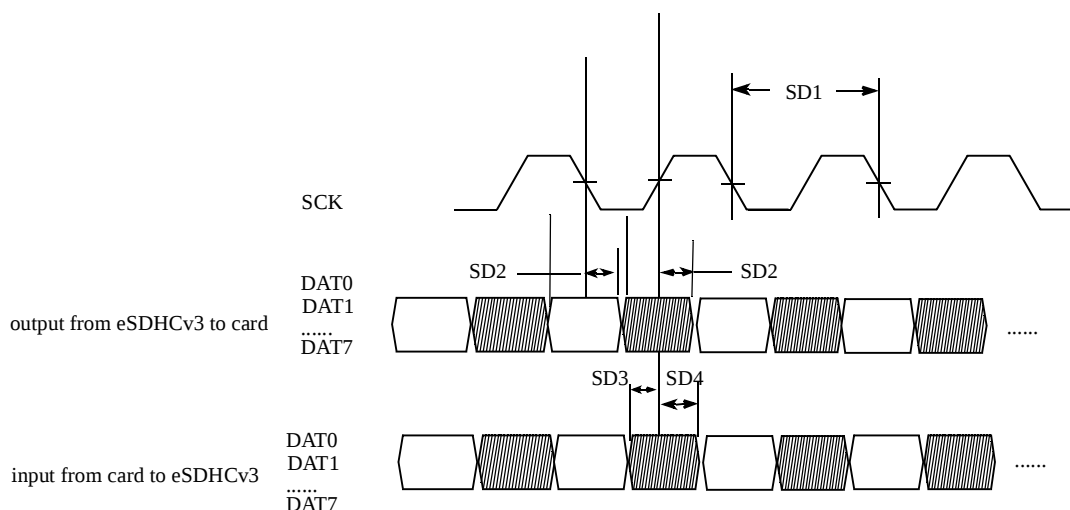
² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 34 depicts the timing of eMMC4.4. Table 50 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

**Figure 34. eMMC4.4 Timing****Table 50. eMMC4.4 Interface Timing Specification**

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					

Table 50. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.10.4.3 SDR50/SDR104 AC Timing

Figure 35 depicts the timing of SDR50/SDR104, and Table 49 lists the SDR50/SDR104 timing characteristics.

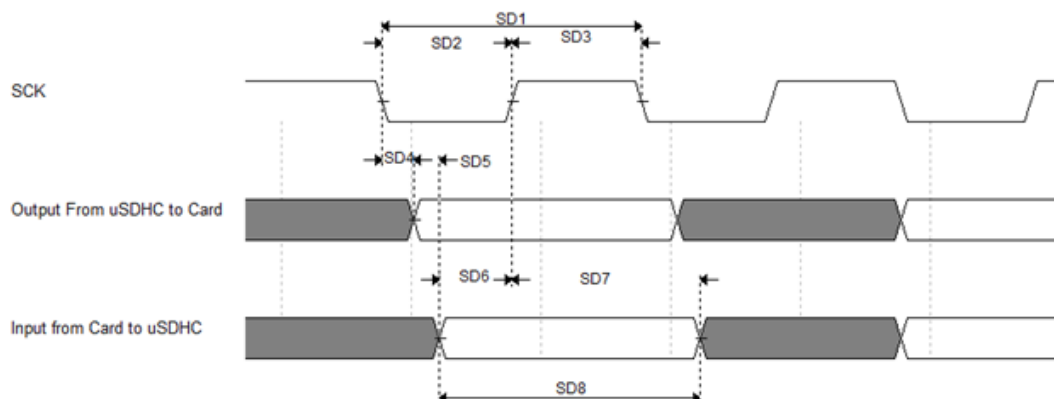


Figure 35. SDR50/SDR104 Timing

Table 51. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
uSDHC Output/Card Inputs CMD, DAT in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs CMD, DAT in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay ¹	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs CMD, DAT in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

Table 51. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK) ²					
SD8	Card Output Data Window	t_{ODW}	$0.5 \cdot t_{CLK}$	—	ns

¹ If using KEY_COL1, KEY_ROW1, KEY_COL2 and KEY_ROW2 for USDHC3_DAT4 - USDHC3_DAT7, please note that the timing is different. t_{od} min is -1.1 and t_{od} max is 1.5

²Data window in SDR100 mode is variable.

4.10.5 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the MII pins), for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see the i.MX 6SoloLite Reference Manual.

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.10.5.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 52 lists the MII receive channel signal timing parameters and Figure 36 shows MII receive signal timings.

Table 52. MII Receive Signal Timing

No.	Characteristics ^{1 2}	Min	Max	Unit
M1	FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

¹ FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

² Test conditions: 25pF on each output signal.

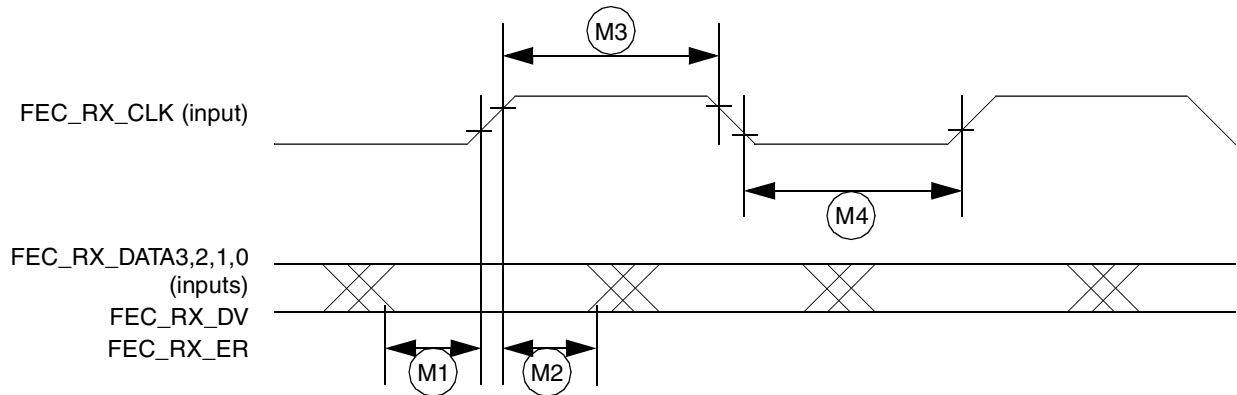


Figure 36. MII Receive Signal Timing Diagram

4.10.5.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Table 53 lists MII transmit channel timing parameters. Figure 37 shows MII transmit signal timing diagram for the values listed in Table 53.

Table 53. MII Transmit Signal Timing

Num	Characteristic ^{1 2}	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TX_DATA3,2,1,0, FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

¹ FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

² Test conditions: 25pF on each output signal.

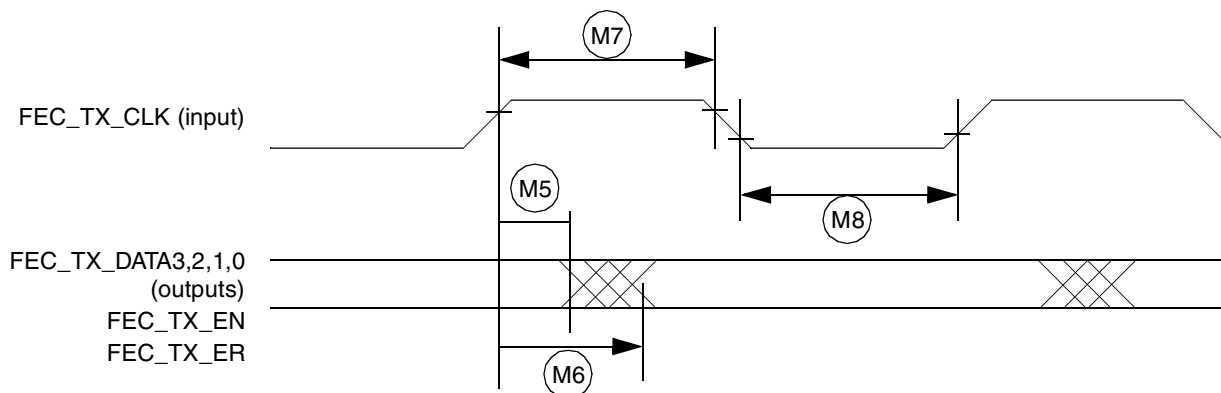


Figure 37. MII Transmit Signal Timing Diagram

4.10.5.3 MII Async Inputs Signal Timing (FEC_CRSS and FEC_COL)

Table 54 lists MII asynchronous inputs signal timing information. Figure 38 shows MII asynchronous input timings listed in Table 54.

Table 54. MII Async Inputs Signal Timing

Num	Characteristic ¹	Min	Max	Unit
M9 ²	FEC_CRSS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

¹ Test conditions: 25pF on each output signal.

² FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

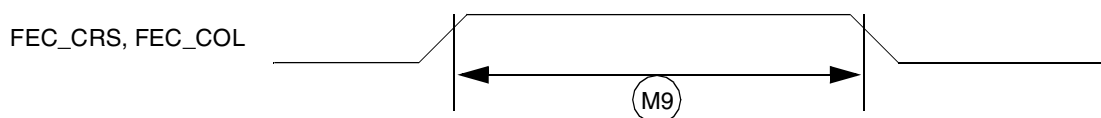


Figure 38. MII Async Inputs Timing Diagram

4.10.5.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 55 lists MII serial management channel timings. Figure 39 shows MII serial management channel timings listed in Table 55. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However, the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 55. MII Transmit Signal Timing

ID	Characteristics ¹	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns

Table 55. MII Transmit Signal Timing (continued)

ID	Characteristics ¹	Min	Max	Unit
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40 %	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40 %	60%	FEC_MDC period

¹ Test conditions: 25pF on each output signal.

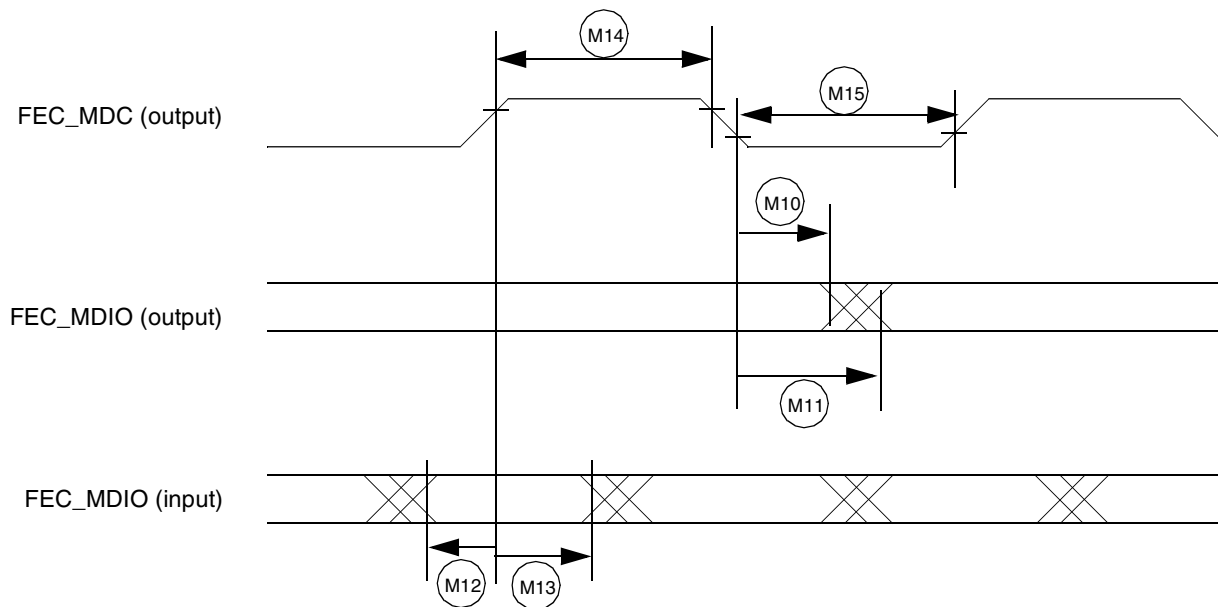


Figure 39. MII Serial Management Channel Timing Diagram

4.10.5.5 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz $\pm$ 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and optional FEC_RX_ER.

The RMII mode timings are shown in Table 56 and Figure 40.

Table 56. RMII Signal Timing

No.	Characteristics ¹	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	16	ns

Table 56. RMII Signal Timing (continued)

No.	Characteristics ¹	Min	Max	Unit
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

¹ Test conditions: 25pF on each output signal.

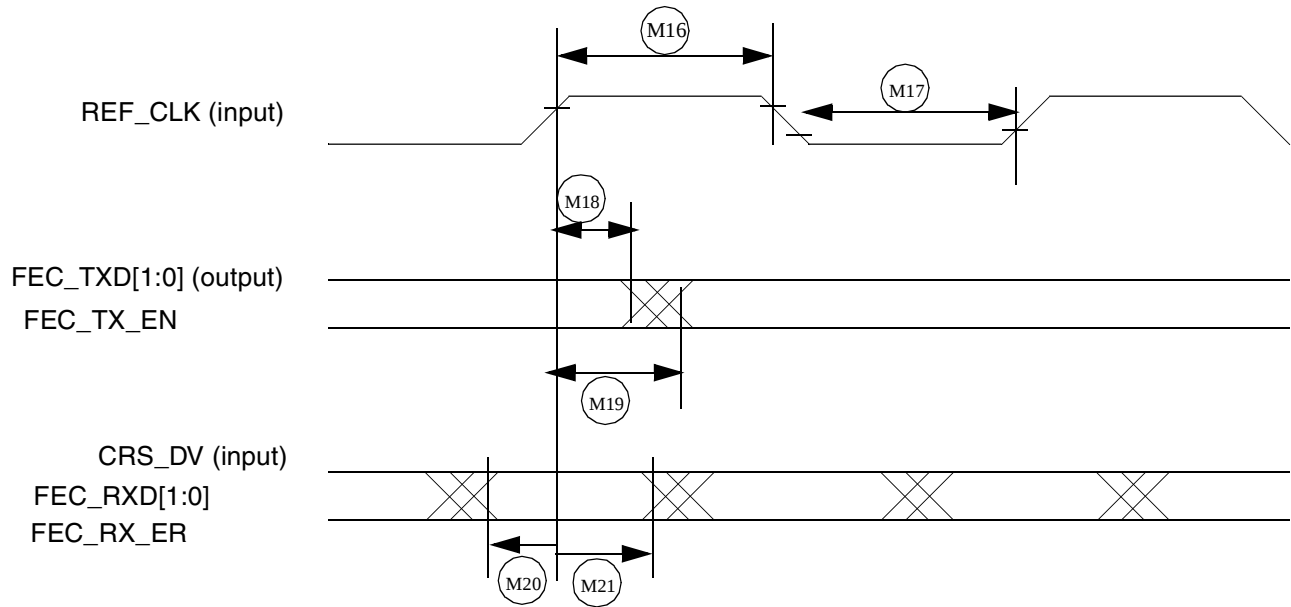


Figure 40. RMII Mode Signal Timing Diagram

4.10.6 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 41 depicts the timing of I²C module, and Table 57 lists the I²C module timing characteristics.

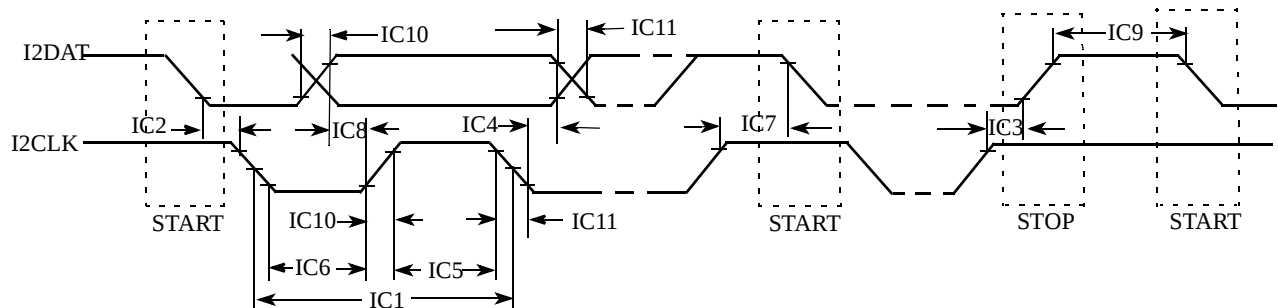
Figure 41. I²C Bus Timing

Table 57. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
IC8	Data set-up time	250	—	100 ³	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	20 + 0.1C _b ⁴	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	20 + 0.1C _b ⁴	300	ns
IC12	Capacitive load for each bus line (C _b)	—	400	—	400	pF

¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

³ A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line
 $\text{max_rise_time (IC9)} + \text{data_setup_time (IC7)} = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

⁴ C_b = total capacitance of one bus line in pF.

4.10.7 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 42 depicts the timing of the PWM, and Table 58 lists the PWM timing parameters.

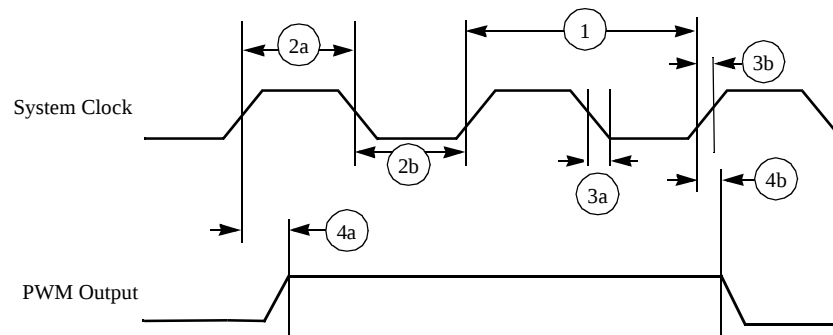


Figure 42. PWM Timing

Table 58. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency ¹	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

¹ CL of PWMO = 30 pF

4.10.8 SCAN JTAG Controller (SJC) Timing Parameters

Figure 43 depicts the SJC test clock input timing. Figure 44 depicts the SJC boundary scan timing. Figure 45 depicts the SJC test access port. Signal parameters are listed in Table 59.

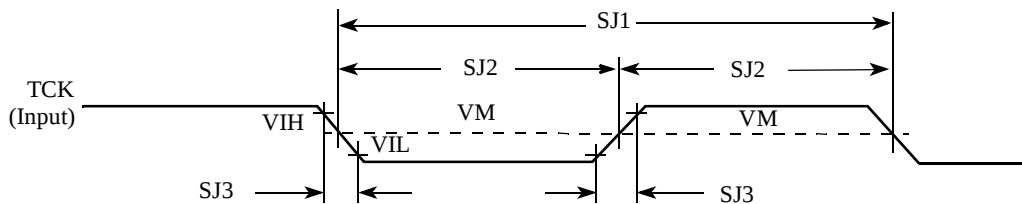


Figure 43. Test Clock Input Timing Diagram

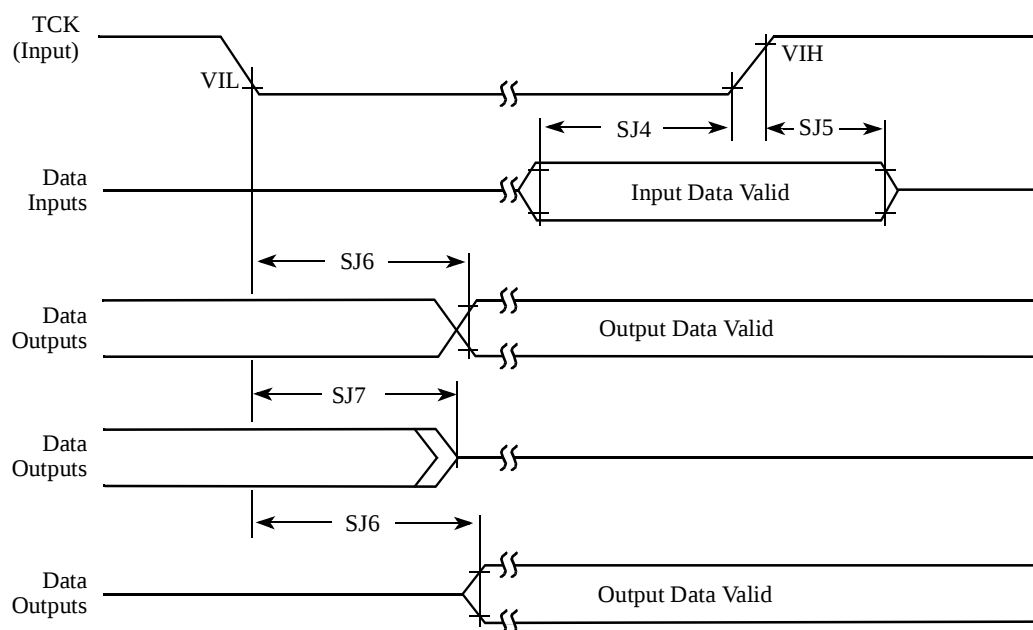


Figure 44. Boundary Scan (JTAG) Timing Diagram

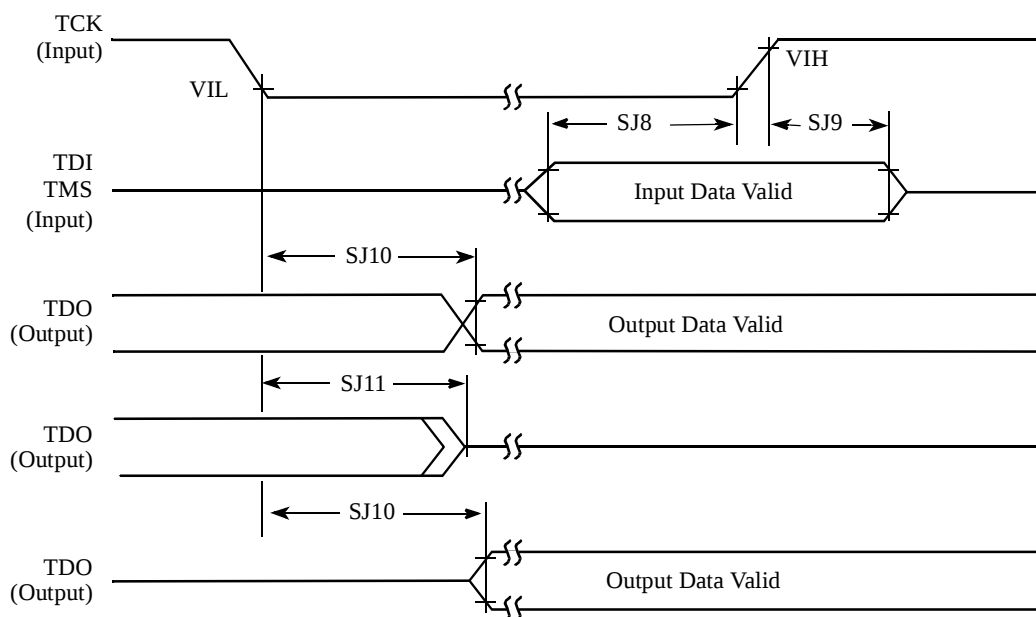


Figure 45. Test Access Port Timing Diagram

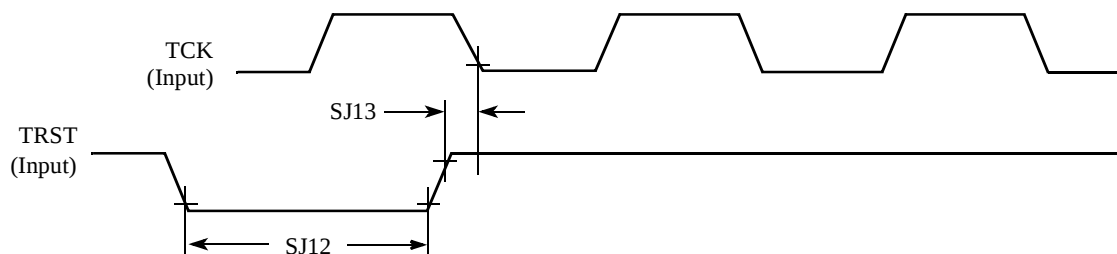
Figure 46. $\overline{\text{TRST}}$ Timing Diagram

Table 59. JTAG Timing

ID	Parameter ^{1,2}	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \cdot T_{DC})^1$	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M^2	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

¹ T_{DC} = target frequency of SJC² V_M = mid-point voltage

4.10.9 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 60 and Figure 47 and Figure 48 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 60. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf)	—	—	1.5	ns
• Skew	—	—	24.2	ns
• Transition rising	—	—	31.3	ns
• Transition falling	—	—	31.3	ns
SPDIFOUT1 output (Load = 30pf)	—	—	1.5	ns
• Skew	—	—	13.6	ns
• Transition rising	—	—	18.0	ns
• Transition falling	—	—	18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stckpl	16.0	—	ns

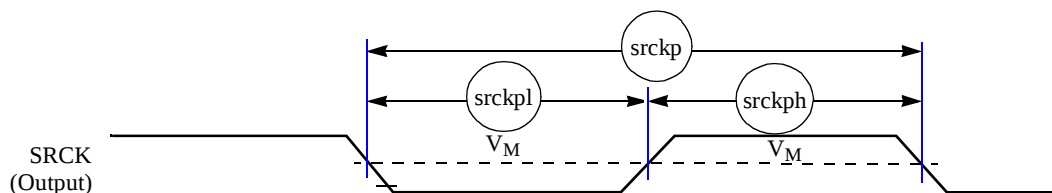


Figure 47. SRCK Timing Diagram

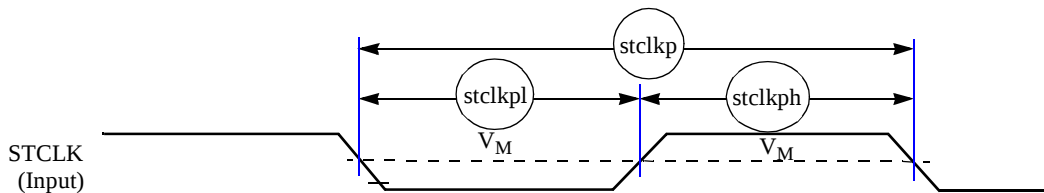


Figure 48. STCLK Timing Diagram

4.10.10 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 61](#).

Table 61. AUDMUX Port Allocation

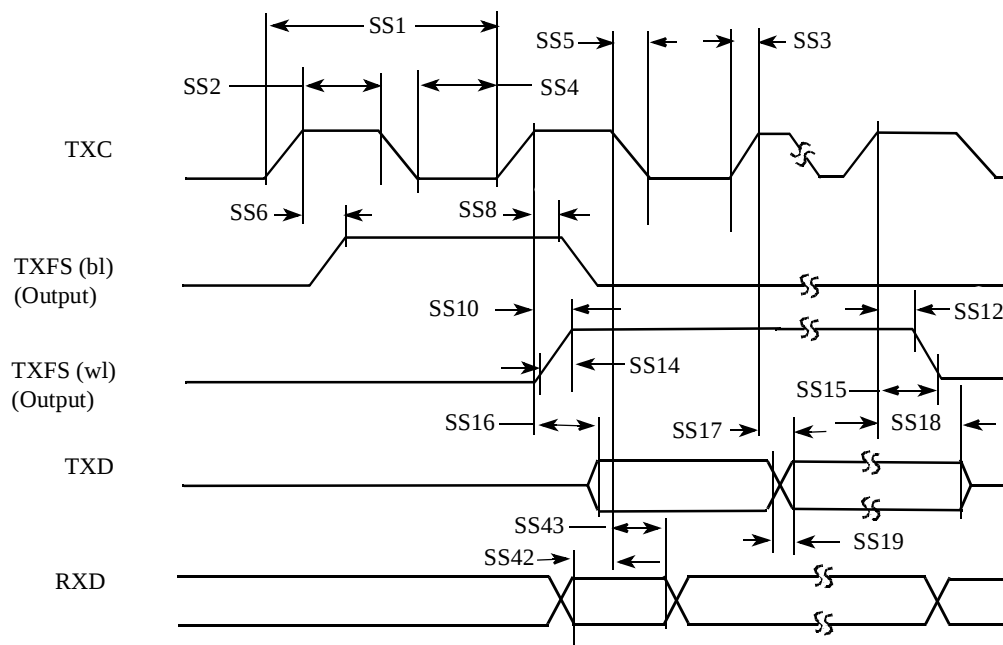
Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – I2C2 and LCD or ECSP11 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EPDC or SD3 I/O through IOMUXC
AUDMUX port 6	AUD6	External – FEC or KEY_ROW and KEY_COL through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX 6SoloLite reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.10.10.1 SSI Transmitter Timing with Internal Clock

Figure 49 depicts the SSI transmitter internal clock timing and Table 62 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 49. SSI Transmitter Internal Clock Timing Diagram

Table 62. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

Table 62. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.10.2 SSI Receiver Timing with Internal Clock

Figure 50 depicts the SSI receiver internal clock timing and Table 63 lists the timing parameters for the receiver timing with the internal clock.

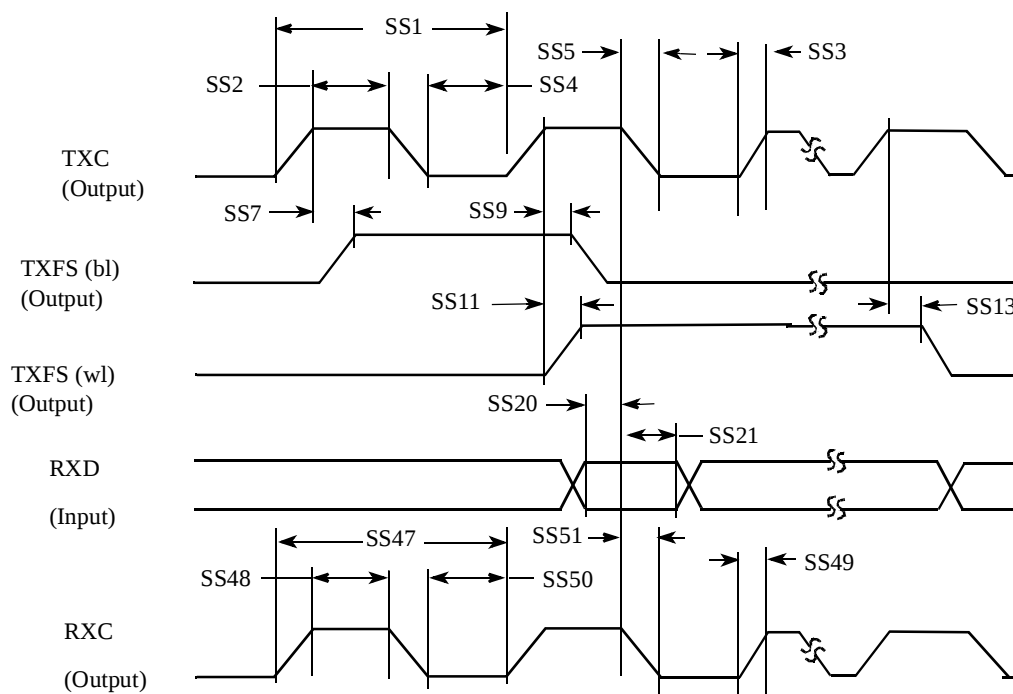


Figure 50. SSI Receiver Internal Clock Timing Diagram

Table 63. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 63. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.10.3 SSI Transmitter Timing with External Clock

Figure 51 depicts the SSI transmitter external clock timing and Table 64 lists the timing parameters for the transmitter timing with the external clock.

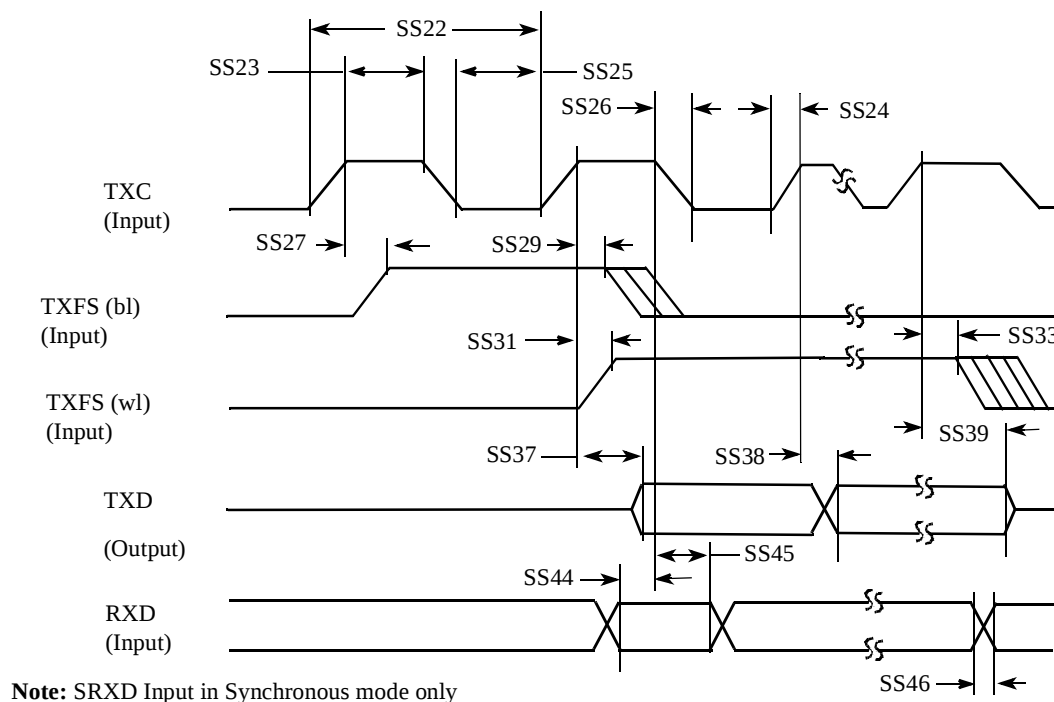


Figure 51. SSI Transmitter External Clock Timing Diagram

Table 64. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 64. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFISI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.10.4 SSI Receiver Timing with External Clock

Figure 52 depicts the SSI receiver external clock timing and Table 65 lists the timing parameters for the receiver timing with the external clock.

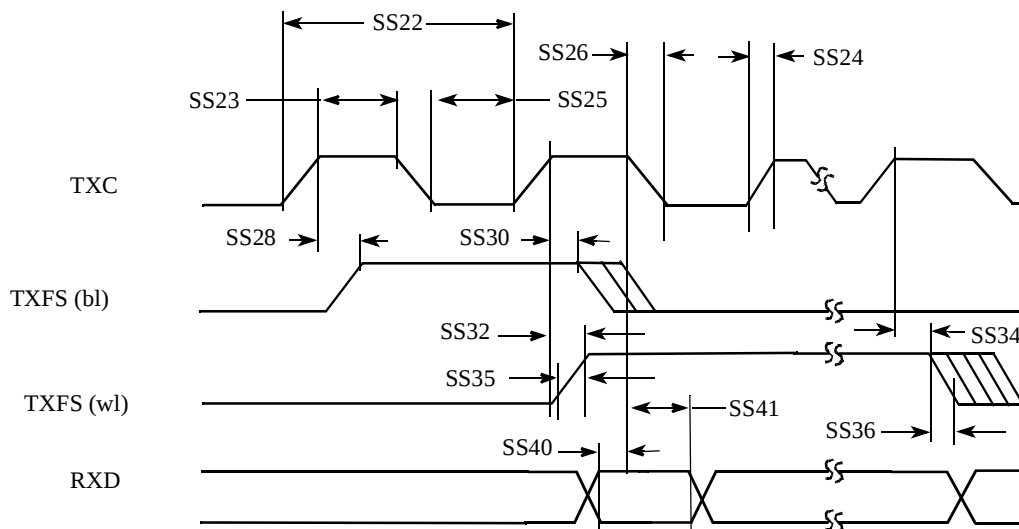


Figure 52. SSI Receiver External Clock Timing Diagram

Table 65. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	-10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.11 UART I/O Configuration and Timing Parameters

4.10.11.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SoloLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 66 shows the UART I/O configuration based on the enabled mode.

Table 66. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.11.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.10.11.2.1 UART Transmitter

Figure 53 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 67 lists the UART RS-232 serial mode transmit timing characteristics.

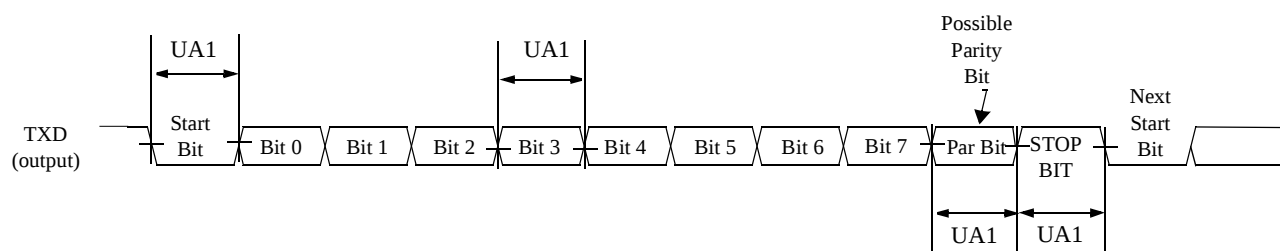


Figure 53. UART RS-232 Serial Mode Transmit Timing Diagram

Table 67. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.10.11.2.2 UART Receiver

Figure 54 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 68 lists serial mode receive timing characteristics.

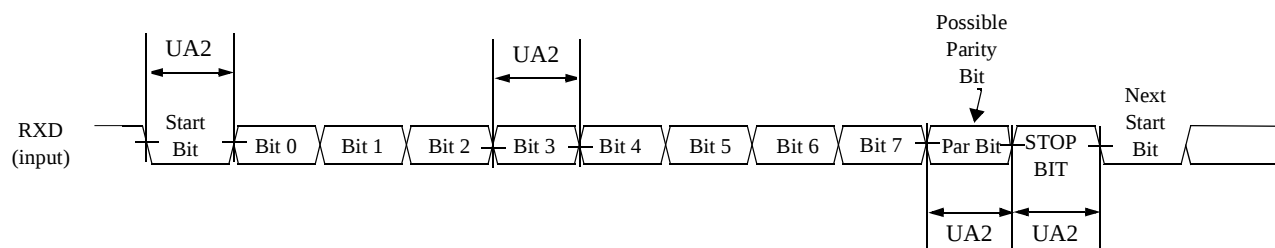


Figure 54. UART RS-232 Serial Mode Receive Timing Diagram

Table 68. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time ¹	t_{Rbit}	$1/F_{baud_rate}^2 - 1/(16 \cdot F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \cdot F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16 \cdot F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \cdot F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.10.11.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 55 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 69 lists the transmit timing characteristics.

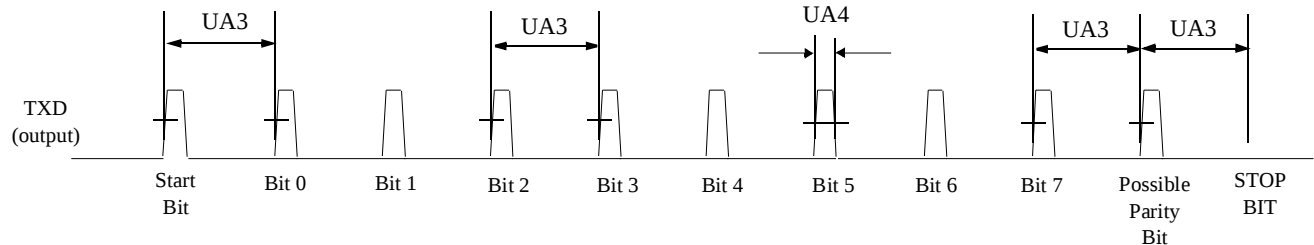


Figure 55. UART IrDA Mode Transmit Timing Diagram

Table 69. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud_rate}) - T_{ref_clk}$	$(3/16)*(1/F_{baud_rate}) + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART IrDA Mode Receiver

Figure 56 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 70 lists the receive timing characteristics.

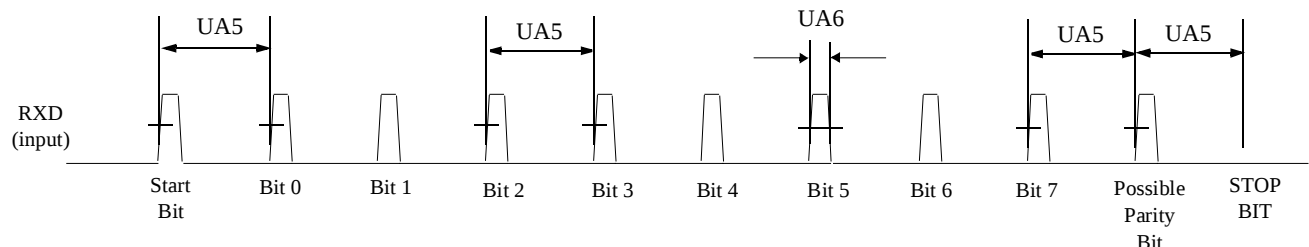


Figure 56. UART IrDA Mode Receive Timing Diagram

Table 70. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time ¹ in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}^2 - 1/(16*F_{baud_rate})$	$1/F_{baud_rate} + 1/(16*F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 μs	$(5/16)*(1/F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16*F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.10.12 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.10.12.1 Transmit Timing

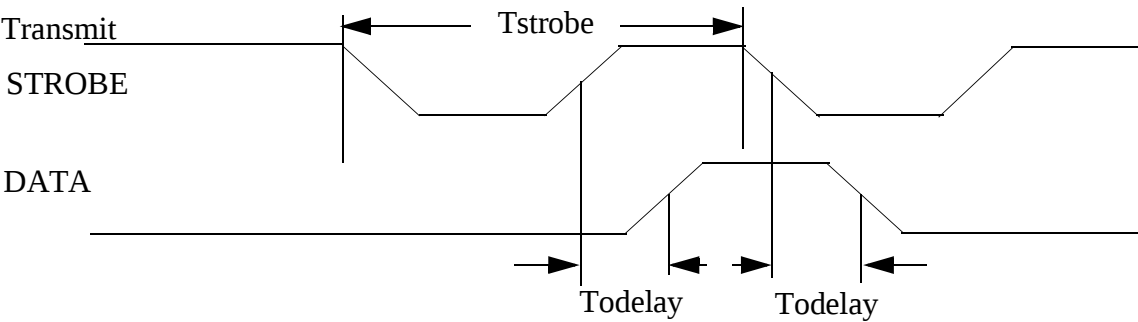


Figure 57. USB HSIC Transmit Waveform

Table 71. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.12.2 Receive Timing

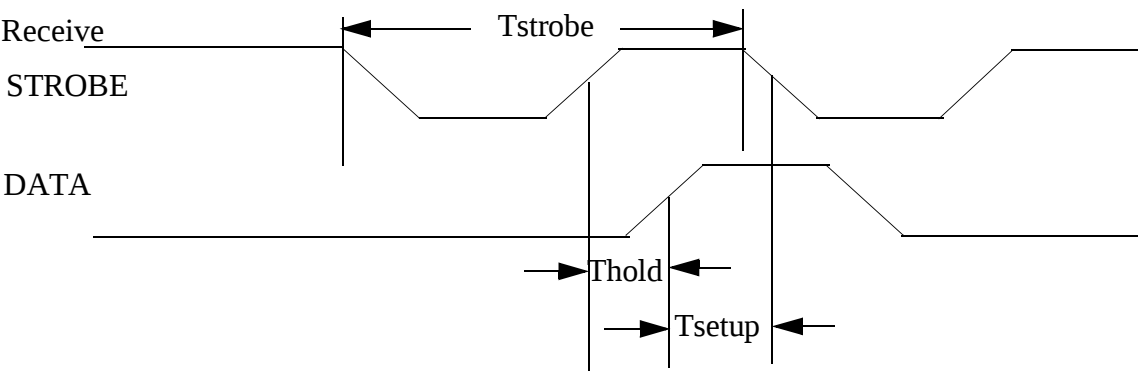


Figure 58. USB HSIC Receive Waveform

Table 72. USB HSIC Receive Parameters¹

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

¹ The timings in the table are guaranteed when:
 —AC I/O voltage is between 0.9x to 1x of the I/O supply
 —DDR_SEL configuration bits of the I/O are set to (10)b

4.10.13 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host.

4.10.14 EPD Timing Controller

4.10.14.1 Source and Gate Driver for K7902 (SPDC)

4.10.14.1.1 Source Driver

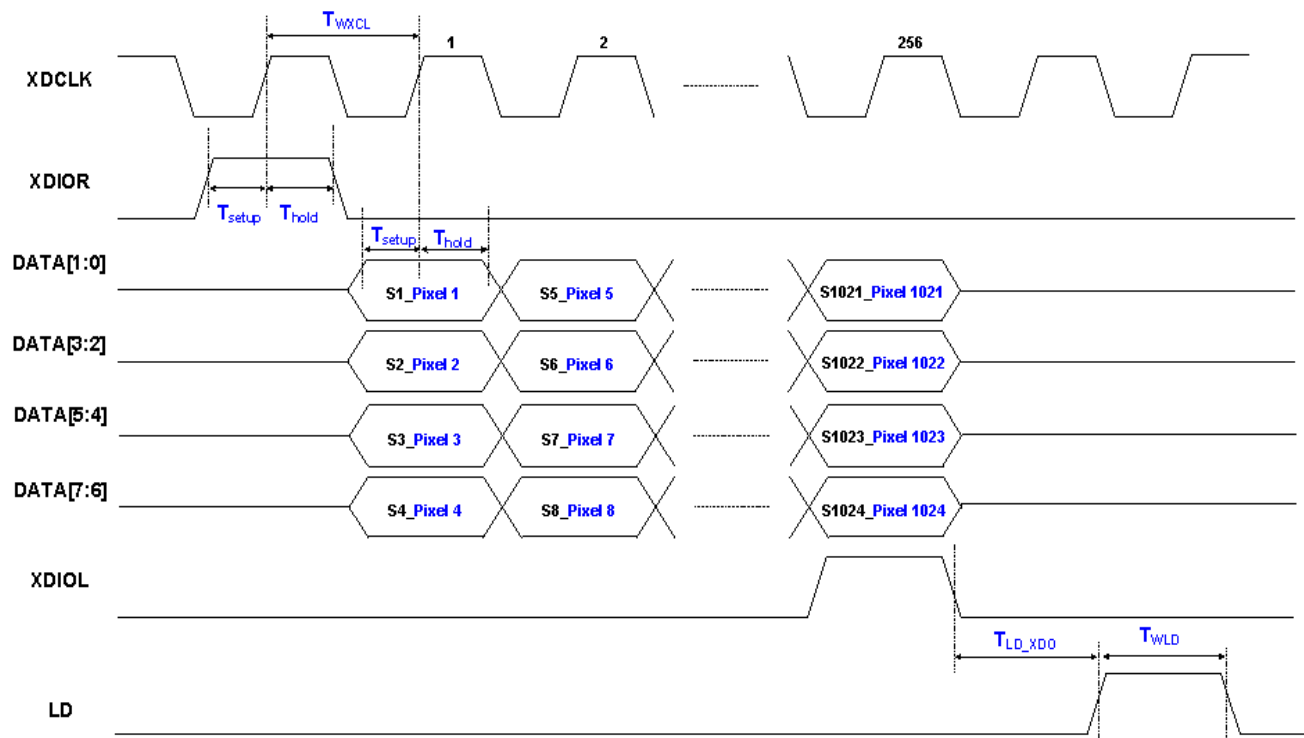


Figure 59. Source Driver Diagram

Table 73. Source Driver Details

Parameter	Symbol	Conditions	Min.	Max.	Unit
Clock period		T_{WXCL}	VDD=3.3V	50	nS
Data setup time		T_{setup}	VDD=3.3V	8	nS
Data hold time		T_{hold}	VDD=3.3V	2	nS
LD pulse width		T_{WLD}	VDD=3.3V	1	XDCLK
Time from XDIOI/XDIOR to LD		T_{LD_XDO}	VDD=3.3V	1	XDCLK

4.10.14.1.2 Gate Driver

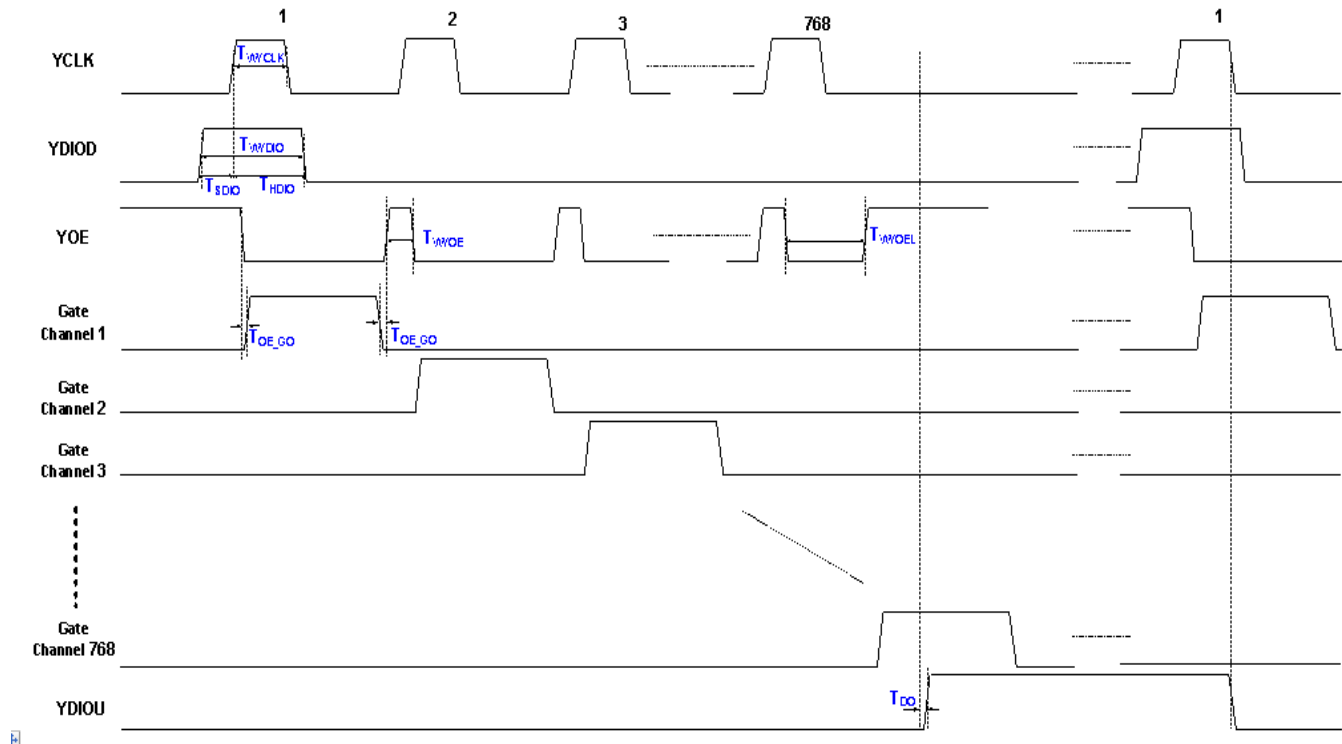


Figure 60. Gate Driver Diagram

Table 74. Gate Driver Details

Signal	Parameter	Symbol	Conditions	Min.	Max.	Unit
YCLK	YCLK "H" pulse width	T_{WYCLK}	VDD=3.3V	400		nS
YDIOU/YDIOD (Input)	YDIOU/YDIOD setup time	T_{SDIO}	VDD=3.3V	500		nS
	YDIOU/YDIOD hold time	T_{HDIO}	VDD=3.3V	500		nS
YOE	YOE "H" pulse width	T_{WYOE}	VDD=3.3V	1		μ S
	YOE last "L" pulse width in one frame	T_{WYOE_L}	VDD=3.3V	0		μ S
YOE-GN	YOE rise/fall to GN rise/fall delay time	T_{OE_GO}	VDD=3.3V		2	μ S
YDIOU/YDIOD (Output)	YDIOU/YDIOD delay time	T_{DO}	VDD=3.3V		2	μ S
	YDIOU/YDIOD "H" pulse width	T_{WYOE}	VDD=3.3V	1		YCLK

4.10.14.2 Source Driver for K7600 (SPDC)

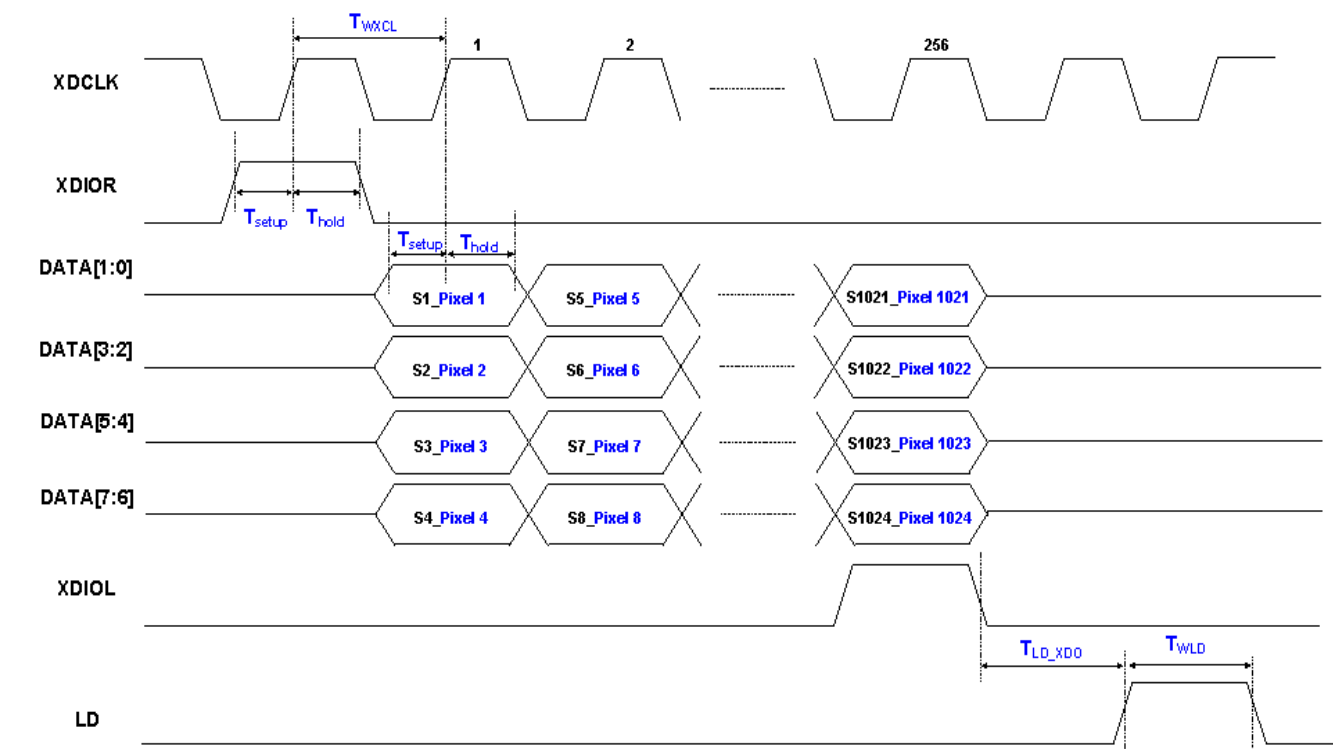


Figure 61. Source Driver Diagram

Table 75. Source Driver Details

Parameter	Symbol	Conditions	Min.	Max.	Units
Clock period	T_{WXCL}	VDD=3.3V	16	-	ns
Data setup time	T_{setup}	VDD=3.3V	5	-	ns
Data hold time	T_{hold}	VDD=3.3V	2	-	ns
LD pulse width	T_{WLD}	VDD=3.3V	1	-	XDCCLK
Time from XDIO/XDIO to LD	T_{LD_XDO}	VDD=3.3V	1	-	XDCCLK

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 76 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloLite Fuse Map document and the System Boot chapter of the i.MX 6SoloLite reference manual.

Table 76. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 76. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
LCD_DAT0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DAT1	Input	BOOT_CFG1[1]	
LCD_DAT2	Input	BOOT_CFG1[2]	
LCD_DAT3	Input	BOOT_CFG1[3]	
LCD_DAT4	Input	BOOT_CFG1[4]	
LCD_DAT5	Input	BOOT_CFG1[5]	
LCD_DAT6	Input	BOOT_CFG1[6]	
LCD_DAT7	Input	BOOT_CFG1[7]	
LCD_DAT8	Input	BOOT_CFG2[0]	
LCD_DAT9	Input	BOOT_CFG2[1]	
LCD_DAT10	Input	BOOT_CFG2[2]	
LCD_DAT11	Input	BOOT_CFG2[3]	
LCD_DAT12	Input	BOOT_CFG2[4]	
LCD_DAT13	Input	BOOT_CFG2[5]	
LCD_DAT14	Input	BOOT_CFG2[6]	
LCD_DAT15	Input	BOOT_CFG2[7]	
LCD_DAT16	Input	BOOT_CFG4[0]	
LCD_DAT17	Input	BOOT_CFG4[1]	
LCD_DAT18	Input	BOOT_CFG4[2]	
LCD_DAT19	Input	BOOT_CFG4[3]	
LCD_DAT20	Input	BOOT_CFG4[4]	
LCD_DAT21	Input	BOOT_CFG4[5]	
LCD_DAT22	Input	BOOT_CFG4[6]	
LCD_DAT23	Input	BOOT_CFG4[7]	

5.2 Boot Devices Interfaces Allocation

Table 77 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 77. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	
EIM	EIM	LCD_DAT[6-21], KEY_COL[0-7], KEY_ROW[0-7], EPDC_D[8-15], EPDC_VCOM0, EPDC_VCOM1, EPDC_BDR0, EPDC_PWRCTRL[0-2], EPDC_SDCE1	
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD, SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D5, NANDF_D6, NANDF_D7, NANDF_D8, KEY_ROW1	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit Fastboot (UHSI not supported)
SD/MMC	USDHC-4	FEC_MDIO, FEC_TX_CLK, FEC_RX_ER, FEC_CRS_DV, FEC_RXD1, FEC_TXD0, FEC_MDC, FEC_RXD0, FEC_TX_EN, FEC_TXD1, EPDC_PWCTRL1, FEC_REFOUT	1, 4, or 8 bit Fastboot
I2C	I2C-1	I2C1_SCL, I2C1_SDA	—
I2C	I2C-2	I2C2_SCL, I2C2_SDA	—
I2C	I2C-3	AUD_RXFS, AUD_RXC	—
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B USB_OTG1_DP, USB_OTG1_DN, and USB_OTG1_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 13 x 13mm Package Information

6.1.1 Case 2240, 13 x 13 mm, 0.5 mm Pitch, 24 x 24 Ball Matrix

Figure 62 shows the top, bottom, and side views of the 13×13 mm BGA package

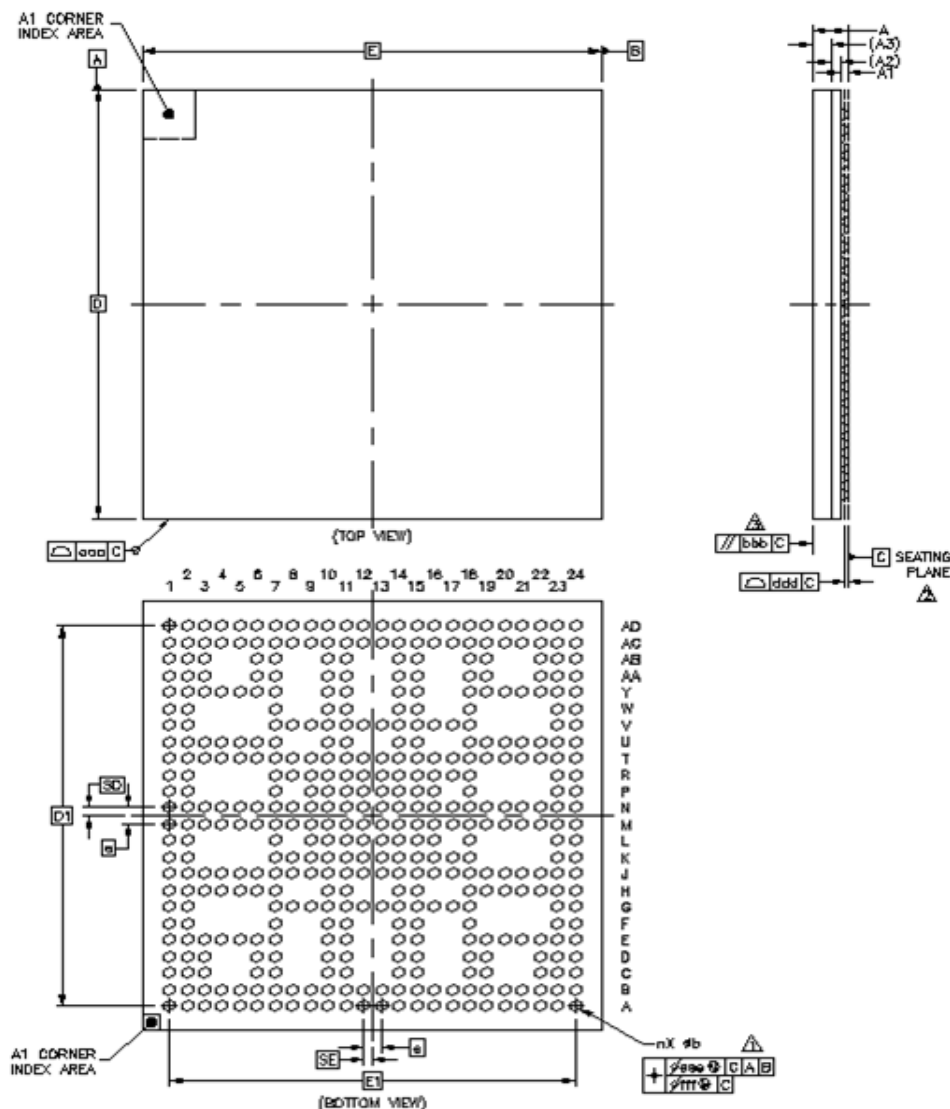


Figure 62. 13 x 13, 0.5 mm BGA Package Top, Bottom, and Side Views

Table 78 shows the 13 x 13 mm BGA package details

Table 78. 13 x 13, 0.5 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	0.88	-	1.1
Stand Off	A1	0.16	-	0.26
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.54 REF		
Body Size	D	13 BSC		
	E	13 BSC		
Ball Diameter		0.3		
Ball Opening		0.275		
Ball Width	b	0.27	-	0.37
Ball Pitch	e	0.5 BSC		
Ball Count	n	432		
Edge Ball Center to Center	D1	11.5 BSC		
	E1	11.5 BSC		
Body Center to Contact Ball	SD	0.25 BSC		
	SE	0.25 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Coplanarity	ddd	0.08		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.05		

6.1.2 13 x 13 mm Ground, Power, Sense, Not Connected and Reference Contact Assignments

Table 79 shows the device connection list for ground, power, sense, and reference contact signals.

Table 79. 13 x 13 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DDR_VREF	N5	
GND	A1, A4, A7, A24, C6, C10, C14, C19, D1, D2, E5, G1, G8, G9, G10, G11, G13, G14, G15, G17, G18, H3, H7, H18, H22, J5, K1, L7, L9, L10, L11, L12, L13, L14, L15, L16, M5, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N3, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N22, P9, P10, P11, P12, P13, P14, P15, P16, R1, T5, U3, U7, U18, U22, V1, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18, Y5, AA1, AA2, AB10, AB14, AB18, AC18, AD1, AD4, AD7, AD24	
GND_Kelvin	V17	Must be connected
GPANAIO	AD22	Analog pad
NVCC_1P2V	W7	
NVCC18_IO	E14, E15, M20, Y11	
NVCC33_IO	H10, H11, H14, H15, L18, M18, T19, U10, U11	
NVCC_DRAM	E6, Y6, G7, H6, J6, N6, P7, T6, U6, V7	Supply of the DDR Interface
NVCC_DRAM_2P5	M6	
NVCC_PLL	Y19	
NVCC_SD1		
NVCC_SD2		
NVCC_SD3		
VDD_ARM_CAP	J15, J16, J17, J18, K15, K16, K17, K18	Secondary Supply for the ARM0 and ARM1 Cores (internal regulator output—requires capacitor if internal regulator is used)
VDD_ARM_IN	J12, J13, J14, K12, K13, K14	Primary Supply, for the ARM0 and ARM1 Core' Regulator
VDD_HIGH_CAP	R14, R15, T14, T15	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDD_HIGH_IN	R12, R13, T12, T13	Primary Supply for the 2.5 V Regulator
VDD_PU_CAP	R7, R8, R9, T7, T8, T9	Secondary Supply for the VPU and GPU's (internal regulator output—requires capacitor if internal regulator is used)
VDD_PU_IN	R10, R11, T10, T11	

Table 79. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLBPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	
USB_OTG2_VBUS	AD18	
ZQPAD	AE17	
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 80 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 80. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_MCLK	H19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	Keeper
AUD_RXFS	J19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_TXC	H20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVIS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVIS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP			CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D12	C1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[12]	Input	PU (100K)
DRAM_D13	C2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[13]	Input	PU (100K)
DRAM_D14	B1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[14]	Input	PU (100K)
DRAM_D15	B2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[15]	Input	PU (100K)
DRAM_D16	AD8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[16]	Input	PU (100K)
DRAM_D17	AC7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[17]	Input	PU (100K)
DRAM_D18	AD6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[18]	Input	PU (100K)
DRAM_D19	AC6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[19]	Input	PU (100K)
DRAM_D2	AB2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[2]	Input	PU (100K)
DRAM_D20	AD5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[20]	Input	PU (100K)
DRAM_D21	AC5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[21]	Input	PU (100K)
DRAM_D22	AC4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[22]	Input	PU (100K)
DRAM_D23	AD3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[23]	Input	PU (100K)
DRAM_D24	A3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[24]	Input	PU (100K)
DRAM_D25	B4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[25]	Input	PU (100K)
DRAM_D26	B5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[26]	Input	PU (100K)
DRAM_D27	A5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[27]	Input	PU (100K)
DRAM_D28	B6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[28]	Input	PU (100K)
DRAM_D29	A6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[29]	Input	PU (100K)
DRAM_D3	AB1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[3]	Input	PU (100K)
DRAM_D30	B7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[30]	Input	PU (100K)
DRAM_D31	A8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[31]	Input	PU (100K)
DRAM_D4	AA3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[4]	Input	PU (100K)
DRAM_D5	Y3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[5]	Input	PU (100K)
DRAM_D6	Y1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[6]	Input	PU (100K)
DRAM_D7	Y2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[7]	Input	PU (100K)
DRAM_D8	E2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[8]	Input	PU (100K)
DRAM_D9	E1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[9]	Input	PU (100K)
DRAM_DQM0	V2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[0]	Output	0
DRAM_DQM1	G2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[1]	Output	0

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_DQM2	AB3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[2]	Output	0
DRAM_DQM3	C3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[3]	Output	0
DRAM_RAS_B	N1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RAS	Output	0
DRAM_RESET_B	D6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RESET	Output	0
DRAM_SDBA0	J1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[0]	Output	0
DRAM_SDBA1	T1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[1]	Output	0
DRAM_SDBA2	H1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[2]	Output	0
DRAM_SDCKE0	P2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[0]	Output	0
DRAM_SDCKE1	M2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[1]	Output	0
DRAM_SDCLK_0	L1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK0	Input	Hi-Z
DRAM_SDCLK_0_B	M1	NVCC_DRAM	DDRCLK		DRAM_SDCLK_0_B	—	—
DRAM_SDOdT0	Y4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[0]	Output	0
DRAM_SDOdT1	E4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[1]	Output	0
DRAM_SDQS0	W2	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	W1	NVCC_DRAM	DDRCLK		DRAM_SDQS0_B	—	—
DRAM_SDQS1	F1	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	F2	NVCC_DRAM	DDRCLK		DRAM_SDQS1_B	—	—
DRAM_SDQS2	AC3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AD2	NVCC_DRAM	DDRCLK		DRAM_SDQS2_B	—	—
DRAM_SDQS3	B3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	A2	NVCC_DRAM	DDRCLK		DRAM_SDQS3_B	—	—
DRAM_WE_B	U1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDWE	Output	0
ECSPi1_MISO	M19	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	Keeper
ECSPi1_MOSI	N20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[9]	Input	Keeper
ECSPi1_SCLK	N19	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[8]	Input	Keeper
ECSPi1_SS0	M21	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[11]	Input	Keeper
ECSPi2_MISO	T20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[14]	Input	Keeper
ECSPi2_MOSI	U20	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[13]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
ECSPI2_SCLK	U19	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[12]	Input	Keeper
ECSPI2_SS0	T21	NVCC_GPIO	ALT5	ALT5	gpio4_GPIO[15]	Input	Keeper
EPDC_BDR0	C18	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[5]	Input	Keeper
EPDC_BDR1	B18	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[6]	Input	Keeper
EPDC_D0	A18	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[7]	Input	Keeper
EPDC_D1	A17	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[8]	Input	Keeper
EPDC_D10	G16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[17]	Input	Keeper
EPDC_D11	F14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[18]	Input	Keeper
EPDC_D12	D14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[19]	Input	Keeper
EPDC_D13	B14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[20]	Input	Keeper
EPDC_D14	A14	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[21]	Input	Keeper
EPDC_D15	A13	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[12]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EPDC_PWRSTAT	E10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[13]	Input	Keeper
EPDC_PWRWAKE UP	D10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[27]	Input	Keeper
EPDC_SDCE1	A10	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[28]	Input	Keeper
EPDC_SDCE2	B9	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[29]	Input	Keeper
EPDC_SDCE3	A9	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[30]	Input	Keeper
EPDC_SDCLK	B10	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[23]	Input	Keeper
EPDC_SDLE	B8	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[24]	Input	Keeper
EPDC_SDOE	E7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[25]	Input	Keeper
EPDC_SDSHR	F7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[26]	Input	Keeper
EPDC_VCOM0	C7	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[3]	Input	Keeper
EPDC_VCOM1	D7	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[4]	Input	Keeper
FEC_CRS_DV	AC9	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[25]	Input	Keeper
FEC_MDC	AA7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[23]	Input	Keeper
FEC_MDIO	AB7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[20]	Input	Keeper
FEC_REF_CLK	W10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[26]	Input	Keeper
FEC_RX_ER	AD9	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[19]	Input	Keeper
FEC_RXD0	AA10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[17]	Input	Keeper
FEC_RXD1	AC10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[18]	Input	Keeper
FEC_TX_CLK	AC8	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[21]	Input	Keeper
FEC_TX_EN	AD10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[22]	Input	Keeper
FEC_TXD0	Y10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[24]	Input	Keeper
FEC_TXD1	W11	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[16]	Input	Keeper
HSIC_DAT	AA6	NVCC_GPIO	DDR		usb_H_DATA	Input	PD (100K)
HSIC_STROBE	AB6	NVCC_GPIO	DDR		usb_H_STROBE	Input	PD (100K)
I2C1_SCL	AC13	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[15]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
JTAG_MOD	Y14	NVCC_JTAG	GPIO	ALT5	sjc_MOD		PU (100K)
JTAG_TCK	AA14	NVCC_JTAG	GPIO	ALT5	sjc_TCK		PU (47K)
JTAG_TDI	W14	NVCC_JTAG	GPIO	ALT5	sjc_TDI		PU (47K)
JTAG_TDO	W15	NVCC_JTAG	GPIO	ALT5	sjc_TDO		Keeper
JTAG_TMS	Y15	NVCC_JTAG	GPIO	ALT5	sjc_TMS		PU (47K)
JTAG_TRSTB	AA15	NVCC_JTAG	GPIO	ALT5	sjc_TRSTB		PU (47K)
KEY_COL0	G23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[3]	Input	Keeper
KEY_ROW6	C24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[5]	Input	Keeper
KEY_ROW7	B24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[7]	Input	Keeper
LCD_CLK	T22	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[15]	Input	Keeper
LCD_DAT0	Y24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[20]	Input	Keeper
LCD_DAT1	W23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[21]	Input	Keeper
LCD_DAT10	R23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[30]	Input	Keeper
LCD_DAT11	R24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[31]	Input	Keeper
LCD_DAT12	P23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[0]	Input	Keeper
LCD_DAT13	P24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[1]	Input	Keeper
LCD_DAT14	N21	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[2]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
LCD_DAT15	N23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[24]	Input	Keeper
LCD_DAT5	U21	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		src_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_WAKEUP_ALARM	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
PWM1	Y7	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[22]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
RTC_XTALI	AB19	VDD_SNV5_CAP			RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNV5_CAP			RTC_XTALO	—	—
SD1_CLK	B20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[13]	Input	Keeper
SD1_DAT3	B22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[6]	Input	Keeper
SD1_DAT4	A22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[12]	Input	Keeper
SD1_DAT5	A21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[9]	Input	Keeper
SD1_DAT6	A20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[7]	Input	Keeper
SD1_DAT7	A19	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[10]	Input	Keeper
SD2_CLK	AC24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[5]	Input	Keeper
SD2_CMD	AB24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[4]	Input	Keeper
SD2_DAT0	AB22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[1]	Input	Keeper
SD2_DAT1	AB23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[30]	Input	Keeper
SD2_DAT2	AA22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[3]	Input	Keeper
SD2_DAT3	AA23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[28]	Input	Keeper
SD2_DAT4	AA24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[2]	Input	Keeper
SD2_DAT5	Y20	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[31]	Input	Keeper
SD2_DAT6	Y21	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[29]	Input	Keeper
SD2_DAT7	Y22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[0]	Input	Keeper
SD2_RST	Y23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[27]	Input	Keeper
SD3_CLK	AB11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[18]	Input	Keeper
SD3_CMD	AA11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[21]	Input	Keeper
SD3_DAT0	AC11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[19]	Input	Keeper
SD3_DAT1	AD11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[20]	Input	Keeper
SD3_DAT2	AC12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[16]	Input	Keeper
SD3_DAT3	AD12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[17]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
TAMPER	Y18	VDD_SNVIS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVIS_TD1	Input	
TEST_MODE	U15	VDD_SNVIS_IN	GPIO	ALT0	Reserved—Factory Use Only	Input	
UART1_RXD	B19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[16]	Input	Keeper
UART1_TXD	D19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[17]	Input	Keeper
USB_OTG_CHD_B	AC22	USB_OTG_VBUS	ANALOG		USB_OTG_CHD_B	—	—
USB_OTG1_DN	AD19	USB_OTG_VBUS	ANALOG		USB_OTG1_DN	—	—
USB_OTG1_DP	AC19	USB_OTG_VBUS	ANALOG		USB_OTG1_DP	—	—
USB_OTG2_DN	AD17	USB_OTG_VBUS	ANALOG		USB_OTG2_DN	—	—
USB_OTG2_DP	AC17	USB_OTG_VBUS	ANALOG		USB_OTG2_DP	—	—
WDOG_B	F18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[18]	Input	Keeper
XTALI	AD21	NVCC_PLL	ANALOG		XTALI	—	—
XTALO	AC21	NVCC_PLL	ANALOG		XTALO	—	—
ZQPAD	H2	NVCC_DRAM	ZQPAD		ZQPAD	Input	Hi-Z

¹ The state immediately after reset and before ROM firmware or software has executed.

6.1.3 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 81 shows the MAPBGA 13 x 13mm, 0.5 mm pitch ball map.

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD
24	GND	KEY_ROW7	KEY_ROW6	KEY_COL5	KEY_ROW2	KEY_ROW1	KEY_ROW0	LCD_RESET	LCD_ENABLE	LCD_DAT23	LCD_DAT21	LCD_DAT19	LCD_DAT16	LCD_DAT13	LCD_DAT11	LCD_DAT9	LCD_DAT7	LCD_DAT4	LCD_DAT2	LCD_DAT0	SD2_DAT4	SD2_CMD	SD2_CLK	GND
23	SD1_DAT1	SD1_DAT0	KEY_COL7	KEY_ROW5	KEY_COL2	KEY_COL1	KEY_COL0	LCD_HSYNC	LCD_VSYNC	LCD_DAT22	LCD_DAT20	LCD_DAT18	LCD_DAT15	LCD_DAT12	LCD_DAT10	LCD_DAT8	LCD_DAT6	LCD_DAT3	LCD_DAT1	SD2_RST	SD2_DAT3	SD2_DAT1	CLK1_P	CLK1_N

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

15	16	17	18	19	20	21	22
EPDC_D5	EPDC_D3	EPDC_D1	EPDC_D0	SD1_DAT7	SD1_DAT6	SD1_DAT5	SD1_DAT4
EPDC_D6	EPDC_D4	EPDC_D2	EPDC_BDR1	UART1_RXD	SD1_CLK	SD1_CMD	SD1_DAT3
EPDC_D7	NC	NC	EPDC_BDR0	GND	NC	NC	SD1_DAT2
EPDC_D8	NC	NC	I2C2_SDA	UART1_TXD	NC	NC	KEY_COL6
NVCC18_IO	NC	NC	I2C2_SCL	KEY_ROW4	KEY_COL4	KEY_ROW3	KEY_COL3
EPDC_D9	NC	NC	WDOG_B	NC	NC	NC	NC
GND	EPDC_D10	GND	GND	NC	NC	NC	NC
NVCC33_IO	NC	NC	GND	AUD_MCLK	AUD_TXC	AUD_TXFS	GND
VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	AUD_RXFS	AUD_RXD	AUD_RXC	AUD_TXD
VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	VDD_ARM_CAP	NC	NC	NC	NC
GND	GND	NC	NVCC33_IO	NC	NC	NC	NC
GND	GND	GND	NVCC33_IO	ECSP11_MISO	NVCC18_IO	ECSP11_SS0	LCD_DAT17
GND	GND	GND	VDD_SOC_CAP	ECSP11_SCLK	ECSP11_MOSI	LCD_DAT14	GND
GND	GND	NC	VDD_SOC_CAP	NC	NC	NC	NC
VDD_HIGH_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_CAP	NC	NC	NC	NC
VDD_HIGH_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	NVCC33_IO	ECSP12_MISO	ECSP1_SS0	LCD_CLK
NVCC_PLL	NC	NC	GND	ECSP12_SCLK	ECSP12_MOSI	LCD_DAT5	GND
GND	GND	GND_KELVIN	GND	NC	NC	NC	NC
JTAG_TDO	NC	NC	TEST_MODE	NC	NC	NC	NC
JTAG_TMS	NC	NC	TAMPER	ONOFF	SD2_DAT5	SD2_DAT6	SD2_DAT7
JTAG_TRSTB	NC	NC	USB_OTG1_VBUS	RTC_XTALO	NC	NC	SD2_DAT2
BOOT_MODE1	NC	NC	GND	RTC_XTALI	NC	NC	SD2_DAT0
BOOT_MODE0	POR_B	USB_OTG2_DP	GND	USB_OTG1_DP	VDD_SNVIS_IN	XTALO	USB_OTG_CHD_B
PMIC_ON_REQ	PMIC_STBY_REQ	USB_OTG2_DN	USB_OTG2_VBUS	USB_OTG1_DN	VDD_SNVIS_CAP	XTALI	GPANAIO

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

8	9	10	11	12	13	14
DRAM_D31	EPDC_SDCE3	EPDC_SDCE1	EPDC_GDSP	EPDC_GDCLK	EPDC_D15	EPDC_D14
EPDC_SDLE	EPDC_SDCE2	EPDC_SDCLK	EPDC_PRWCOM	EPDC_GDRL	EPDC_GDOE	EPDC_D13
NC	NC	GND	EPDC_SDCE0	NC	NC	GND
NC	NC	EPDC_PWRWAKEUP	EPDC_PWRCTRL0	NC	NC	EPDC_D12
NC	NC	EPDC_PWRSTAT	EPDC_PWRCTRL1	NC	NC	NVCC18_IO
NC	NC	EPDC_PWRINT	EPDC_PWRCTRL2	NC	NC	EPDC_D11
GND	GND	GND	GND	EPDC_PWRCTRL3	GND	GND
NC	NC	NVCC33_IO	NVCC33_IO	NC	NC	NVCC33_IO
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
NC	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
NC	GND	GND	GND	GND	GND	GND
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
NC	NC	NVCC_3V3	NHVCC_3V3	NC	NC	VDD_USB_CAP
GND	GND	GND	GND	GND	GND	GND
NC	NC	FEC_REF_CLK	FEC_TXD1	NC	NC	JTAG_TDI
NC	NC	FEC_TXD0	NVCC18_IO	NC	NC	JTAG_MOD
NC	NC	FEC_RXD0	SD3_CMD	NC	NC	JTAG_TCK
NC	NC	GND	SD3_CLK	NC	NC	GND
FEC_TX_CLK	FEC_CRS_DV	FEC_RXD1	SD3_DAT0	SD3_DAT2	I2C1_SCL	REF_CLK_24M
DRAM_D16	FEC_RX_ER	FEC_TX_EN	SD3_DAT1	SD3_DAT3	I2C1_SDA	REF_CLK_32K

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

1	2	3	4	5	6	7
GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND
DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30
DRAM_D12	DRAM_D13	DRAM_DQM3	NC	NC	GND	EPDC_VCOM0
GND	GND	DRAM_D11	NC	NC	DRAM_RESET	EPDC_VCOM1
DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE
DRAM_SDQS1	DRAM_SDQS1_B	NC	NC	NC	NC	EPDC_SDSHR
GND	DRAM_DQM1	NC	NC	NC	NC	NVCC_DRAM
DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND
DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP
GND	DRAM_A15	NC	NC	NC	NC	VDD_SOC_CAP
DRAM_SDCLK_0	DRAM_CS1	NC	NC	NC	NC	GND
DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND
DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND
DRAM_CAS	SDCKE0	NC	NC	NC	NC	NVCC_DRAM
GND	DRAM_A14	NC	NC	NC	NC	VDD_PU_CAP
DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP
DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND
GND	DRAM_DQM0	NC	NC	NC	NC	NVCC_DRAM
DRAM_SDQS0_B	DRAM_SDQS0	NC	NC	NC	NC	NVCC_1P2
DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1
GND	GND	DRAM_D4	NC	NC	HSIC_DAT	FEC_MDC
DRAM_D3	DRAM_D2	DRAM_DQM2	NC	NC	HSIC_STROBE	FEC_MDIO
DRAM_D1	DRAM_D0	DRAM_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17
GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D20	GND

7 Revision History

[Table 83](#) provides a revision history for this data sheet.

Table 83. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	Updated Table 77, "Interfaces Allocation During Boot," on page 97.
Rev 0.1	11/2012	- Updated Table 8, "Package Thermal Resistance Data," on page 18. - Corrected title of Table 79, "13 x 13 mm Supplies Contact Assignment," on page 100. - Corrected title of Table 81, "13 x 13 mm, 0.5 mm Pitch Ball Map," on page 110.
Rev. 0	10/2012	Initial public release.

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