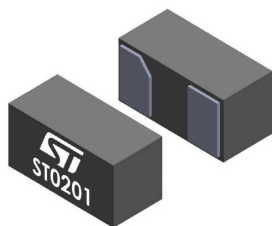
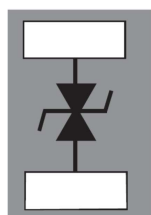


## Ultra low clamping single line bidirectional ESD protection



0201 package

**Figure 1. Functional diagram**



### Features

- Ultra low clamping voltage: 7 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns / 16 A TLP)
- Bidirectional device
- Low leakage current
- 0201 package
- **ECOPACK2** compliant component
- Exceeds the following standard:
  - IEC 61000-4-2 level 4 =  $\pm 30$  kV (air discharge) and  $\pm 18$  kV (contact discharge)

### Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

### Description

The ESDZV5-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

#### Product status

ESDZV5-1BF4

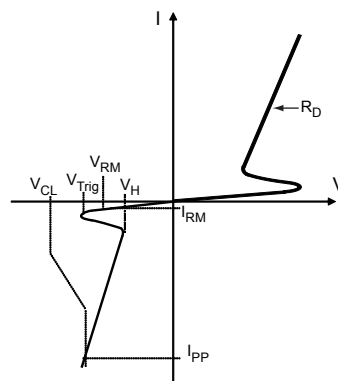
# 1 Characteristics

**Table 1. Absolute ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Value	Unit
$V_{PP}$	Peak pulse voltage	Contact discharge	kV
		Air discharge	
$P_{PP}$	Peak pulse power dissipation (8/20 $\mu\text{s}$ )	70	W
$I_{PP}$	Peak pulse current (8/20 $\mu\text{s}$ )	7	A
$T_j$	Operating junction temperature range	-55 to +150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$

**Figure 2. Electrical characteristics (definitions)**

Symbol	Parameter
$V_{Trig}$	= Trigger voltage
$V_{CL}$	= Clamping voltage
$I_{RM}$	= Leakage current @ $V_{RM}$
$V_{RM}$	= Stand-off voltage
$I_{PP}$	= Peak pulse current
$R_D$	= Dynamic resistance
$V_H$	= Holding voltage
$C_{LINE}$	= Input capacitance per line

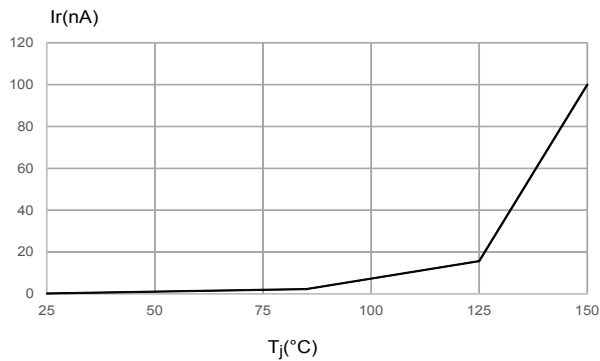

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Test condition	Min.	Typ.	Max.	Unit
$V_{Trig}$	Higher voltage than $V_{Trig}$ guarantees the protection turn-on	5.8		10	V
$V_H$	Lower voltage than $V_H$ guarantees the protection turn-off	4	4.6		
$I_{RM}$	$V_{RM} = 5.5\text{ V}^{(1)}$			100	nA
$V_{CL}$	8 kV contact discharge after 30 ns, IEC 61000-4-2		7		V
$V_{CL}$	8/20 $\mu\text{s}$ waveform, $I_{PP} = 7\text{ A}$			10	V
$C_{LINE}$	$F = 1\text{ MHz}$ , $V_{LINE} = 0\text{ V}$ , $V_{OSC} = 30\text{ mV}$		6	7.5	pF
$R_D$	Pulse duration 100 ns		0.18		$\Omega$

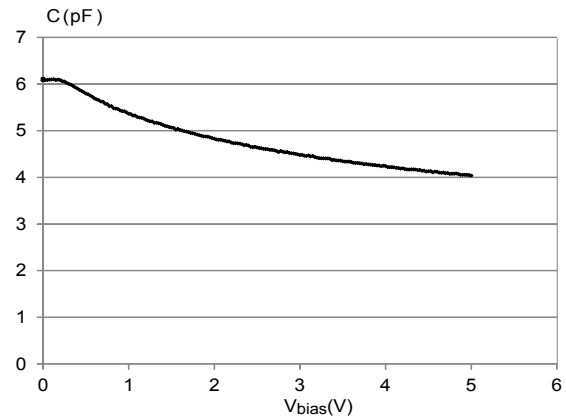
1. Application note: when used to protect a line connected to a DC source, the DC voltage must be lower than the minimum  $V_H$  to enable the diode to return to its non-conducting state after the transient.

## 1.1 Characteristics (curves)

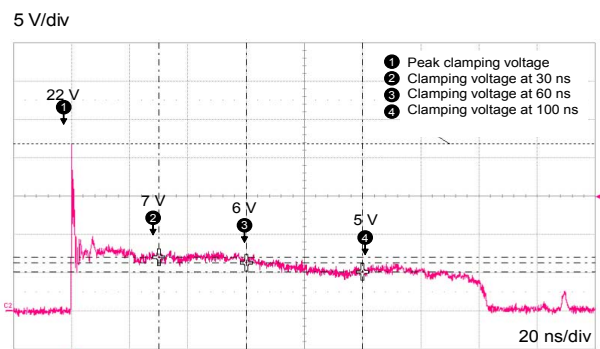
**Figure 3. Leakage current versus junction temperature (typical values)**



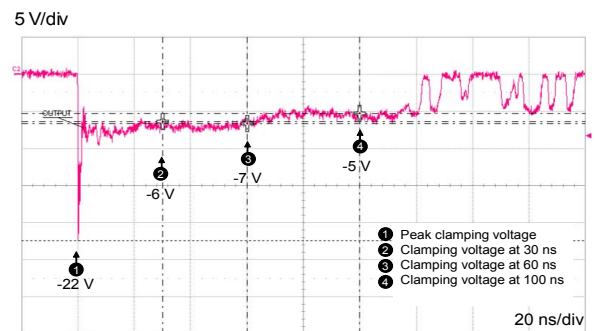
**Figure 4. Junction capacitance versus reverse voltage applied (typical values)**



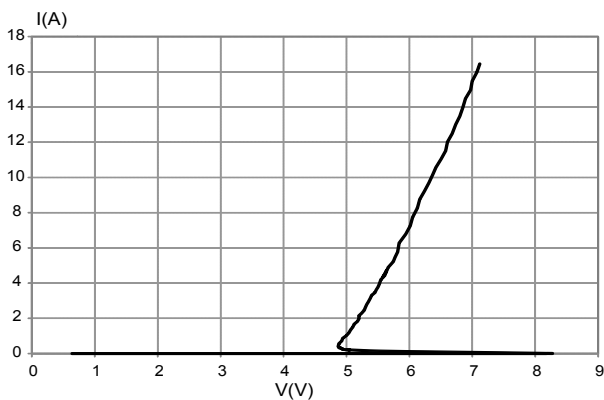
**Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)**



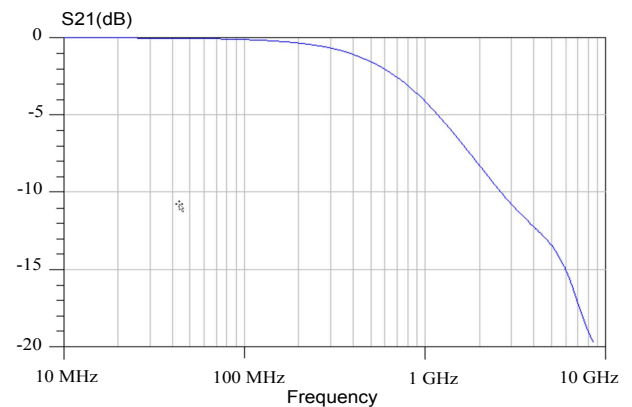
**Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)**



**Figure 7. TLP characteristic**



**Figure 8. S21 attenuation measurement result**

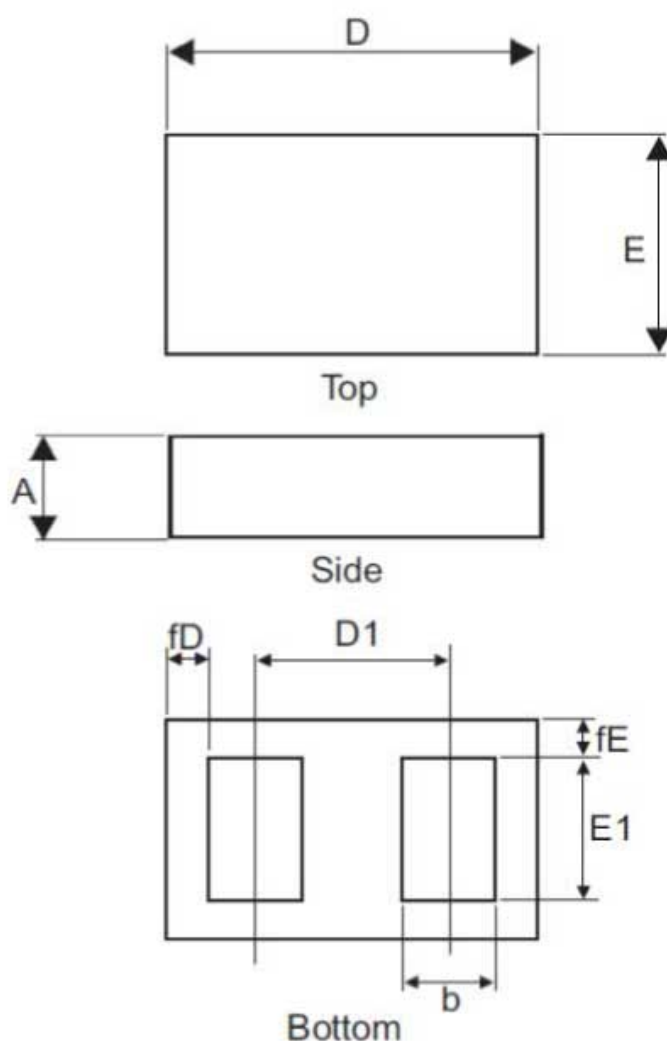


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 2.1 0201 package information

**Figure 9. 0201 package outline**



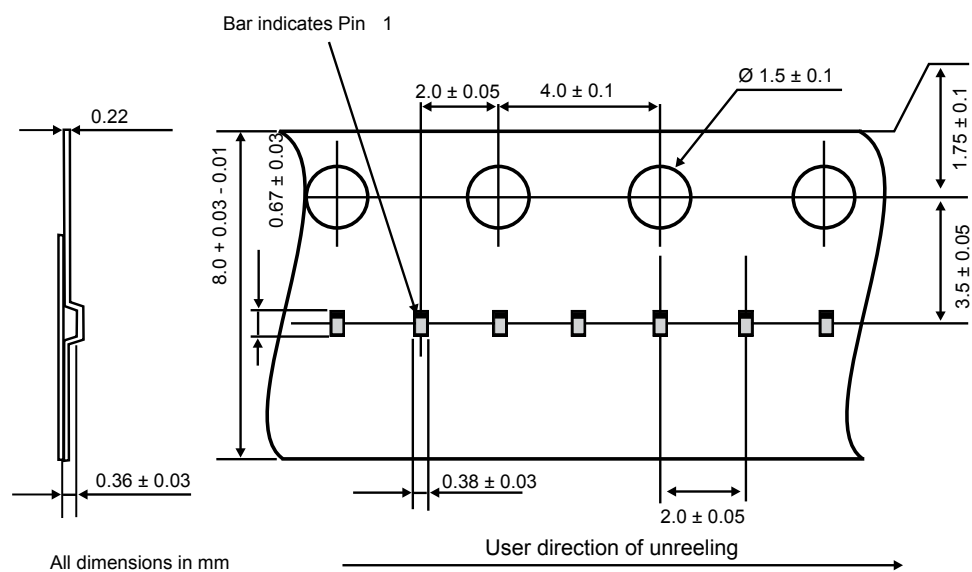
**Note:** The marking codes can be rotated by 90 ° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

**Table 3. 0201 package mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.270	0.300	0.330
b	0.1675	0.1875	0.2075
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.205	0.225	0.245
fD	0.0175	0.0275	0.0375
fE	0.0175	0.0275	0.0375

**Figure 10. Marking**

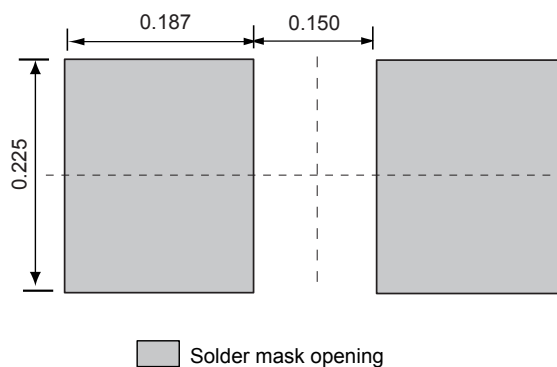

**Note:** The marking can be rotated by multiples of 90° to differentiate assembly location.

**Figure 11. Tape and reel specification (in mm)**


## 3 Recommendation on PCB assembly

### 3.1 Footprint

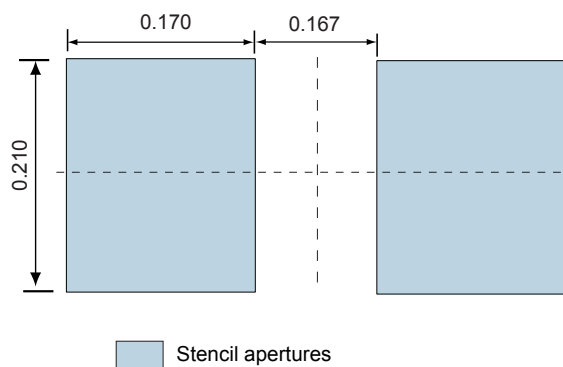
**Figure 12. Recommended footprint in mm**



### 3.2 Stencil opening design

1. Reference design
  - a. Stencil opening thickness: 75  $\mu\text{m}$  / 3 mils

**Figure 13. Recommended stencil window position in mm**



### 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38  $\mu\text{m}$ .

### 3.4 Placement

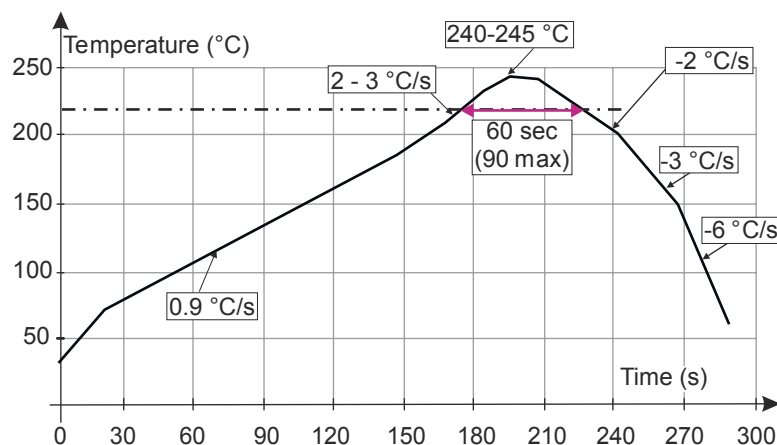
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.6 Reflow profile

**Figure 14. ST ECOPACK recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 4 Ordering information

Figure 15. Ordering information scheme

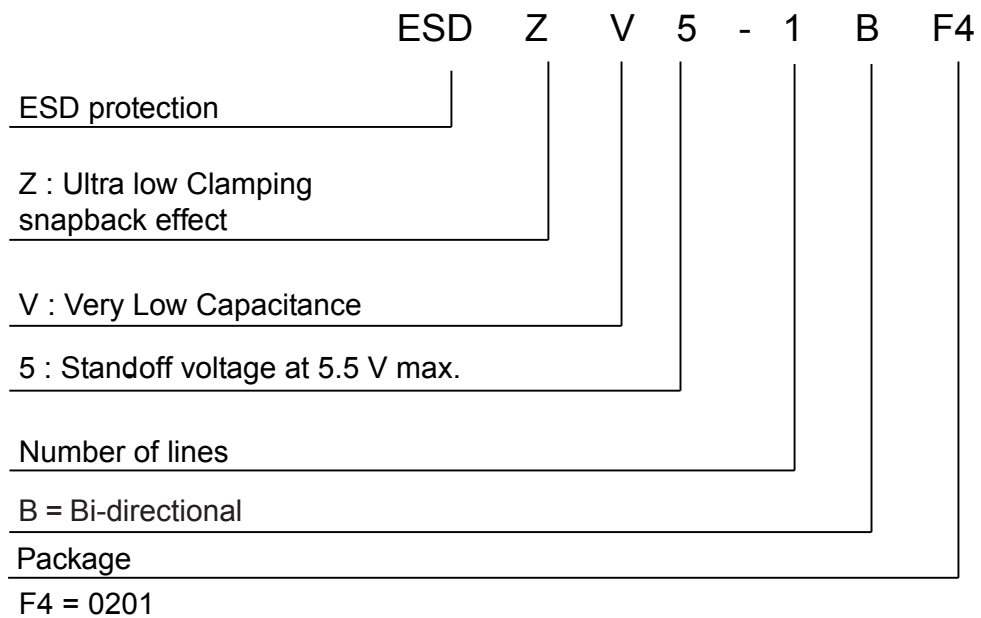


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDZV5-1BF4	A <sup>(1)</sup>	0201	0.116 mg	15000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location



## Revision history

**Table 5. Document revision history**

Date	Revision	Changes
06-Apr-2017	1	First issue.
28-Jul-2017	2	Updated footprint title.
19-Jan-2022	3	Updated <a href="#">Figure 12</a> . Minor text changes.

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