MOSFET - Power, 4.4 Amps, 20 Volts

P−Channel TSOP−6

NTGS3443, NVGS3443

Features

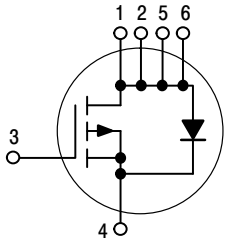
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP−6 Surface Mount Package
- These Devices are Pb−Free and are RoHS Compliant
- NVGS Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

4.4 AMPERES
20 VOLTS
$R_{DS(on)}$ = 65 mΩ

P−Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

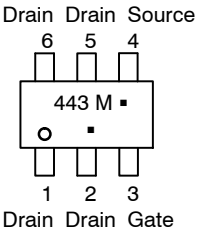
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	Volts
Gate−to−Source Voltage − Continuous	V_{GS}	±12	Volts
Thermal Resistance Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (T_p < 10 μS)	$R_{\theta JA}$ P_d I_D I_{DM}	244 0.5 −2.2 −10	°C/W Watts Amps Amps
Thermal Resistance Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (T_p < 10 μS)	$R_{\theta JA}$ P_d I_D I_{DM}	128 1.0 −3.1 −14	°C/W Watts Amps Amps
Thermal Resistance Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (T_p < 10 μS)	$R_{\theta JA}$ P_d I_D I_{DM}	62.5 2.0 −4.4 −20	°C/W Watts Amps Amps
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR−4 or G−10 PCB, operating to steady state.
2. Mounted onto a 2 in square FR−4 board (1 in sq, 2 oz. Cu. 0.06″ thick single sided), operating to steady state.
3. Mounted onto a 2 in square FR−4 board (1 in sq, 2 oz. Cu. 0.06″ thick single sided), t < 5.0 seconds.

MARKING DIAGRAM & PIN ASSIGNMENT

TSOP−6
CASE 318G
STYLE 1



443 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3443T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NVGS3443T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Notes 4 & 5)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −10 μA)		$V_{(BR)DSS}$	−20	–	–	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −20 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = −20 Vdc, T_J = 70°C)		I_{DSS}	– –	– –	−1.0 −5.0	μAdc
Gate−Body Leakage Current (V_{GS} = −12 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	−100	nAdc
Gate−Body Leakage Current (V_{GS} = +12 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc)		$V_{GS(th)}$	−0.60	−0.95	−1.50	Vdc
Static Drain−Source On−State Resistance (V_{GS} = −4.5 Vdc, I_D = −4.4 Adc) (V_{GS} = −2.7 Vdc, I_D = −3.7 Adc) (V_{GS} = −2.5 Vdc, I_D = −3.5 Adc)		$R_{DS(on)}$	– – –	0.058 0.082 0.092	0.065 0.090 0.100	Ω
Forward Transconductance (V_{DS} = −10 Vdc, I_D = −4.4 Adc)		g_{FS}	–	8.8	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −5.0 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	565	–	pF
Output Capacitance		C_{oss}	–	320	–	pF
Reverse Transfer Capacitance		C_{rss}	–	120	–	pF
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	(V_{DD} = −20 Vdc, I_D = −1.0 Adc, V_{GS} = −4.5 Vdc, R_g = 6.0 Ω)	$t_{d(on)}$	–	10	25	ns
Rise Time		t_r	–	18	45	ns
Turn−Off Delay Time		$t_{d(off)}$	–	30	50	ns
Fall Time		t_f	–	31	50	ns
Total Gate Charge	(V_{DS} = −10 Vdc, V_{GS} = −4.5 Vdc, I_D = −4.4 Adc)	Q_{tot}	–	7.5	15	nC
Gate−Source Charge		Q_{gs}	–	1.4	–	nC
Gate−Drain Charge		Q_{gd}	–	2.9	–	nC
BODY−DRAIN DIODE RATINGS						
Diode Forward On−Voltage	(I_S = −1.7 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	−0.83	−1.2	Vdc
Reverse Recovery Time	(I_S = −1.7 Adc, dI_S/dt = 100 A/μs)	t_{rr}	–	30	–	ns

4. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.
5. Handling precautions to protect against electrostatic discharge are mandatory.

TYPICAL ELECTRICAL CHARACTERISTICS

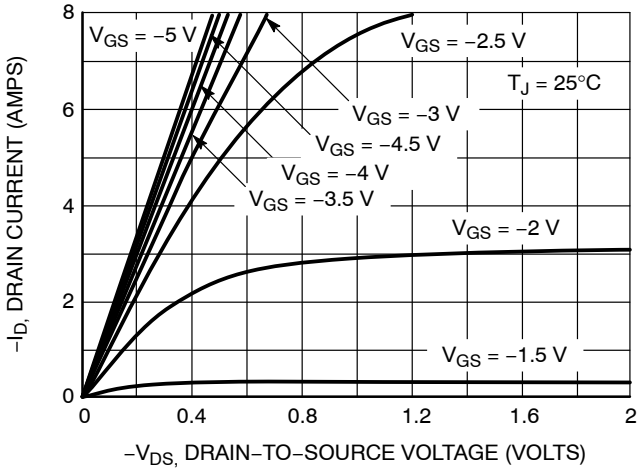


Figure 1. On−Region Characteristics

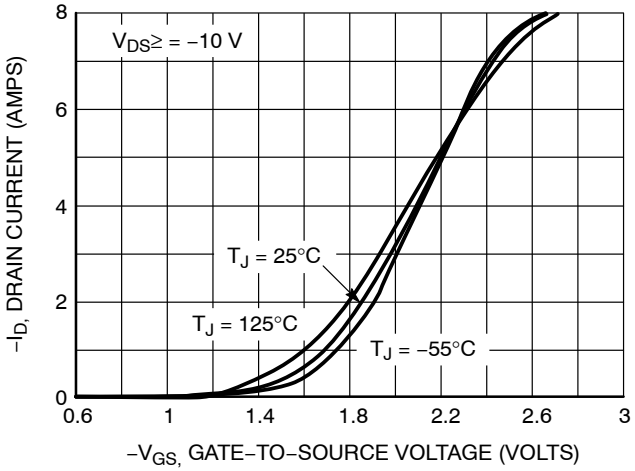


Figure 2. Transfer Characteristics

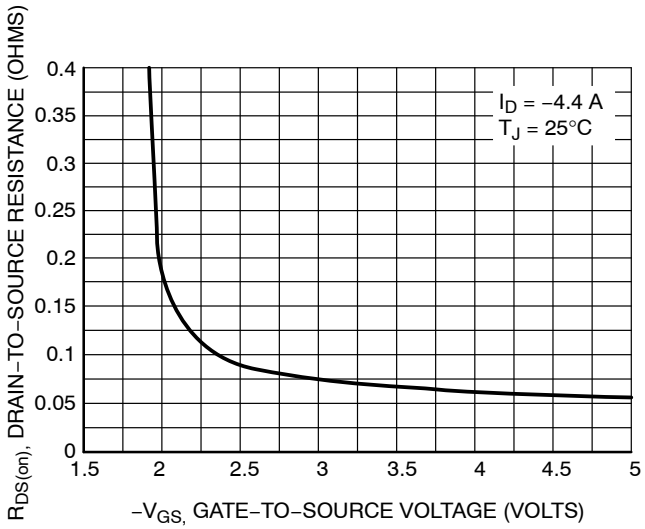


Figure 3. On−Resistance vs. Gate−to−Source Voltage

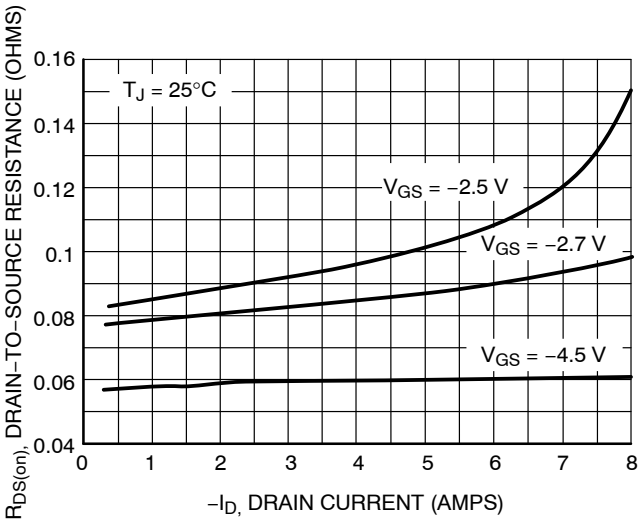


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

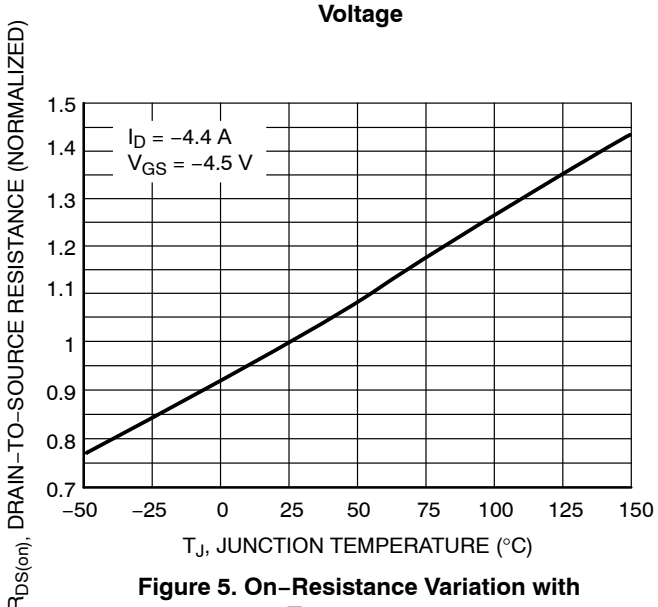


Figure 5. On−Resistance Variation with Temperature

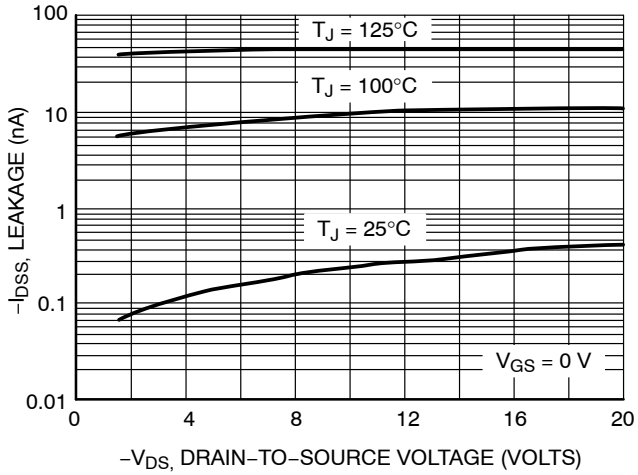


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

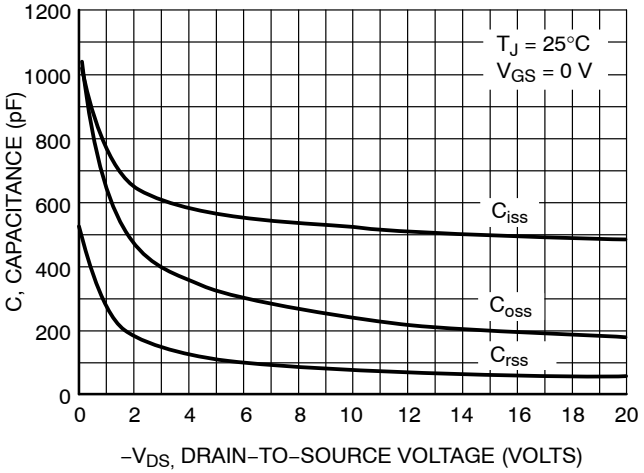


Figure 7. Capacitance Variation

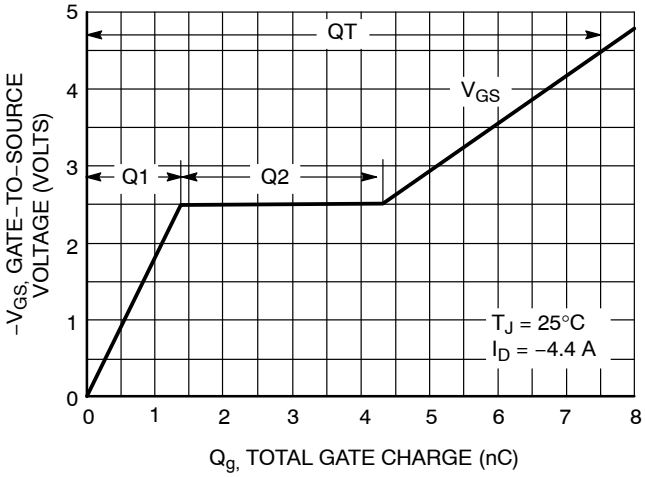


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

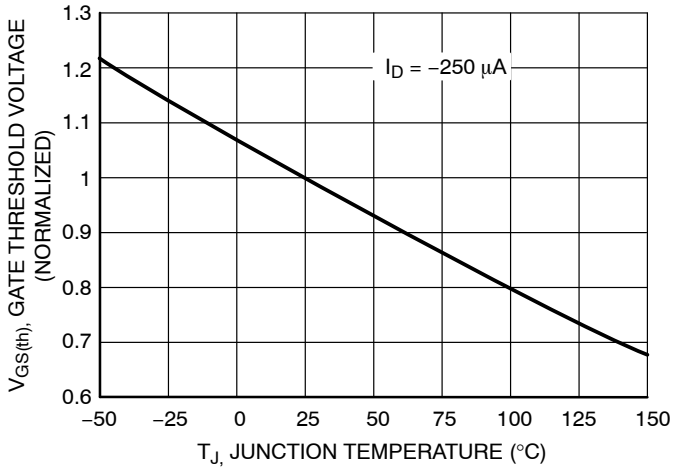


Figure 9. Gate Threshold Voltage Variation with Temperature

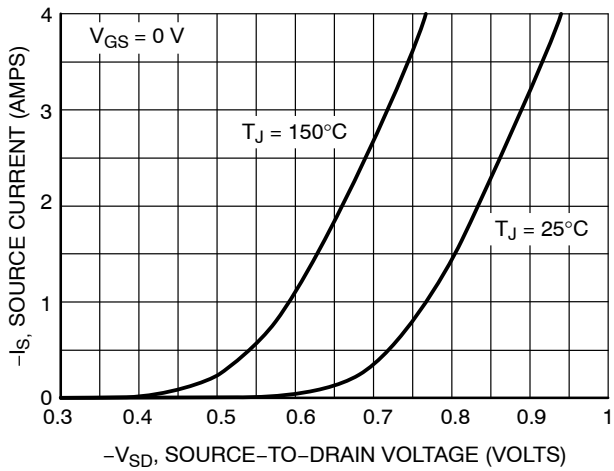


Figure 10. Diode Forward Voltage vs. Current

TYPICAL ELECTRICAL CHARACTERISTICS

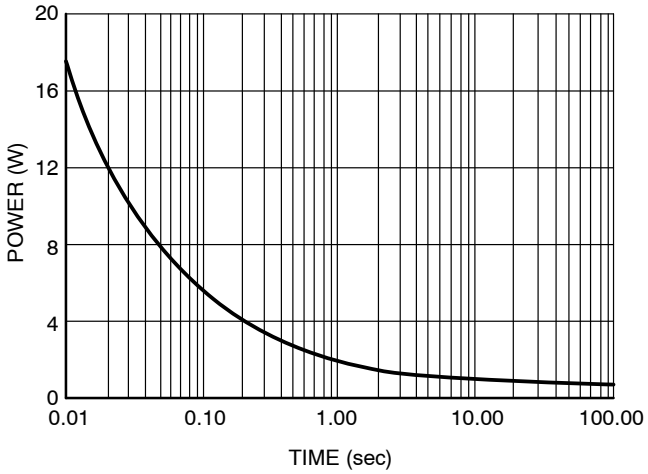


Figure 11. Single Pulse Power

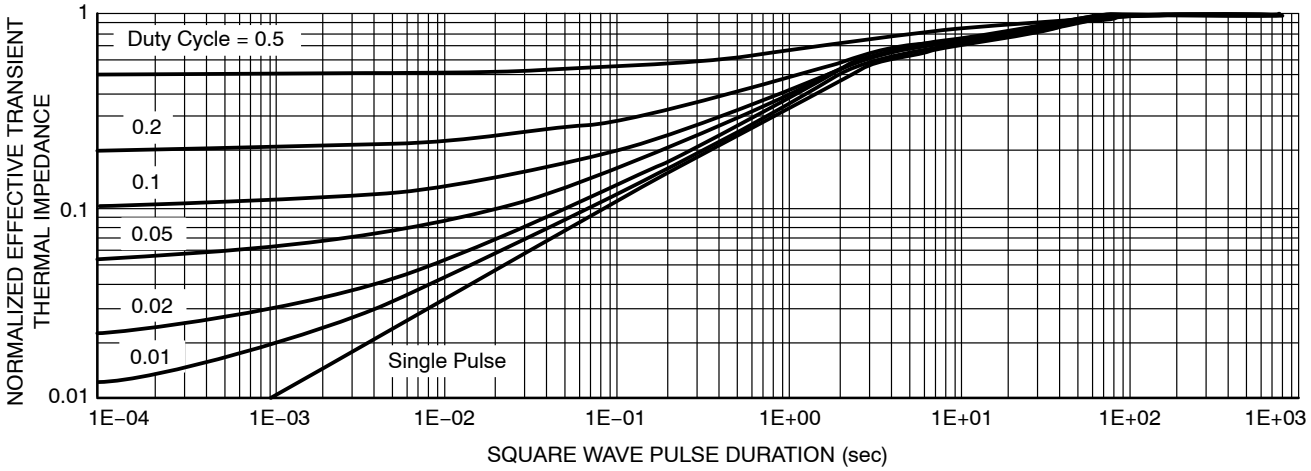
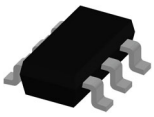
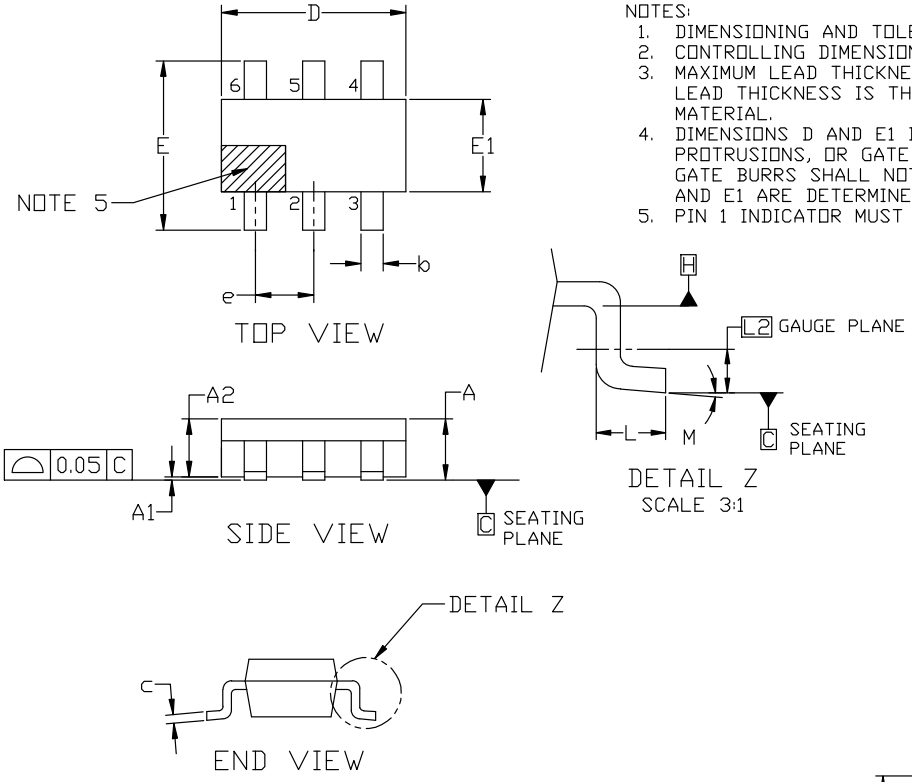


Figure 12. Normalized Thermal Transient Impedance, Junction−to−Ambient



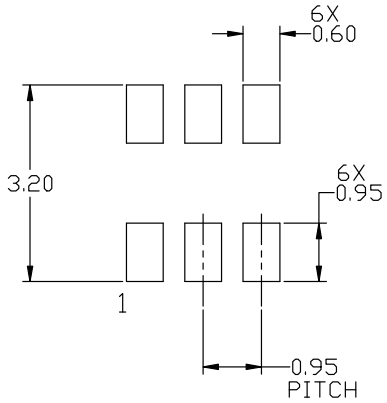
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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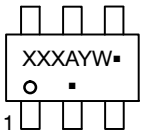
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

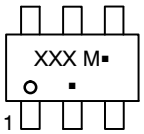
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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