10MHz to 12GHz Low Noise Amplifier with 10MHz to 14GHz Bypass Switches

FEATURES

- Wideband amplifier with multiple bypass modes
- 4 pin-selectable operating modes
  - Internal amplifier mode operating from 10MHz to 12GHz
  - Internal bypass mode operating from 10MHz to 14GHz
  - Two external bypass modes from 10MHz to 14GHz
- Integrated power-supply decoupling
- Reflective bypass switches
- In internal amplifier mode
  - Small signal gain: 14.0dB typical from 200MHz to 6GHz
  - OP1dB: 20.5dBm typical from 200MHz to 6GHz
  - OIP3: 35.5dBm typical from 200MHz to 6GHz
  - OIP2: 44.6dBm typical from 9GHz to 12GHz
  - Noise figure: 3.8dB typical from 200MHz to 6GHz
- In internal bypass switch mode
  - Insertion loss: 2.2dB typical from 200MHz to 6GHz
- Operating temperature range: −40°C to +85°C
- RoHS-compliant, 6mm × 6mm, 28-terminal LGA

APPLICATIONS

- Electronic test and measurement equipment
- Electronic warfare
- Wireless receivers

FUNCTIONAL BLOCK DIAGRAM

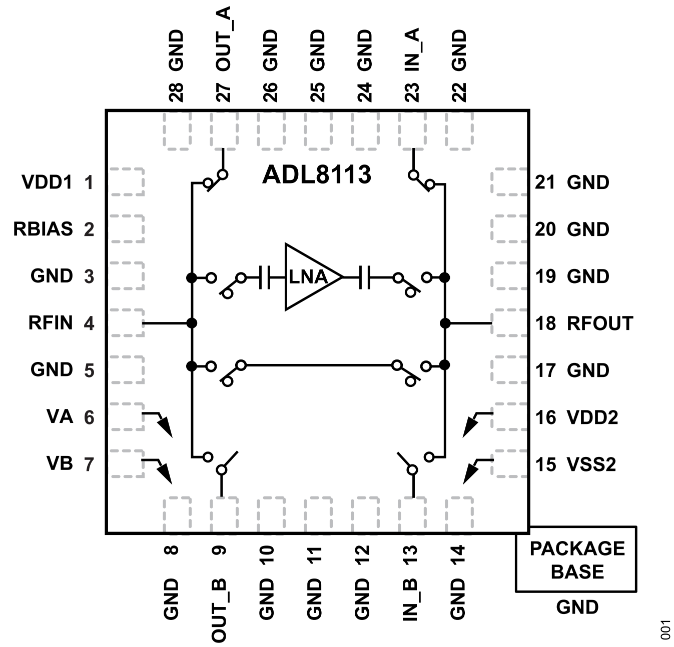

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADL8113 is a low noise amplifier (LNA) with bypass switches that provides broadband operation from 10MHz to 12GHz. The ADL8113 provides a low noise figure of 3.8dB and an output third-order intercept point (OIP3) of 35.5dBm from 200MHz to 6GHz. The ADL8113 provides a small signal gain of 14.0dB that is stable over frequency, temperature, power supply, and from device to device.

The integration of an amplifier and two SP4T reflective switches allows multiple paths through the device. The addition of switches also offers a high input third-order intercept (IIP3) path when large input signals are present. With the integration of power-supply decoupling capacitors, minimal external power-supply decoupling is required.

The ADL8113 is fully specified for operation across a temperature range of −40°C to +85°C. The ADL8113 is available in a 6mm × 6mm, 28-terminal land grid array (LGA) package.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

3/2025—Revision 0: Initial Version

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SPECIFICATIONS

0.01GHz TO 200MHz FREQUENCY RANGE

Amplifier drain bias voltage (V_{DD1}) = +5V, quiescent drain supply current (I_{DQ}) = 110mA, switch negative bias voltage (V_{SS2}) = −3.3V, switch positive supply voltage (V_{DD2}) = +3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 0.01GHz to 200MHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.01		200	MHz
INTERNAL AMPLIFIER MODE					
Small Signal Gain		12.5	14.5		dB
Gain Flatness			±0.5		dB
Input Return Loss (S11)			12.4		dB
Output Return Loss (S22)			11.5		dB
Output 1dB Compression (OP1dB)		17.5	19.5		dBm
Output Third-Order Intercept (OIP3)	Measurement taken at output power (P_{OUT}) per tone = 5dBm		37.7		dBm
Output Second-Order Intercept (OIP2)	Measurement taken at P_{OUT} per tone = 5dBm		48.2		dBm
Noise Figure			7		dB
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			1.8		dB
S11			19		dB
S22			19		dB
Input P1dB Compression (IP1dB)			28		dBm
Input P0.1dB Compression (IP0.1dB)			27.5		dBm
Input Third-Order Intercept (IIP3)	Measurement taken at input power (P_{IN}) per tone = 14dBm		50		dBm
EXTERNAL BYPASS A MODE					
Insertion Loss	RFIN to OUT_A or IN_A to RFOUT		0.9		dB
S11	Looking into RFIN		24		dB
	Looking into IN_A		24		dB
	Looking into IN_B		1		dB
S22	Looking into RFOUT		24		dB
	Looking into OUT_A		24		dB
	Looking into OUT_B		1		dB
IP1dB	RFIN to OUT_A or IN_A to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_A or IN_A to RFOUT		27.5		dBm
IIP3	RFIN to OUT_A or IN_A to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS B MODE					
Insertion Loss	RFIN to OUT_B or IN_B to RFOUT		0.9		dB
S11	Looking into RFIN		24		dB
	Looking into IN_A		1		dB
	Looking into IN_B		24		dB
S22	Looking into RFOUT		24		dB
	Looking into OUT_A		1		dB
	Looking into OUT_B		24		dB
IP1dB	RFIN to OUT_B or IN_B to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_B or IN_B to RFOUT		27.5		dBm

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SPECIFICATIONS

Table 1. 0.01GHz to 200MHz Frequency Range Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IIP3	RFIN to OUT_B or IN_B to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm

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SPECIFICATIONS

200MHz TO 6GHz FREQUENCY RANGE

V_{DD1} = +5V, I_{DQ} = 110mA, V_{SS2} = −3.3V, V_{DD2} = +3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 200MHz to 6GHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		0.200		6	GHz
INTERNAL AMPLIFIER MODE					
Small Signal Gain		12.0	14.0		dB
Gain Flatness			±0.25		dB
S11			15		dB
S22			17		dB
OP1dB		18.5	20.5		dBm
OIP3	Measurement taken at P_{OUT} per tone = 5dBm		35.5		dBm
OIP2	Measurement taken at P_{OUT} per tone = 5dBm		41.7		dBm
Noise Figure			3.8		dB
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			2.2		dB
S11			21		dB
S22			23		dB
IIP3	Measurement taken at P_{IN} per tone = 14dBm		50		dBm
IP0.1dB			27.5		dBm
IP1dB			28		dBm
EXTERNAL BYPASS A MODE					
Insertion Loss	RFIN to OUT_A or IN_A to RFOUT		1.2		dB
S11	Looking into RFIN		23.5		dB
	Looking into IN_A		23.5		dB
	Looking into IN_B		1.5		dB
S22	Looking into RFOUT		25		dB
	Looking into OUT_A		25		dB
	Looking into OUT_B		1.5		dB
IP0.1dB	Looking into RFIN to OUT_A or IN_A to RFOUT		27.5		dBm
IP1dB	Looking into RFIN to OUT_A or IN_A to RFOUT		28		dBm
IIP3	Looking into RFIN to OUT_A or IN_A to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS B MODE					
Insertion Loss	RFIN to OUT_B or IN_B to RFOUT		1.2		dB
S11	Looking into RFIN		23.5		dB
	Looking into IN_A		1.5		dB
	Looking into IN_B		23.5		dB
S22	Looking into RFOUT		25		dB
	Looking into OUT_A		1.5		dB
	Looking into OUT_B		25		dB
IP0.1dB	RFIN to OUT_B or IN_B to RFOUT		27.5		dBm
IP1dB	RFIN to OUT_B or IN_B to RFOUT		28		dBm

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SPECIFICATIONS

Table 2. 200MHz to 6GHz Frequency Range Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IIP3	Looking into RFIN to OUT_B or IN_B to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm

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SPECIFICATIONS

6GHz TO 9GHz FREQUENCY RANGE

V_{DD1}= +5V, I_{DQ} = 110mA, V_{SS2} = −3.3V, V_{DD2} = +3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 6GHz to 9GHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		6		9	GHz
INTERNAL AMPLIFIER MODE					
Small Signal Gain		11.9	13.9		dB
Gain Flatness			±0.1		dB
S11			13.6		dB
S22			24		dB
OP1dB		16.8	18.8		dBm
OIP3	Measurement taken at P_{OUT} per tone = 5dBm		31.7		dBm
OIP2	Measurement taken at P_{OUT} per tone = 5dBm		41		dBm
Noise Figure			3.9		dB
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			2.6		dB
S11			19.8		dB
S22			24.7		dB
IP1dB			28		dBm
IP0.1dB			27.5		dBm
IIP3	Measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS A MODE					
Insertion Loss	RFIN to OUT_A or IN_A to RFOUT		1.5		dB
S11	Looking into RFIN		22.7		dB
	Looking into IN_A		22.7		dB
	Looking into IN_B		2.5		dB
S22	Looking into RFOUT		25.5		dB
	Looking into OUT_A		25.5		dB
	Looking into OUT_B		2.5		dB
IP1dB	RFIN to OUT_A or IN_A to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_A or IN_A to RFOUT		27.5		dBm
IIP3	RFIN to OUT_A or IN_A to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS B MODE					
Insertion Loss	RFIN to OUT_B or IN_B to RFOUT		1.5		dB
S11	Looking into RFIN		22.7		dB
	Looking into IN_A		2.5		dB
	Looking into IN_B		22.7		dB
S22	Looking into RFOUT		25.5		dB
	Looking into OUT_A		2.5		dB
	Looking into OUT_B		22.7		dB
IP1dB	RFIN to OUT_B or IN_B to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_B or IN_B to RFOUT		27.5		dBm

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SPECIFICATIONS

Table 3. 6GHz to 9GHz Frequency Range Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IIP3	RFIN to OUT_B or IN_B to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm

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SPECIFICATIONS

9GHz TO 12GHz FREQUENCY RANGE

V_{DD1} = +5V, I_{DQ} = 110mA, V_{SS2} = −3.3V, V_{DD2} = +3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 4. 9GHz to 12GHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		9		12	GHz
INTERNAL AMPLIFIER MODE					
Small Signal Gain		11.7	13.7		dB
Gain Flatness			±0.3		dB
S11			18.5		dB
S22			25		dB
OP1dB		13.8	15.8		dBm
OIP3	Measurement taken at P_{OUT} per tone = 5dBm		30.7		dBm
OIP2	Measurement taken at P_{OUT} per tone = 5dBm		44.6		dBm
Noise Figure			4.6		dB
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			2.8		dB
S11			19.2		dB
S22			24.2		dB
IP1dB			28		dBm
IP0.1dB			27.5		dBm
IIP3	Measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS A MODE					
Insertion Loss	RFIN to OUT_A or IN_A to RFOUT		1.6		dB
S11	Looking into RFIN		23.2		dB
	Looking into IN_A		23.2		dB
	Looking into IN_B		3		dB
S22	Looking into RFOUT		24.4		dB
	Looking into OUT_A		24.4		dB
	Looking into OUT_B		3		dB
IP1dB	RFIN to OUT_A or IN_A to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_A or IN_A to RFOUT		27.5		dBm
IIP3	RFIN to OUT_A or IN_A to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS B MODE					
Insertion Loss	RFIN to OUT_B or IN_B to RFOUT		1.6		dB
S11	Looking into RFIN		23.2		dB
	Looking into IN_A		3		dB
	Looking into IN_B		23.2		dB
S22	Looking into RFOUT		24.4		dB
	Looking into OUT_A		3		dB
	Looking into OUT_B		24.4		dB
IP1dB	RFIN to OUT_B or IN_B to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_B or IN_B to RFOUT		27.5		dBm

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SPECIFICATIONS

Table 4. 9GHz to 12GHz Frequency Range Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IIP3	RFIN to OUT_B or IN_B to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm

12GHz TO 14GHz FREQUENCY RANGE

V_{SS2} = −3.3V, V_{DD2} = +3.3V, and T_{CASE} = 25°C, unless otherwise noted.

Table 5. 12GHz to 14GHz Frequency Range Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		12		14	GHz
INTERNAL BYPASS SWITCH MODE					
Insertion Loss			3.1		dB
S11			17.6		dB
S22			20.4		dB
IP1dB			28		dBm
IP0.1dB			27.5		dBm
IIP3	Measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS A MODE					
Insertion Loss	RFIN to OUT_A or IN_A to RFOUT		1.8		dB
S11	Looking into RFIN		20.8		dB
	Looking into IN_A		20.8		dB
	Looking into IN_B		3		dB
S22	Looking into RFOUT		22.4		dB
	Looking into OUT_A		22.4		dB
	Looking into OUT_B		3		dB
IP1dB	RFIN to OUT_A or IN_A to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_A or IN_A to RFOUT		27.5		dBm
IIP3	RFIN to OUT_A or IN_A to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm
EXTERNAL BYPASS B MODE					
Insertion Loss	RFIN to OUT_B or IN_B to RFOUT		1.8		dB
S11	Looking into RFIN		18.6		dB
	Looking into IN_A		3		dB
	Looking into IN_B		18.6		dB
S22	Looking into RFOUT		20.9		dB
	Looking into OUT_A		3		dB
	Looking into OUT_B		20.9		dB
IP1dB	RFIN to OUT_B or IN_B to RFOUT		28		dBm
IP0.1dB	RFIN to OUT_B or IN_B to RFOUT		27.5		dBm
IIP3	RFIN to OUT_B or IN_B to RFOUT; measurement taken at P_{IN} per tone = 14dBm		50		dBm

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SPECIFICATIONS

DC SPECIFICATIONS

Table 6. Power Supplies

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE				
V_{DD1}	3.0	5.0	6.0	V
V_{DD2}	3.0	3.3	3.6	V
V_{SS2}	−3.6	−3.3	−3.0	V
SUPPLY CURRENT				
Total Current (I_{DQ}) at 5V		110		mA
Amplifier Current (I_{DQ_AMP})		105		mA
RBIAS Current (I_{RBIAS})		5		mA
Switch Positive Bias Current (I_{DD2})		4		μA
Switch Negative Bias Current (I_{SS2})		−200		μA

Table 7. Logic Control Voltage (VA and VB)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS					
Low	<1μA typical current	0		0.8	V
High	<35μA typical current	1.2		V_{DD2}	V
SWITCHING CHARACTERISTICS					
Internal Amplifier Mode					
Rise (t_{RISE}) Time and Fall Time (t_{FALL})	10% to 90% of RF output		3		ns
On Time (t_{ON}) and Off Time (t_{OFF})	50% control voltage (VA or VB) to 90% of RF output		17		ns
Internal Bypass Mode					
t_{RISE} and t_{FALL}	10% to 90% of RF output		4		ns
t_{ON} and t_{OFF}	50% control voltage (VA or VB) to 90% of RF output		16		ns
External Bypass A and External Bypass B Modes					
t_{RISE} and t_{FALL}	10% to 90% of RF output		3		ns
t_{ON} and t_{OFF}	50% control voltage (VA or VB) to 90% of RF output		16		ns
RF SETTLING TIME					
Internal Amplifier Mode					
0.1dB	50% VA or VB to 0.1dB of final RF output		45		μs
0.05dB	50% VA or VB to 0.05dB of final RF output		125		μs
Internal Bypass Mode					
0.1dB	50% VA or VB to 0.1dB of final RF output		50		ns
0.05dB	50% VA or VB to 0.05dB of final RF output		60		ns
External Bypass A and External Bypass B Modes					
0.1dB	50% VA or VB to 0.1dB of final RF output		50		ns
0.05dB	50% VA or VB to 0.05dB of final RF output		60		ns

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ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD1}	7V
V_{DD2}	−0.3V to +3.6V
V_{SS2}	−3.6V to +0.3V
Control Voltage (VA and VB) Range	−0.3V to V_{DD2} + 0.3V
RF Input Power (RFIN)	
Internal Amplifier Mode	31dBm
Internal and External Bypass Mode (Derate at Lower Frequencies, According to Figure 2)	27.5dBm
Hot Switch Power Level	
External and Internal Switch Mode	27.5dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 85°C, Derate 11.1mW/°C Above 85°C)	1W
Temperature Range	
Storage	−40°C to +125°C
Operating	−40°C to +85°C
Nominal Channel (T_{CASE} = 85°C, V_{DD} = 5V, I_{DQ} = 110mA, P_{IN} = Off)	134.5°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance (channel to exposed metal ground paddle/pad on the underside of the device).

Table 9. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-28-4		
Worst Case, T_{CASE} = 85°C[1]	90	°C/W

[1] Across all specified conditions.

RF INPUT POWER DERATING CURVE

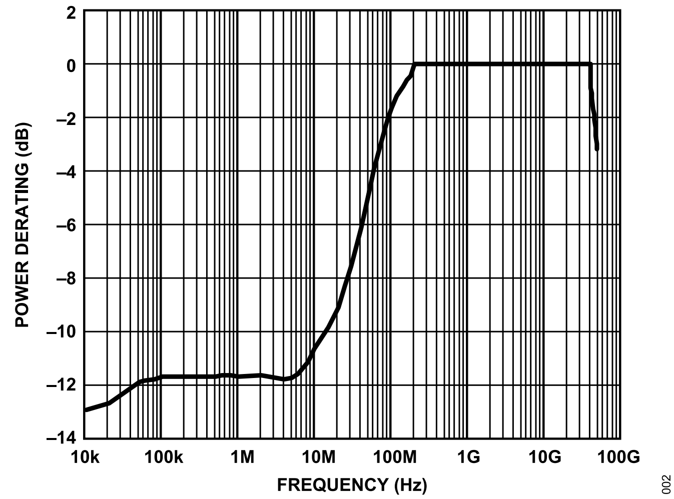


Figure 2. RF Input Power Derating Curve

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

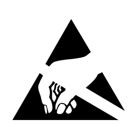
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8113

Table 10. ADL8113, 28-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

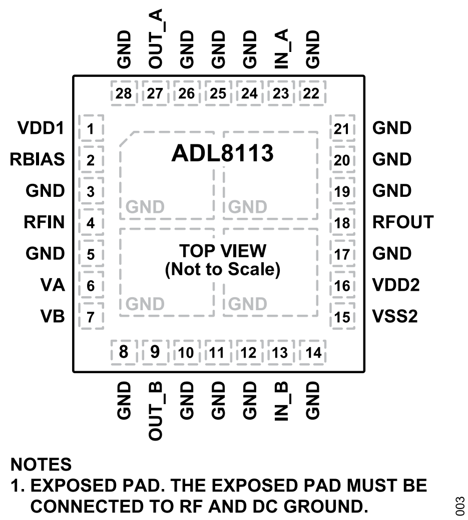

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD1	Amplifier Drain Bias Voltage. See Figure 4 for the interface schematic.
2	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD1 to set I_{DQ}. See Figure 5 for the interface schematic.
3, 5, 8, 10 to 12, 14, 17, 19 to 22, 24 to 26, 28	GND	RF and DC Ground. See Figure 6 for the interface schematic.
4	RFIN	RF Input. The RFIN pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0V DC. See Figure 7 for the interface schematic.
6, 7	VA , VB	Switch Control Inputs. See Figure 8 and Figure 9 for the interface schematics.
9, 13	OUT_B, IN_B	External Bypass Path B. The OUT_B and IN_B pins are DC-coupled and matched to 50Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0V DC. See Figure 7 for the interface schematic.
15	VSS2	Switch Negative Bias Voltage.
16	VDD2	Switch Positive Bias Voltage.
18	RFOUT	RF Output. The RFOUT pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0V DC. See Figure 7 for the interface schematic
23, 27	IN_A, OUT_A	External Bypass Path A. The IN_A and OUT_A pins are DC-coupled and matched to 50Ω. A DC blocking capacitor is required if the RF line potential is not equal to 0V DC. See Figure 7 for the interface schematic.
	EPAD	Exposed Ground Pad. The exposed pad must be connected to RF and DC ground.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

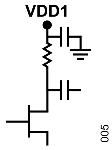

Figure 4. VDD1 Interface Schematic

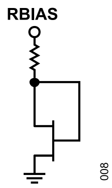

Figure 5. RBIAS Interface Schematic

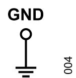

Figure 6. GND Interface Schematic

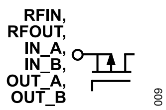

Figure 7. RFIN, RFOUT, IN_A, IN_B, OUT_A and OUT_B Interface Schematic

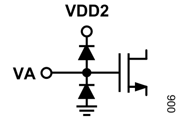

Figure 8. VA Interface Schematic

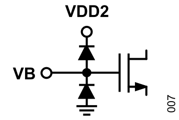

Figure 9. VB Interface Schematic

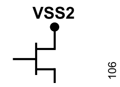

Figure 10. VSS2 Interface Schematic

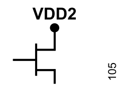

Figure 11. VDD2 Interface Schematic

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INTERNAL AMPLIFIER MODE

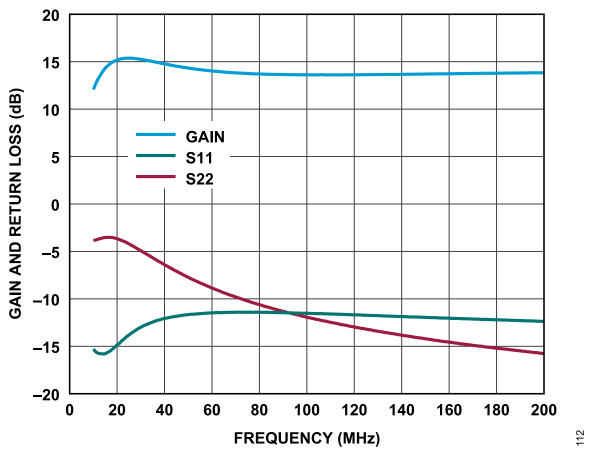

Figure 12. Gain and Return Loss vs. Frequency, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

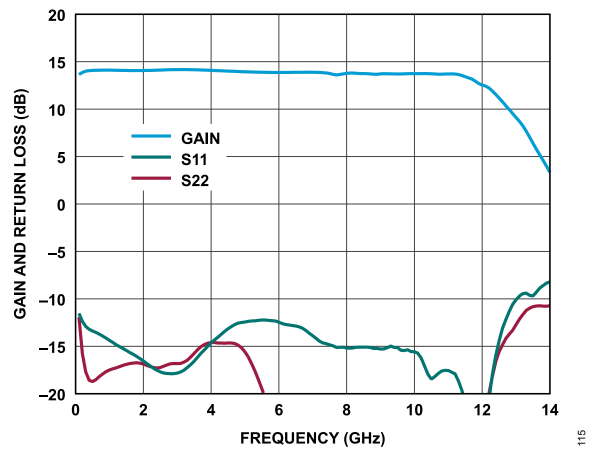

Figure 15. Gain and Return Loss vs. Frequency, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

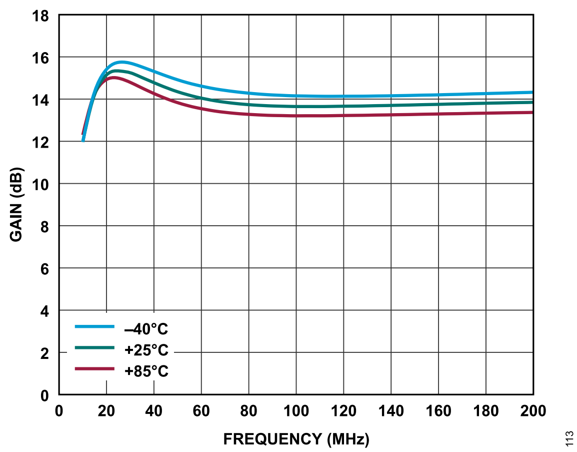

Figure 13. Gain vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

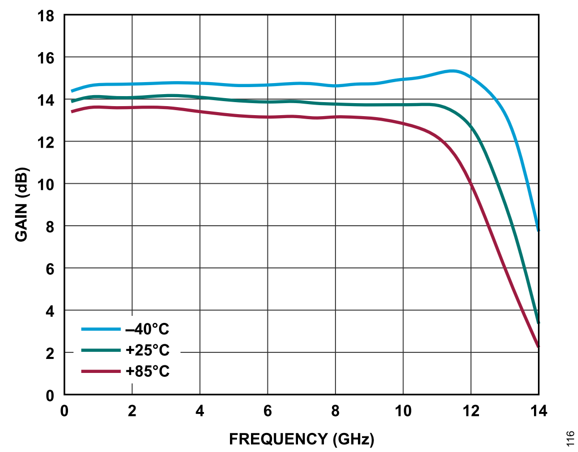

Figure 16. Gain vs. Frequency for Various Temperatures, I_{DQ} = 110mA, 200MHz to 14GHz

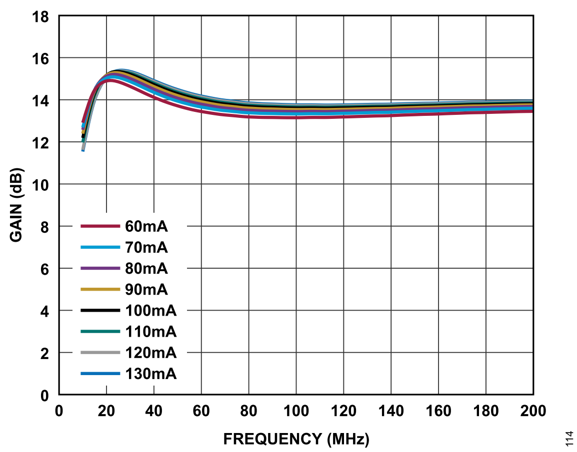

Figure 14. Gain vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

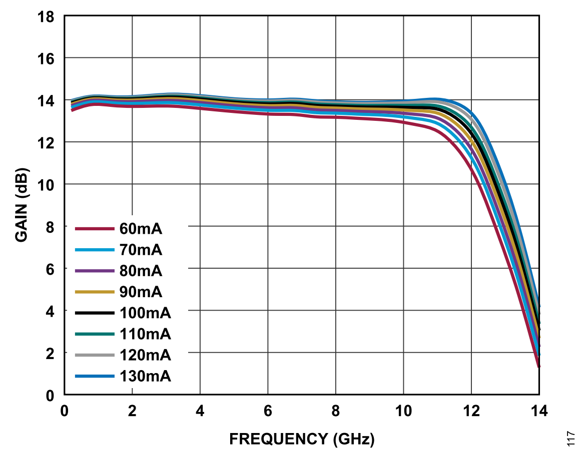

Figure 17. Gain vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

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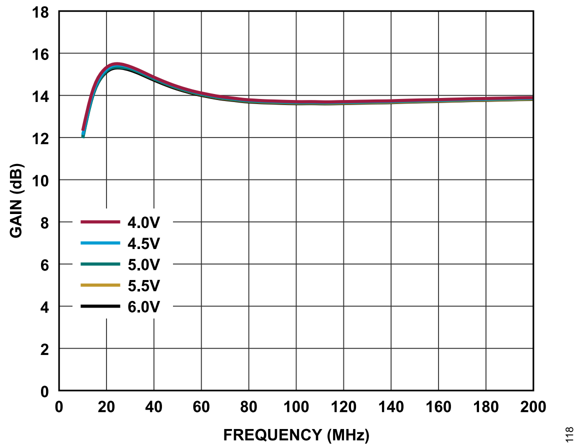

Figure 18. Gain vs. Frequency for Various Supply Voltages, 10MHz to 200 MHz, V_{DD} = 5V, I_{DQ} = 110mA

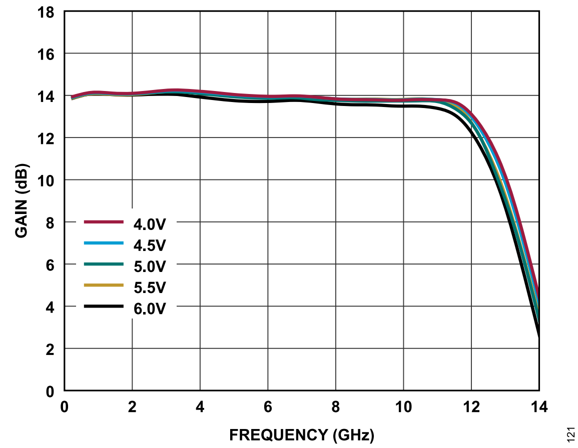

Figure 21. Gain vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

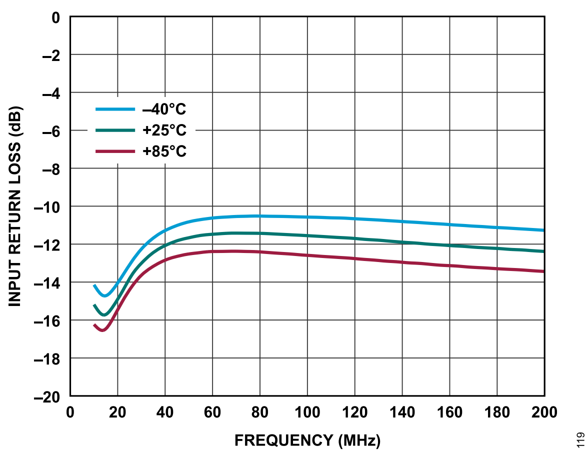

Figure 19. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

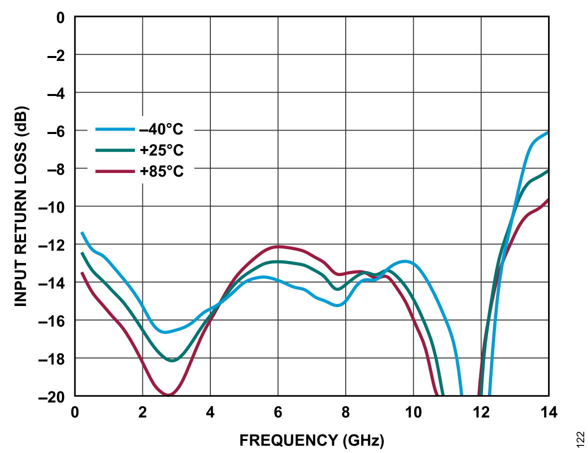

Figure 22. Input Return Loss vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

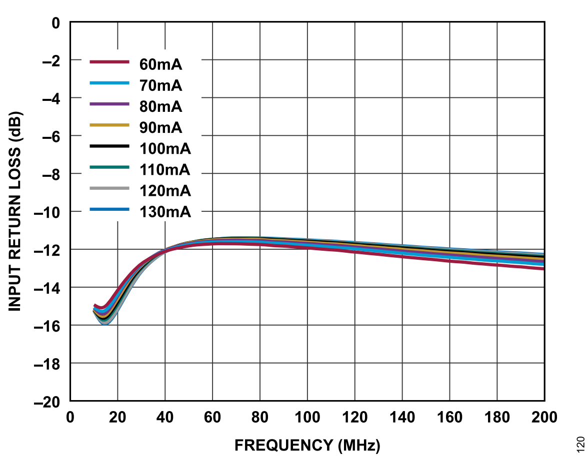

Figure 20. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

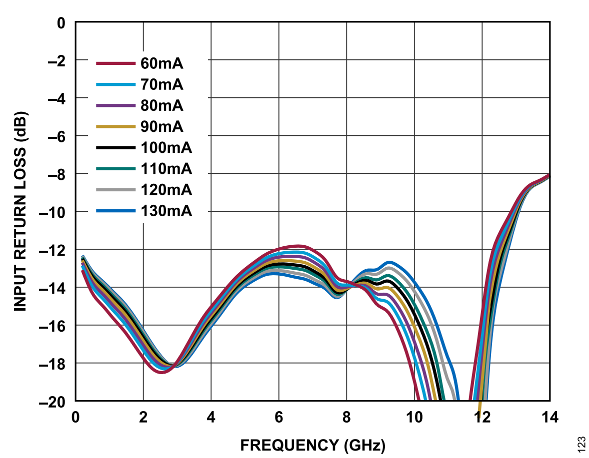

Figure 23. Input Return Loss vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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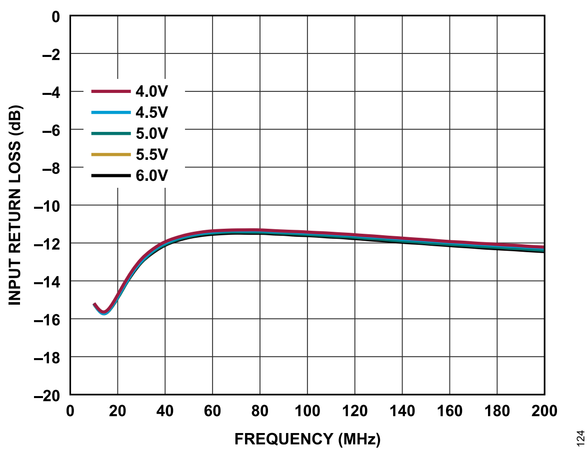

Figure 24. Input Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

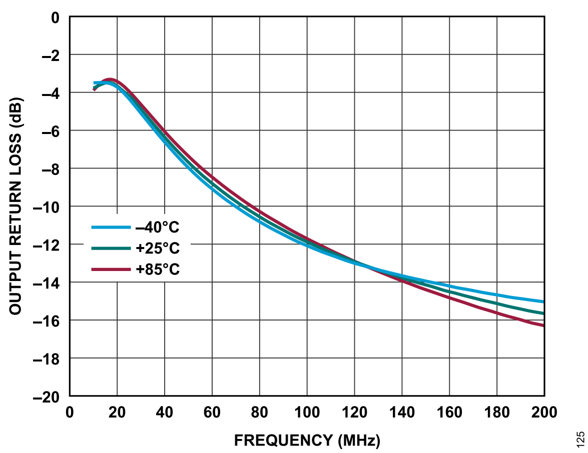

Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

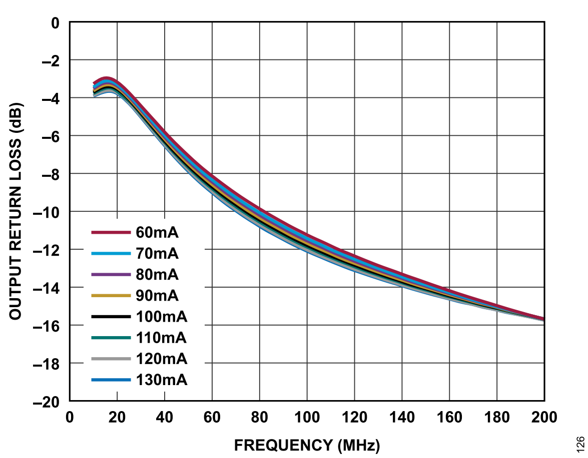

Figure 26. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

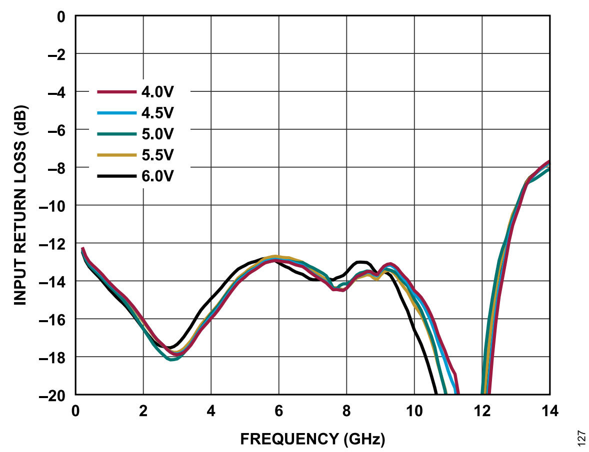

Figure 27. Input Return Loss vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

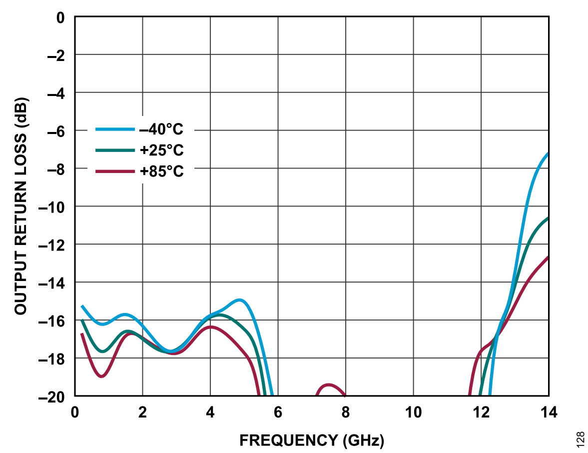

Figure 28. Output Return Loss vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

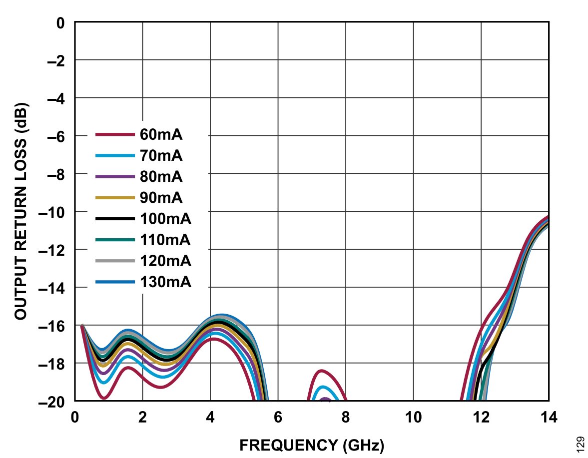

Figure 29. Output Return Loss vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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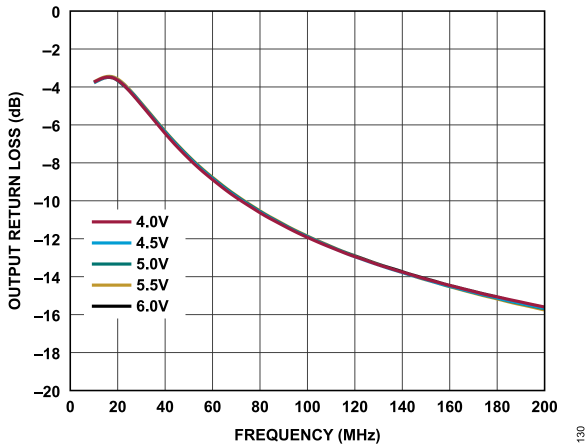

Figure 30. Output Return Loss vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

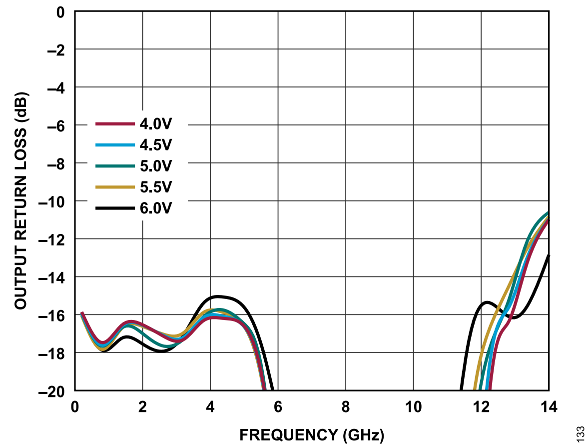

Figure 33. Output Return Loss vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

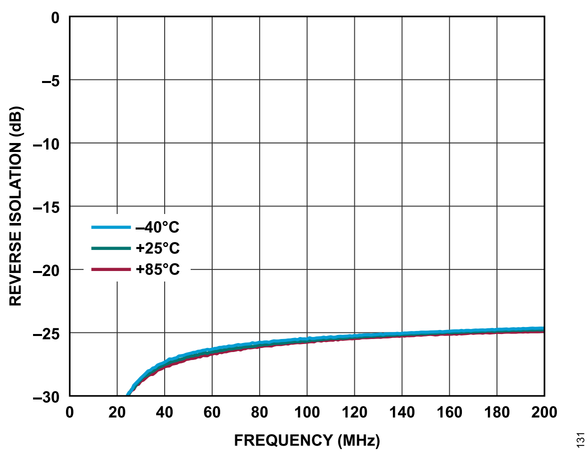

Figure 31. Reverse Isolation vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

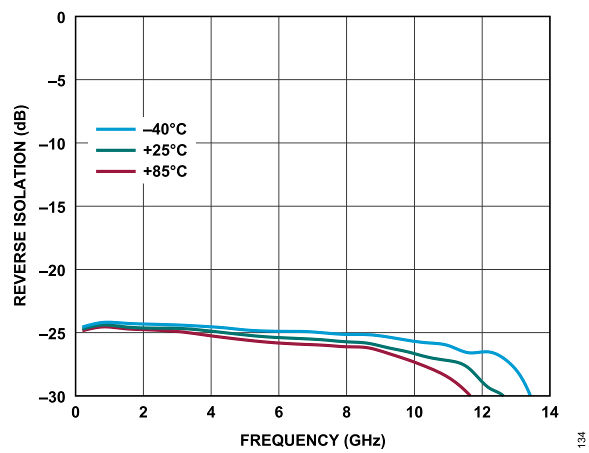

Figure 34. Reverse Isolation vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

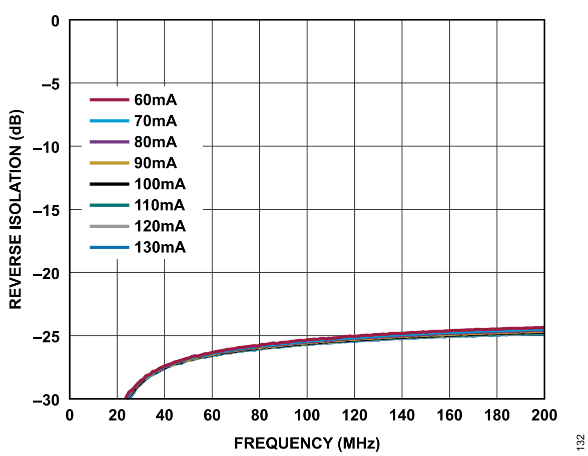

Figure 32. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

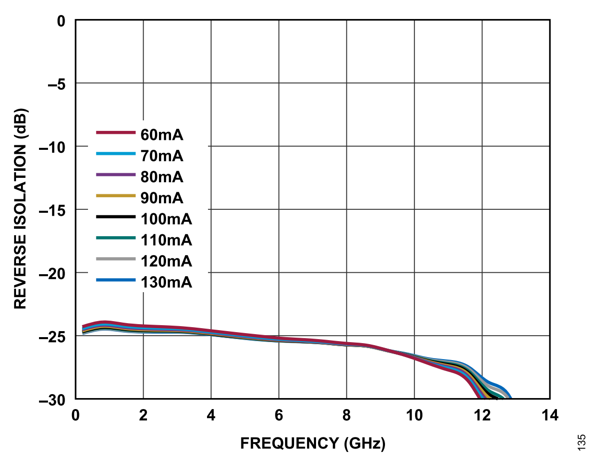

Figure 35. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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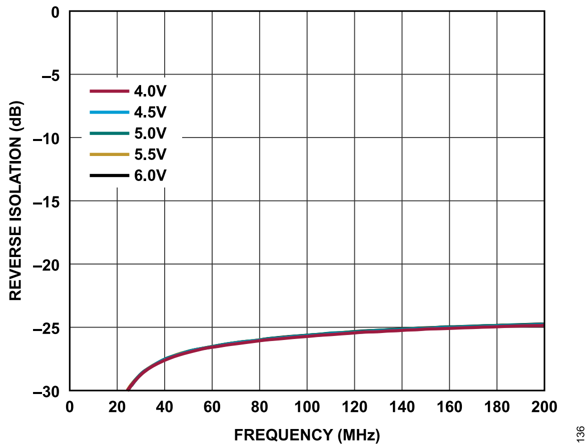

Figure 36. Reverse Isolation vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

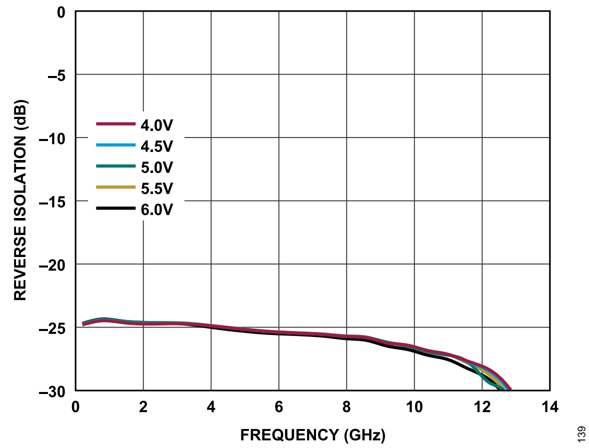

Figure 39. Reverse Isolation vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

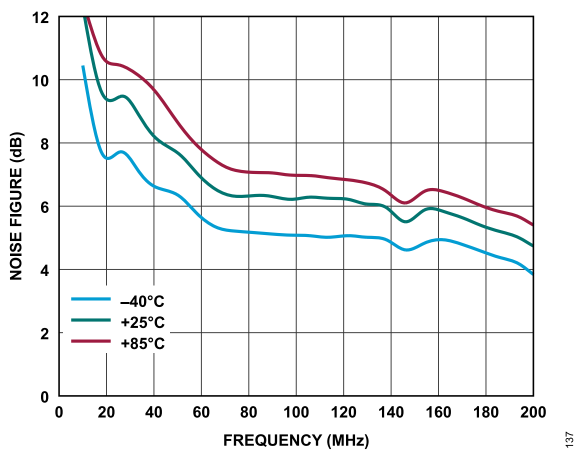

Figure 37. Noise Figure vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

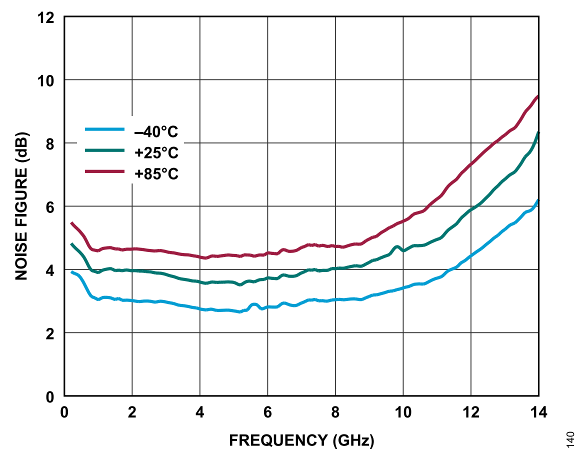

Figure 40. Noise Figure vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

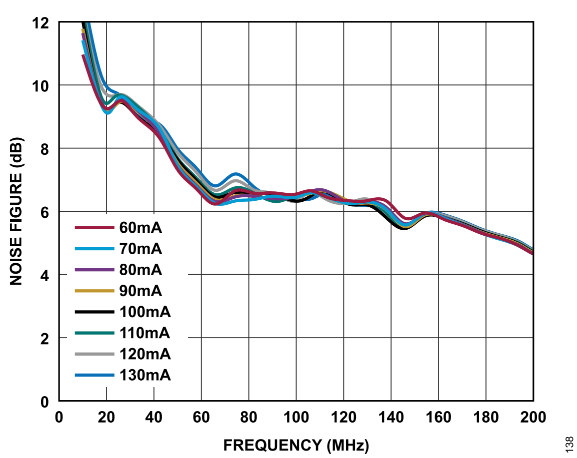

Figure 38. Noise Figure vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

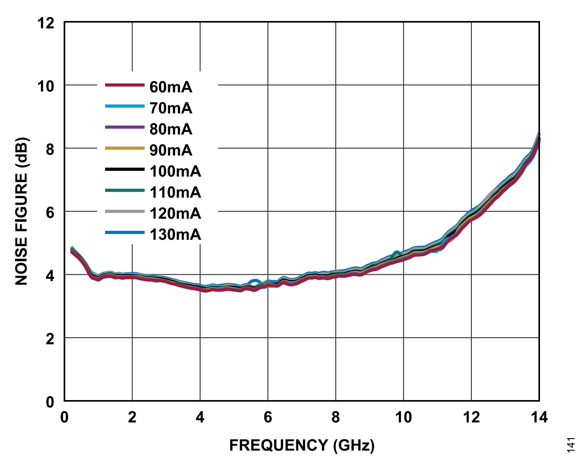

Figure 41. Noise Figure vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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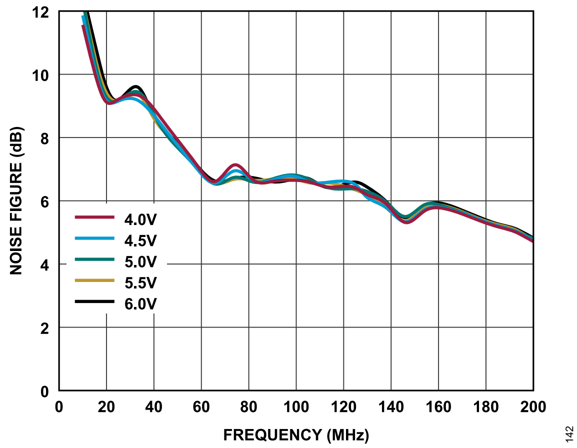

Figure 42. Noise Figure vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

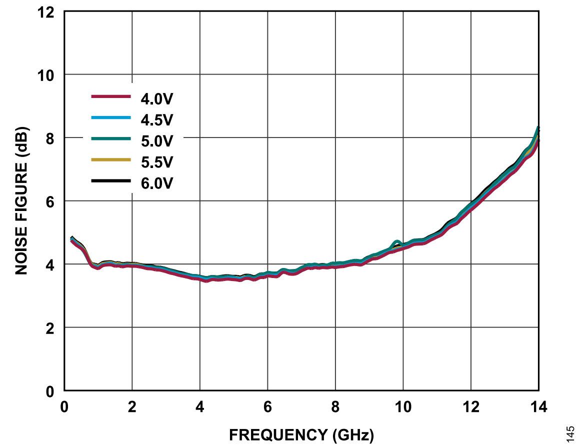

Figure 45. Noise Figure vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

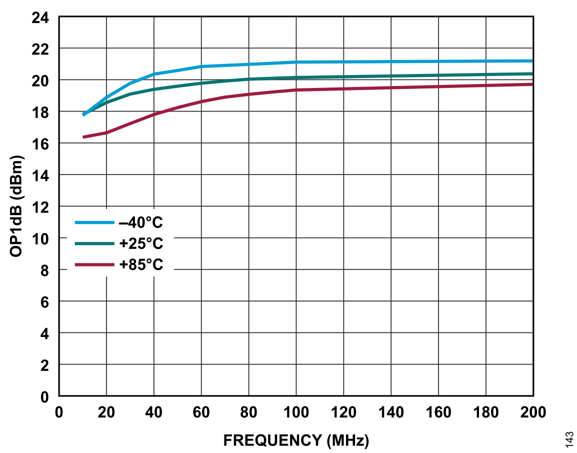

Figure 43. OP1dB vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

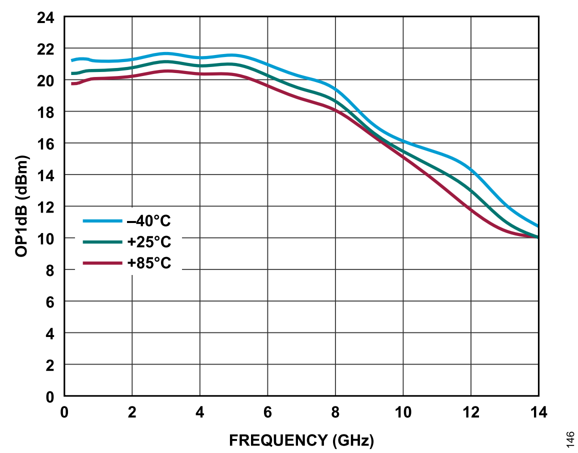

Figure 46. OP1dB vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

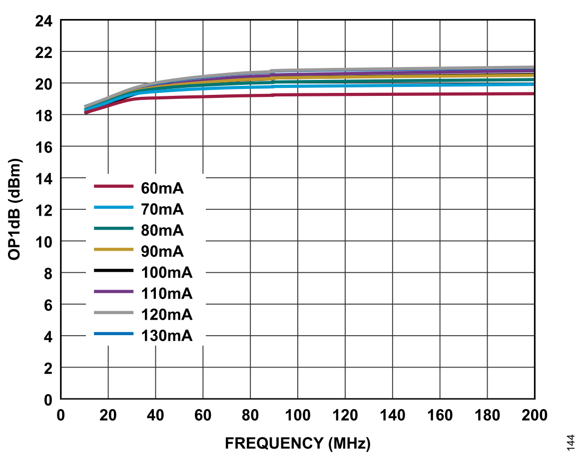

Figure 44. OP1dB vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

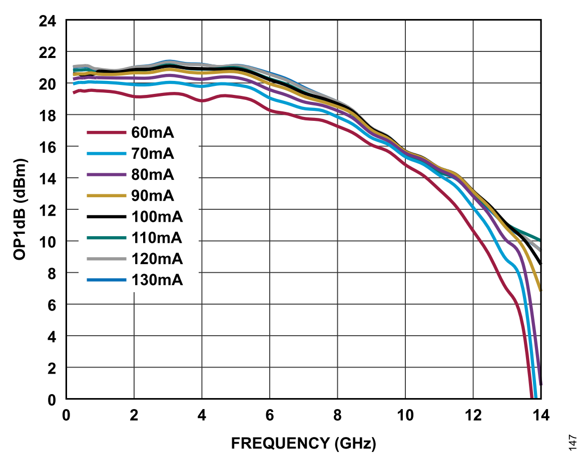

Figure 47. OP1dB vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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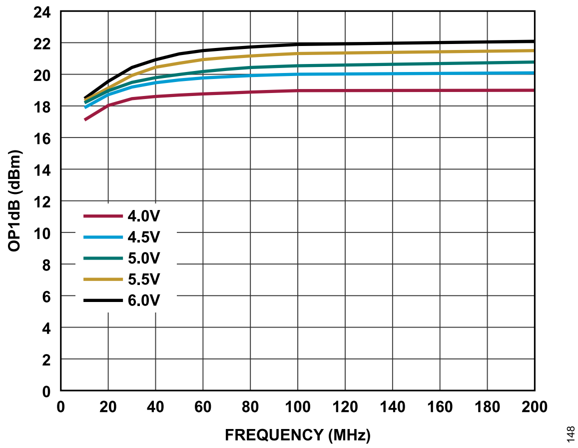

Figure 48. OP1dB vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

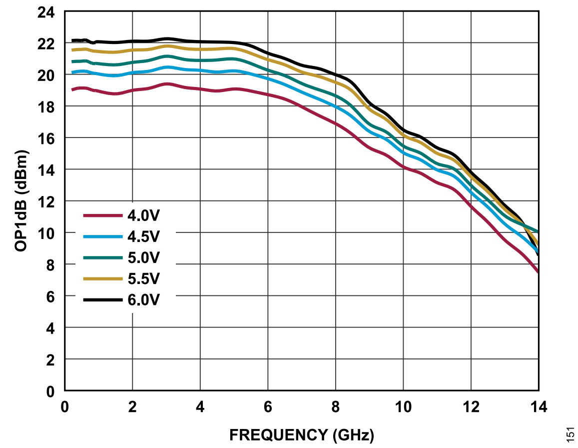

Figure 51. OP1dB vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

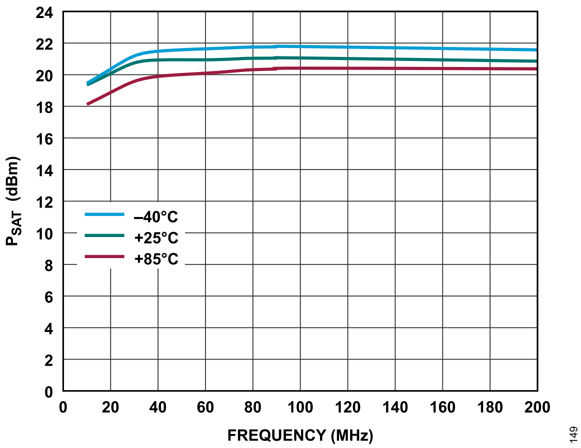

Figure 49. Saturated Power (P_{SAT}) vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

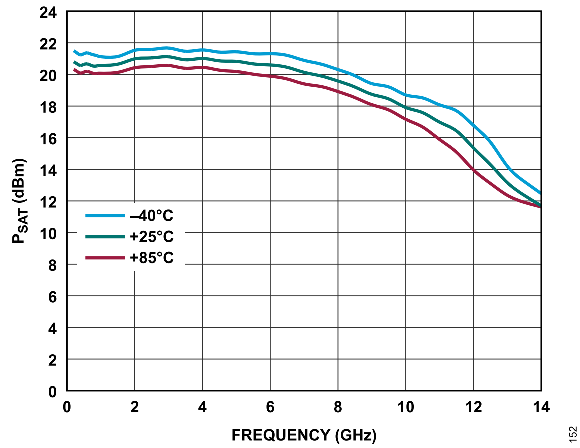

Figure 52. P_{SAT} vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

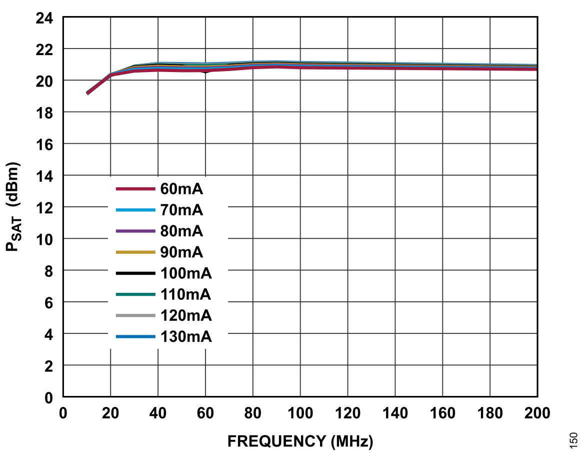

Figure 50. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

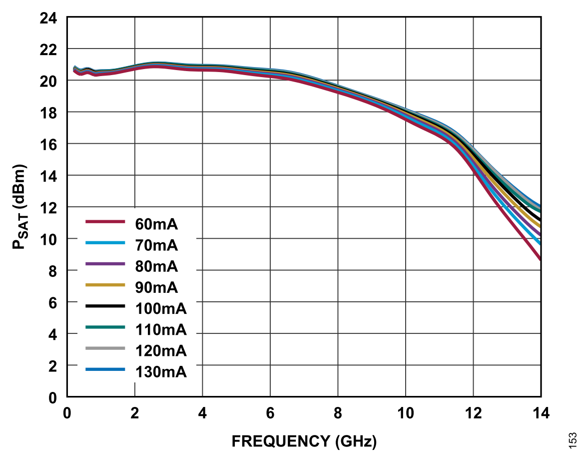

Figure 53. P_{SAT} vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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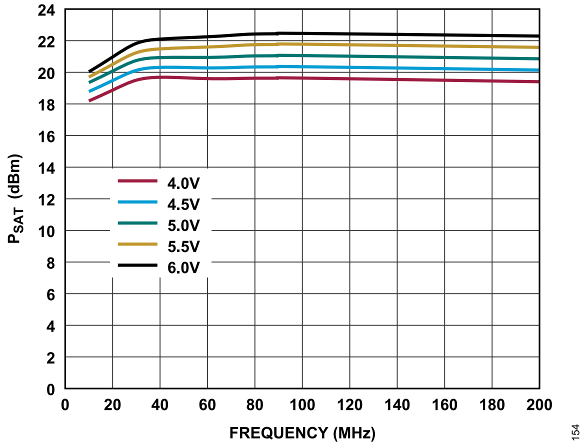

Figure 54. P_{SAT} vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

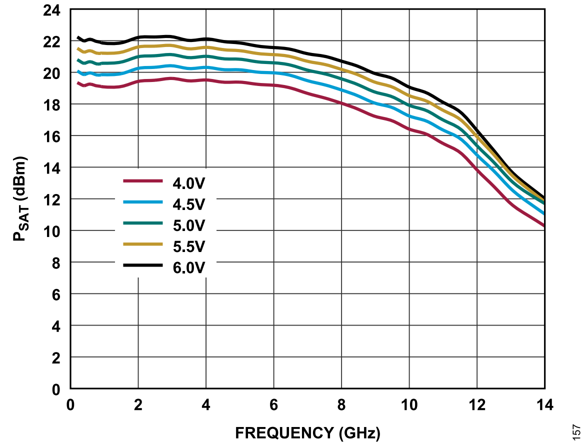

Figure 57. P_{SAT} vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

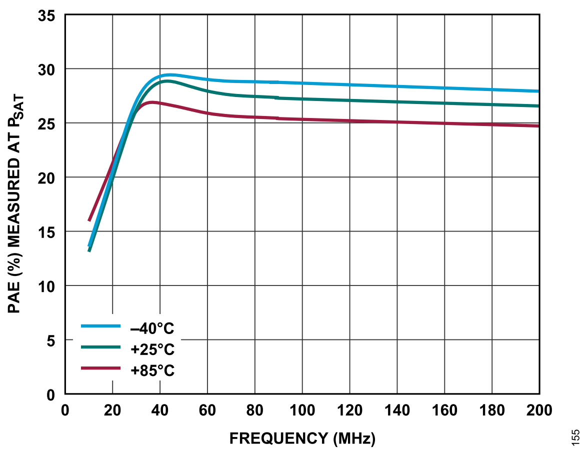

Figure 55. Power Added Efficiency (PAE) Measured at P_{SAT} vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

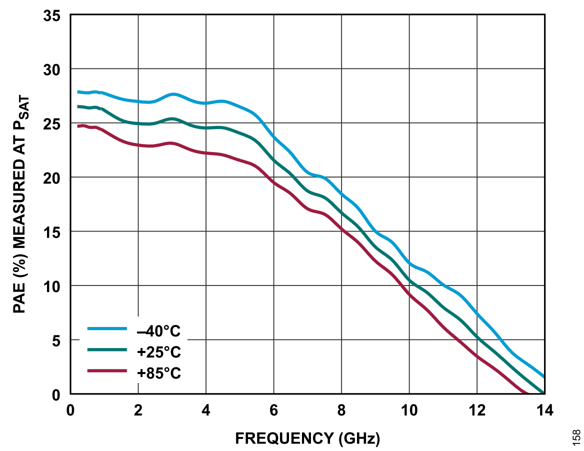

Figure 58. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

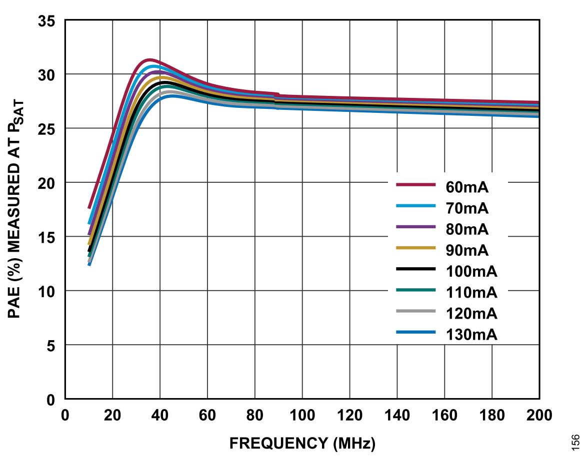

Figure 56. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

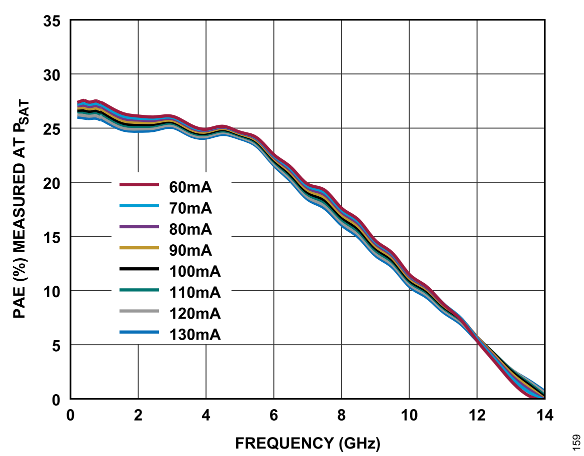

Figure 59. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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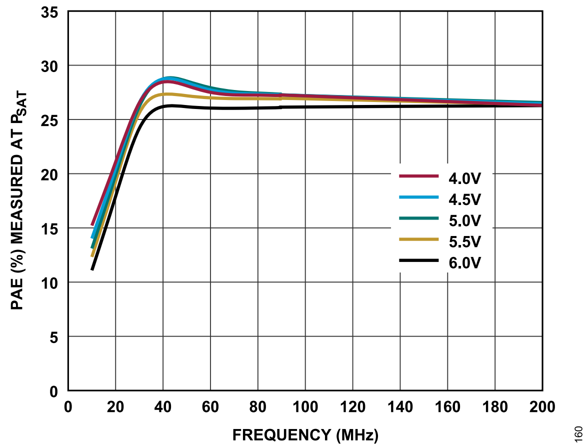

Figure 60. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

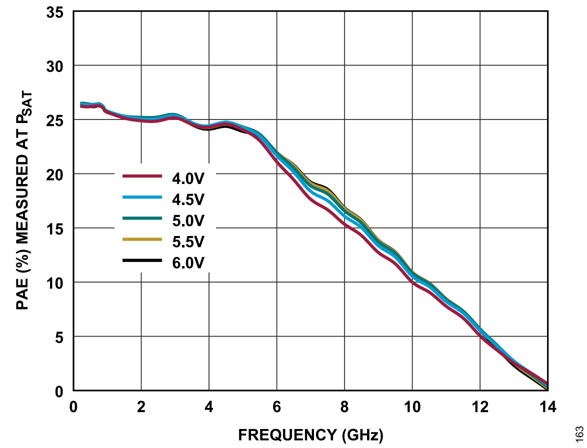

Figure 63. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

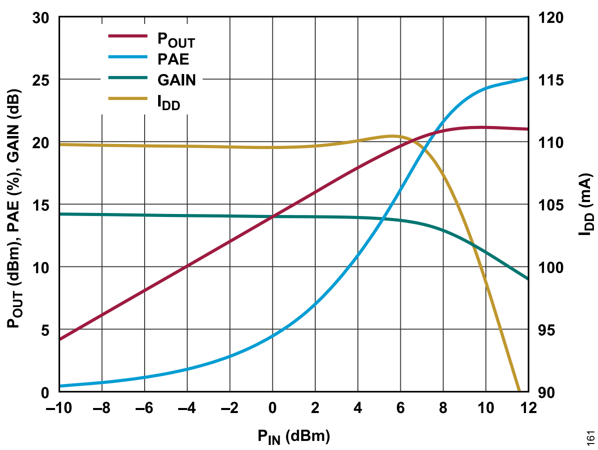

Figure 61. Output Power (P_{OUT}), PAE, Gain, and I_{DD} vs. P_{IN}, Power Compression at 2GHz, V_{DD} = 5V

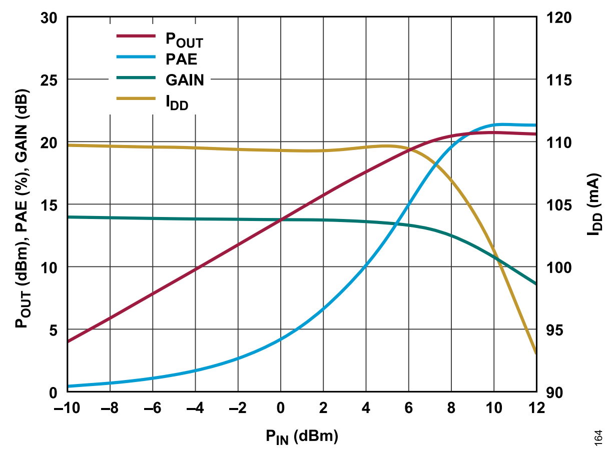

Figure 64. P_{OUT}, PAE, Gain, and I_{DD} vs. P_{IN}, Power Compression at 6GHz, V_{DD} = 5V

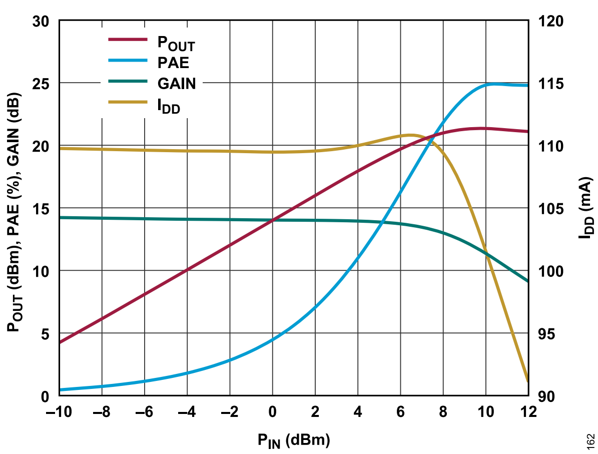

Figure 62. P_{OUT}, PAE, Gain, and I_{DD} vs. P_{IN}, Power Compression at 4GHz, V_{DD} = 5V

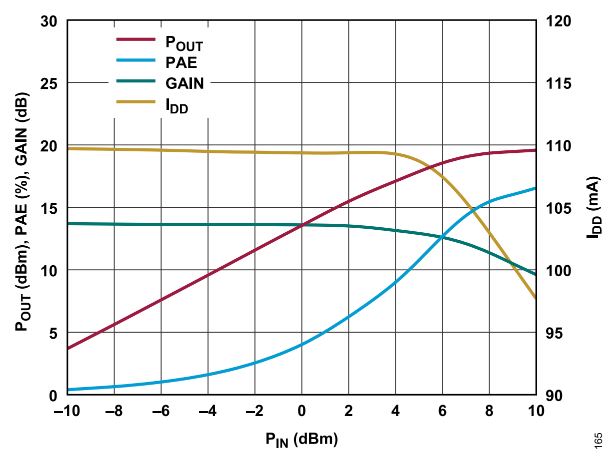

Figure 65. P_{OUT}, PAE, Gain, and I_{DD} vs. P_{IN}, Power Compression at 8GHz, V_{DD} = 5V

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TYPICAL PERFORMANCE CHARACTERISTICS

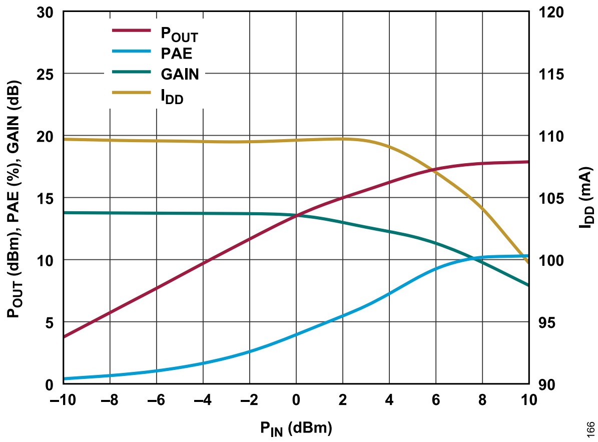

Figure 66. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10GHz, V_{DD} = 5V

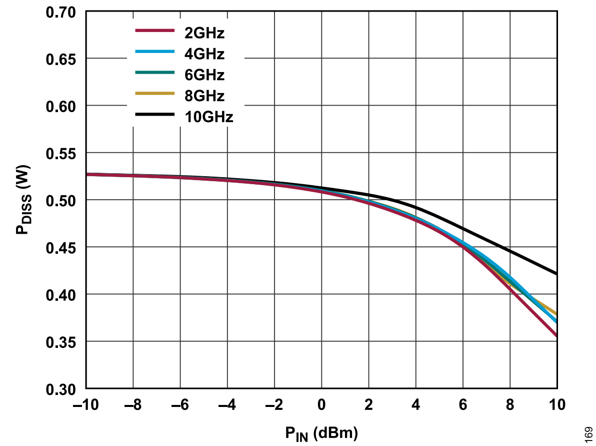

Figure 69. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 5V

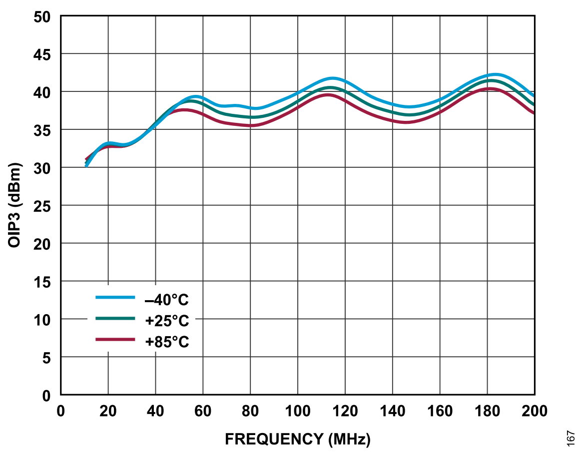

Figure 67. OIP3 vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

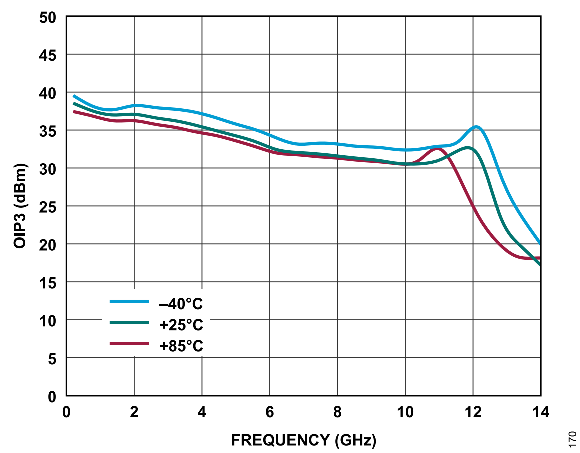

Figure 70. OIP3 vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

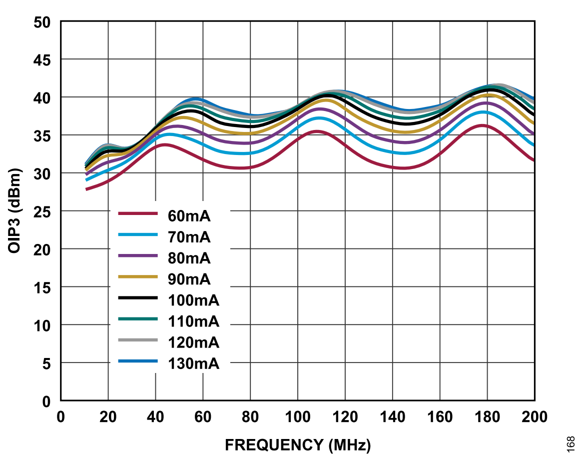

Figure 68. OIP3 vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

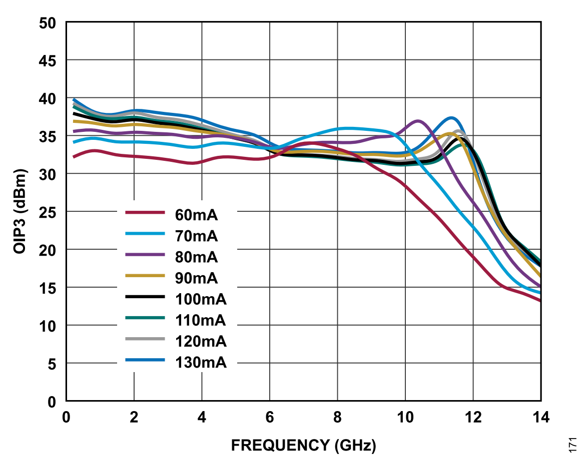

Figure 71. OIP3 vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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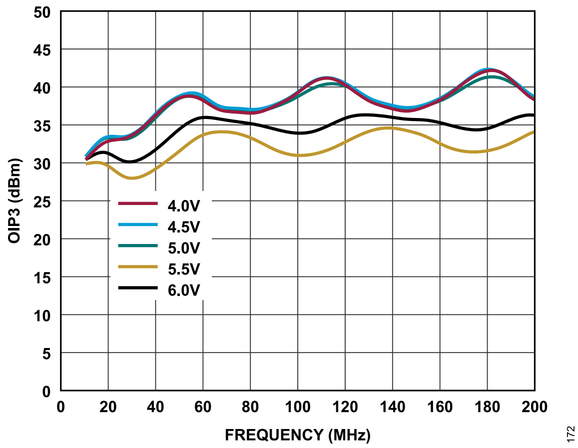

Figure 72. OIP3 vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

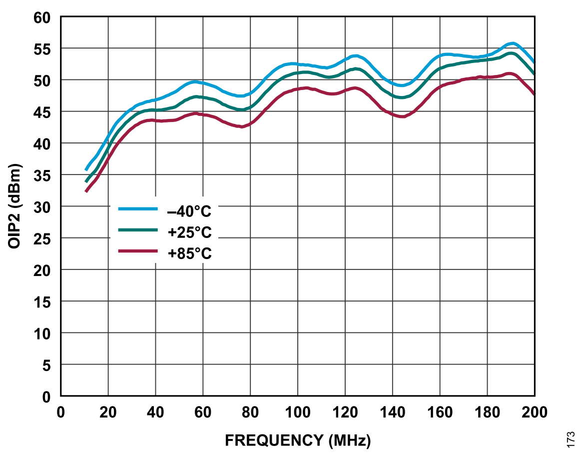

Figure 73. OIP2 vs. Frequency for Various Temperatures, 10MHz to 200MHz, V_{DD} = 5V, I_{DQ} = 110mA

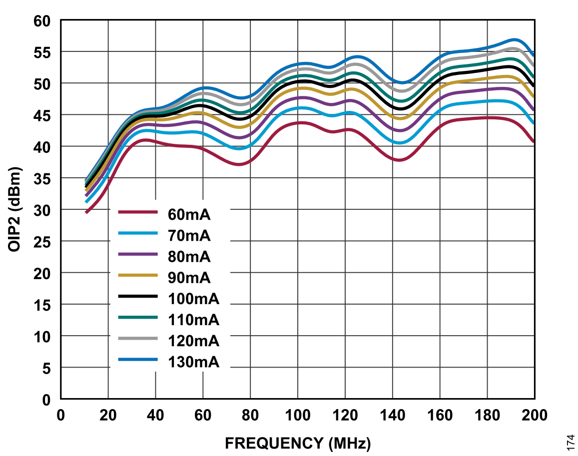

Figure 74. OIP2 vs. Frequency for Various I_{DQ} Values, 10MHz to 200MHz, V_{DD} = 5V

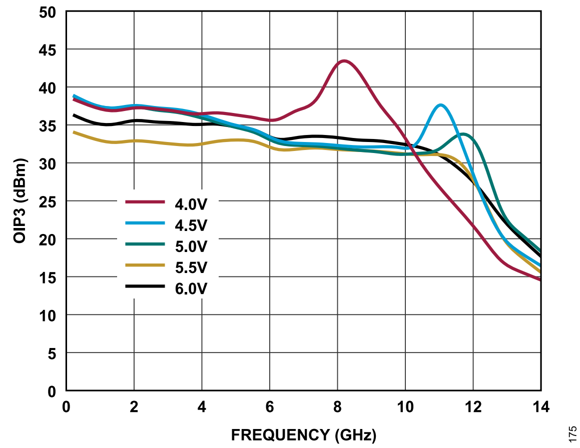

Figure 75. OIP3 vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

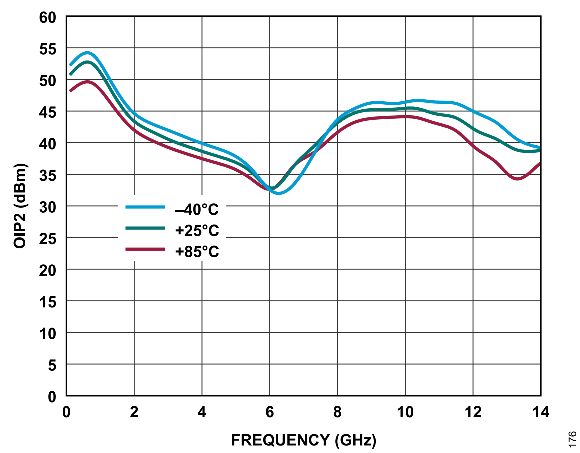

Figure 76. OIP2 vs. Frequency for Various Temperatures, 200MHz to 14GHz, V_{DD} = 5V, I_{DQ} = 110mA

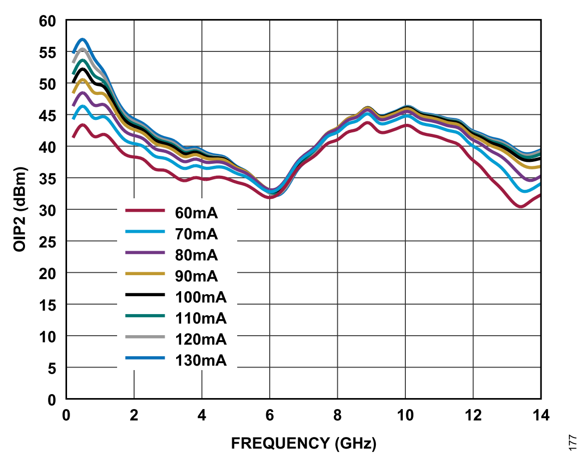

Figure 77. OIP2 vs. Frequency for Various I_{DQ} Values, 200MHz to 14GHz, V_{DD} = 5V

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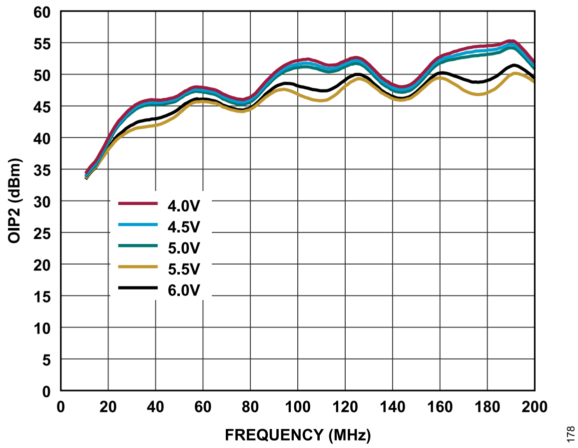

Figure 78. OIP2 vs. Frequency for Various Supply Voltages, 10MHz to 200MHz, I_{DQ} = 110mA

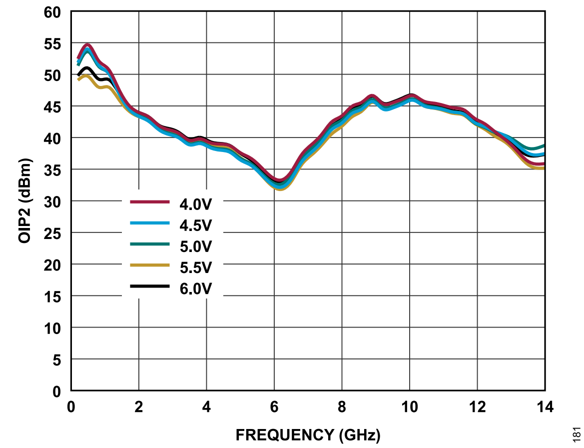

Figure 81. OIP2 vs. Frequency for Various Supply Voltages, 200MHz to 14GHz, I_{DQ} = 110mA

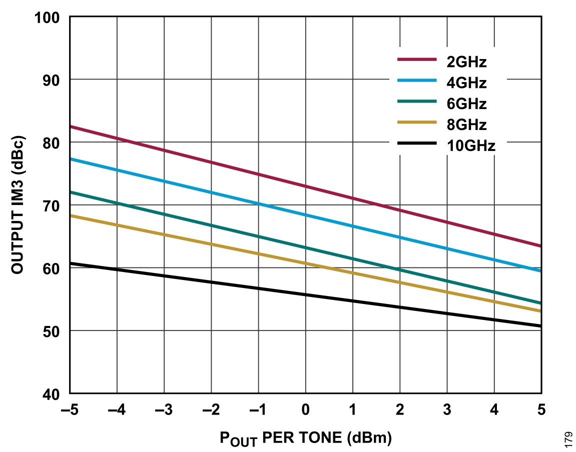

Figure 79. Output Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5V, I_{DQ} = 110mA

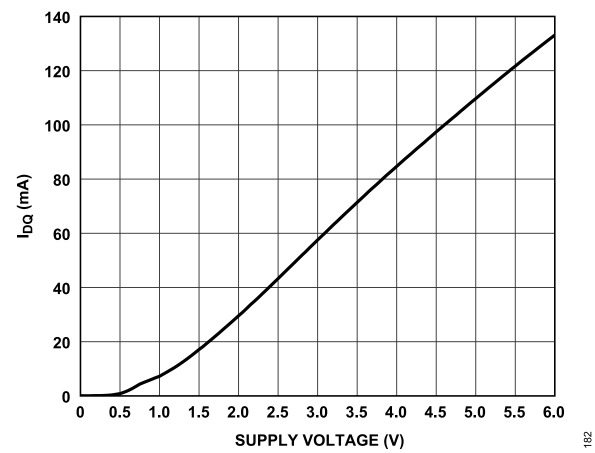

Figure 82. I_{DQ} vs. Supply Voltage, R_{BIAS} = 280Ω

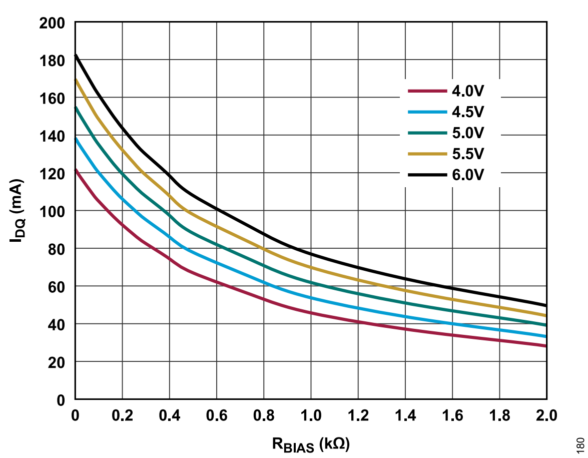

Figure 80. I_{DQ} vs. Bias Resistor Signal (R_{BIAS}) for Various Supply Voltages, 0Ω to 2.0kΩ

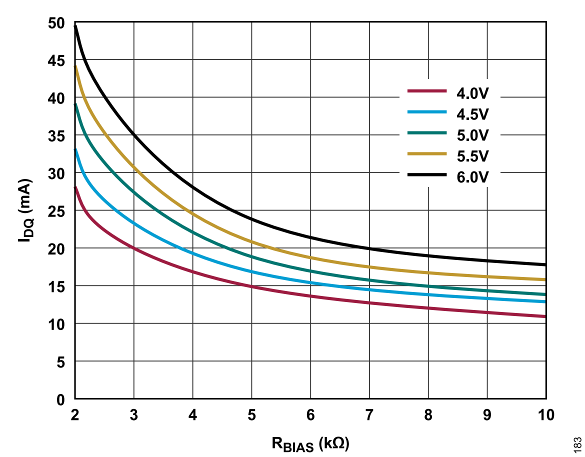

Figure 83. I_{DQ} vs. R_{BIAS} for Various Supply Voltages, 2kΩ to 10kΩ

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TYPICAL PERFORMANCE CHARACTERISTICS

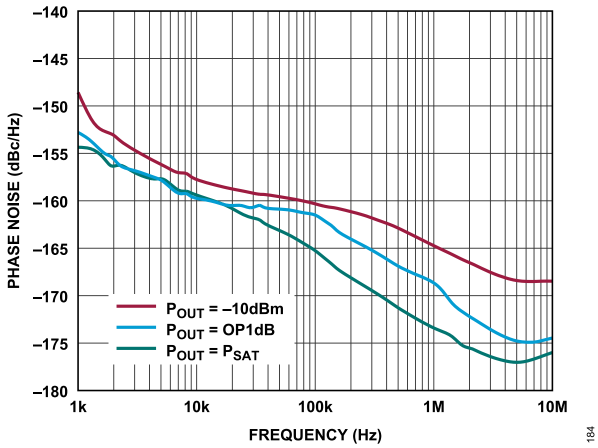

Figure 84. Phase Noise vs. Frequency at 5GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 110mA

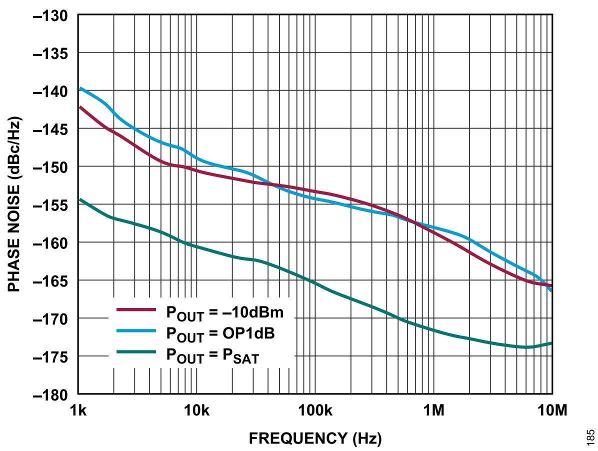

Figure 85. Phase Noise vs. Frequency at 10GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 110mA

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TYPICAL PERFORMANCE CHARACTERISTICS

INTERNAL BYPASS MODE

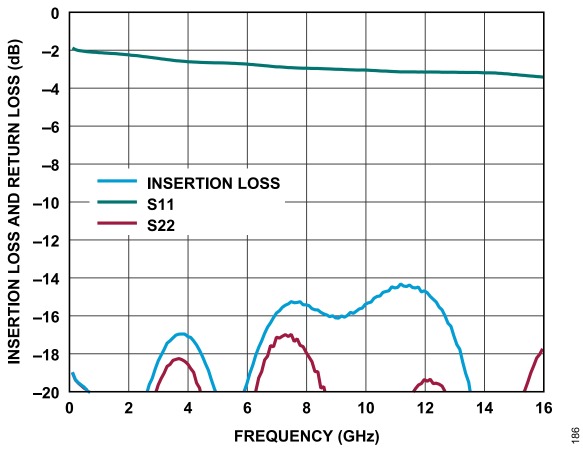

Figure 86. Insertion Loss and Return Loss vs. Frequency, 10MHz to 16GHz

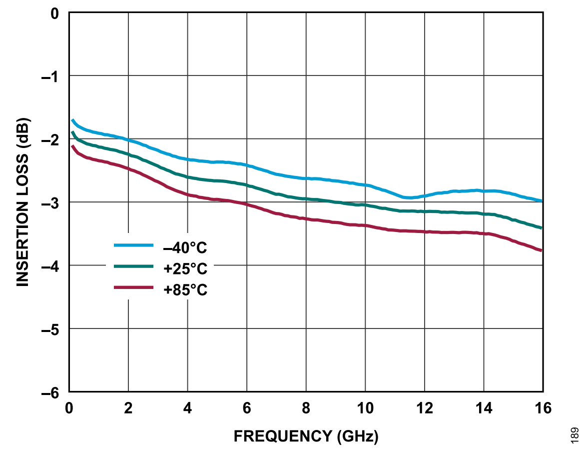

Figure 89. Insertion Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

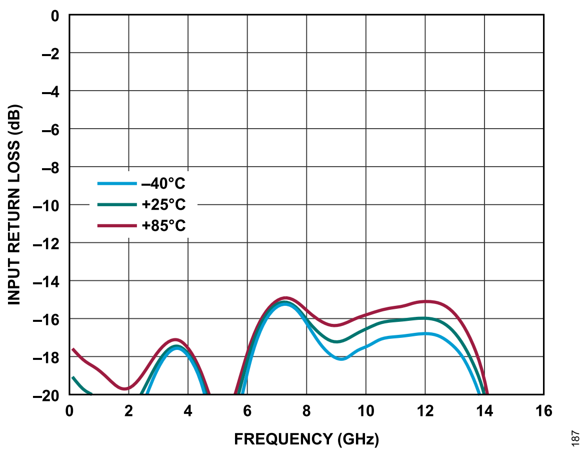

Figure 87. Input Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

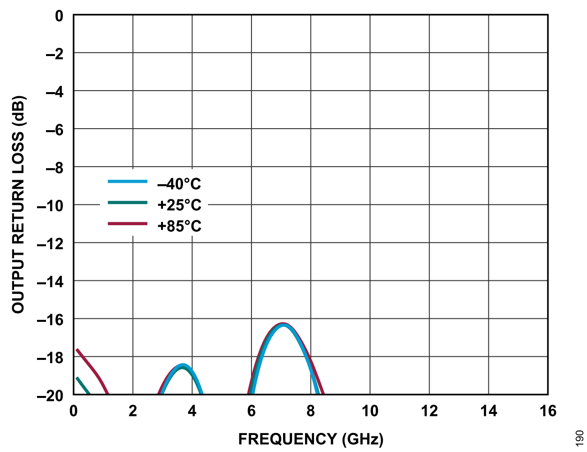

Figure 90. Output Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

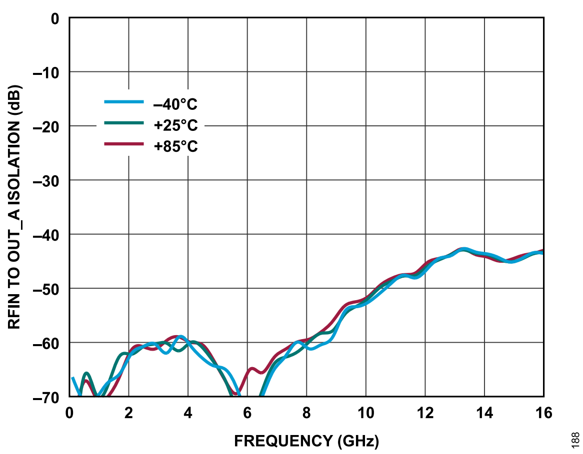

Figure 88. RFIN to OUT A Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

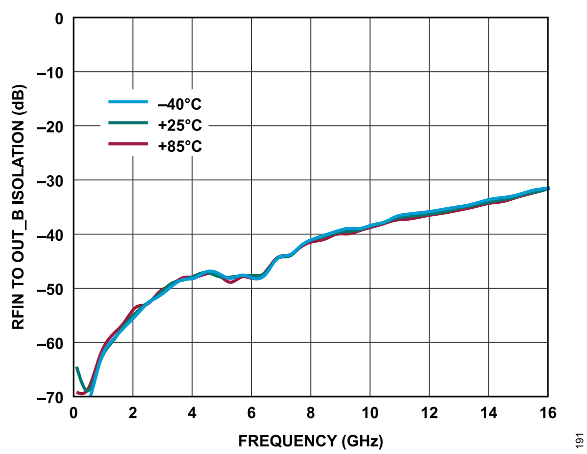

Figure 91. RFIN to OUT_B Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

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TYPICAL PERFORMANCE CHARACTERISTICS

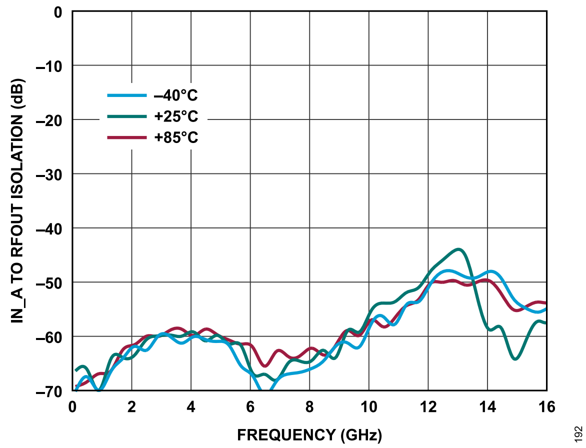

Figure 92. IN_A to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

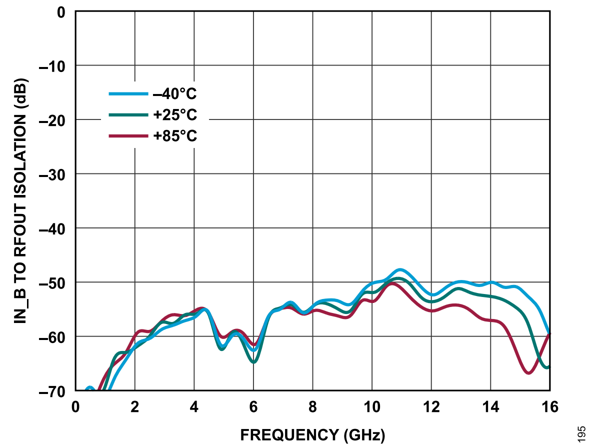

Figure 95. IN_B to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

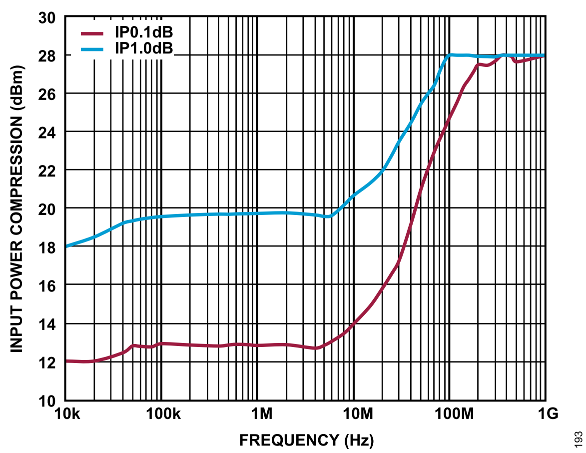

Figure 93. Input Power Compression vs. Frequency for Various Compressions, 10kHz to 1GHz, Mode = Internal Bypass, External Bypass A, and External Bypass B

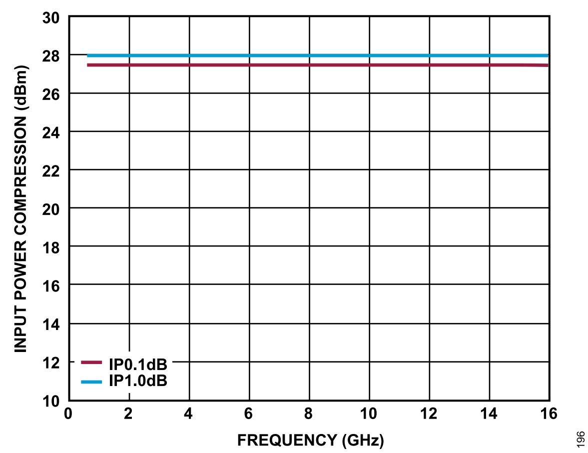

Figure 96. Input Power Compression vs. Frequency for Various Compressions, 1GHz to 16GHz, Mode = Internal, External Bypass A, and External Bypass B

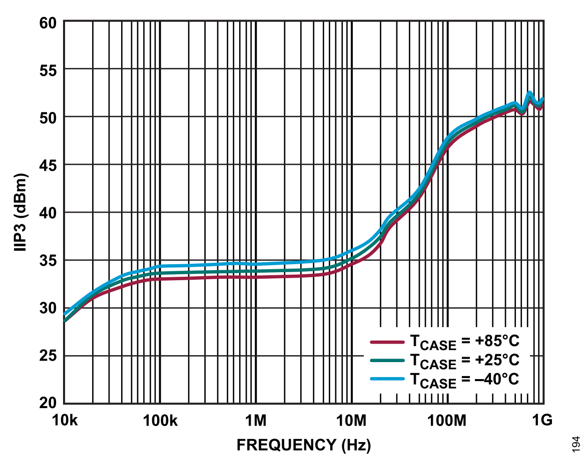

Figure 94. IIP3 vs. Frequency for Various Temperatures, 10kHz to 1GHz, Mode = Internal Bypass, External Bypass A, and External Bypass B

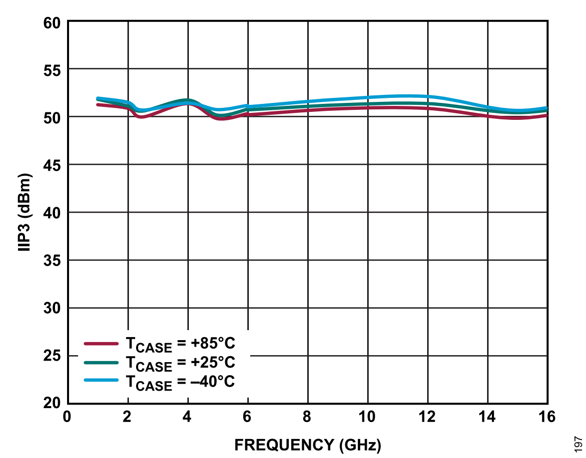

Figure 97. IIP3 vs. Frequency for Various Temperatures, 1GHz to 16GHz, Mode = Internal Bypass, External Bypass A, and External Bypass B

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TYPICAL PERFORMANCE CHARACTERISTICS

EXTERNAL BYPASS A MODE

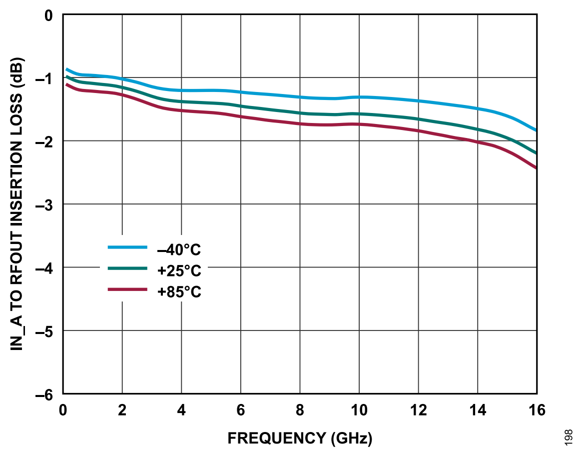

Figure 98. IN_A to RFOUT Insertion Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

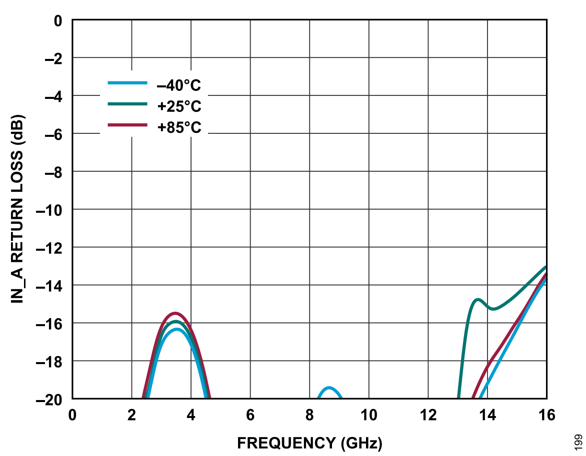

Figure 99. IN_A Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

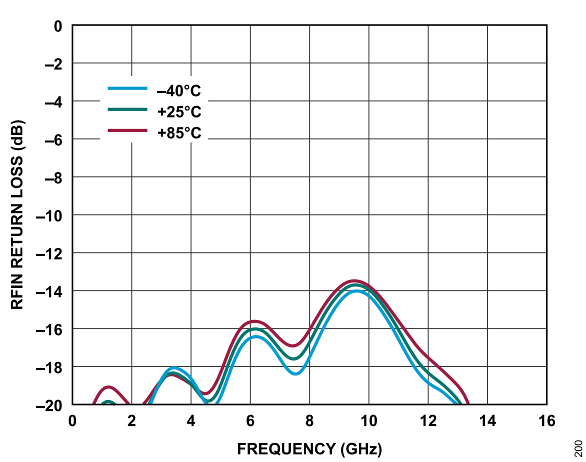

Figure 100. RFIN Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

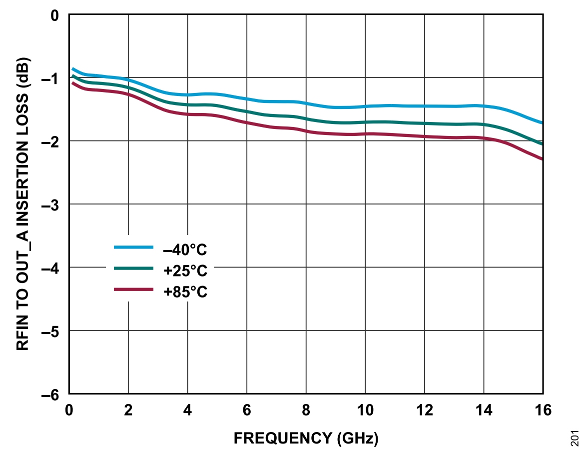

Figure 101. RFIN to OUT_A Insertion Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

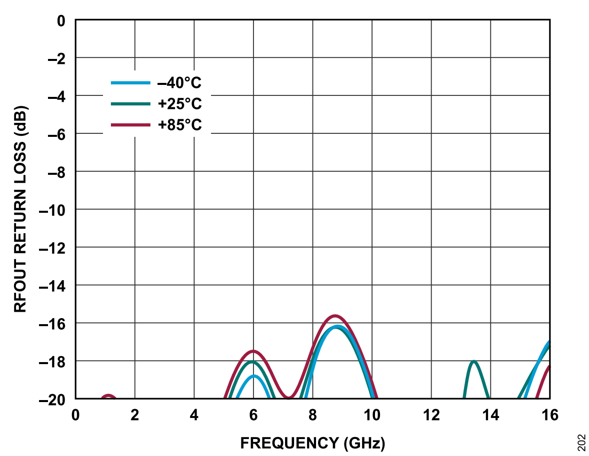

Figure 102. RFOUT Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

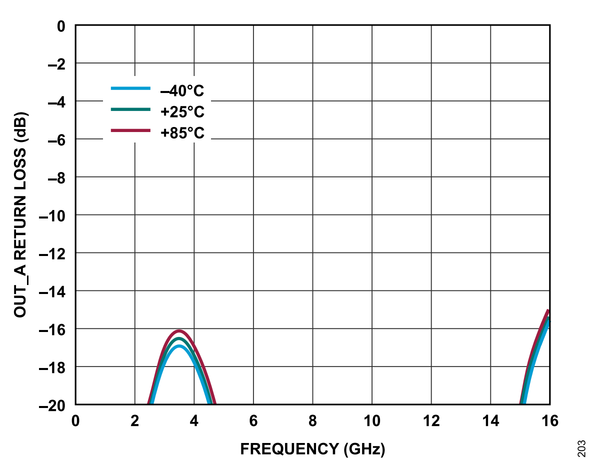

Figure 103. OUT_A Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

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TYPICAL PERFORMANCE CHARACTERISTICS

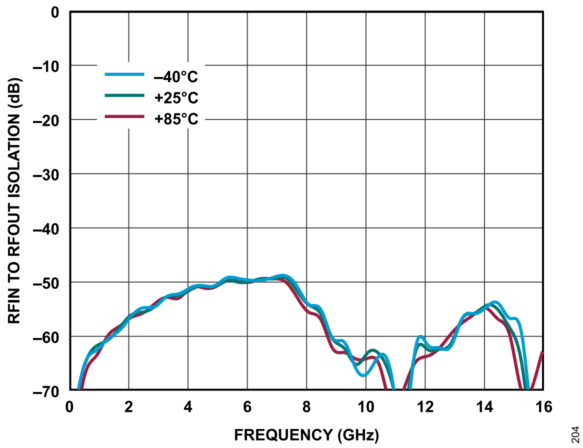

Figure 104. RFIN to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

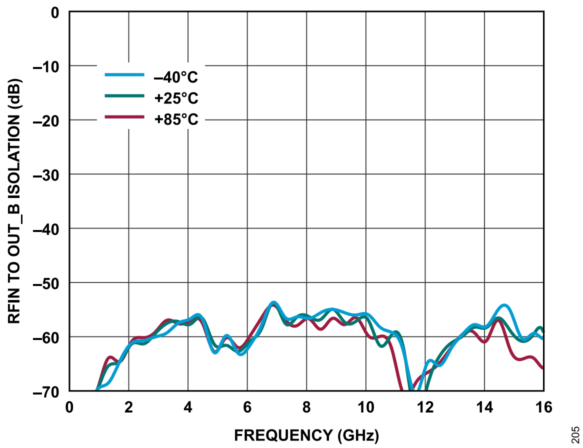

Figure 105. RFIN to OUT_B Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

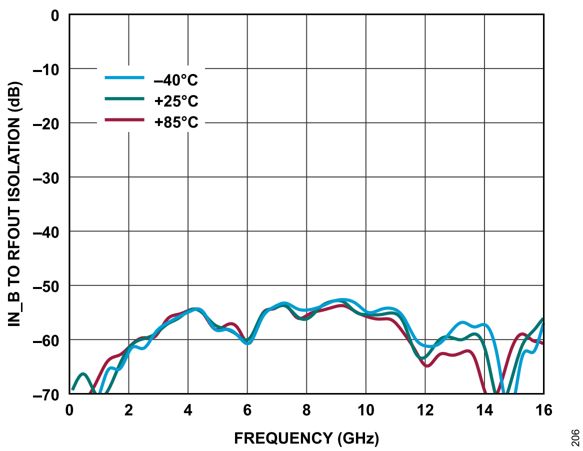

Figure 106. IN_B to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

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TYPICAL PERFORMANCE CHARACTERISTICS

EXTERNAL BYPASS B MODE

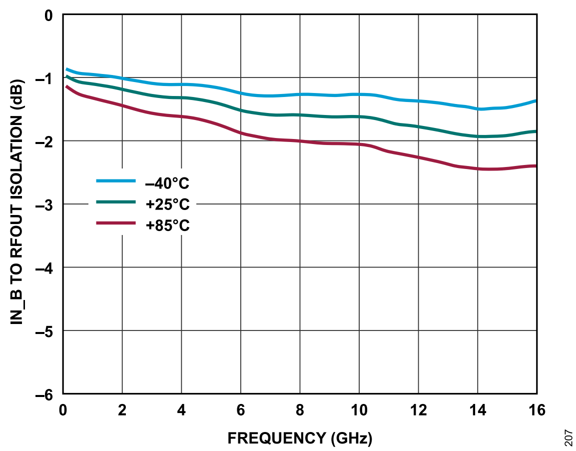

Figure 107. IN_B to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

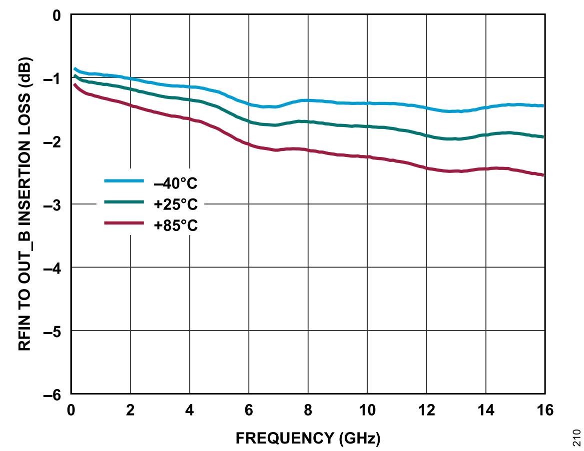

Figure 110. RFIN to OUT_B Insertion Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

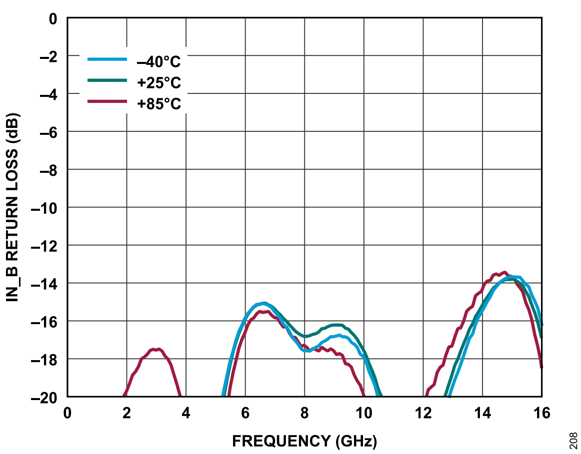

Figure 108. IN_B Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

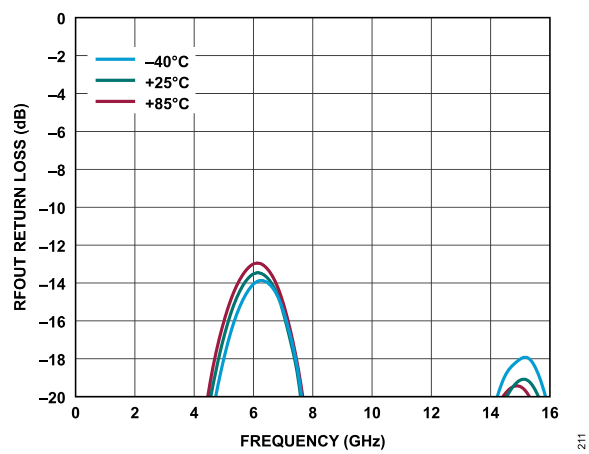

Figure 111. RFOUT Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

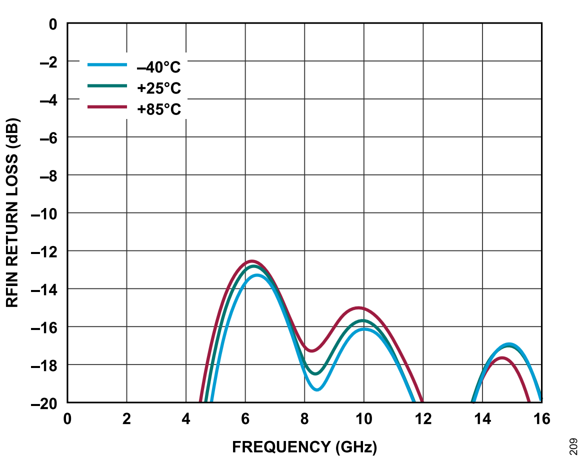

Figure 109. RFIN Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

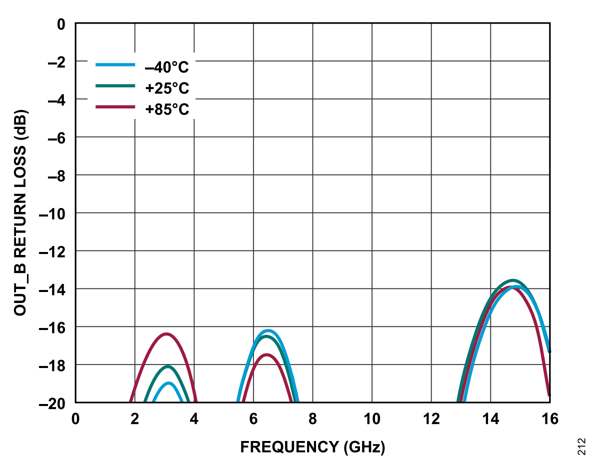

Figure 112. OUT_B Return Loss vs. Frequency for Various Temperatures, 10MHz to 16GHz

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TYPICAL PERFORMANCE CHARACTERISTICS

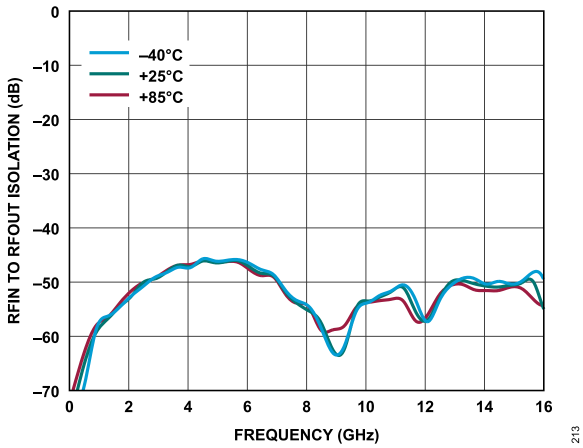

Figure 113. RFIN to RFOUT Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

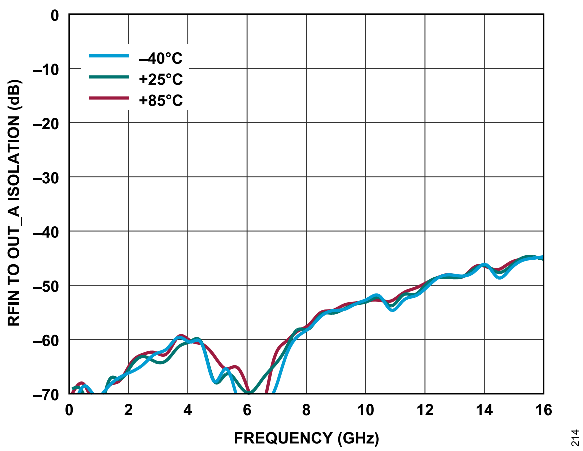

Figure 114. RFIN to OUT_A Isolation vs. Frequency for Various Temperatures, 10MHz to 16GHz

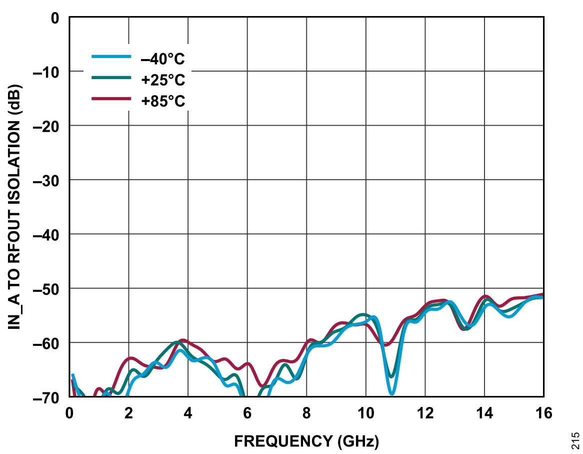

Figure 115. IN_A to RFOUT Isolation vs. Frequency for Various Temperature, 10MHz to 16GHz

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THEORY OF OPERATION

The ADL8113 integrates an amplifier with two switching networks located at the RF input and output. The amplifier, which is internally AC-coupled on its input and output, uses a gallium arsenide (GaAs) LNA die. The switching network employs robust silicon-on-insulator (SOI) technology for fast switching and a short settling time. This integrated solution has four different signal path modes available: internal amplifier, internal bypass, External Bypass A, and External Bypass B. Signal path modes are controlled through the VA and VB digital pins. The internal amplifier is biased up by applying 5V to VDD1 and by connecting a bias resistor between VDD1 and RBIAS. The reflective switch network is powered by applying +3.3V and −3.3V to VDD2 and VSS2, respectively. DC bias to the switches is independent of the LNA. Turning off the bias to VDD1 that controls the LNA provides better isolation between RF ports.

SIGNAL PATH MODES FOR DIGITAL CONTROL INPUTS

Figure 116 through Figure 119 show the signal path modes for the digital control inputs, while Table 12 details these modes for the digital control inputs.

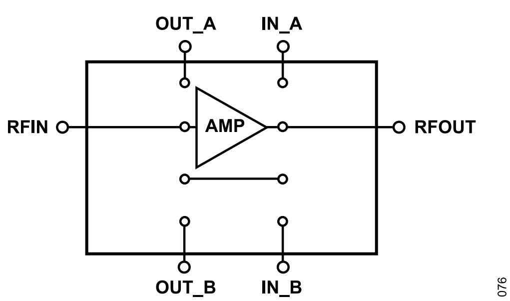

Figure 116. Internal Amplifier Mode, VA = 0V and VB = 0V

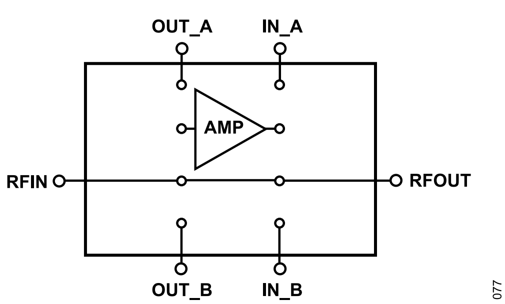

Figure 117. Internal Bypass Mode, VA = 3.3V and VB = 3.3V

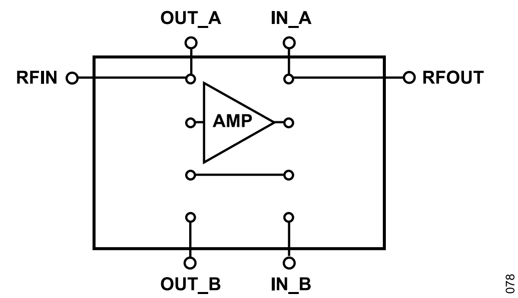

Figure 118. External Bypass A Mode, VA = 0V and VB = 3.3V

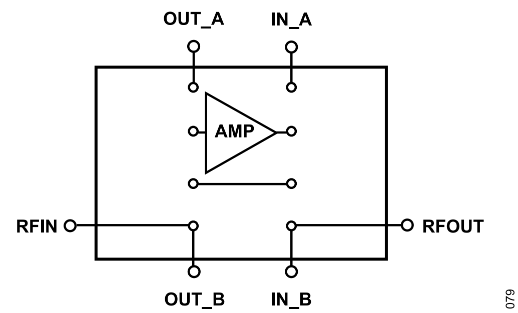

Figure 119. External Bypass B Mode, VA = 3.3V and VB = 0V

Table 12. Truth Table for the Signal Path Modes for the Digital Control Inputs

	Digital Control		
Mode Name	**VA**	**VB**	**Signal Path Mode**
Internal Amplifier	Low	Low	RFIN to RFOUT through the amplifier path
Internal Bypass	High	High	RFIN to RFOUT through the bypass path
External Bypass A	Low	High	RFIN to OUT_A and IN_A to RFOUT
External Bypass B	High	Low	RFIN to OUT_B and IN_B to RFOUT

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APPLICATIONS INFORMATION

The basic connections for operating the ADL8113 are shown in Figure 120. A 5V DC bias is supplied to the amplifier via VDD PA. The bias current of the amplifier is set by a resistor (R1) connected between RBIAS and VDD PA. Table 13 details various R_{BIAS} values vs. I_{DQ}, I_{DQ_AMP}, and I_{RBIAS} for a given 5V DC operation. Do not leave RBIAS open.

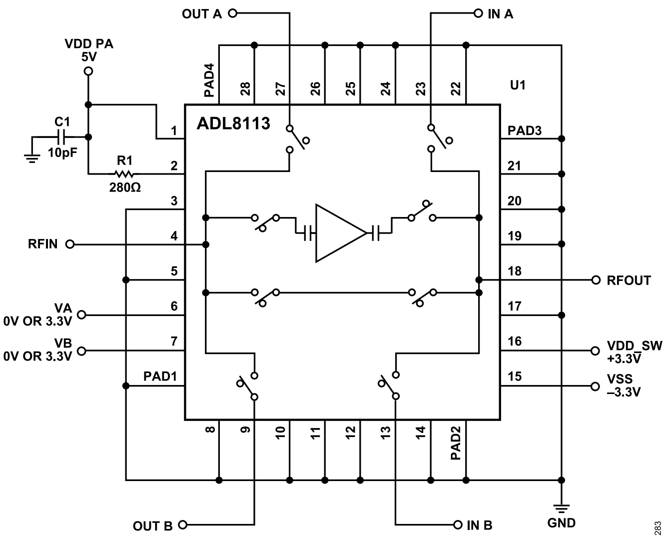

Figure 120. ADL8113 Basic Connections and Evaluation Board Schematic

Table 13. Recommended R_{BIAS} Values at VDD PA Voltage (V_{DD_PA}) = 5V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
121	130	125	5
187	120	115	5
280	110	105	5
360	100	95	5
470	90	85	5
619	80	76	4
787	70	66	4
1050	60	57	3

Power for the two SP4T switches comes from the +3.3V and −3.3V applied to the VDD_SW and VSS pins, respectively.

The VA and VB digital inputs, signal path states are detailed in Table 12. A high logic state is between 1.2V and 3.3V, and a low logic state is between 0.8V and 0V.

Figure 121 shows the time domain response at RFOUT to the switching voltages on VA and VB when RFIN is driven by a steady level of approximately 2.5dBm at 250MHz. Both of the external bypass connection paths (External Bypass A and External Bypass B) are left open. When VA and VB are low, the ADL8113 is in internal amplifier mode. When VA and VB are high, the ADL8113 switches to internal bypass mode, and the output drops accordingly. When VA and VB are nonsimultaneously low or high, the ADL8113 switches to either External Bypass A or External Bypass B because these two paths are left open; therefore, no signal appears at the output for both cases.

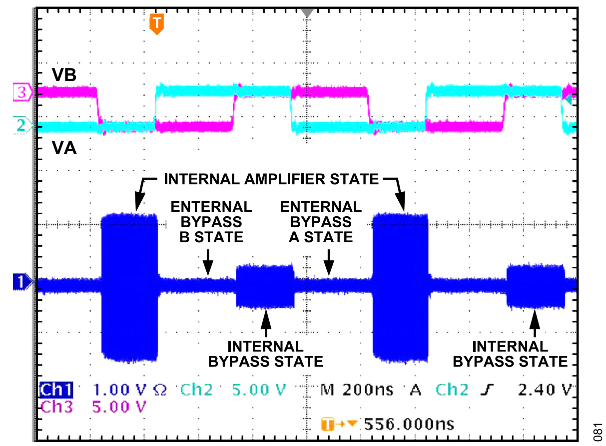

Figure 121. Time Domain Response of RFOUT to the Switching of the VA and VB Voltages with a Continuous 2.5dBm RF Input

RECOMMENDED TURN-ON AND TURN-OFF BIAS SEQUENCING

Turn-On Bias Sequencing

The recommended bias sequence during power-up is as follows:

1. Set VDD_SW = 3.3V.
2. Set VSS = −3.3V.
3. Set VDD PA = 5V.
4. Set VA = 0V or 3.3V.
5. Set VB = 0V or 3.3V.
6. Apply the RF signal.

Turn-Off Bias Sequencing

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set VB = 0V
3. Set VA = 0V
4. Set VDD PA = 0V.
5. Set VSS = 0V.
6. Set VDD_SW = 0V.

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APPLICATIONS INFORMATION

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 122 shows a recommended power management circuit that uses MAX1697 inverting charge pump, MAX17651 linear regulator, and LT3042 linear regulator. The LT3042 linear regulator is used to step down the 12V input voltage to a low noise 5V output to the VDD PA pin of the ADL8113 evaluation board.

The output voltage (V_{OUT}) for the LT3042 is set by the R4 resistor connected to the SET pin, according to the following equation:

$$R_4 = (V_{OUT}/100\mu A) \quad (1)$$

The PGFB resistors (R5 and R6) are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature and by adding resistors it results in a bit more (5%); therefore, putting 5% between the output and PGFB works well. In addition, the PG open collector is pulled up to the 5V output to give a convenient 0V to 5V voltage range.

The MAX17651 linear regulator is used to provide a +3.3V input voltage to the MAX1697 inverting charge pump and a +3.3V output voltage to the VDD_SW pin of the ADL8113 evaluation board. The switching frequency for the MAX1697 is set to 250kHz by the 1µF capacitor, which sets the minimum output resistance to 12Ω. The MAX1697 data sheet provides a table of capacitor values that can be used to select other switching frequencies ranging from 12kHz to 250kHz.

The output voltage (V_{OUT}) for the MAX17651 is set by the R1 and R2 resistors connected to the OUT and FB pins, according to the following equation:

$$R1 = R2 \times (((\text{Input Voltage } (V_{IN})/V_{OUT}) - 1))$$

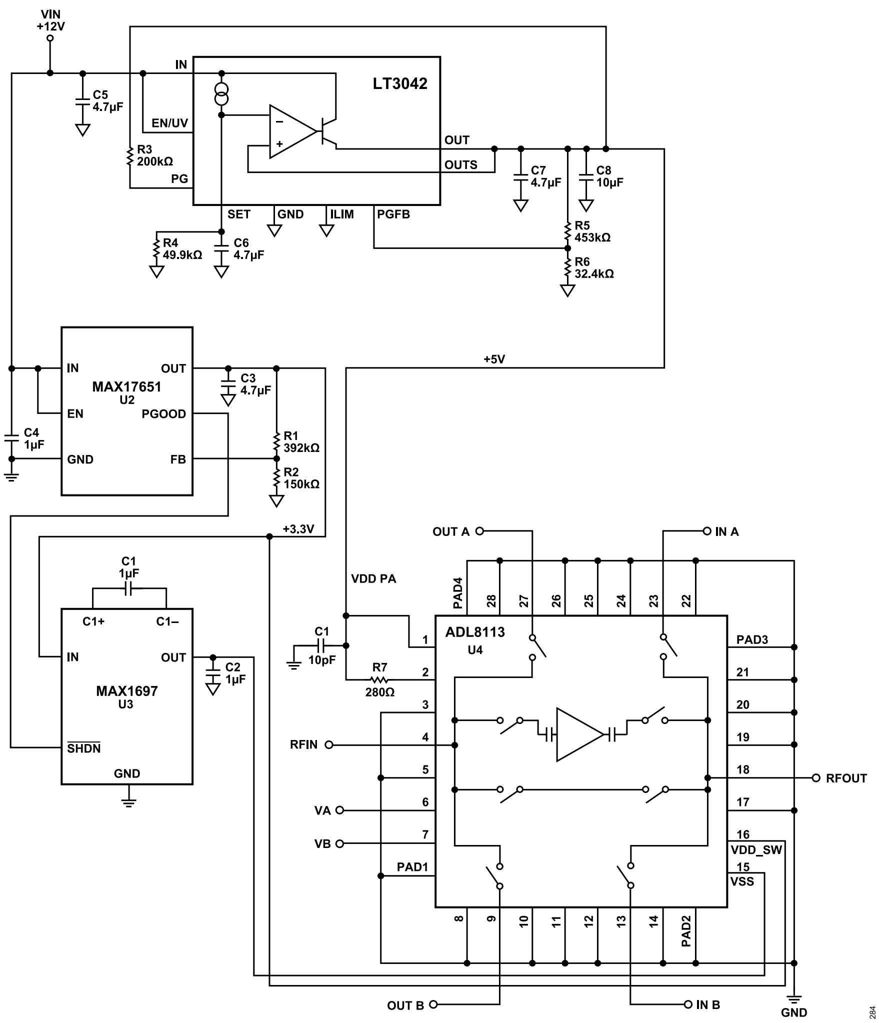

Figure 122. Power Management Circuit Schematic

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OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-28-4	LGA	28-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8113ACCZ	−40°C to +85°C	28-Terminal Land Grid Array [LGA]	Reel, 500	CC-28-4
ADL8113ACCZ-R7	−40°C to +85°C	28-Terminal Land Grid Array [LGA]	Reel, 500	CC-28-4

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 14. Evaluation Boards

Model[1]	Package Description
ADL8113-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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