HV2733

16-Channel Low-Harmonic-Distortion High-Voltage Analog Switch with Bleed Resistors

Features

- Low Harmonic Distortion
- Integrated Bleed Resistors on the Outputs
- 3.3V or 5.5V CMOS Input Logic Level
- 20 MHz Data Shift Clock Frequency
- –10 µA Low-quiescent Power Dissipation
- Low Parasitic Capacitance
- DC to 50 MHz Small-signal Frequency Response
- CMOS Logic Circuitry for Low Power
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Flexible Operating Supply Voltages

Applications

- Medical Ultrasound Imaging
- Non-destructive Testing Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Optical MEMS Modules

General Description

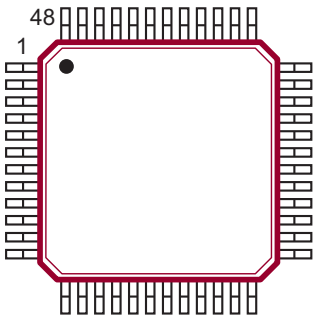
The HV2733 is a low-charge injection, 16-channel, low-harmonic-distortion, high-voltage analog switch integrated circuit (IC) intended for applications requiring high-voltage switching controlled by low-voltage control signals such as medical ultrasound imaging, piezoelectric transducer drivers, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

The outputs are configured as single-pole double-throw analog switches. Data are shifted into an 8-bit Shift register using an external clock. The $\overline{LE}$ latches the Shift register data into the individual switch latches. A logic high connects a switch common YX to $\overline{SWX}$. On the other hand, a logic low connects YX to $\overline{SWX}$. A logic high in CLR resets all switches to $\overline{SWX}$ simultaneously.

To reduce any possible clock feed-through noise, the latch enable bar ($\overline{LE}$) should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. The HV2733 combines high-voltage bilateral DMOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

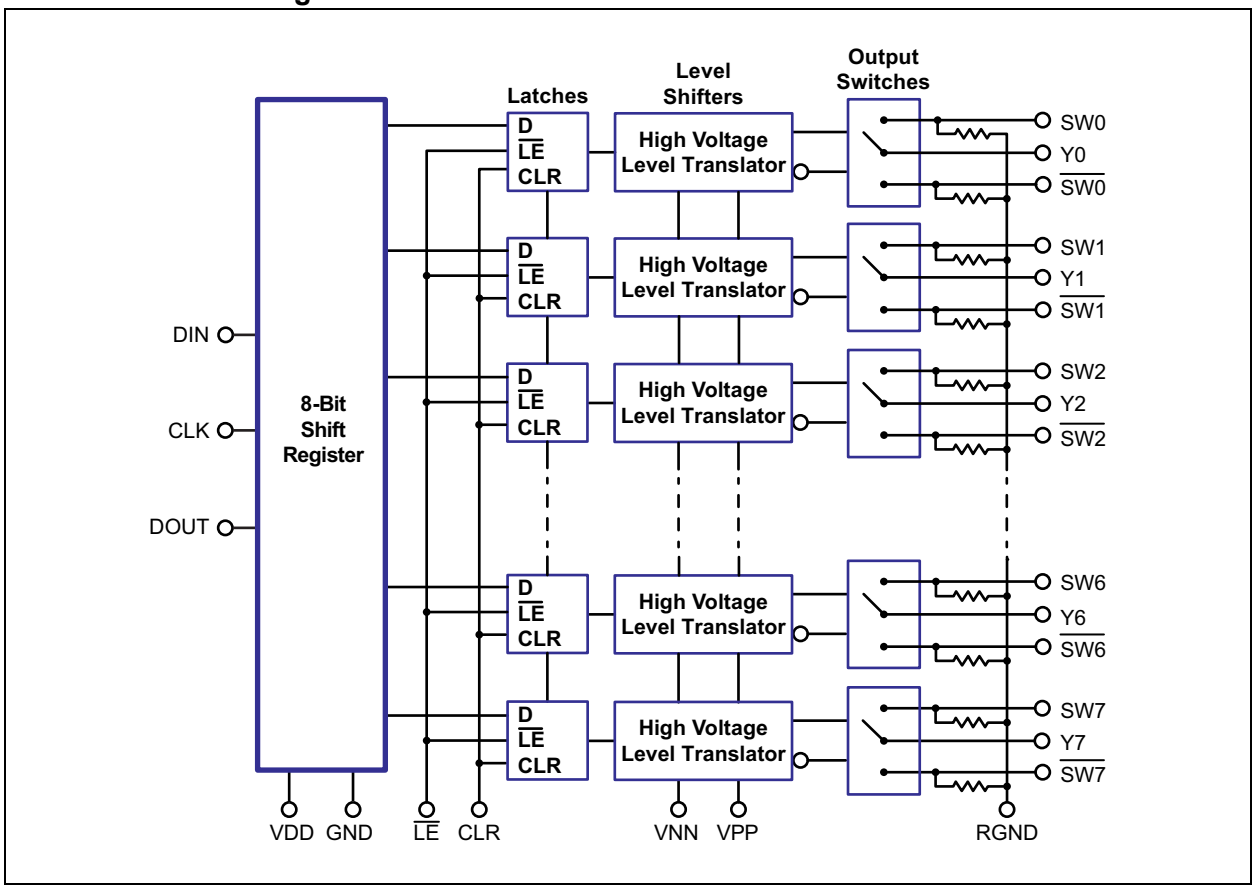
Package Type

48-lead LQFP
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Logic Power Supply Voltage, V_{DD} ..... –0.5V to +7V
Differential Supply Voltage, V_{PP}–V_{NN} 220V
High-voltage Positive Supply, V_{PP} ..... –0.5V to +200V
High-voltage Negative Supply, V_{NN} ..... +0.5V to –200V
Logic Input Voltage ..... –0.5V to V_{DD}+0.3V
Analog Signal Range, V_{SIG} ..... V_{NN} to V_{PP}
Peak Analog Signal Current/Channel 2.5A
Storage Temperature, T_S ..... –65°C to 150°C
Power Dissipation:
48-lead LQFP 1W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Power Supply Voltage	V_{DD}	3	—	5.5	V	**Note 1**, **Note 3**
High-voltage Positive Supply	V_{PP}	+40	—	V_{NN} +200	V	**Note 1**, **Note 3**
High-voltage Negative Supply	V_{NN}	–40	—	–160	V	**Note 1**, **Note 3**
High-level Input Voltage	V_{IH}	0.9 V_{DD}	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	0.1 V_{DD}	V	
Analog Signal Voltage Peak-to-peak	V_{SIG}	V_{NN}+10V	—	V_{PP}–10V	V	**Note 2**
Operating Ambient Temperature	T_A	0	—	70	°C	

Note 1: Power-up/down sequence is arbitrary except GND must be powered up first and powered down last.
2: V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power-up/down transition.
3: Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1 millisecond.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
Small Signal Switch On-resistance	R_{ONS}	—	30	—	26	38	—	48	Ω	I_{SIG} = 5 mA	V_{PP} = +40V, V_{NN} = –160V
		—	25	—	22	27	—	32		I_{SIG} = 200 mA	
		—	25	—	22	27	—	30		I_{SIG} = 5 mA	V_{PP} = +100V, V_{NN} = –100V
		—	18	—	18	24	—	27		I_{SIG} = 200 mA	
		—	23	—	20	25	—	30		I_{SIG} = 5 mA	V_{PP} = +160V, V_{NN} = –40V
		—	22	—	16	25	—	27		I_{SIG} = 200 mA	
Small Signal Switch On-resistance Matching	ΔR_{ONS}	—	20	—	5	20	—	20	%	I_{SIG} = 5 mA, V_{PP} = +100V, V_{NN} = –100V	
Large Signal Switch On-resistance	R_{ONL}	—	—	—	15	—	—	—	Ω	V_{SIG} = V_{PP}–10V, I_{SIG} = 1A	
Output Switch Shunt Resistance	R_{INT}	—	—	35	50	65	—	—	kΩ	Output switch to R_{GND}, I_{RINT} = 0.5 mA	
Switch-off Leakage per Switch	I_{SOL}	—	5	—	1	10	—	15	µA	V_{SIG} = V_{PP}–10V and V_{NN}+10V	
DC Offset Switch Off	V_{OS}	—	50	—	—	50	—	50	mV	No load, R_{GND} = 0V	
DC Offset Switch On		—	50	—	—	50	—	50	mV	No load, R_{GND} = 0V	
V_{PP} Supply Quiescent Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches off	
V_{NN} Supply Quiescent Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches off	
V_{PP} Supply Quiescent Current	I_{PPQ}	—	—	—	10	50	—	—	µA	All switches on, I_{SW} = 5 mA	
V_{NN} Supply Quiescent Current	I_{NNQ}	—	—	—	–10	–50	—	—	µA	All switches on, I_{SW} = 5 mA	
Switch Output Peak Current	I_{SW}	—	2	—	—	2	—	2	A	V_{SIG} duty cycle < 0.1%, pulse width ≤1 µs	
Output Switching Frequency	f_{SW}	—	—	—	—	50	—	—	kHz	Duty cycle = 50%	
Average V_{PP} Supply Current	I_{PP}	—	5.2	—	—	5.6	—	6.4	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	3.2	—	—	4.5	—	4.5		V_{PP} = +100V, V_{NN} = –100V	
		—	3.2	—	—	4	—	4.5		V_{PP} = +160V, V_{NN} = –40V	
Average V_{NN} Supply Current	I_{NN}	—	5.2	—	—	5.6	—	6.4	mA	V_{PP} = +40V, V_{NN} = –160V	All output switches turn on and off at 50 kHz with no load.
		—	3.2	—	—	4	—	4.5		V_{PP} = +100V, V_{NN} = –100V	
		—	3.2	—	—	4	—	4.5		V_{PP} = +160V, V_{NN} = –40V	
Logic Supply Average Current	I_{DD}	—	2	—	—	2	—	2	mA	f_{CLK} = 5 MHz, V_{DD} = 5V	
Logic Supply Quiescent Current	I_{DDQ}	—	10	—	—	10	—	10	µA	All logic inputs are static	
Data Out Source Current	I_{SOR}	0.45	—	0.45	0.7	—	0.4	—	mA	V_{OUT} = V_{DD}–0.7V	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all values are over operating conditions.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Data Out Sink Current	I_{SINK}	0.45	—	0.45	0.7	—	0.4	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	10	—	—	10	—	10	pF	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions, V_{DD} = 5V, $t_R = t_F \leq 5$ ns, 50% duty cycle, C_{LOAD} = 20 pF unless otherwise specified.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Set-up Time before $\overline{LE}$ Rises	t_{SD}	25	—	25	—	—	25	—	ns	
Time Width of $\overline{LE}$	t_{WLE}	12	—	—	12	—	12	—	ns	V_{DD} = 5V
Clock Delay Time to Data Out	t_{DO}	15	40	15	30	40	15	40	ns	V_{DD} = 5V
Time Width of CLR	t_{WCL}	55	—	55	—	—	55	—	ns	
Set-up Time Data to Clock	t_{SU}	7	—	—	7	—	7	—	ns	V_{DD} = 5V
Hold Time Data from Clock	t_H	2	—	2	—	—	2	—	ns	
Clock Frequency	f_{CLK}	—	20	—	—	20	—	20	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
Clock Rise and Fall Times	t_r, t_f	—	50	—	—	50	—	50	ns	
Turn-on Time	t_{ON}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP}–10V$, R_{LOAD} = 10 kΩ
Turn-off Time	t_{OFF}	—	5	—	—	5	—	5	µs	$V_{SIG} = V_{PP}–10V$, R_{LOAD} = 10 kΩ
Maximun V_{SIG} Slew Rate	dv/dt	—	20	—	—	20	—	20	V/ns	V_{PP} = +40V, V_{NN} = –160V
		—	20	—	—	20	—	20		V_{PP} = +100V, V_{NN} = –100V
		—	20	—	—	20	—	20		V_{PP} = +160V, V_{NN} = –40V
Off Isolation	K_O	–30	—	–30	–33	—	–30	—	dB	f = 5 MHz, 1 kΩ//15 pF load
		–58	—	–58	—	—	–58	—		f = 5 MHz, 50Ω load
Switch Crosstalk	K_{CR}	–60	—	–60	–70	—	–60	—	dB	f = 5 MHz, 50Ω load
Output Switch Isolation Diode Current	I_{ID}	—	300	—	—	300	—	300	mA	300 ns pulse width, 2% duty cycle
Off Capacitance SW to GND	$C_{SG(OFF)}$	5	17	5	12	17	5	17	pF	0V, f = 1 MHz
On Capacitance SW to GND	$C_{SG(ON)}$	25	50	25	38	50	25	50	pF	0V, f = 1 MHz

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

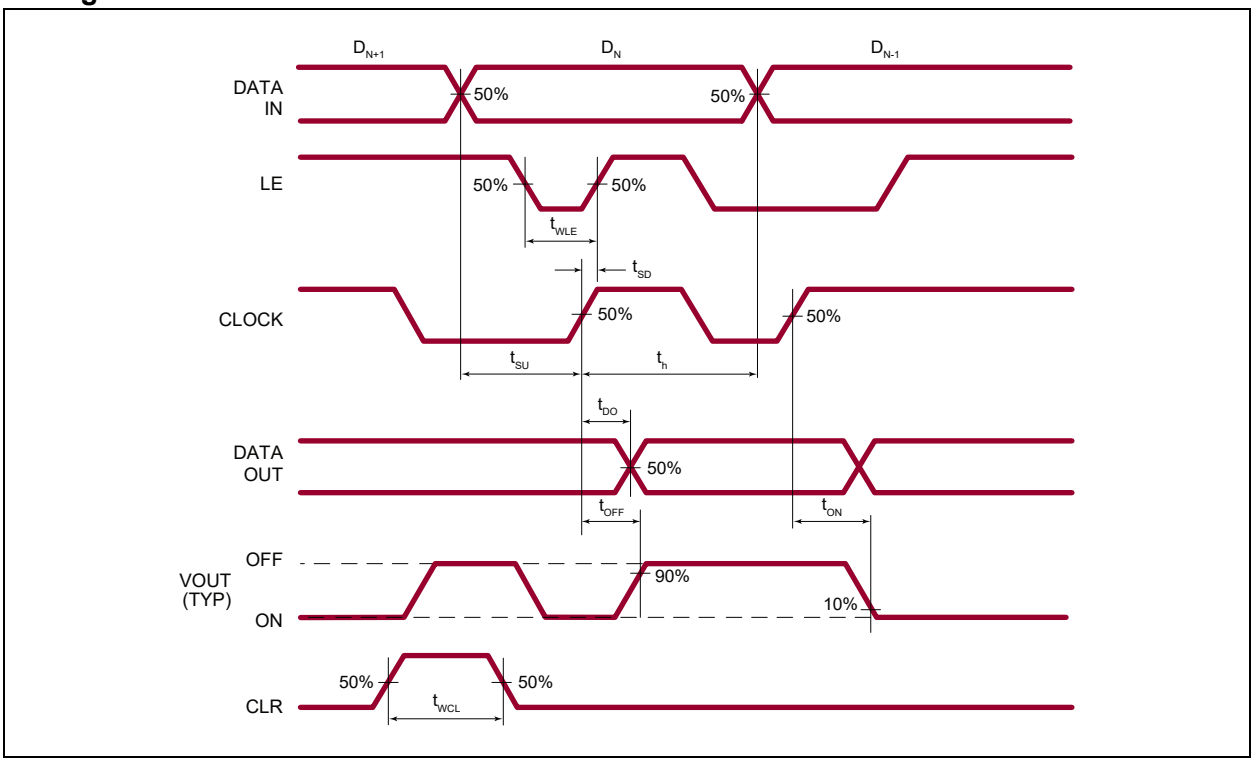
Electrical Specifications: Over operating conditions, V_{DD} = 5V, $t_R = t_F \leq 5$ ns, 50% duty cycle, C_{LOAD} = 20 pF unless otherwise specified.

Parameter	Sym.	0°C		+25°C			+70°C		Unit	Conditions
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
Output Voltage Spike	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +40V, V_{NN} = –160V, R_{LOAD} = 50Ω
	$-V_{SPK}$	—	—	—	—	150	—	—		
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +100V, V_{NN} = –100V, R_{LOAD} = 50Ω
	$-V_{SPK}$	—	—	—	—	150	—	—		
	$+V_{SPK}$	—	—	—	—	150	—	—	mV	V_{PP} = +160V, V_{NN} = –40V, R_{LOAD} = 50Ω
	$-V_{SPK}$	—	—	—	—	150	—	—		

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	0	—	70	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
48-lead LQFP	θ_{JA}	—	52	—	°C/W	

Timing Waveforms



TRUTH FUNCTION TABLE

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L								L	L	$\overline{SW0}$							
H								L	L	SW0							
	L							L	L		$\overline{SW1}$						
	H							L	L		SW1						
		L						L	L			$\overline{SW2}$					
		H						L	L			SW2					
			L					L	L				$\overline{SW3}$				
			H					L	L				SW3				
				L				L	L					$\overline{SW4}$			
				H				L	L					SW4			
					L			L	L						$\overline{SW5}$		
					H			L	L						SW5		
						L		L	L							$\overline{SW6}$	
						H		L	L							SW6	
							L	L	L								$\overline{SW7}$
							H	L	L								SW7
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	$\overline{SW0}$	$\overline{SW1}$	$\overline{SW2}$	$\overline{SW3}$	$\overline{SW4}$	$\overline{SW5}$	$\overline{SW6}$	$\overline{SW7}$

Note 1: Serial data is clocked in on the L to H transition clock.

2: All switches go to a state retaining their present condition at the rising edge of $\overline{LE}$.

3: When $\overline{LE}$ is low, the Shift register data flow through the latch.

4: D_{OUT} is high when data in the Shift register 7 is high.

5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR clear input overrides all other inputs.

2.0 PIN DESCRIPTION

The description of pins in HV2733 are listed in Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SW0	SW terminal of analog switch 0
2	Y0	Y terminal of analog switch 0
3	$\overline{SW0}$	$\overline{SW}$ terminal of analog switch 0
4	NC	No connection
5	SW1	SW terminal of analog switch 1
6	Y1	Y terminal of analog switch 1
7	$\overline{SW1}$	$\overline{SW}$ terminal of analog switch 1
8	NC	No connection
9	SW2	SW terminal of analog switch 2
10	Y2	Y terminal of analog switch 2
11	$\overline{SW2}$	$\overline{SW}$ terminal of analog switch 2
12	NC	No connection
13	SW3	SW terminal of analog switch 3
14	Y3	Y terminal of analog switch 3
15	$\overline{SW3}$	$\overline{SW}$ terminal of analog switch 3
16	NC	No connection
17	VNN	High-voltage negative supply
18	NC	No connection
19	NC	No connection
20	VPP	High-voltage positive supply
21	NC	No connection
22	$\overline{SW4}$	$\overline{SW}$ terminal of analog switch 4
23	Y4	Y terminal of analog switch 4
24	SW4	SW terminal of analog switch 4
25	NC	No connection
26	$\overline{SW5}$	$\overline{SW}$ terminal of analog switch 5
27	Y5	Y terminal of analog switch 5
28	SW5	SW terminal of analog switch 5
29	NC	No connection
30	$\overline{SW6}$	$\overline{SW}$ terminal of analog switch 6
31	Y6	Y terminal of analog switch 6
32	SW6	SW terminal of analog switch 6
33	NC	No connection
34	$\overline{SW7}$	$\overline{SW}$ terminal of analog switch 7
35	Y7	Y terminal of analog switch 7
36	SW7	SW terminal of analog switch 7
37	RGND	Ground for bleed resistor

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
38	GND	Ground
39	VDD	Logic supply voltage
40	DOUT	Data out logic output
41	NC	No connection
42	NC	No connection
43	NC	No connection
44	CLR	Latch clear logic input
45	$\overline{LE}$	Latch enable logic input, low active
46	CLK	Clock logic input for shift registers
47	DIN	Data in logic input
48	RGND	Ground for bleed resistor

3.0 FUNCTIONAL DESCRIPTION

3.1 Test Circuits

Figure 3-1 to Figure 3-7 show the test circuits for HV2733.

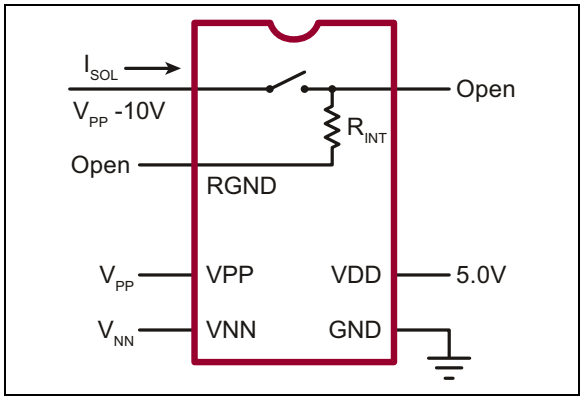


FIGURE 3-1: *Switch Off Leakage.*

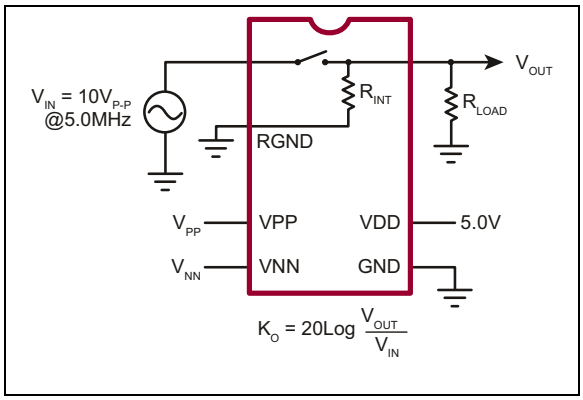


FIGURE 3-4: *Off Isolation.*

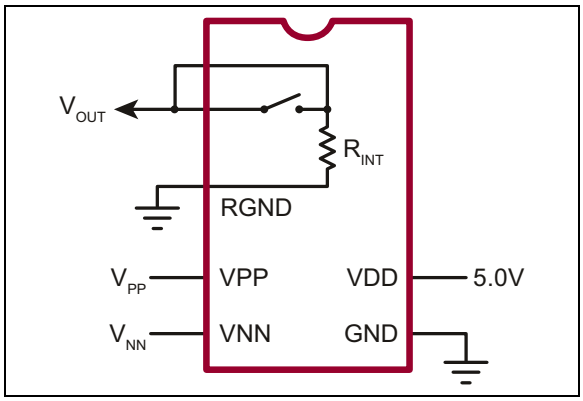


FIGURE 3-2: *DC Offset On/Off.*

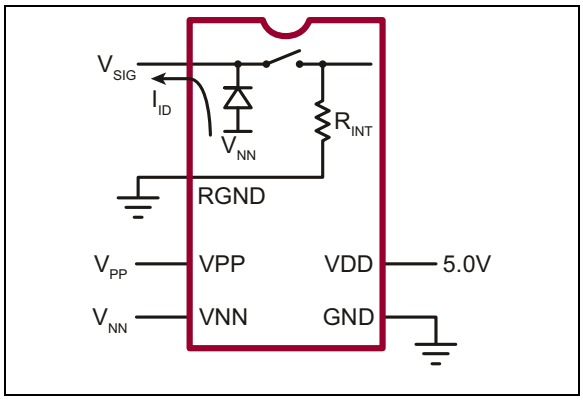


FIGURE 3-5: *Isolation Diode Current.*

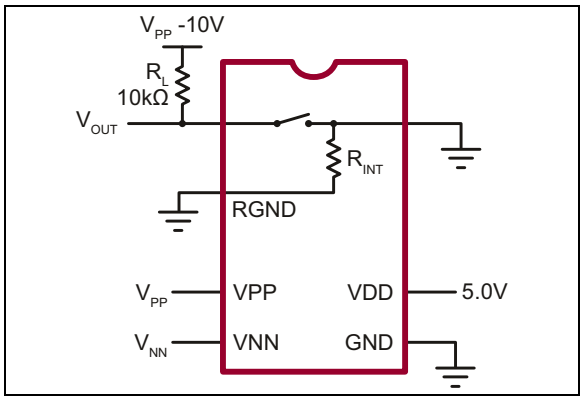


FIGURE 3-3: *T_{ON}/T_{OFF} Test Circuit.*

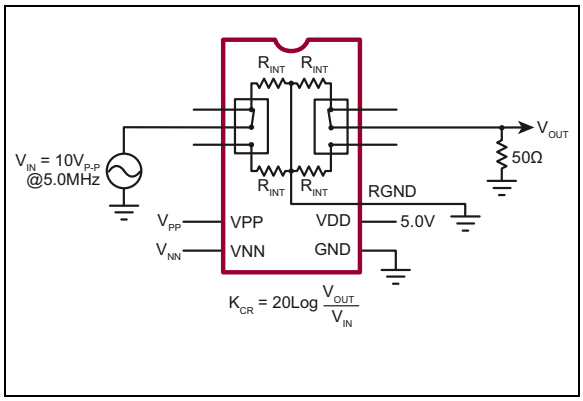


FIGURE 3-6: *Crosstalk.*

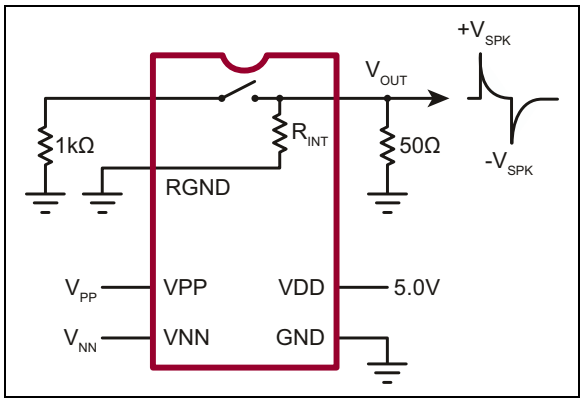
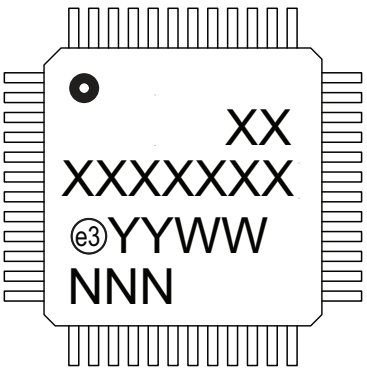


FIGURE 3-7: *Output Voltage Spike.*

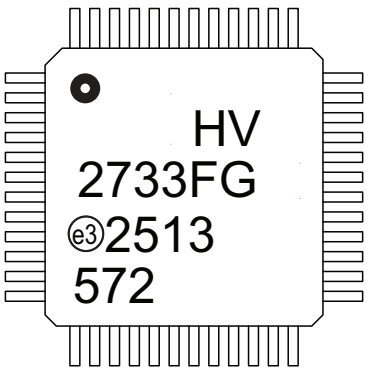
4.0 PACKAGE MARKING INFORMATION

4.1 Package Marking Information

48-lead LQFP



Example

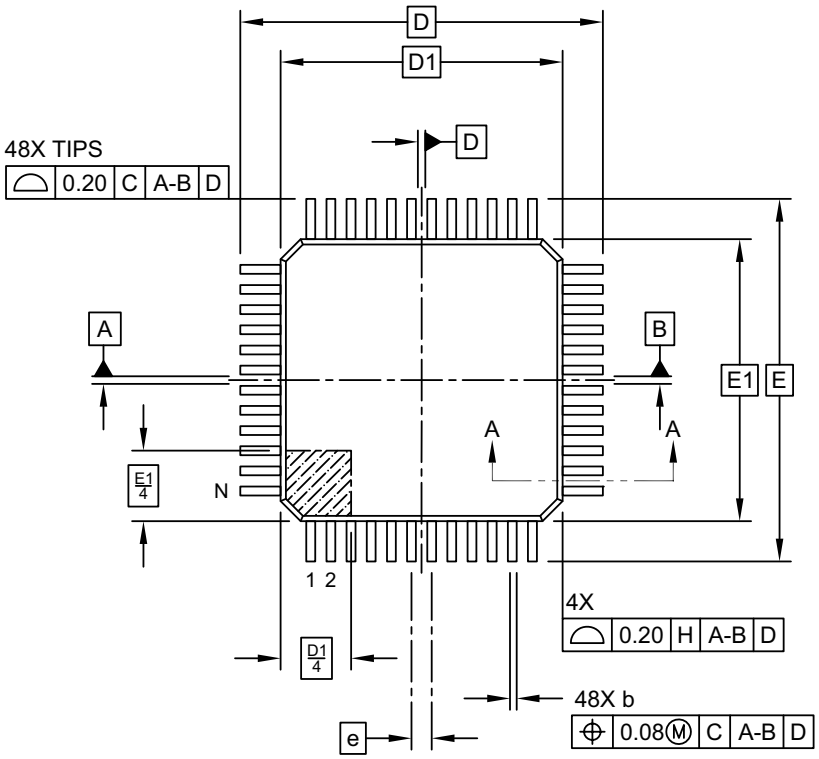


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

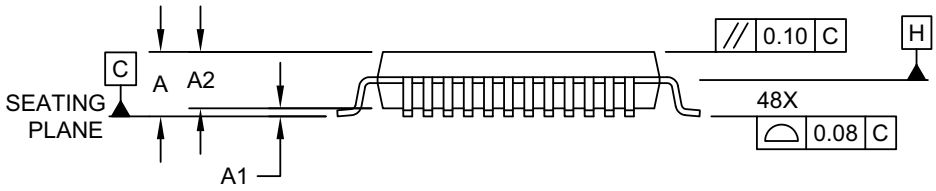
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

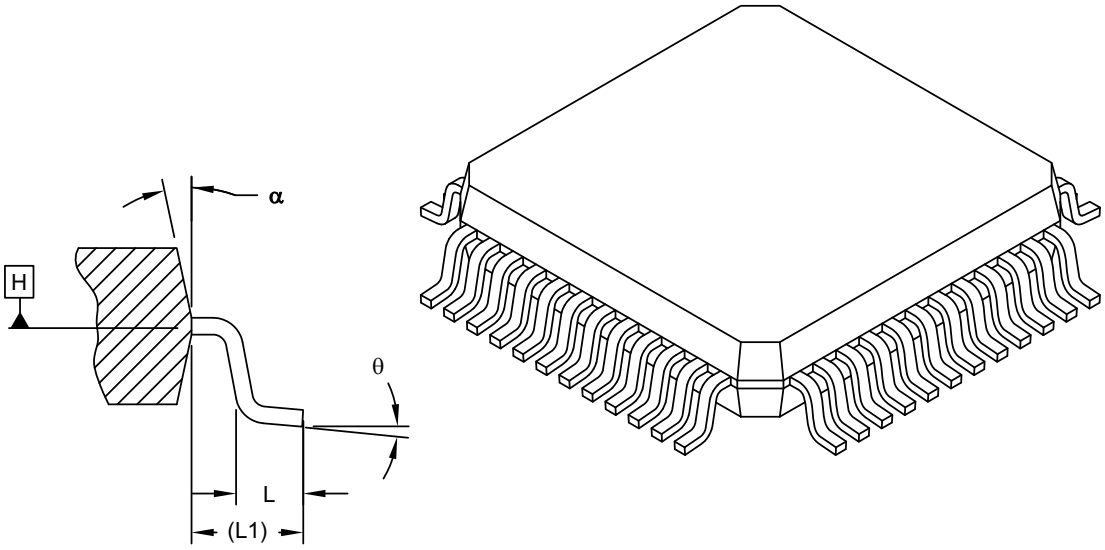


SIDE VIEW

Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

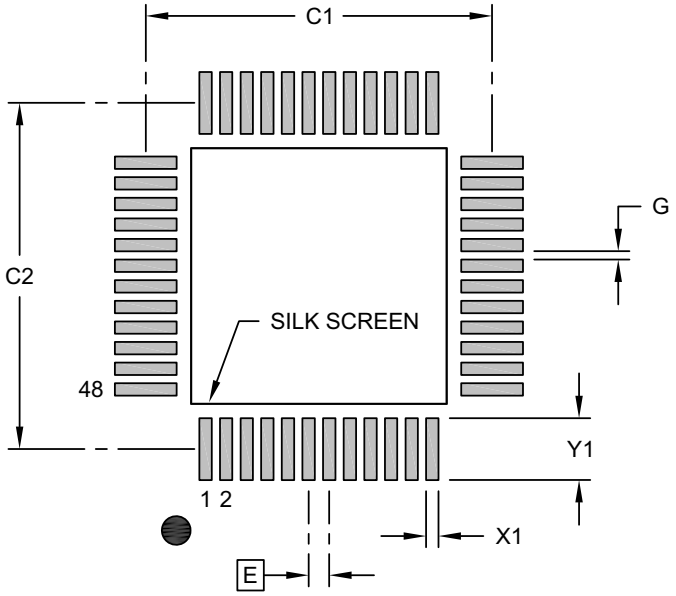
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278 Rev A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2278 Rev A

APPENDIX A: REVISION HISTORY

Revision A (February 2025)

- Converted Supertex Doc # DSFP-HV2733 to Microchip DS20005838A
- Removed “HVCMOS® Technology for high performance” in the Features and General Description sections
- Removed the 48-lead LQFP M931 media type to align packaging specifications with the actual BQM
- Changed the package marking format
- Updated package outline drawings
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV2733	=	16-Channel Low-Harmonic-Distortion High-Voltage Analog Switch with Bleed Resistors
Package:	FG	=	48-lead LQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	250/Tray for an FG Package

Example:

a) HV2733FG-G: 16-Channel Low-Harmonic-Distortion High-Voltage Analog Switch with Bleed Resistors, 48-lead LQFP, 250/Tray

NOTES:

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