Ultralow Profile, 500 mA, 6 MHz, Synchronous, Step-Down, DC-to-DC Converters

Data Sheet

ADP2126/ADP2127

FEATURES

- 1.20 V and 1.26 V fixed output voltage options
- Clock signal enable
  - Logic signal enable also available on certain models
- 6 MHz operating frequency
- Spread spectrum frequency modulation to reduce EMI
- 500 mA continuous output current
- Input voltage: 2.1 V to 5.5 V
- 0.3 µA (typical) shutdown supply current
- Pin-selectable power-saving mode
- Compatible with tiny multilayer inductors
- Internal synchronous rectifier
- Internal compensation
- Internal soft start
- Output-to-ground short-circuit protection
- Current-limit protection
- Undervoltage lockout
- Thermal shutdown protection
- 0.330 mm height (maximum), 6-ball BUMPED_CHIP (ADP2126)
- 0.200 mm height (maximum), 6-pad EWLP (ADP2127)

APPLICATIONS

- Mobile phones
- Digital still/video cameras
- Digital audio
- Portable equipment
- Camera modules
- Image stabilization systems

TYPICAL APPLICATIONS CIRCUIT

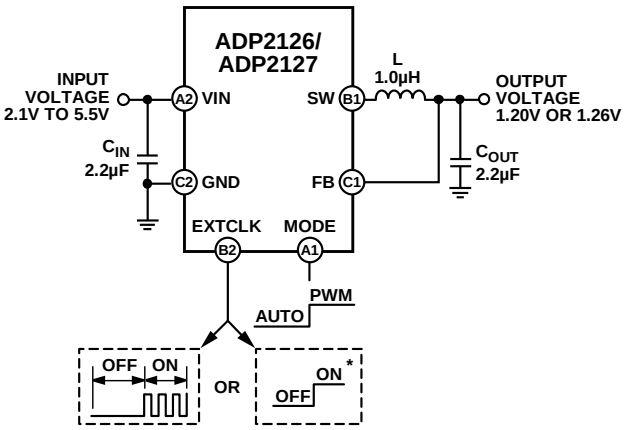

Figure 1.

GENERAL DESCRIPTION

The ADP2126/ADP2127 are high frequency, step-down, dc-to-dc converters optimized for portable applications in which board area and battery life are critical constraints. The fixed 6 MHz operating frequency enables the use of tiny ceramic inductors and capacitors and the regulators use spread spectrum frequency modulation to reduce EMI. Additionally, synchronous rectification improves efficiency and results in fewer external components.

At high load currents, the ADP2126/ADP2127 use a voltage regulating pulse-width modulation (PWM) mode that maintains a constant frequency with excellent stability and transient response. Light load operation is determined by the state of the MODE pin. In forced PWM mode, the converter continues operating in PWM for light loads. Under light load conditions in auto mode, the ADP2126/ADP2127 automatically enter a power-saving mode, which uses pulse frequency modulation (PFM) to reduce the effective switching frequency, thus ensuring the longest battery life in portable applications.

The ADP2126/ADP2127 are enabled by a 6 MHz to 27 MHz external clock signal applied to the EXTCLK pin. Certain models can also be enabled with a logic high signal. When the external clock is not switching and in a low logic state, the ADP2126/ADP2127 stop regulating and shut down to draw less than 0.3 µA (typical) from the source.

The ADP2126/ADP2127 have an input voltage range of 2.1 V to 5.5 V, allowing the use of single Li+/Li polymer cell, three-cell alkaline, NiMH cell, and other standard power sources. The ADP2126/ADP2127 are internally compensated to minimize external components and can source up to 500 mA. Other key features, such as cycle-by-cycle peak current limit, soft start, undervoltage lockout (UVLO), output-to-ground short-circuit protection, and thermal shutdown provide protection for internal and external circuit components.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

3/12—Rev. A to Rev. B

Combined Figure 1 and Figure 2; Renumbered Sequentially ... 1
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Changes to Ordering Guide ... 18

5/11—Rev. 0 to Rev. A

Changes to Figure 35 ... 17

5/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, T_A = 25°C for typical specifications, and T_A = T_J = −40°C to +85°C for minimum and maximum specifications, unless otherwise noted. All specifications at temperature extremes are guaranteed via correlation using the standard statistical quality control (SQC) methods. Typical specifications are not guaranteed.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Operating Input Voltage Range	V_{IN}		2.1		5.5	V
PWM Mode Quiescent Current		No load, $V_{MODE} = V_{IN}$		12		mA
Auto Mode Quiescent Current		No load, V_{MODE} = 0 V, $V_{FB} > V_{OUT}$, SW = open		300	500	µA
Shutdown Current[1]		V_{EXTCLK} = 0 V, open loop		0.3	1.5	µA
UNDERVOLTAGE LOCKOUT						
Rising V_{IN} Threshold				1.9	2.1	V
Falling V_{IN} Threshold			1.5	1.8		V
OUTPUT						
Continuous Output Current[2]	I_{LOAD}	V_{IN} = 2.1 V to 5.5 V	500			mA
PWM Mode Output Accuracy[3]	V_{OUT}	V_{IN} = 2.1 V to 5.5 V, no load	V_{OUT} − 2%		V_{OUT} + 2%	V
PFM Mode Output Accuracy[3, 4]		V_{IN} = 2.1 V to 5.5 V	V_{OUT} − 3%		V_{OUT} + 3%	V
FB Bias Current		$V_{FB} = V_{OUT}$		4	9	µA
FB Pull-Down Resistance	R_{DSCHG}	V_{EXTCLK} = 0 V, I_{FB} = 10 mA		110	180	Ω
SWITCHING CHARACTERISTICS						
PMOS On Resistance		I_{SW} = 500 mA		180	340	mΩ
NMOS On Resistance		I_{SW} = 500 mA		250		mΩ
SW Leakage Current		V_{SW} = 0 V, V_{IN} = 5.5 V			10	µA
PMOS Switch Current Limit		Open loop	770	1000	1291	mA
PFM Current Limit		V_{MODE} = 0 V, V_{IN} = 3.6 V	170	260	305	mA
Oscillator Frequency	f_{SW}		4.8	6	6.8	MHz
SHORT-CIRCUIT PROTECTION						
Rising V_{OUT} Threshold				0.55	0.7	V
Falling V_{OUT} Threshold			0.4	0.52		V
EXTCLK INPUT						
High Threshold Voltage	$V_{EXTCLK(H)}$	V_{IN} = 2.1 V to 5.5 V	1.3			V
Low Threshold Voltage	$V_{EXTCLK(L)}$	V_{IN} = 2. 1 V to 5.5 V			0.4	V
Leakage Current		V_{IN} = 5.5 V, V_{EXTCLK} = 2.1 V to 5.5 V		0.01	1	µA
Duty Cycle Operating Range	D_{EXTCLK}		40		60	%
Frequency Operating Range	f_{EXTCLK}		6		27	MHz
MODE INPUT LOGIC						
High Threshold Voltage	$V_{MODE(H)}$	V_{IN} = 2.1 V to 5.5 V	1.3			V
Low Threshold Voltage	$V_{MODE(L)}$	V_{IN} = 2.1 V to 5.5 V			0.4	V
Leakage Current		V_{EXTCLK} = 0 V, $V_{IN} = V_{MODE}$ = 5.5 V		0.005	1	µA
THERMAL SHUTDOWN[5]		PWM mode only				
Thermal Shutdown Threshold				146		°C
Thermal Shutdown Hysteresis				13		°C

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TIMING		See Figure 2 and Figure 3				
VIN High to EXTCLK On[2]	t_1	V_{IN} = 2.1 V to 5.5 V	200			µs
EXTCLK On to V_{OUT} Rising	$t_{2\ (CLOCK)}$	D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 6 MHz	250	320	400	µs
		D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 27 MHz	250	320	400	µs
EXTCLK On to V_{OUT} Rising	$t_{2\ (LOGIC)}$	EXTCLK = logic high	285	315	385	µs
V_{OUT} Power-Up Time (Soft Start)[2]	t_3	C_{OUT} = 2.2 µF, R_{LOAD} = 3.6 Ω		70	200	µs
EXTCLK Off to V_{OUT} Falling	$t_{5\ (CLOCK)}$	D_{EXTCLK} = 40% to 60%, f_{EXTCLK} = 6 MHz to 27 MHz		9	17	µs
EXTCLK Off to V_{OUT} Falling	$t_{5\ (LOGIC)}$	EXTCLK = logic high, no load		0		µs
V_{OUT} Power-Down Time	t_6	C_{OUT} = 2.2 µF, R_{LOAD} = 3.6 Ω		16		µs
		C_{OUT} = 2.2 µF, no load		465		µs
Minimum Shutdown Time[2]	$t_5 + t_6$	C_{OUT} = 2.2 µF, no load	1400			µs
Minimum Power-Off Time[2]	t_7		500			µs

[1] The total shutdown current is the addition of VIN shutdown current and SW leakage.
[2] Guaranteed by design.
[3] Transients not included in voltage accuracy specifications.
[4] The PFM output voltage will be higher than the PWM output voltage. See the Typical Performance Characteristics section.
[5] Thermal shutdown protection is only active in PWM mode.

TIMING DIAGRAMS

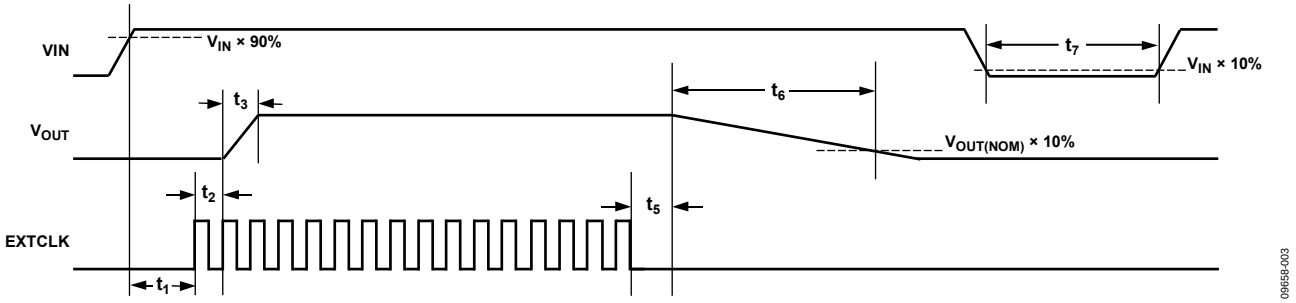

Figure 2. Clock Enable I/O Timing Diagram

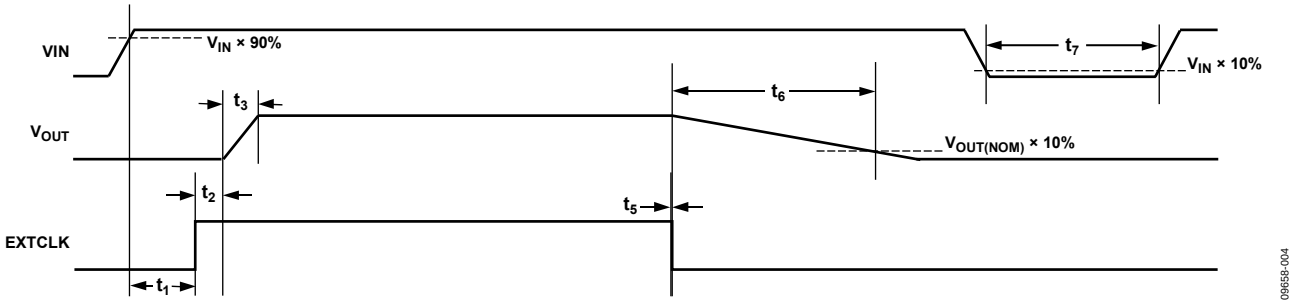

Figure 3. Logic Enable I/O Timing Diagram (Logic High Enable Feature Available Only on Certain Models)

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +6 V
EXTCLK to GND	−0.3 V to +6 V
SW, MODE to GND	−0.3 V to VIN
FB to GND	−0.3 V to +3.6 V
Operating Ambient Temperature (T_A)	−40°C to +85°C[1]
Operating Junction Temperature (T_J) at I_{LOAD} = 500 mA	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

[1] The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$). See the Thermal Considerations section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL CONSIDERATIONS

The maximum operating junction temperature ($T_{J(MAX)}$) supersedes the maximum operating ambient temperature ($T_{A(MAX)}$) because the ADP2126/ADP2127 may be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits.

In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and good PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The operating junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). T_J is calculated using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

See the Applications Information section for further information on calculating the operating junction temperature for a specific application.

THERMAL RESISTANCE

θ_{JA} of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions.

θ_{JA} is specified for worst-case conditions, that is, a device soldered on a circuit board for surface-mount packages. θ_{JA} is determined according to JEDEC Standard JESD51-9 on a 4-layer printed circuit board (PCB).

Table 3. Thermal Resistance (4-Layer PCB)

Package Type	θ_{JA}	Unit
6-Ball Bumped Bare Die Sales	105	°C/W
6-Pad Embedded Wafer Level Package	105	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

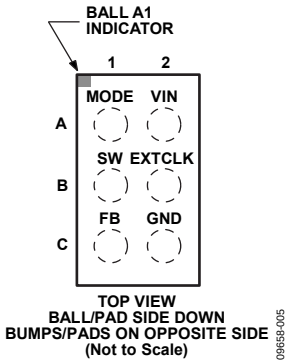

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	MODE	Mode Select. This pin toggles between auto mode (PFM and PWM switching) and PWM mode. Set MODE low to allow the part to operate in auto mode. Pull MODE high to force the part to operate in PWM mode. The voltage applied to MODE should never be higher than the voltage applied to VIN. Do not leave this pin floating.
A2	VIN	Power Supply Input.
B1	SW	Switch Node.
B2	EXTCLK	External Clock Enable Signal. The ADP2126/ADP2127 power up when a clock signal (6 MHz to 27 MHz) or a logic high signal (EXTCLK ≥ 1.3 V) is detected on this pin. (The logic high enable feature is only available on certain models.)
C1	FB	Feedback Divider Input. Connect the output capacitor from FB to GND to set the output voltage ripple and to complete the control loop.
C2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, f_{EXTCLK} = 10 MHz, V_{OUT} = 1.20 V, L = 1.0 µH (CKP1608S1R0), C_{IN} = 2.2 µF (GRM153R60J225ME95), C_{OUT} = 2.2 µF (GRM153R60G225M), and T_A = 25°C, unless otherwise noted.

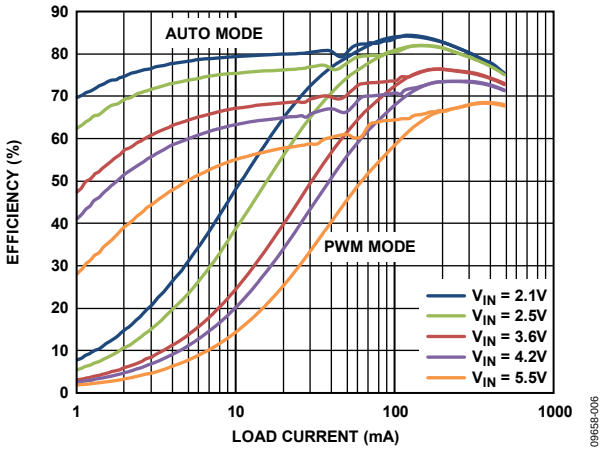

Figure 5. Efficiency vs. Load Current

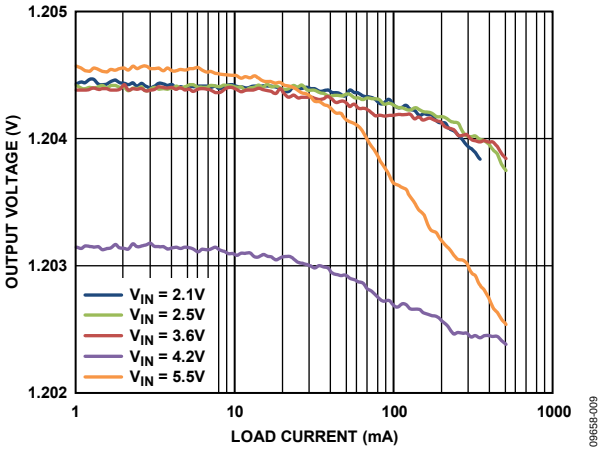

Figure 8. PWM Mode Output Voltage Accuracy

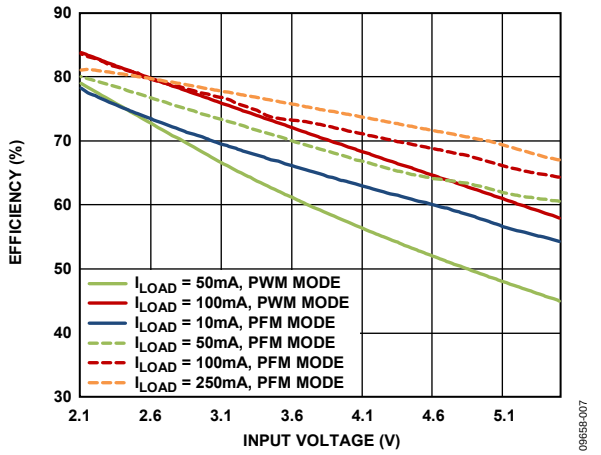

Figure 6. Efficiency vs. Input Voltage

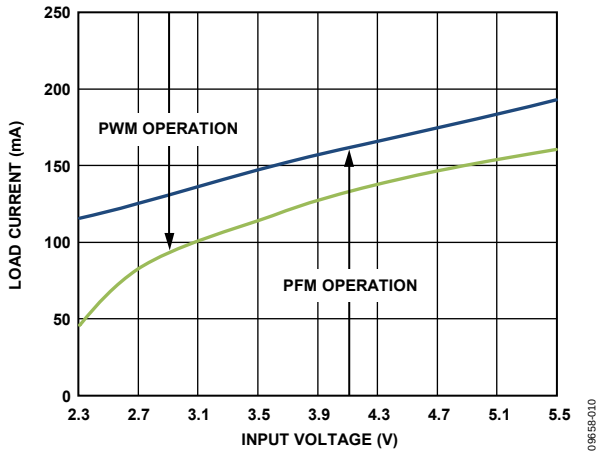

Figure 9. Auto Mode Switching Threshold vs. Input Voltage

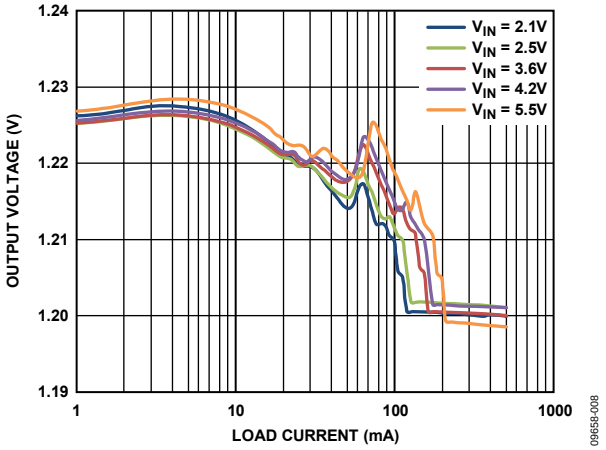

Figure 7. Auto Mode Output Voltage Accuracy

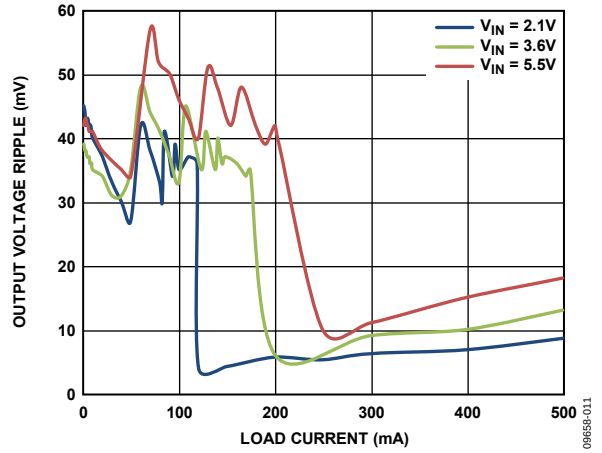

Figure 10. Output Voltage Ripple vs. Load Current

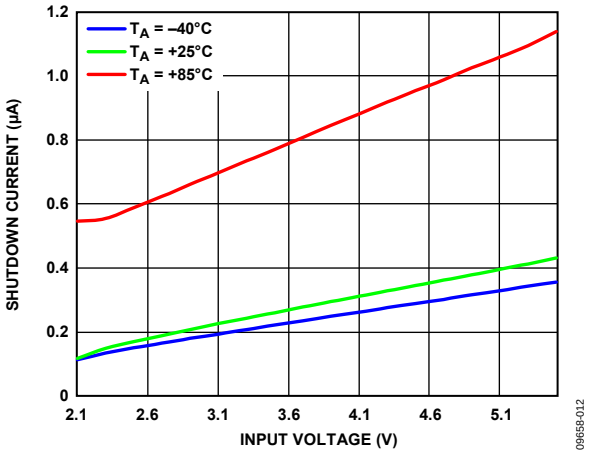

Figure 11. Shutdown Current vs. Input Voltage

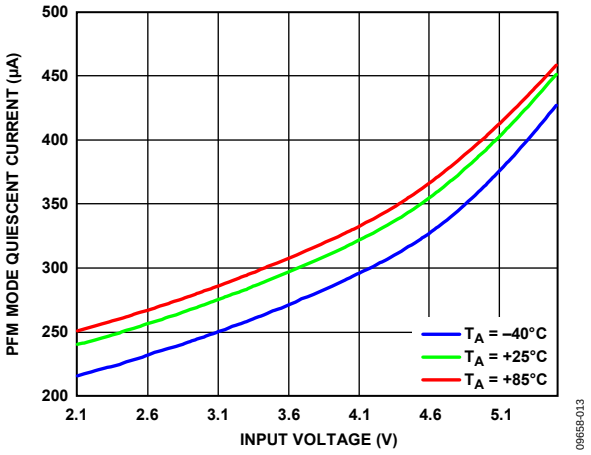

Figure 12. PFM Mode Quiescent Current vs. Input Voltage

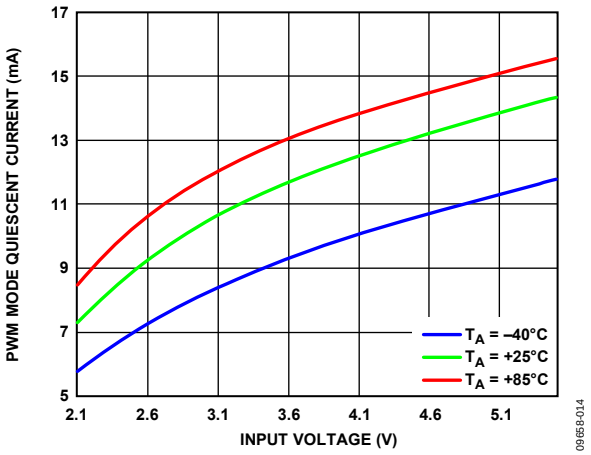

Figure 13. PWM Mode Quiescent Current vs. Input Voltage

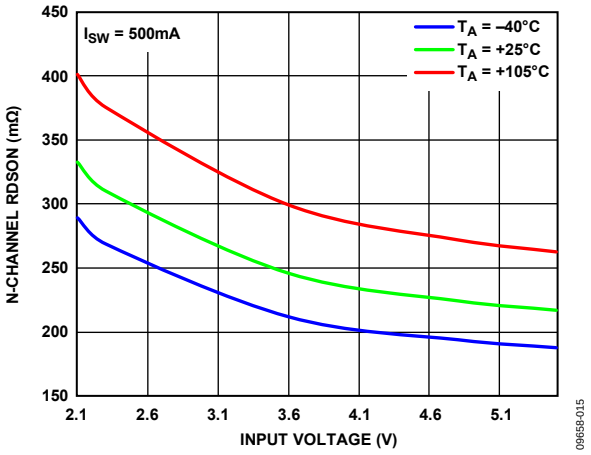

Figure 14. NMOS Drain-to-Source On Resistance

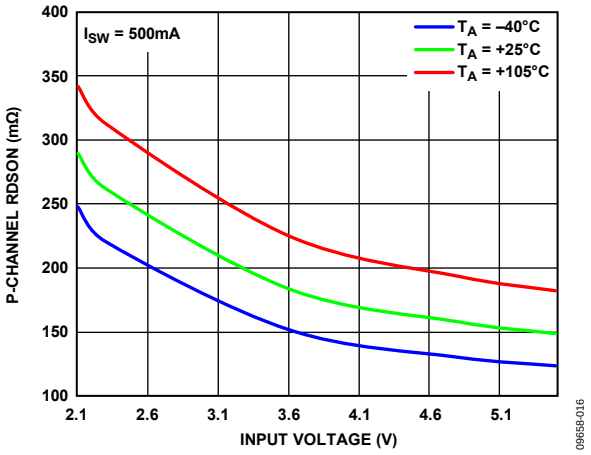

Figure 15. PMOS Drain-to-Source On Resistance

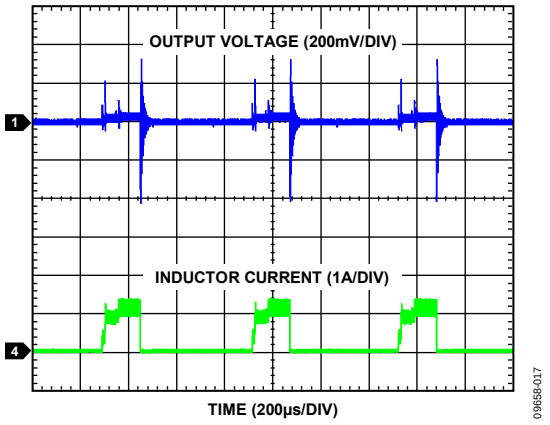

Figure 16. Output Short-Circuit Response

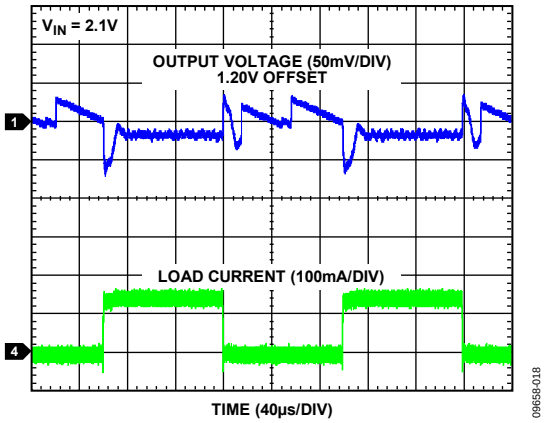

Figure 17. Load Transient Response, 0 mA to 150 mA, V_{IN} = 2.1 V

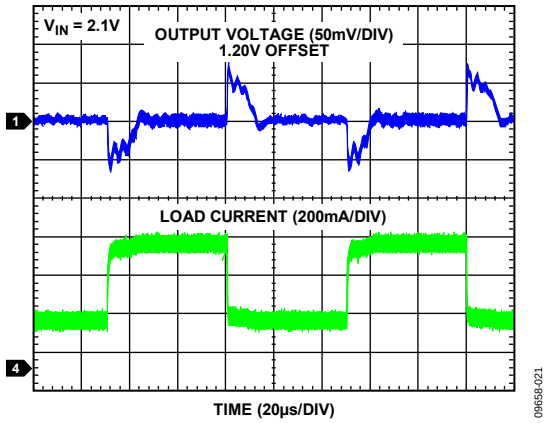

Figure 20. Load Transient Response, 250 mA to 420 mA, V_{IN} = 2.1 V

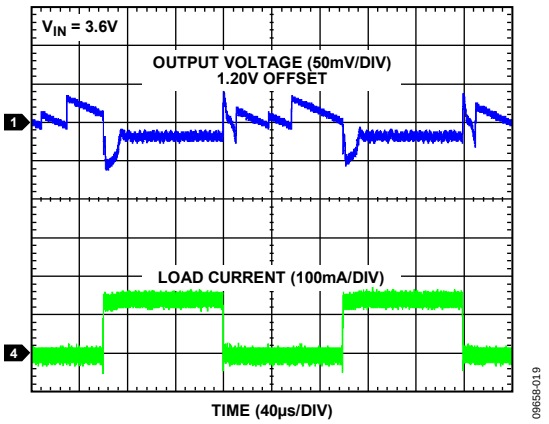

Figure 18. Load Transient Response, 0 mA to 150 mA, V_{IN} = 3.6 V

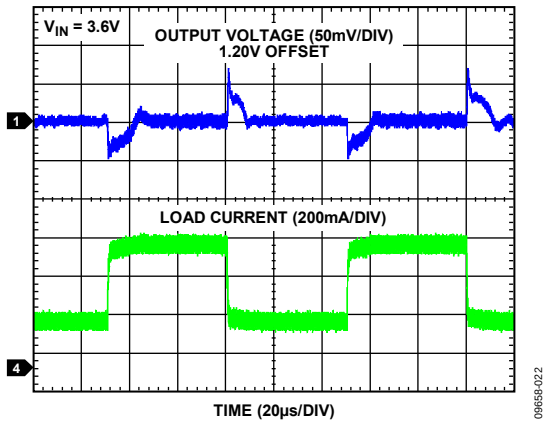

Figure 21. Load Transient Response, 250 mA to 420 mA, V_{IN} = 3.6 V

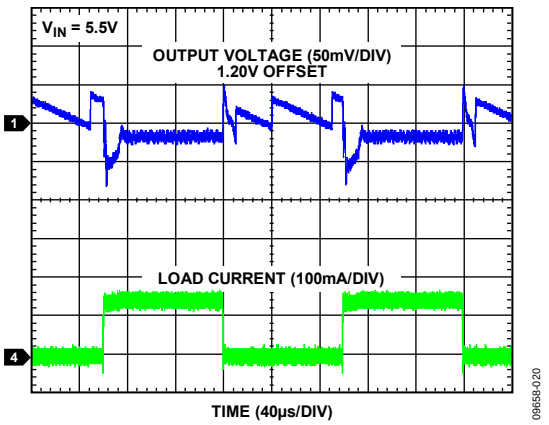

Figure 19. Load Transient Response, 0 mA to150 mA, V_{IN} = 5.5 V

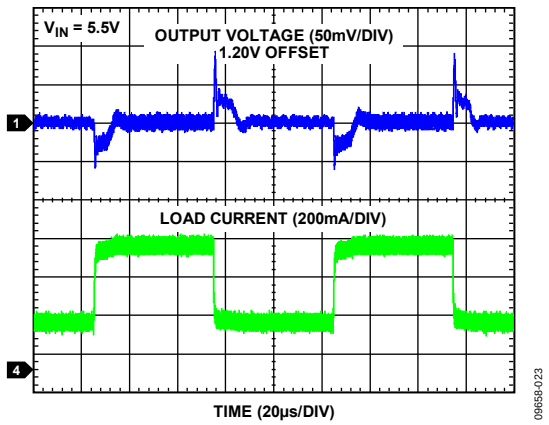

Figure 22. Load Transient Response, 250 mA to 420 mA, V_{IN} = 5.5 V

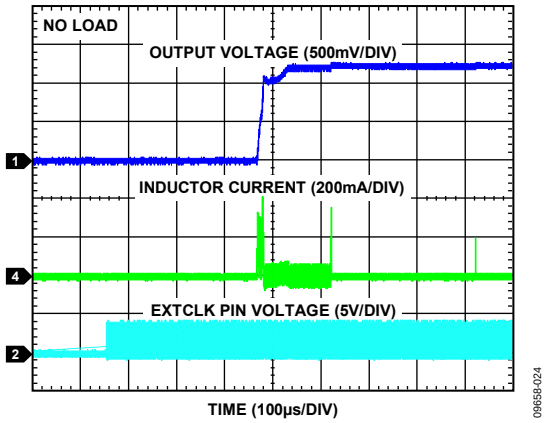

Figure 23. Startup, No Load

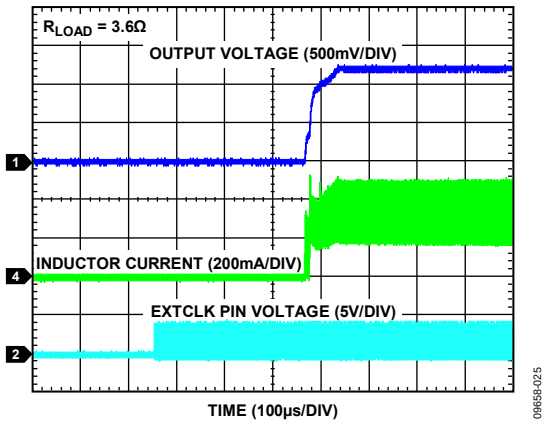

Figure 24. Startup, R_{LOAD} = 3.6 Ω

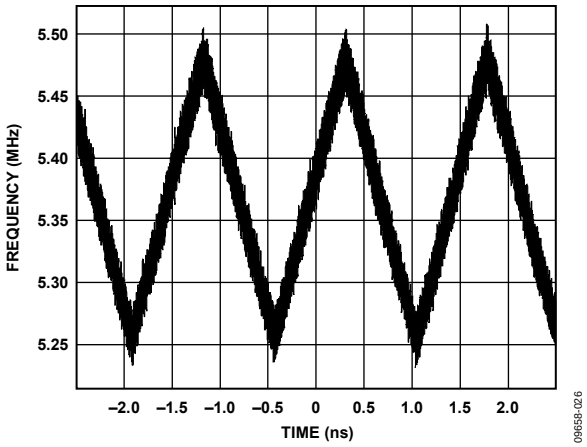

Figure 25. Spread Spectrum Switching Frequency

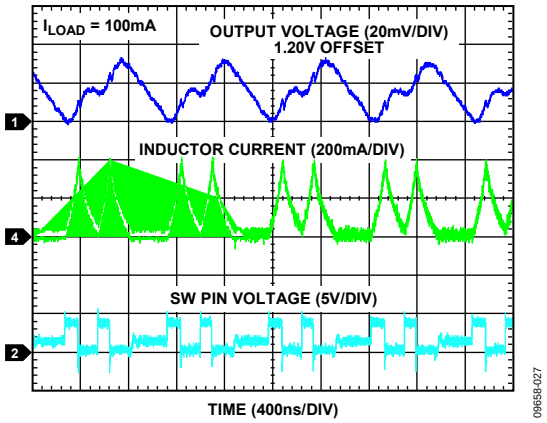

Figure 26. Typical PFM Mode Operation, I_{LOAD} = 100 mA

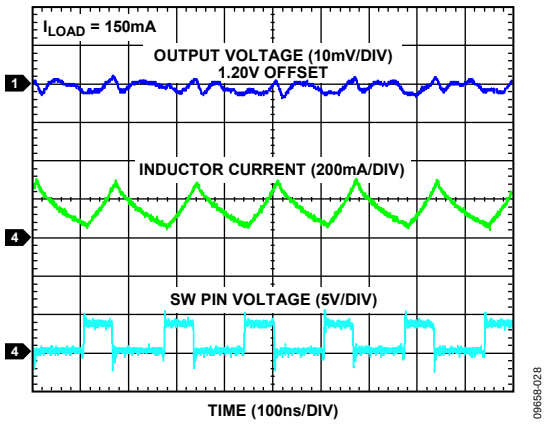

Figure 27. Typical PWM Mode Operation, I_{LOAD} = 150 mA

THEORY OF OPERATION

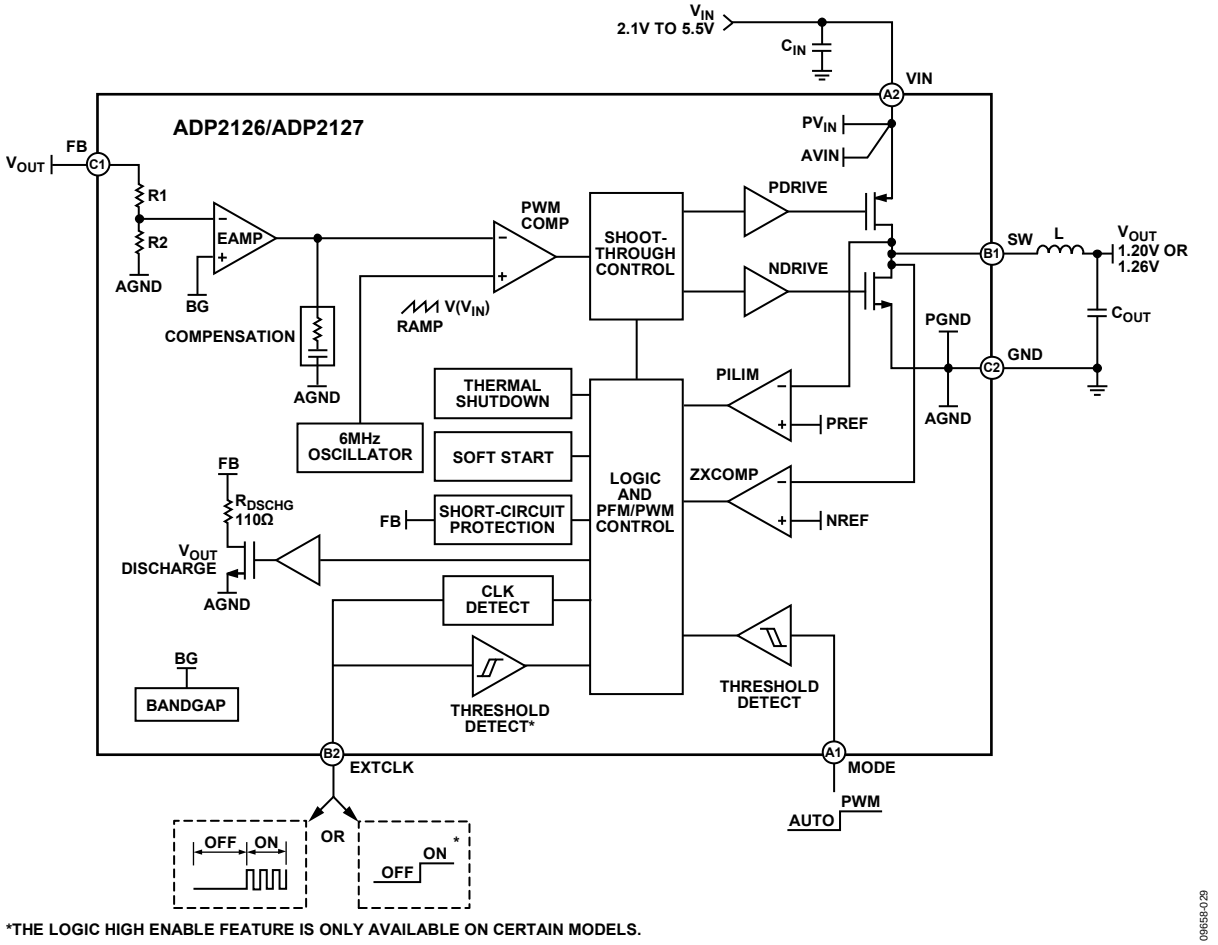

Figure 28. Internal Block Diagram

OVERVIEW

The ADP2126/ADP2127 are high efficiency, synchronous, step-down, dc-to-dc regulators that operate from a 2.1 V to 5.5 V input voltage. They provide up to 500 mA of continuous output current at a fixed output voltage. The 6 MHz operating frequency enables the use of tiny external components. External control for mode selection provides a power-saving option. The internal control schemes of the ADP2126/ADP2127 give excellent stability and transient response. Other internal features, such as cycle-by-cycle peak current limit, soft start, undervoltage lockout, output-to-ground short-circuit protection, and thermal shutdown provide protection for internal circuit components.

EXTERNAL CLOCK (EXTCLK) ENABLE

The ADP2126/ADP2127 are enabled by a 6 MHz to 27 MHz external clock signal applied to the EXTCLK pin. Certain models can also be enabled with a logic high signal (see Figure 2, Figure 3, and Figure 28). When the ADP2126/ ADP2127 are enabled, the converter is able to power up, and the output voltage rises to its nominal value. When the external clock is not switching and in a low logic state, the ADP2126/ADP2127 stop regulating and shut down to draw less than 0.3 µA (typical) from the source.

SPREAD SPECTRUM OSCILLATOR

The ADP2126/ADP2127 incorporate spread spectrum functionality to modulate electromagnetic interference (EMI) for EMI sensitive applications. A typical switching converter with a regulated switching frequency has a narrow frequency spectrum centered at the target switching frequency. This results in a high spectral density around the target frequency with peak emission levels that can exceed the regulatory levels for EMI in many portable, cellular, and wireless applications.

To maintain acceptable levels of EMI, the ADP2126/ADP2127 employs spread spectrum via a controlled variance of the switching frequency over a wider band of frequencies. Figure 25 shows the variance of the frequency over time. This distribution of the frequency content spreads the spectral density over a wider bandwidth, resulting in lower peak emission levels.

MODE SELECTION

The ADP2126/ADP2127 have two modes of operation (PWM mode and auto mode), determined by the state of the MODE pin.

Pull the MODE pin high to force the converter to operate in PWM mode, regardless of the output current. Otherwise, set MODE low to put the converter into auto mode and allow the converter to automatically transition from PWM mode to the power-saving PFM mode at light load currents. Do not leave this pin floating.

Pulse-Width Modulation (PWM) Mode

The PWM mode forces the part to maintain a fixed frequency of 6 MHz (maximum) under all load conditions. The ADP2126/ADP2127 use a proprietary, hybrid voltage-mode control scheme to control the duty cycle under all load current and line voltage variations. This control scheme provides excellent stability, transient response, and output regulation. PWM mode results in lower efficiencies at light load currents.

Auto Mode (PFM and PWM Switching)

Auto mode is a power-saving feature that enables the converter to switch between PWM and PFM in response to the output load. Auto mode is enabled when the MODE pin is pulled low. In auto mode, the ADP2126/ADP2127 operate in PFM mode for light load currents and switch to PWM mode for medium and heavy load currents.

Pulse Frequency Modulation (PFM) Mode

When the converter is operating under light load conditions, the effective switching frequency and supply current are decreased and varied using PFM to regulate the output voltage. This results in improved efficiencies and lower quiescent currents. In PFM mode, the converter only switches when necessary to keep the output voltage within the PFM limits set by an internal comparator. Switching stops when the upper limit is reached and resumes when the lower limit is reached.

When the upper level is reached, the output stage and most control circuitry turn off to reduce the quiescent current. During this stage, the output capacitor supplies the current to the load. As the output capacitor discharges and the output voltage reaches the lower PFM comparator threshold, switching resumes and the process repeats.

Mode Transition

When the MODE pin is low, the converter switches between PFM and PWM modes automatically to maintain optimal transient response and efficiency. The mode transition point depends on the input voltage. Hysteresis exists in the transition point to prevent instability and decreased efficiencies that could result if the converter were able to oscillate between PFM and PWM for a fixed input voltage and load current. See Figure 9 for the typical PFM and PWM mode boundaries of the ADP2126/ADP2127.

A switch from PFM to PWM occurs when the output voltage dips below the nominal value of the output voltage option. Switching to PWM allows the converter to maintain efficiency and supply a larger current to the load. The output voltage in PFM mode is slightly higher to keep the ADP2126/ADP2127 from oscillating between modes, ensuring stable operation.

The switch from PWM to PFM occurs when the output current is below the PFM threshold for multiple consecutive switching cycles. Switching to PFM allows the converter to save power by supplying the lighter load current with fewer switching cycles.

INTERNAL CONTROL FEATURES

Synchronous Rectification

In addition to the P-channel MOSFET switch, the ADP2126/ADP2127 include an N-channel MOSFET switch to build the synchronous rectifier. The synchronous rectifier improves efficiency, especially for small load currents, and reduces cost and board space by eliminating the need for an external rectifier.

Soft Start

To prevent excessive input inrush current at startup, the ADP2126/ADP2127 operate with an internal soft start. When EXTCLK begins to oscillate, or when the part recovers from a fault (UVLO, TSD, or SCP), a soft start timer begins. During this time, the peak current limit is gradually increased to its maximum. The output voltage increases in stages to ensure that the converter is able to start up effectively and in proper sequence. After the soft start period expires, the peak PMOS switch current limit remains at 1 A (typical), and the part begins normal operation.

PROTECTION FEATURES

Overcurrent Protection

To ensure that excessively high currents do not damage the MOSFET switches, the ADP2126/ADP2127 incorporate cycle-by-cycle overcurrent protection. This function is accomplished by monitoring the instantaneous peak current on the power PMOS switch. If this current exceeds the PMOS switch current limit (1 A typical), then the PMOS is immediately turned off. This minimizes the potential for damage to power components during certain faults and transient events.

Output Short-Circuit Protection (SCP)

If the output voltage is shorted to GND, a standard dc-to-dc controller delivers maximum power into that short. This may result in a potentially catastrophic failure. To prevent this, the ADP2126/ADP2127 sense when the output voltage is below the SCP threshold (typically 0.52 V). At this point, the controller turns off for approximately 450 µs and then automatically initiates a soft start sequence. This cycle repeats until the short is removed or the part is disabled. Figure 16 shows the operating behavior of the ADP2126/ADP2127 during a short-circuit fault. The SCP dramatically reduces the power delivered into the short circuit, yet still allows the converter to recover when the fault is removed.

Thermal Shutdown (TSD) Protection

The ADP2126/ADP2127 also include TSD protection when the part is in PWM mode only. If the die temperature exceeds 146°C (typical), the TSD protection activates and turns off both MOSFET power devices. They remain off until the die temperature falls to 133°C (typical), at which point the regulator restarts.

Undervoltage Lockout (UVLO)

If the input voltage drops below the UVLO falling threshold, the ADP2126/ADP2127 automatically turn off the power switches and enter a low power consumption mode. This prevents potentially erratic operation at low input voltages. The parts remain in this state until the input voltage rises above the UVLO rising threshold. The UVLO levels have approximately 100 mV of hysteresis to ensure glitch-free startup.

For the logic high enable option, during startup and UVLO recovery after the input voltage drops below the UVLO falling threshold, EXTCLK must be powered with the logic high signal after VIN. If V_{IN} dips below the UVLO falling threshold and EXTCLK is powered before VIN with a logic high signal, the UVLO does not become active. If VIN and EXTCLK are powered from the same source, an RC circuit (see Figure 1) is recommended to ensure that the ADP2126/ADP2127 are powered correctly. R_τ and C_τ should be selected so that the RC time constant (τ) is greater than the 200 µs minimum specification for VIN high to EXTCLK on (t_1). τ is calculated using the following equation:

$$\tau = R_\tau \times C_\tau$$

where $\tau \geq t_1$.

See Table 1 and Figure 3 for the timing specifications and diagrams.

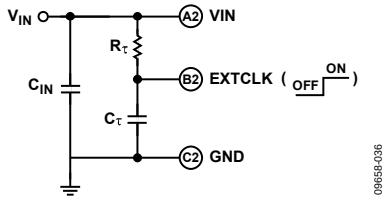

Figure 29. Recommended Logic Enable Startup Circuit

TIMING CONSTRAINTS

Shutdown Time

When the ADP2126/ADP2127 enter shutdown mode after the EXTCLK signal is removed, the ADP2126/ADP2127 must remain in shutdown mode for a minimum of 1400 µs, if no load is applied, before the EXTCLK signal can be reapplied. This allows all internal nodes to discharge to an off state.

Power-Off Time

When V_{IN} drops, thereby triggering UVLO, the ADP2126/ADP2127 have a minimum power-off time (t_7) of 500 µs that must elapse before V_{IN} can be reapplied. This allows all internal nodes to discharge enough power so that all internal devices are in an off state.

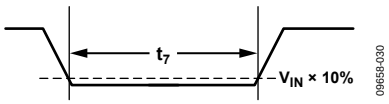

Figure 30. Power-Off Time

APPLICATIONS INFORMATION

The low-profile ADP2126/ADP2127 are compatible with chip inductors and multilayer ceramic capacitors that are ideal for use in portable applications due to their small footprint and low height. The recommended components for low-profile applications may change as this technology advances. Table 5 and Table 6 list compatible inductors and capacitors.

This section describes the selection of external components. The component value ranges are limited to optimize efficiency and transient performance while maintaining stability over the full operating range.

INDUCTOR SELECTION

The high switching frequency of the ADP2126/ADP2127 allows for minimal output voltage ripple, even with small inductors. Inductor sizing is a trade-off between efficiency and transient response. A small value inductor leads to a larger inductor current ripple, which provides excellent transient response but degrades efficiency. A small footprint and low height chip inductor can be used for an overall smaller solution size but has a higher dc resistance (DCR) value and lower current rating that can degrade performance. Shielded ferrite core inductors are advantageous for their low core losses and low electromagnetic interference (EMI). For optimal performance and stability, use inductor values between 1.5 µH and 0.5 µH. Recommended inductors are shown in Table 5.

The inductor peak-to-peak current ripple, ΔI_L, is calculated from

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times L \times f_{SW}} \quad (2)$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

It is important that the minimum dc current rating of the inductor be greater than the peak inductor current (I_{PK}) in the application. I_{PK} is calculated from

$$I_{PK} = I_{LOAD(MAX)} + \Delta I_L/2 \quad (3)$$

The dc current rating of the inductor should be greater than the calculated I_{PK} to prevent core saturation.

INPUT CAPACITOR SELECTION

The input capacitor must be rated to support the maximum input operating voltage. Higher value input capacitors reduce the input voltage ripple caused by the switch currents on the VIN pin. Maximum rms input current for the application is calculated using

$$I_{RMS\_MAX(CIN)} = I_{LOAD(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (4)$$

Place the input capacitor as close as possible to the VIN pin to minimize supply noise.

In principle, different types of capacitors can be considered, but for battery-powered applications, the best choice is the multilayer ceramic capacitor, due to its small size, low equivalent series resistance (ESR), and low equivalent series inductance (ESL).

It is recommended that the VIN pin be bypassed with at least a 2.2 µF input capacitor. For a 0.22 mm height solution using the ADP2127, at least 2 × 1.0 µF capacitors will be necessary on the input. The input capacitor can be increased without any limit for better input voltage filtering. X5R or X7R dielectrics with a voltage rating of 6.3 V or higher are recommended.

Table 5. Inductor Selection

Manufacturer	Series	Inductance (µH)	DCR (mΩ) (Typ)	Current Rating (mA)	Size (L × W × H) (mm)	Package
Murata	LQM18PN1R0-A52	1.0	520	500	1.6 × 0.8 × 0.33	0603
Taiyo Yuden	CKP1608S1R5M	1.5	420	500	1.6 × 0.8 × 0.33	0603

Table 6. Input/Output Capacitor Selection

Manufacturer	Part Number	Capacitance (µF)	Voltage Rating (V)	Temperature Coefficient	Size (L × W × H) (mm)	Package
Murata	GRM153R60J225ME95	2.2 ± 20%	6.3	X5R	1.0 × 0.5 × 0.33	0402
	GRM153R60G225M	2.2 ± 20%	4	X5R	1.0 × 0.5 × 0.33	0402
Taiyo Yuden	JMK105BJ225MP	2.2 ± 20%	6.3	X5R	1.0 × 0.5 × 0.33	0402
	AMK105BJ225MP	2.2 ± 20%	4	X5R	1.0 × 0.5 × 0.33	0402
	AMK105BJ105MC	1.0 ± 20%	4	X5R	1.0 × 0.5 × 0.22	0402
	ADC105BJ105ME	1.0 ± 20%	4	X5R	1.0 × 0.5 × 0.20	0402
	JMK105BJ474KC	0.47 ± 10%	6.3	X5R	1.0 × 0.5 × 0.22	0402
	JMK105BJ474MC	0.47 ± 20%	6.3	X5R	1.0 × 0.5 × 0.22	0402
TDK	CGB2A3X5R0J105K	1.0 ± 10%	6.3	X5R	1.0 × 0.5 × 0.33	0402
	CGB2A3X5R0J105M	1.0 ± 20%	6.3	X5R	1.0 × 0.5 × 0.33	0402

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. For a given loop crossover frequency (the frequency at which the loop gain drops to 0 dB), the maximum voltage transient excursion (overshoot) is inversely proportional to the value of the output capacitor.

When choosing output capacitors, it is important to account for the loss of capacitance due to output voltage dc bias. This may result in using a capacitor with a higher rated voltage to achieve the desired capacitance value. Additionally, if ceramic output capacitors are used, the capacitor's rms ripple current rating should always meet or exceed the application requirements. The rms ripple current is calculated from

$$I_{RMS(COUT)} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{L \times f_{SW} \times V_{IN(MAX)}} \quad (5)$$

At nominal load currents, the converter operates in forced PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor.

$$\Delta V_{OUT} = \Delta I_L \times (ESR + 1/(8 \times C_{OUT} \times f_{SW})) \quad (6)$$

The largest voltage ripple occurs at the highest input voltage.

The ADP2126/ADP2127 are designed to operate with one small 2.2 µF capacitor. For a 0.22 mm height solution using the ADP2127, at least 2 × 1.0 µF capacitors will be necessary on the output. X5R or X7R dielectrics that have low ESR, low ESL, and a voltage rating of 4 V or higher are recommended. These low ESR components help the ADP2126/ADP2127 meet tight output voltage ripple specifications.

THERMAL CONSIDERATIONS

The operating junction temperature (T_J) of the device is dependent on the ambient operating temperature (T_A) of the application, the power dissipation of the ADP2126/ADP2127 (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). The operating junction temperature (T_J) is calculated from

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (7)$$

where θ_{JA} is 105°C/W, as provided in Table 3.

The ADP2126/ADP2127 may be damaged when the operating junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

- In applications with high P_D and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.
- In applications with moderate P_D and good PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The power dissipation (P_D) of the ADP2126/ADP2127 is only a portion of the power loss of the overall application. For a given application with known operating conditions, the application power loss is calculated by combining the following equations for power loss (P_{LOSS}) and efficiency (η):

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (8)$$

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100 \quad (9)$$

The resulting equation uses the output power and the efficiency to determine the P_{LOSS}.

$$P_{LOSS} = P_{OUT}\left(\frac{100}{\eta} - 1\right) \quad (10)$$

The power loss calculated using this approach is the combined loss of the ADP2126/ADP2127 device (P_D), the inductor (P_L), input capacitor (P_{CIN}), and the output capacitor (P_{COUT}), as shown in the following equation:

$$P_{LOSS} = P_D + P_L + P_{CIN} + P_{COUT} \quad (11)$$

The power loss for the inductor, input capacitor, and output capacitor is calculated using

$$P_L = I_{RMS}^2 \times DCR \quad (12)$$

$$P_{CIN} = \left(\frac{I_{RMS}}{2}\right)^2 \times ESR_{CIN} \quad (13)$$

$$P_{COUT} = (\Delta_{IOUT})^2 \times ESR_{COUT} \quad (14)$$

If multilayer chip capacitors with low ESR are used, the power loss in the input and output capacitors is negligible and

$$P_D + P_L >> P_{CIN} + P_{COUT} \quad (15)$$

$$P_{LOSS} \approx P_D + P_L \quad (16)$$

The final equation for calculating P_D can be used in Equation 7 to ensure that the operating junction temperature is not exceeded.

$$P_D \approx P_{LOSS} - P_L \approx P_{OUT}\left(\frac{100}{\eta} - 1\right) - P_L \quad (17)$$

PCB LAYOUT GUIDELINES

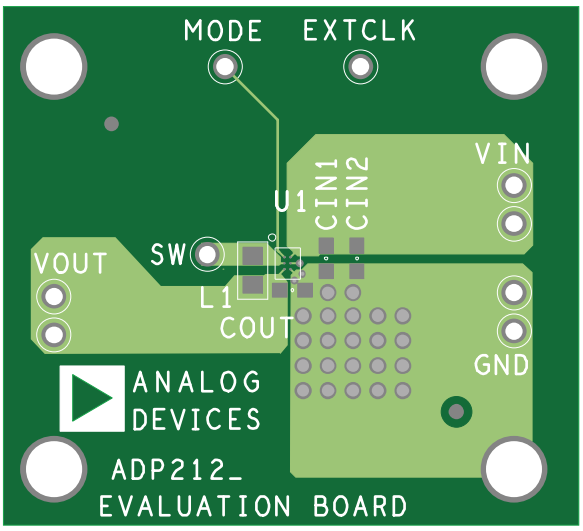

Figure 31. ADP2126/ADP2127 Recommended Top Layer Layout

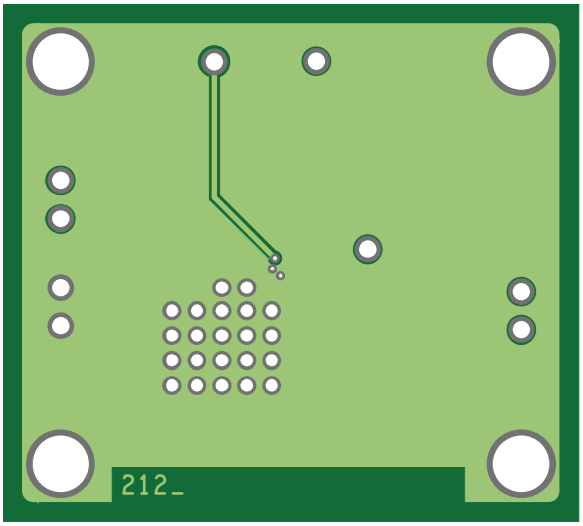

Figure 32. ADP2126/ADP2127 Recommended Bottom Layer Layout

For high efficiency, good regulation, and stability, a well-designed and manufactured PCB is required.

Use the following guidelines when designing PCBs:

- Keep the low ESR input capacitor, C_{IN}, close to VIN and GND.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, C_{OUT}, close to the FB and GND pins of the ADP2126/ADP2127. Long trace lengths from the part to the output capacitor add series inductance that may cause instability or increased ripple.

To ensure package reliability, consider the following guidelines when designing the footprint for the ADP2126/ADP2127. The BUMPED_CHIP device footprint must ultimately be determined according to application and customer specific reliability requirements, PCB fabrication quality, and PCB assembly capabilities.

- The Cu pad on the PCB for each solder bump should be 80% to 100% of the width of the solder bump. A smaller pad opening favors solder joint reliability (SJR) performance, whereas a larger pad opening favors drop test performance. The maximum pad size, including tolerance, should not exceed 180 µm.
- Electroplated nickel, immersion gold (ENIG) and organic solderability preservative (OSP) were used for internal reliability testing and are recommended.
- Nonsolder mask defined (NSMD) Cu pads are recommended for the BUMPED_CHIP package.
- The solder mask opening should be approximately 100 µm larger than the pad opening.
- The trace width should be less than two-thirds the size of the pad opening.
- The routing of traces from the Cu pads should be symmetrical in X and Y directions. Symmetrical routing of the traces prevents part rotation due to uneven solder wetting/surface tension forces.
- Stencil design is important for proper transfer of paste onto the Cu pads. Area ratio (AR), the relationship between the surface area of the stencil aperture and the inside surface area of the aperture walls, is critically important. Stencil thickness has the greatest impact on this ratio. AR values from 0.66 to 0.8 provide the best paste transfer efficiency and repeatability. The AR is calculated from

$$AR = \frac{Ap}{Aw}$$

where:
Ap is the area of the aperture opening.
Aw is the wall area.

OUTLINE DIMENSIONS

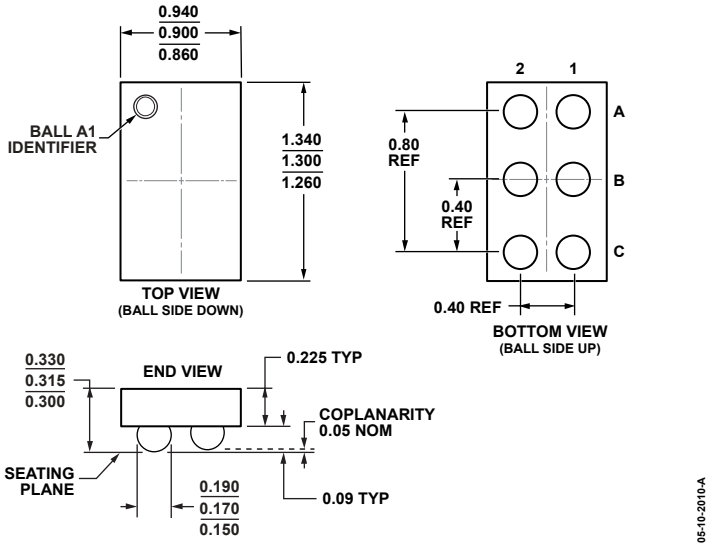

Figure 33. 6-Ball Bumped Bare Die Sales [BUMPED_CHIP]
(CD-6-4)
Dimensions shown in millimeters

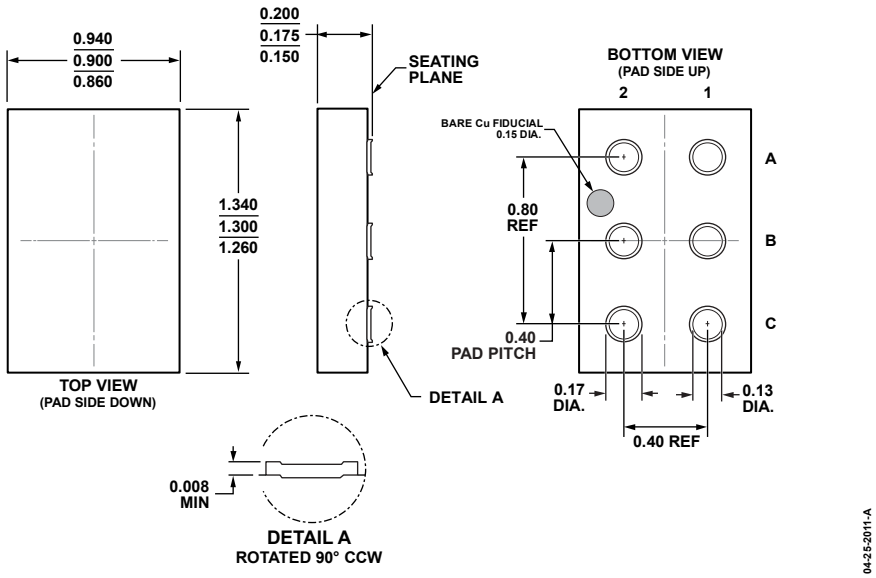

Figure 34. 6-Pad Embedded Wafer Level Package [EWLP]
(CN-6-1)
Dimensions shown in millimeters

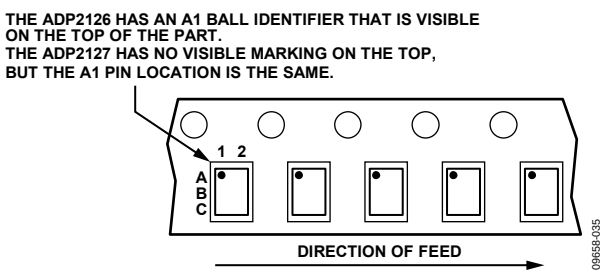

Figure 35. Tape and Reel Orientation for the ADP2126/ADP2127

ORDERING GUIDE

Model[1]	Output Voltage	EXTCLK Enable Type	Temperature Range	Package Description	Package Option[2]	Branding[3]
ADP2126ACDZ-1.20R7	1.20 V	Clock and logic	−40°C to +85°C	6-Ball Bumped Bare Die Sales [BUMPED_CHIP]	CD-6-4	LHY
ADP2127ACNZ-1.20R7	1.20 V	Clock and logic	−40°C to +85°C	6-Pad Embedded Wafer Level [EWLP]	CN-6-1	
ADP2127ACNZ1.260R7	1.26 V	Clock only	−40°C to +85°C	6-Pad Embedded Wafer Level [EWLP]	CN-6-1	
ADP2126-1.2-EVALZ	1.20 V	Clock and logic		Evaluation Board for ADP2126		

[1] Z = RoHS Compliant Part.
[2] These package options are halide free.`
[3] The ADP2127 does not have a Pin 1 indicator or a branding code. The bare Cu fiducial on the pad side can be used for device orientation.

NOTES

NOTES

D09658-0-3/12(B)