Datasheet

Serial EEPROM Series Standard EEPROM

WLCSP EEPROM

BRCC064GWZ-3

General Description

BRCC064GWZ-3 is a serial EEPROM of I²C BUS Interface Method

Features

- Completely conforming to the world standard I²C BUS.
  All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.6V to 5.5V Single Power Source Operation most suitable for battery use
- 1.6V to 5.5V wide limit of Operating Voltage, possible FAST MODE 400KHz operation
- Page Write Mode useful for initial value write at factory shipment
- Self-timed Programming Cycle
- Low Current Consumption
- Prevention of write mistake
  - ➢ Write (write protect) Function added
  - ➢ Prevention of write mistake at low voltage
- More than 1 million write cycles
- More than 40 years data retention
- Noise filter built in SCL / SDA terminal
- Initial delivery state FFh

Packages W(Typ) x D(Typ) x H(Max)

UCSP30L1 1.50mm x1.00mm x 0.35mm

BRCC064GWZ-3

Capacity	Bit Format	Type	Power Source Voltage	Package
64Kbit	8K×8	BRCC064GWZ-3	1.6V to 5.5V	UCSP30L1

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	220 (UCSP30L1)	mW	Derate by 2.2mW/°C when operating above Ta=25°C
Storage Temperature	Tstg	-65 to +125	°C	
Operating Temperature	Topr	-40 to +85	°C	
Input Voltage/ Output Voltage	-	-0.3 to Vcc+1.0	V	The Max value of Input Voltage/Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input Voltage/Output Voltage is not below 1.0V.
Junction Temperature	Tjmax	150	°C	Junction temperature at the storage condition

Memory Cell Characteristics (Ta=25°C, Vcc=1.6V to 5.5V)

Parameter	Limit			Unit
	Min	Typ	Max	
Write Cycles (1)	1,000,000	-	-	Times
Data Retention (1)	40	-	-	Years

(1)Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Rating	Unit
Power Source Voltage	Vcc	1.6 to 5.5	V
Input Voltage	V_{IN}	0 to Vcc	

DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.6V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage1	V_{IH1}	0.7Vcc	-	Vcc+1.0	V	1.7V≦ Vcc≦ 5.5V
Input Low Voltage1	V_{IL1}	-0.3(2)	-	+0.3Vcc	V	1.7V≦ Vcc≦ 5.5V
Input High Voltage2	V_{IH2}	0.8Vcc	-	Vcc+1.0	V	1.6V≦ Vcc＜1.7V
Input Low Voltage2	V_{IL2}	-0.3(2)	-	+0.2Vcc	V	1.6V≦ Vcc＜1.7V
Output Low Voltage1	V_{OL1}	-	-	0.4	V	I_{OL}=3.0mA, 2.5V≦ Vcc≦ 5.5V (SDA)
Output Low Voltage2	V_{OL2}	-	-	0.2	V	I_{OL}=0.7mA, 1.6V≦ Vcc＜2.5V (SDA)
Input Leakage Current	I_{LI}	-1	-	+1	µA	V_{IN}=0 to Vcc
Output Leakage Current	I_{LO}	-1	-	+1	µA	V_{OUT}=0 to Vcc (SDA)
Supply Current (Write)	I_{CC1}	-	-	2.0	mA	Vcc=5.5V, f_{SCL}=400kHz, t_{WR}=5ms, Byte Write, Page Write
Supply Current (Read)	I_{CC2}	-	-	0.5	mA	Vcc=5.5V, f_{SCL}=400kHz Random Read, current Read, Sequential Read WP=GND or Vcc
Standby Current	I_{SB}	-	-	2.0	µA	Vcc=5.5V, SDA, SCL=Vcc WP=GND or Vcc, SLV=GND or Vcc

(2) When the pulse width is 50ns or less, it is -1.0V.

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AC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.6V to 5.5V)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Clock Frequency	f_{SCL}	-	-	400	kHz
Data Clock High Period	t_{HIGH}	0.6	-	-	µs
Data Clock Low Period	t_{LOW}	1.2	-	-	µs
SDA,SCL(INPUT) Rise Time (1)	t_R	-	-	1.0	µs
SDA,SCL (INPUT)Fall Time (1)	t_{F1}	-	-	1.0	µs
SDA(OUTPUT)Fall Time (1)	t_{F2}	-	-	0.3	µs
Start Condition Hold Time	$t_{HD:STA}$	0.6	-	-	µs
Start Condition Setup Time	$t_{SU:STA}$	0.6	-	-	µs
Input Data Hold Time	$t_{HD:DAT}$	0	-	-	ns
Input Data Setup Time	$t_{SU:DAT}$	100	-	-	ns
Output Data Delay Time	t_{PD}	0.1	-	0.9	µs
Output Data Hold Time	t_{DH}	0.1	-	-	µs
Stop Condition Setup Time	$t_{SU:STO}$	0.6	-	-	µs
Bus Free Time	t_{BUF}	1.2	-	-	µs
Write Cycle Time	t_{WR}	-	-	5	ms
Noise Spike Width (SDA and SCL)	t_I	-	-	0.1	µs
WP Hold Time	$t_{HD:WP}$	1.0	-	-	µs
WP Setup Time	$t_{SU:WP}$	0.1	-	-	µs
WP High Period	$t_{HIGH:WP}$	1.0	-	-	µs

(1) Not 100% TESTED.

Condition Input Data Level: V_{IL}=0.2×Vcc V_{IH}=0.8×Vcc
Input Data Timing Reference Level: 0.3×Vcc/0.7×Vcc
Output Data Timing Reference Level: 0.3×Vcc/0.7×Vcc
Rise/Fall Time : ≦ 20ns

Serial Input / Output Timing

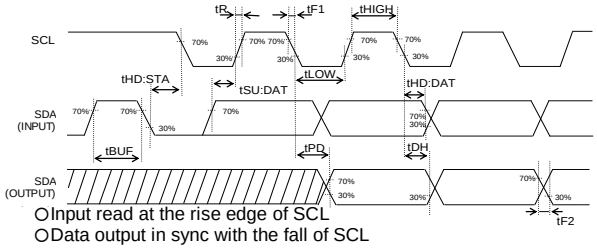


Figure 1.-(a). Serial Input / Output Timing

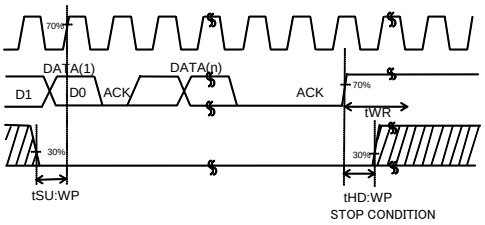


Figure 1.-(d). WP Timing at Write Execution

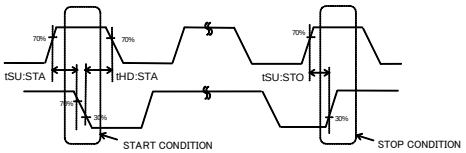


Figure 1.-(b) Start-Stop Bit Timing

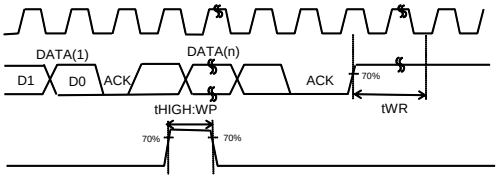


Figure 1.-(e). WP Timing at Write Cancel

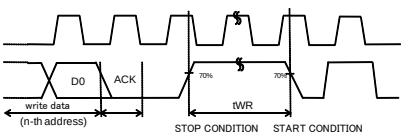


Figure 1.-(c). Write Cycle Timing

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Block Diagram

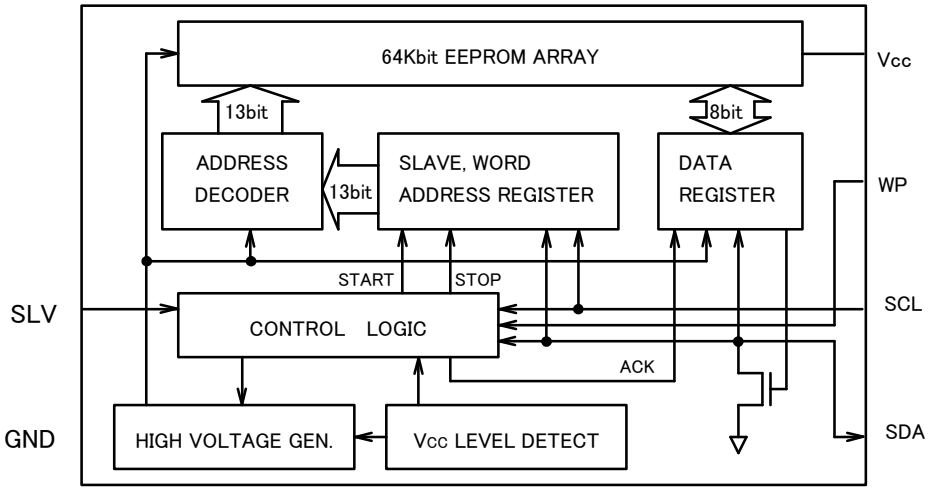


Figure 2. Block Diagram

Pin Configuration

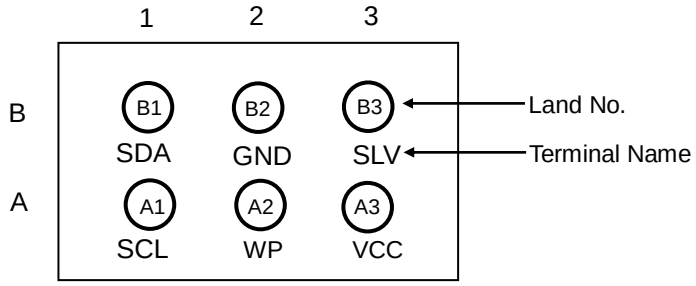


Figure 3. Pin Configuration
(BOTTOM VIEW)

Pin Descriptions

Land No.	Terminal Name	Input / Output	Descriptions
B3	SLV	Input	Slave address setting
B2	GND	-	Reference voltage of all input / output, 0V
B1	SDA	Input / Output	Slave and word address Serial data input, serial data output
A3	VCC	-	Power Supply
A2	WP	Input	Write protect terminal
A1	SCL	Input	Serial clock input

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Typical Performance Curves

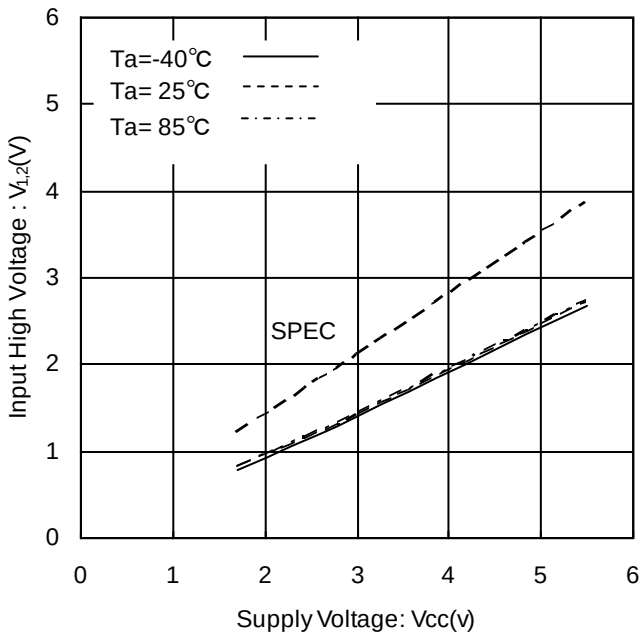


Figure 4. Input High Voltage1,2,
vs Supply Voltage

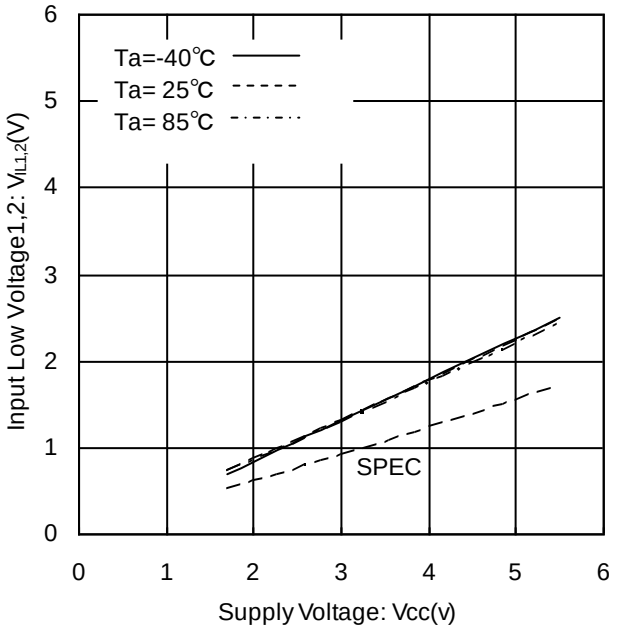


Figure 5. Input Low Voltage1,2
vs Supply Voltage

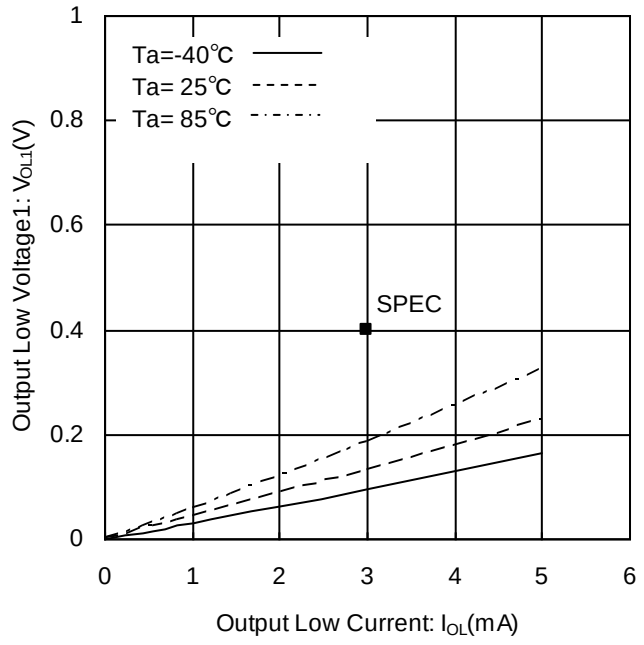


Figure 6. Output Low Voltage1
vs Output Low Current
(Vcc=2.5V)

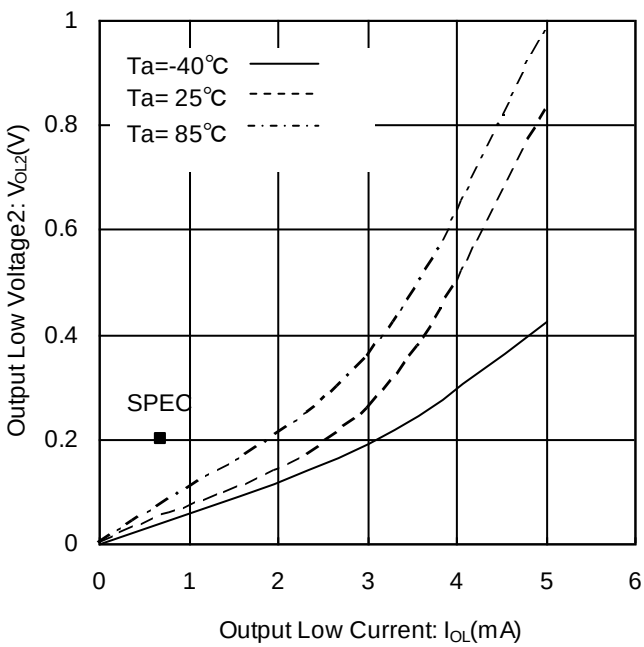


Figure 7. Output Low Voltage2
vs Output Low Current
(Vcc=1.6V)

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Typical Performance Curves - continued

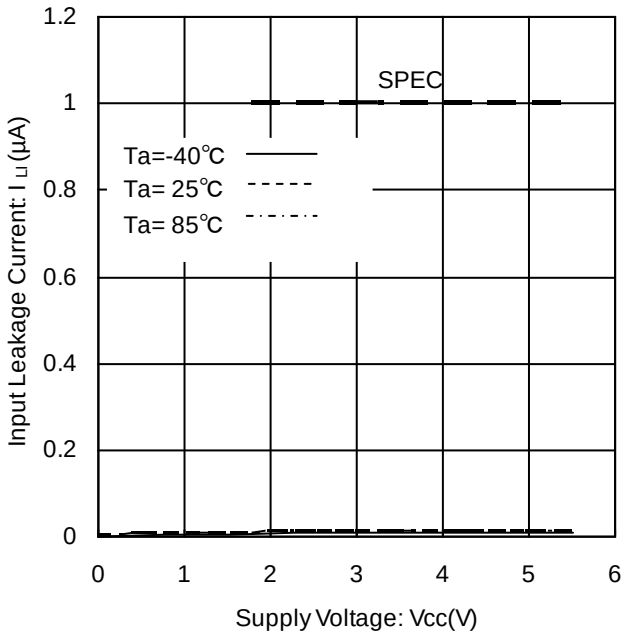


Figure 8. Input Leakage Current vs Supply Voltage (SCL, WP, SLV)

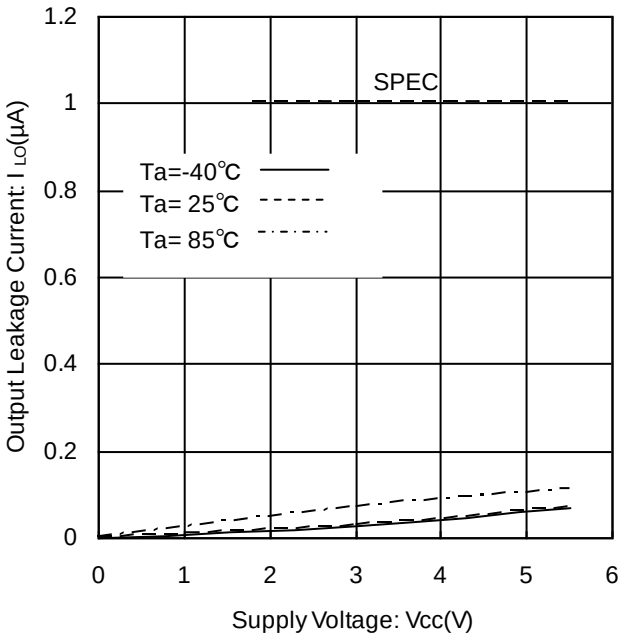


Figure 9. Output Leakage Current vs Supply Voltage (SDA)

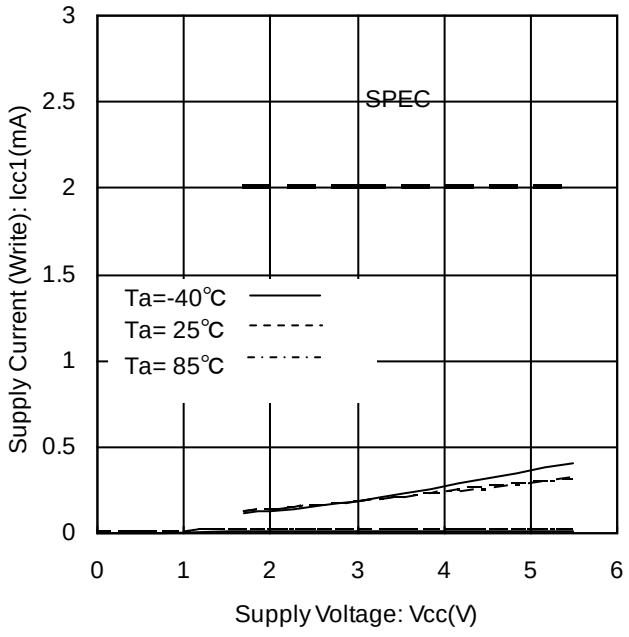


Figure 10. Supply Current (Write) vs Supply Voltage (f_{SCL}=400kHz)

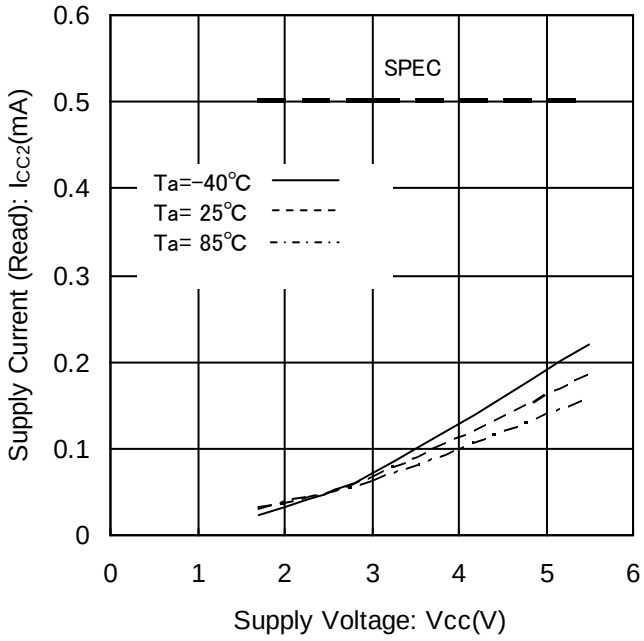


Figure 11. Supply Current (Read) vs Supply Voltage (f_{SCL}=400kHz)

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Typical Performance Curves - continued

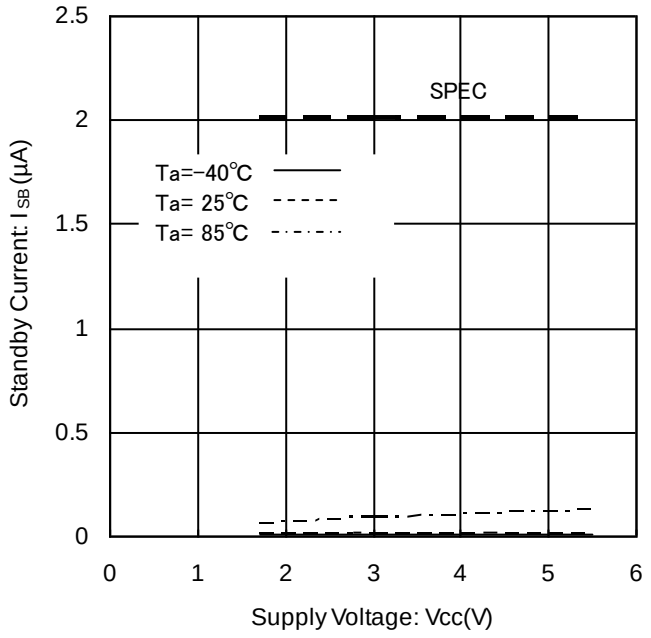


Figure 12. Standby Current vs Supply Voltage

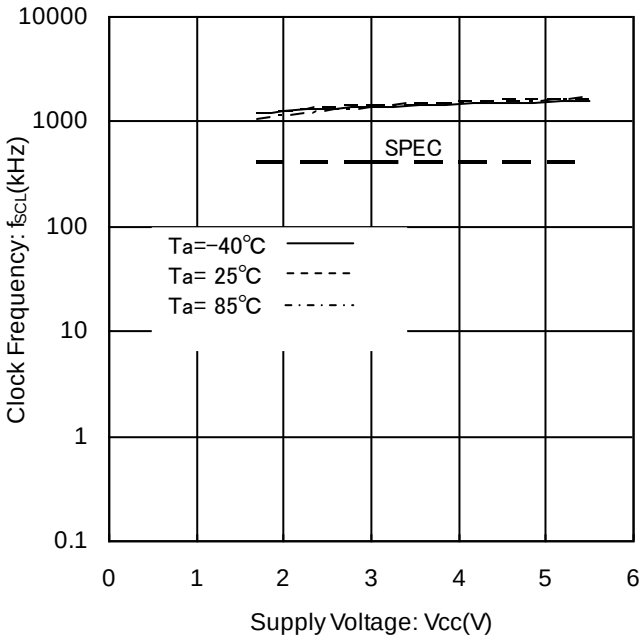


Figure 13. Clock Frequency vs Supply Voltage

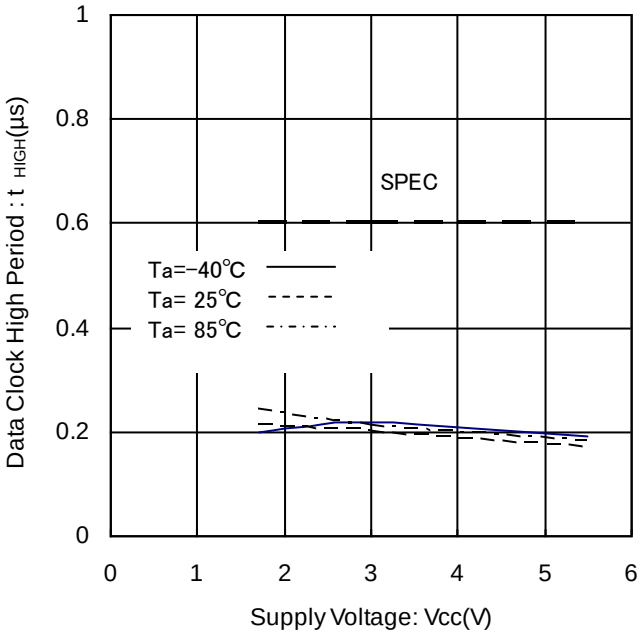


Figure 14. Data Clock High Period vs Supply Voltage

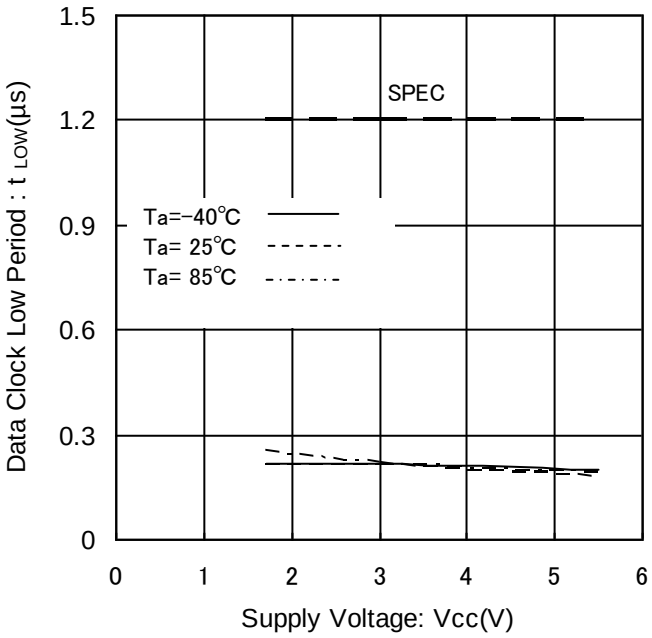


Figure 15. Data Clock Low Period vs Supply Voltage

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Typical Performance Curves - continued

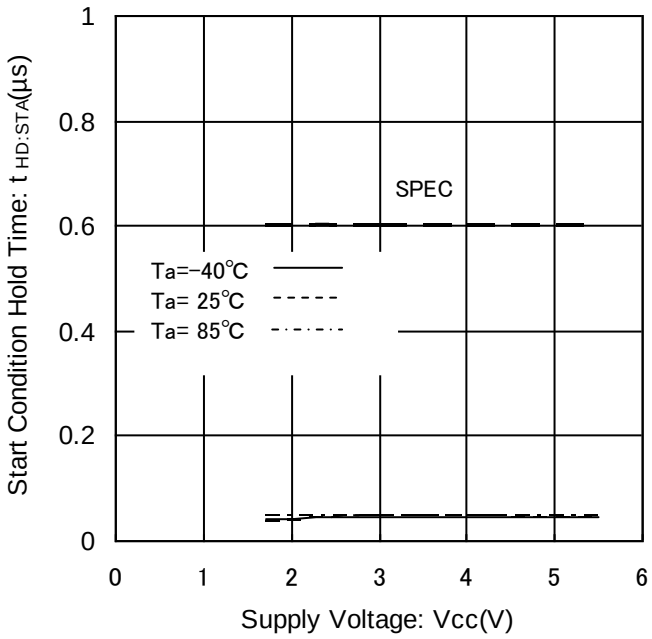


Figure 16. Start Condition Hold Time vs Supply Voltage

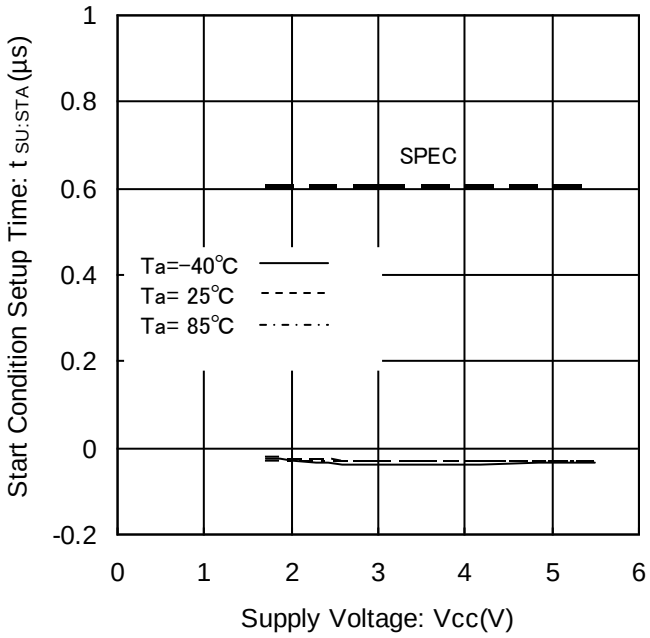


Figure 17. Start Condition Setup Time vs Supply Voltage

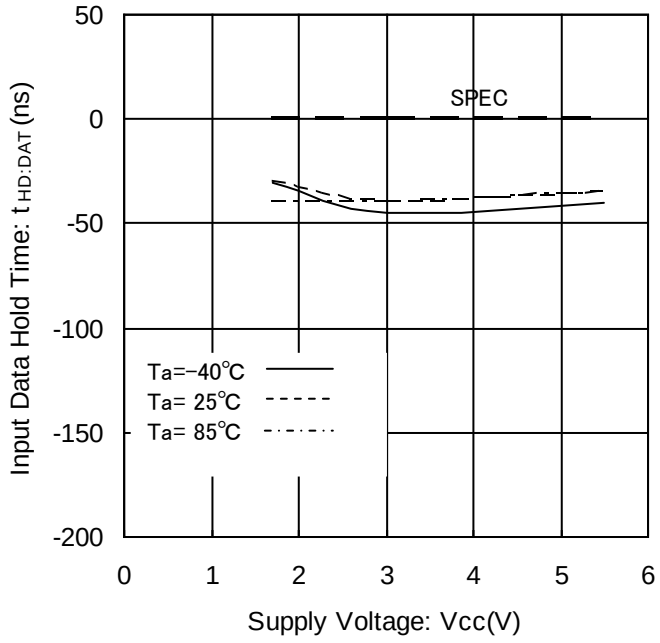


Figure 18. Input Data Hold Time vs Supply Voltage (HIGH)

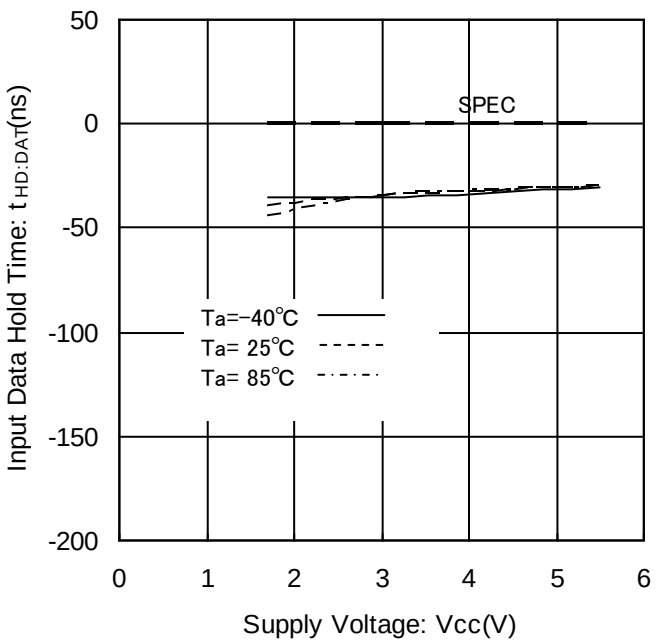


Figure 19. Input Data Hold Time vs Supply Voltage (LOW)

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Typical Performance Curves - continued

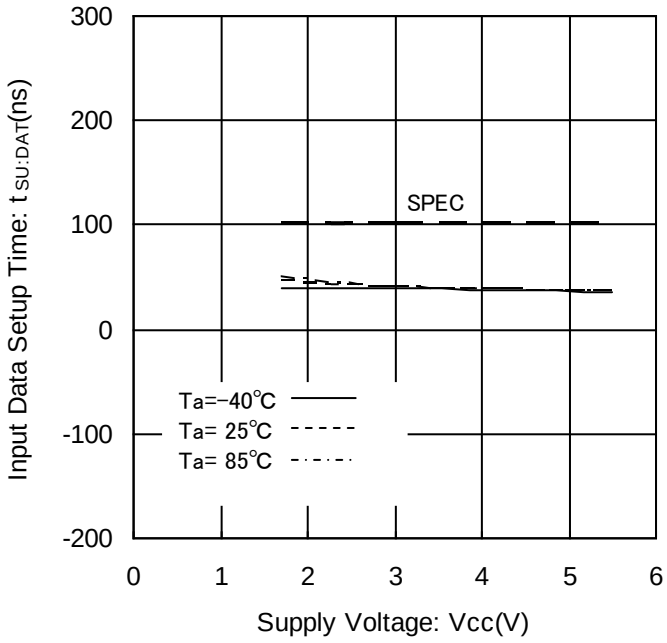


Figure 20. Input Data Setup Time vs Supply Voltage (HIGH)

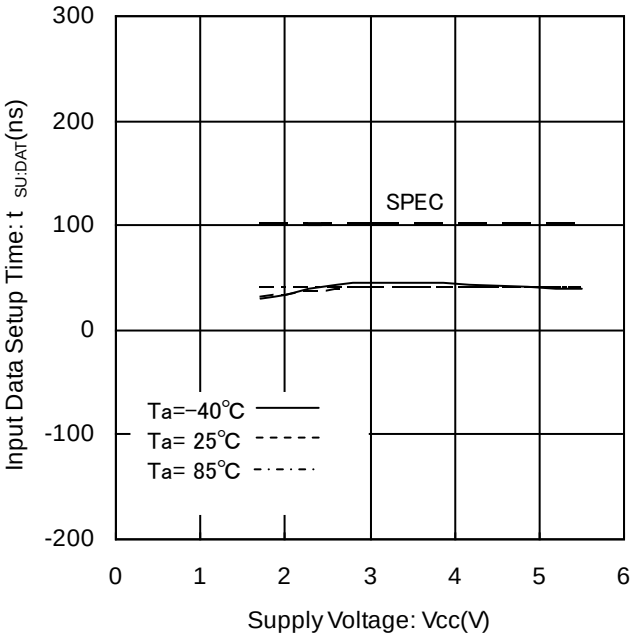


Figure 21. Input Data Setup Time vs Supply Voltage (LOW)

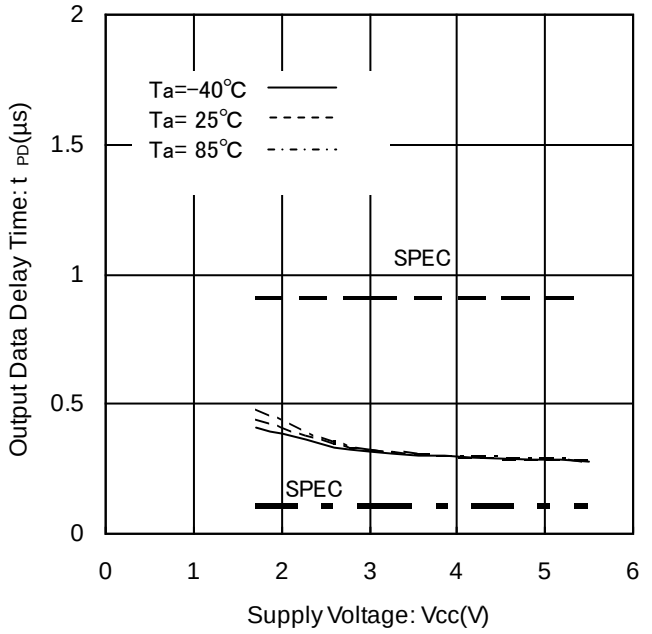


Figure 22. Output Data Delay Time vs Supply Voltage (LOW)

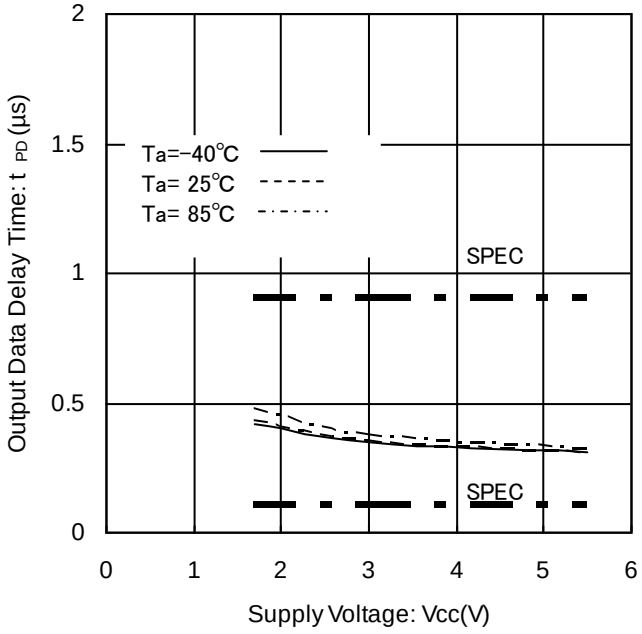


Figure 23. Output Data Delay Time vs Supply Voltage (HIGH)

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Typical Performance Curves - continued

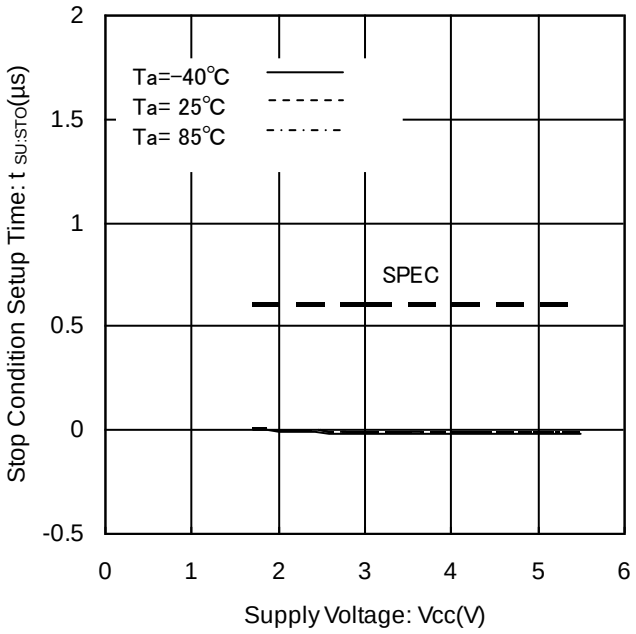


Figure 24. Stop Condition Setup Time vs Supply Voltage

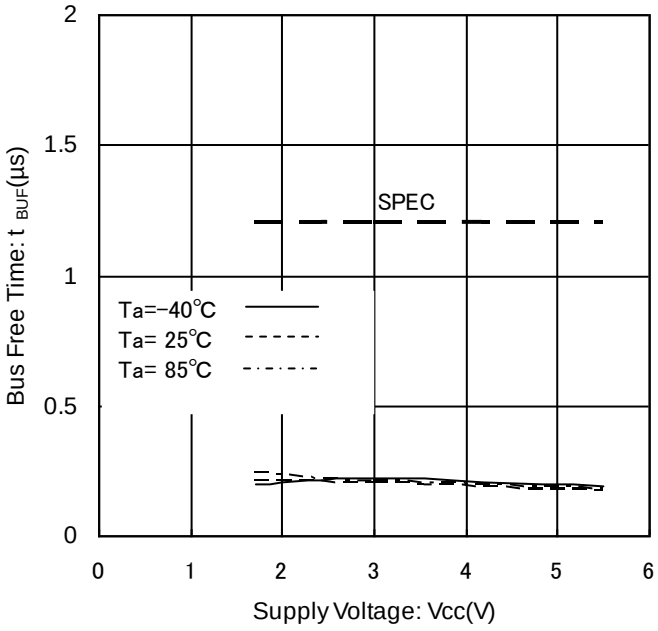


Figure 25. Bus Free Time vs Supply Voltage

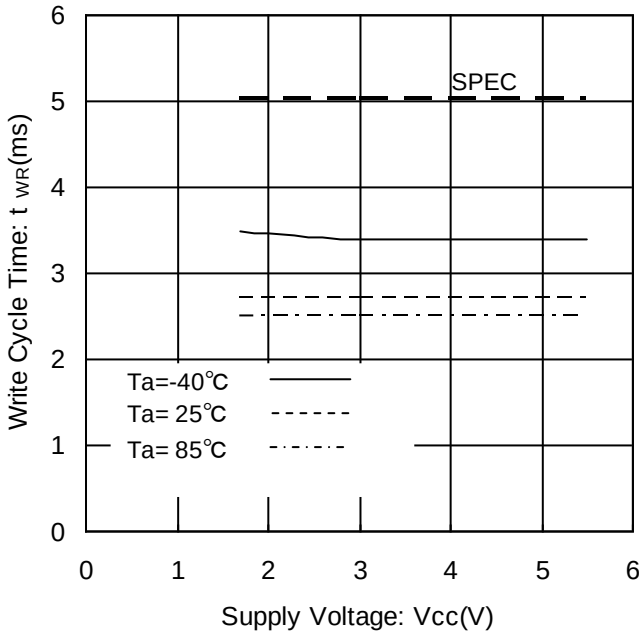


Figure 26. Write Cycle Time vs Supply Voltage

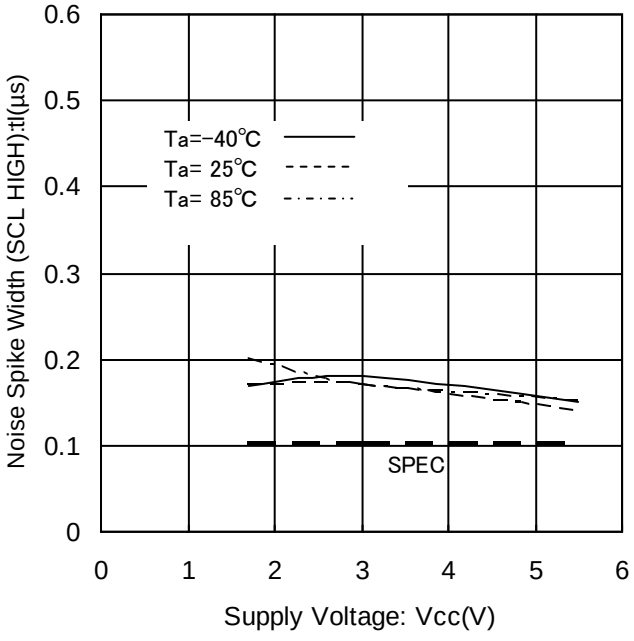


Figure 27. Noise Spike Width vs Supply Voltage (SCL HIGH)

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Typical Performance Curves - continued

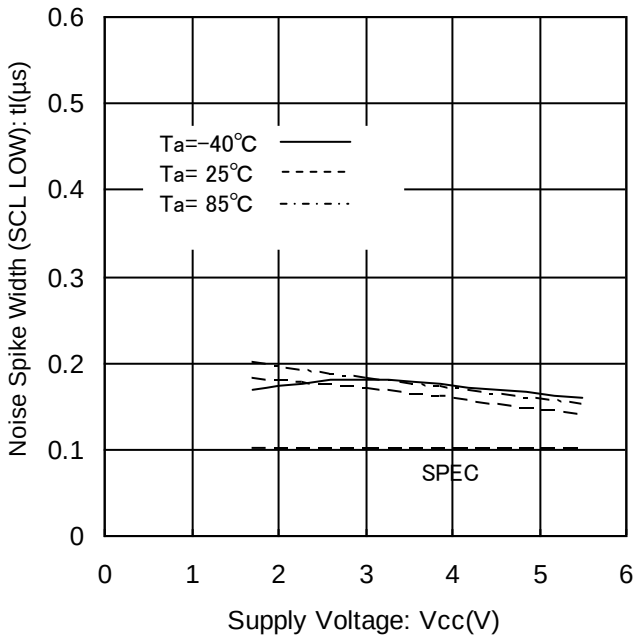


Figure 28. Noise Spike Width vs Supply Voltage (SCL LOW)

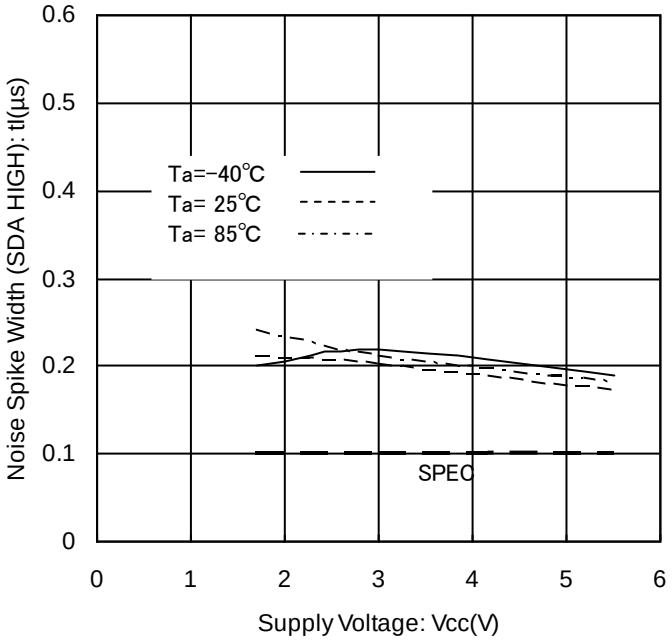


Figure 29. Noise Spike Width vs Supply Voltage (SDA HIGH)

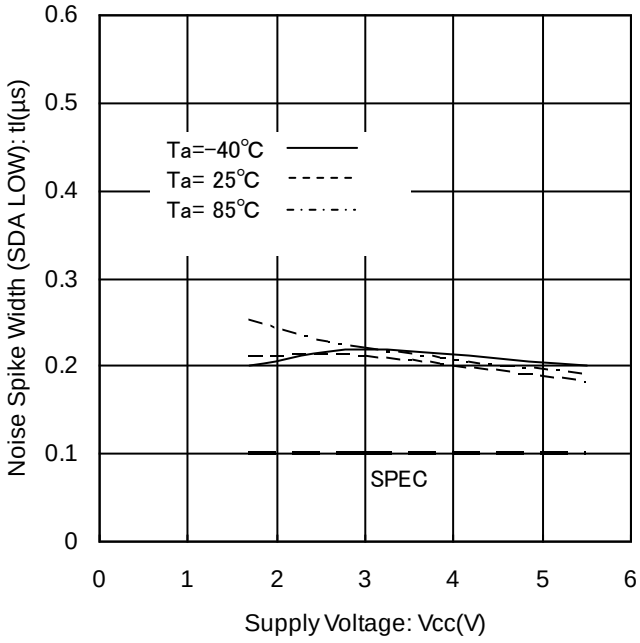


Figure 30. SDA Noise Spike Width (LOW) vs Supply Voltage (SDA LOW)

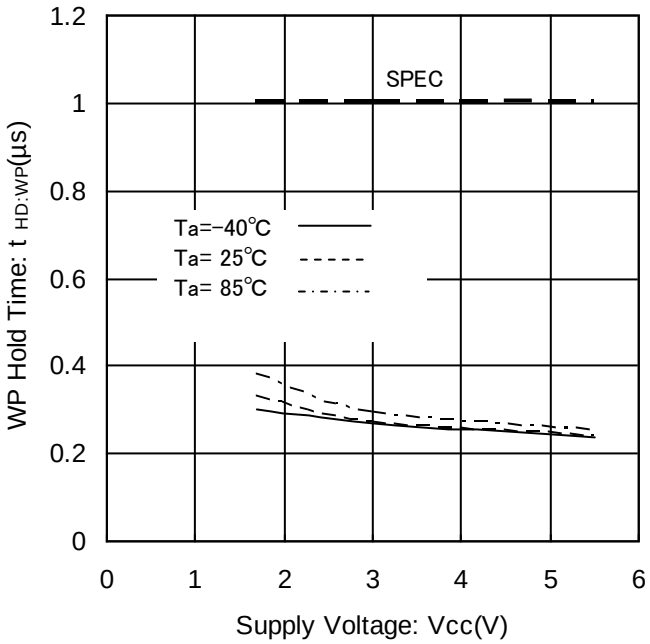


Figure 31. WP Hold Time vs Supply Voltage

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Typical Performance Curves - continued

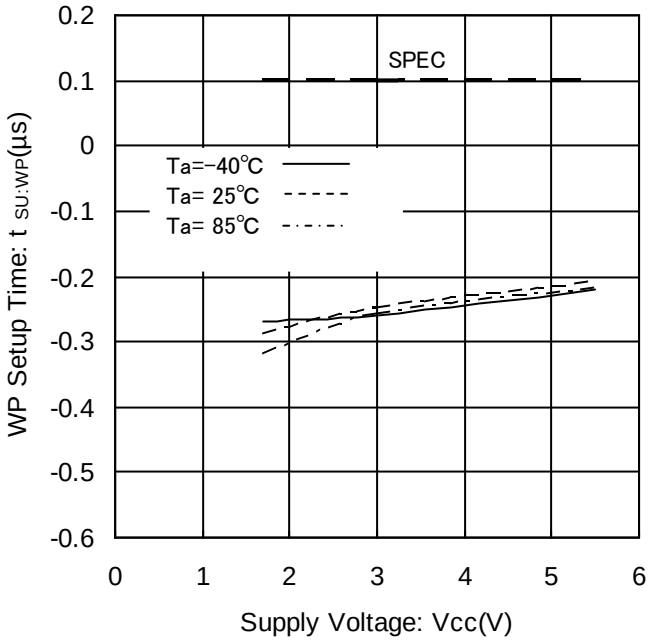


Figure 32. WP Setup Time vs Supply Voltage

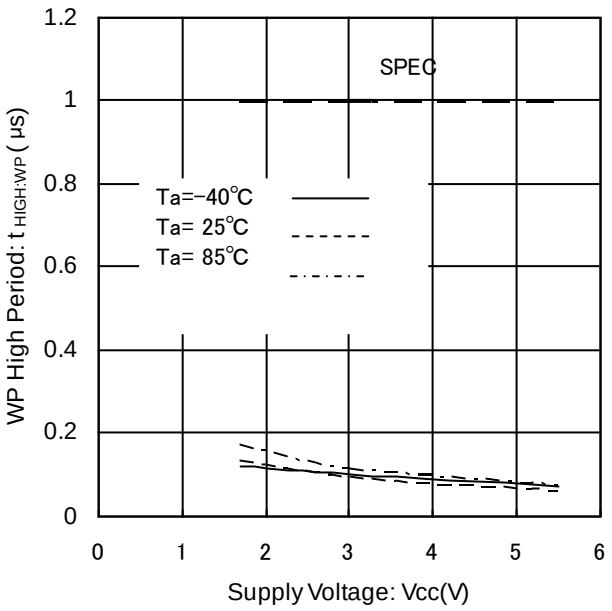


Figure 33. WP High Period vs Supply Voltage

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Timing Chart

1. I²C BUS Data Communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS data communication with several devices is possible by connecting with 2 communication lines: serial data (SDA) and serial clock (SCL).
Among the devices, there should be a “master” that generates clock and control communication start and end. The rest become “slave” which are controlled by an address peculiar to each device, like this EEPROM. The device that outputs data to the bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

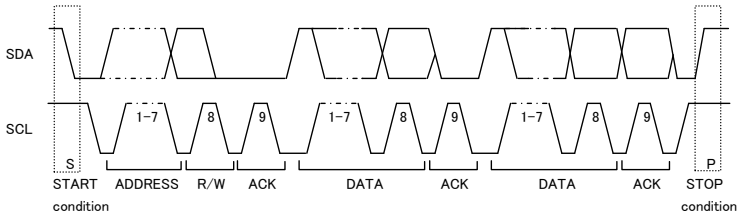


Figure 34. Data Transfer Timing

2. Start Condition (Start Bit Recognition)

(1) Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
(2) This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command cannot be executed.

3. Stop Condition (Stop Bit Recognition)

(1) Each command can be ended by a stop condition (stop bit) where SDA goes from 'LOW' to 'HIGH' while SCL is 'HIGH'.

4. Acknowledge (ACK) Signal

(1) The acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In a master-slave communication, the device (Ex. µ-COM sends slave address input for write or read command, to this IC) at the transmitter (sending) side releases the bus after output of 8bit data.
(2) The device (Ex. This IC receives the slave address input for write or read command from the µ-COM) at the receiver (receiving) side sets SDA 'LOW' during the 9th clock cycle, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
(3) This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
(4) After receiving 8bit data (word address and write data) during each write operation, this IC outputs acknowledge signal (ACK signal) 'LOW'..
(5) During read operation, this IC outputs 8bit data (read data) and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (µ-COM) side, this IC continues to output data. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, recognizes stop condition (stop bit), and ends read operation. Then this IC becomes ready for another transmission.

5. Device Addressing

(1) Slave address comes after start condition from master.
(2) The significant 4 bits of slave address are used for recognizing a device type.
The device code of this IC is fixed to '1010'.
(3) The next slave addresses (SLV 0 0 --- device address) are for selecting devices, and multiple devices can be used on a same bus according to the number of device addresses. It is possible to select and operate only EEPROM that has matched ‘HIGH’ ‘LOW’ input conditions of the SLV pin and the ‘1’ ‘0’ input conditions of slave address sent from the master.

Table 1. The relationship of SLV Pin and Slave Address SLV Bit where EEPROM can operate

SLV Pin Input	Slave address SLV Bit
HIGH	1
LOW	0

(4) The least significant bit ($R/\overline{W}$ --- READ / $\overline{WRITE}$) of slave address is used for designating write or read operation, and is as shown below.

Setting $R/\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
Setting $R/\overline{W}$ to 1 ------- read

Slave address	Maximum number of Connected buses
1 0 1 0 SLV 0 0 $R/\overline{W}$	2

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Write Command

1. Write Cycle

(1) Arbitrary data can be written to this EEPROM. When writing only 1 byte, Byte Write is normally used, and when writing continuous data of 2 bytes or more, simultaneous write is possible by Page Write cycle. The maximum number of bytes is specified per device of each capacity. Up to 32 arbitrary bytes can be written.

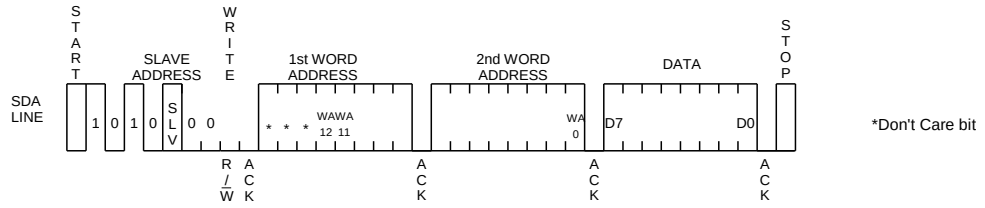


Figure 35. Byte Write Cycle

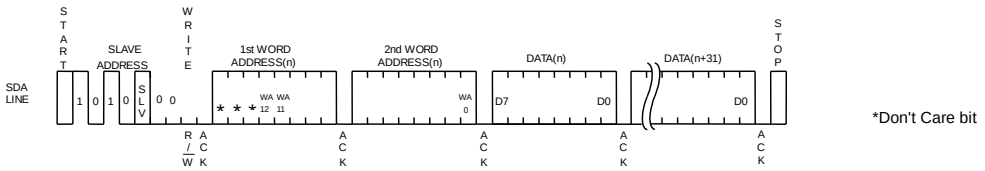


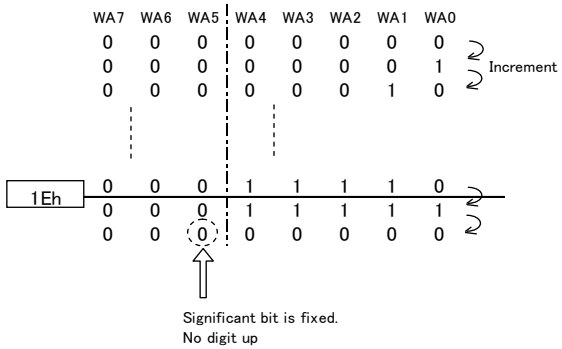
Figure 36. Page Write Cycle

(2) During internal write execution, all input commands are ignored, therefore ACK is not returned.
(3) Data is written to the address designated by word address (n-th address)
(4) By issuing stop bit after 8bit data input, internal write to memory cell starts.
(5) When internal write is started, command is not accepted for t_{WR} (5ms at maximum).
(6) Using page write cycle, writing in bulk is done as follows: When data of more than 32 bytes is sent, the bytes in excess overwrites the data already sent first.
(Refer to "Internal Address Increment".)
(7) As for page write cycle of BRCC064GWZ-3 where 2 or more bytes of data is intended to be written, after the 8 significant bits of word address are designated arbitrarily, only the value of 5 least significant bits in the address is incremented internally, so that data up to 32 addresses of memory only can be written.

In the case BRCC064GWZ-3, 1 page=32bytes, but the page
Write Cycle Time is 5ms at maximum for 32byte bulk write.
It does not stand 5ms at maximum × 32byte=160ms(Max)

2. Internal Address Increment

Page Write Mode (in the case of BRCC064GWZ-3)



For example, when it is started from address 1Eh, then, increment is made as below,
1Eh→1Fh→00h→01h··· please take note.

*1Eh···1E in hexadecimal, therefore,
00011110 becomes a binary number.

3. Write Protect (WP) Terminal

Write Protect (WP) Function
When WP terminal is set at Vcc (H level), data rewrite of all addresses is prohibited. When it is set at GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not leave it open.
At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', write error can be prevented.

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Read Command

1. Read Cycle

Read cycle is when data of EEPROM is read. Read cycle could be random read cycle or current read cycle. Random read cycle is a command to read data by designating a specific address, and is used generally. Current read cycle is a command to read data of internal address register without designating an address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available where the next address data can be read in succession.

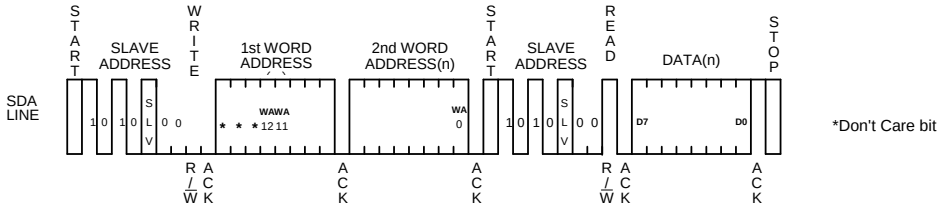


Figure 37. Random Read Cycle

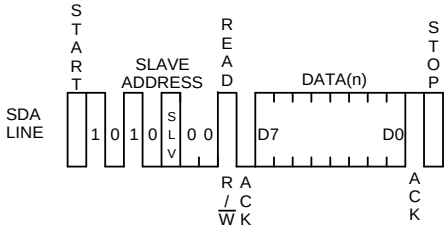


Figure 38. Current Read Cycle

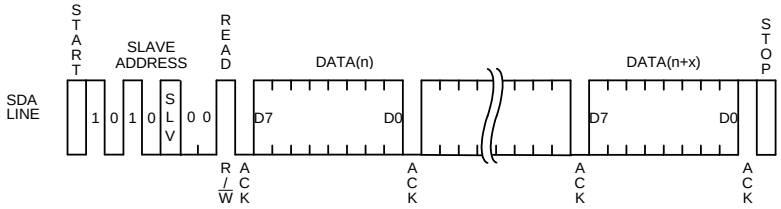


Figure 39. Sequential Read Cycle (in the case of Current Read Cycle)

(1) In Random Read Cycle, data of designated word address can be read.
(2) When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th, i.e., data of the (n+1)-th address, is output.
(3) When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (µ-COM) side, the next address data can be read in succession.
(4) Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal goes from ‘L’ to ‘H’ while SCL signal is 'H' .
(5) When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
Therefore, read command cycle cannot be ended. To end the read command cycle, be sure to input 'H' to ACK signal after D0, and the stop condition where SDA goes from ‘L’ to ‘H’ while SCL signal is 'H'.
(6) Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is asserted from ‘L’ to ‘H’ while SCL signal is 'H'.

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Software Reset

Software reset is executed to avoid malfunction after power on and during command input. Software reset has several kinds and 3 kinds of them are shown in the figure below. (Refer to Figure 40.-(a), Figure 40.-(b), and Figure 40.-(c).) Within the dummy clock input area, the SDA bus is released ('H' by pull up) and ACK output and read data '0' (both 'L' level) may be output from EEPROM. Therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

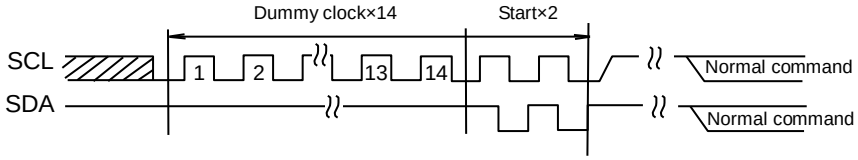


Figure 40.-(a) The case of dummy clock×14 + START+START+ command input

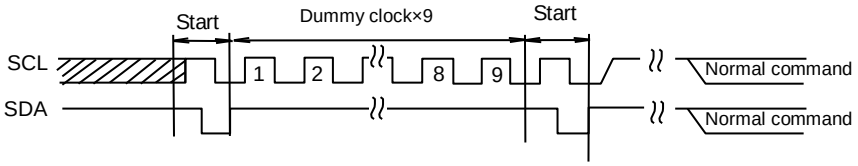


Figure 40.-(b) The case of START + dummy clock×9 + START + command input

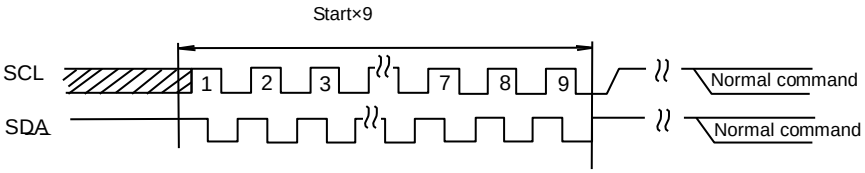


Figure 40.-(c) START×9 + command input

*Start command from START input.

Acknowledge Polling

During internal write execution, all input commands are ignored, therefore ACK is not returned. During internal automatic write execution after write cycle input, next command (slave address) is sent.If the first ACK signal sends back 'L', then it means end of write operation, else 'H' is returned, which means writing is still in progress. By the use of acknowledge polling, next command can be executed without waiting for t_{WR} = 5ms.

To write continuously, R/$\overline{W}$ = 0, then to carry out current read cycle after write, slave address with R/$\overline{W}$ = 1 is sent. If ACK signal sends back 'L', then execute word address input and data output and so forth.

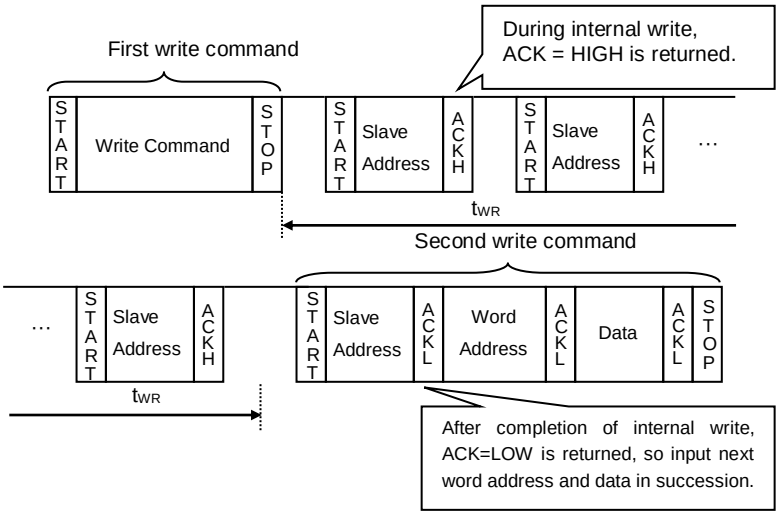


Figure 41. Case of continuous write by Acknowledge Polling

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WP Valid Timing (Write Cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so on, pay attention to the following WP valid timing. During write cycle execution, inside cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to take in D0 of data(in page write cycle, the first byte data) is the cancel invalid area.
WP input in this area becomes 'Don't care'. The area from the rise of SCL to take in D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status.

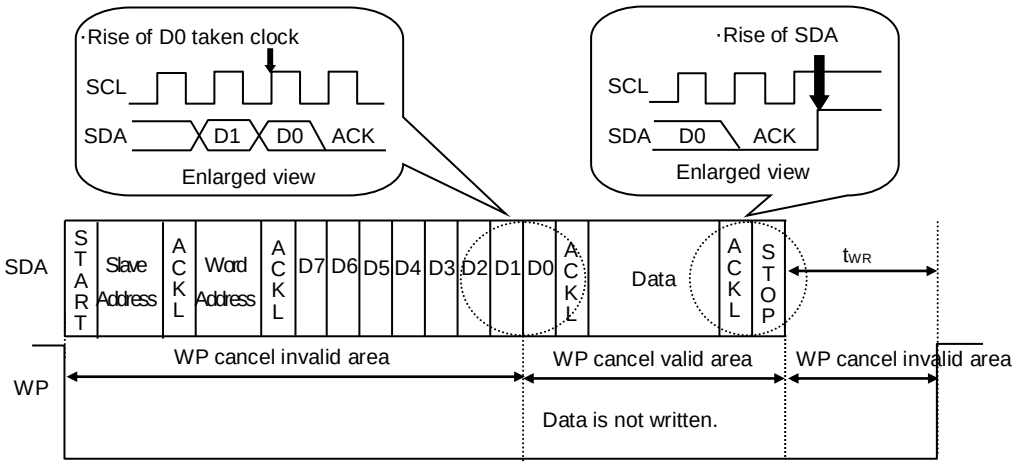


Figure 42. WP Valid Timing

Command Cancel by Start Condition and Stop Condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Figure 43.) However, within ACK output area and during data read, SDA bus may output 'L'. In this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. When command is cancelled by start-stop condition during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined. Therefore, it is not possible to carry out current read cycle in succession. To carry out read cycle in succession, carry out random read cycle.

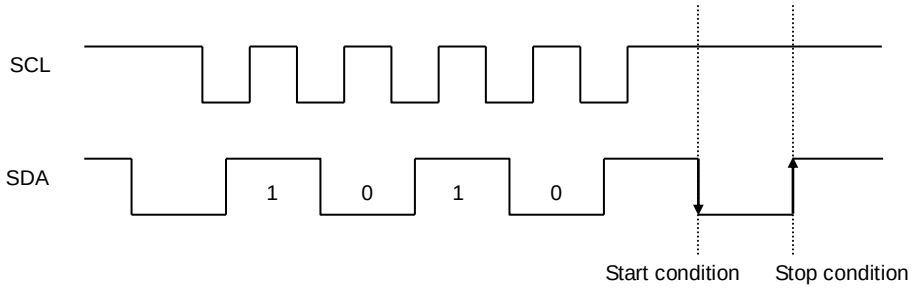


Figure 43. Case of cancel by start, stop condition during Slave Address Input

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I/O Peripheral Circuit

1. Pull Up Resistance of SDA Terminal

SDA is NMOS open drain, so it requires a pull up resistor. As for this resistance value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger is the supply current (Read).

2. Maximum Value of R_{PU}

The maximum value of R_{PU} is determined by the following factors:

(1)SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2)The bus' electric potential Ⓐ to be determined by the input current leak total (I_L) of the device connected to the bus with output of 'H' to the SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin of 0.2Vcc.

$$V_{CC}-I_L R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8Vcc-V_{IH}}{I_L}$$

Ex.) Vcc =3V I_L=10μA V_{IH}=0.7 Vcc

from(2)

$$R_{PU} \leqq \frac{0.8\times 3-0.7\times 3}{10\times 10^{-6}}$$

$$\leqq 30\ [k\Omega]$$

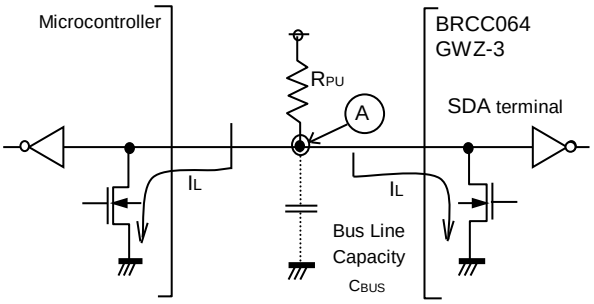


Figure 44. I/O Circuit Diagram

3. Minimum Value of R_{PU}

The minimum value of R_{PU} is determined by the following factors:

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{Vcc-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{Vcc-V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including the recommended noise margin of 0.1Vcc.

$$V_{OLMAX} \leqq V_{IL}-0.1\,Vcc$$

Ex.) V_{CC} =3V, V_{OL}=0.4V, I_{OL}=3mA, microcontroller, EEPROM V_{IL}=0.3Vcc

from (1)

$$R_{PU} \geqq \frac{3-0.4}{3\times 10^{-3}}$$

$$\geqq 867[\Omega]$$

And V_{OL}=0.4[V]

V_{IL}=0.3×3

=0.9[V]

Therefore, the condition (2) is satisfied.

4. Pull-up Resistance of SCL Terminal

When SCL control is made at the CMOS output port, there is no need for a pull up resistor. But when there is a time where SCL becomes 'Hi-Z', add a pull up resistor. As for the pull up resistor value, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

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Cautions on Microcontroller Connection

1. R_S

In I^2C BUS, it is recommended that SDA port is of open drain input/output. However, when using CMOS input / output of tri state to SDA port, insert a series resistance R_S between the pull up resistor R_{PU} and the SDA terminal of EEPROM. This is to control over current that may occur when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. R_S also plays the role of protecting the SDA terminal against surge. Therefore, even when SDA port is open drain input/output, R_S can be used.

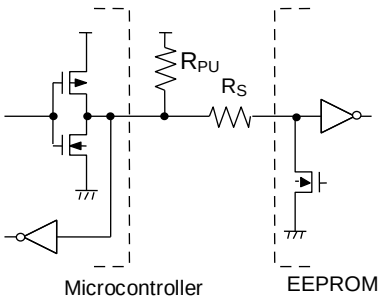


Figure 45. I/O Circuit Diagram

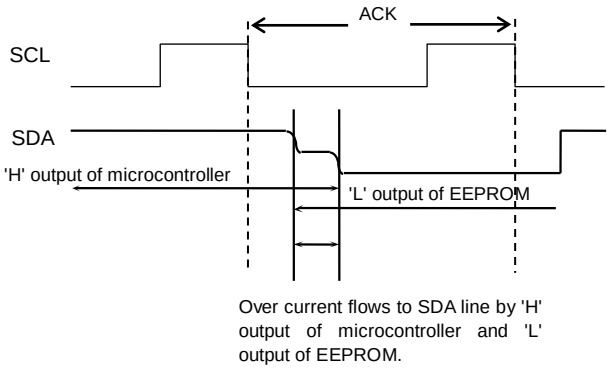


Figure 46. Input / Output Collision Timing

2. Maximum Value of R_S

The maximum value of R_S is determined by the following relations:

(1)SDA rise time to be determined by the capacitance (C_{BUS}) of bus line and R_{PU} of SDA should be t_R or lower. Furthermore, AC timing should be satisfied even when SDA rise time is slow.

(2)The bus' electric potential Ⓐ to be determined by R_{PU} and R_S the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin of 0.1Vcc.

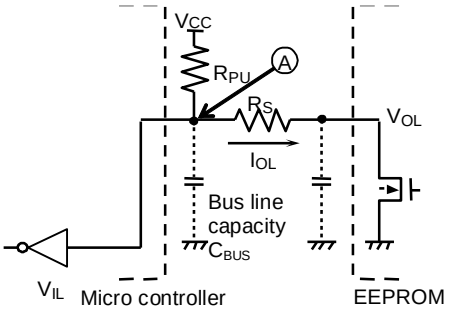


Figure 47. I/O Circuit Diagram

$$\frac{(Vcc-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL} + 0.1Vcc \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1Vcc}{1.1Vcc-V_{IL}} \times R_{PU}$$

Ex)V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

$$R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leqq 1.67[k\Omega]$$

3. Minimum Value of R_S

The minimum value of R_S is determined by over current at bus collision. When over current flows, noises in power source line and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of the impedance of power source line in set and so forth. Set the over current to EEPROM at 10mA or lower.

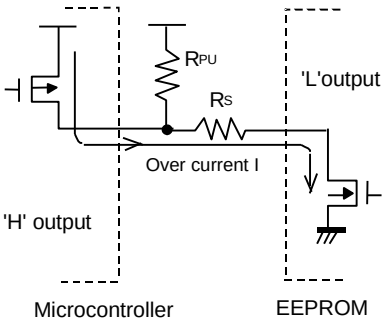


Figure 48. I/O circuit diagram

$$\frac{Vcc}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{Vcc}{I}$$

EX) V_{CC}=3V I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300[\Omega]$$

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I/O Equivalence Circuit

1. Input (SCL, WP, SLV)

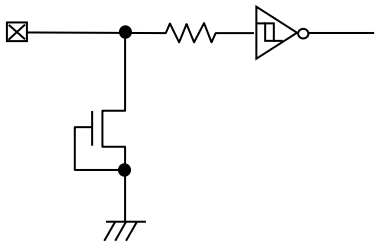


Figure 49. Input Pin Circuit Diagram

2. Input / Output (SDA)

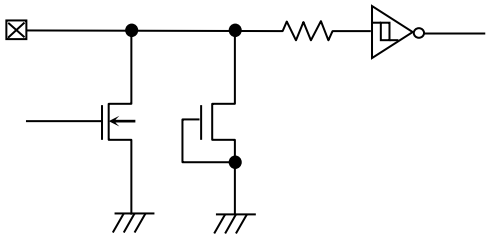


Figure 50. Input / Output Pin Circuit Diagram

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Power-Up/Down Conditions

At power on, the IC's internal circuits may go through unstable low voltage area as the Vcc rises, making the IC's internal logic circuit not completely reset, hence, malfunction may occur. To prevent this, the IC is equipped with POR circuit and LVCC circuit. To assure the operation, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and V_{bot} for operating POR circuit.

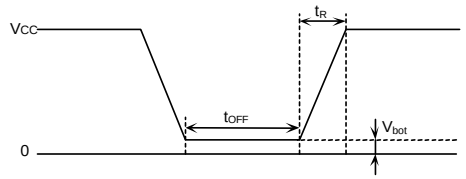


Figure 51. Rise Waveform Diagram

Recommended conditions of t_R, t_{OFF},V_{bot}t

t_R	t_{OFF}	V_{bot}
10ms or below	10ms or larger	0.3V or below
100ms or below	10ms or larger	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.
   When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

(1) In the case when the above condition 1 cannot be observed such that SDA becomes 'L' at power on.
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

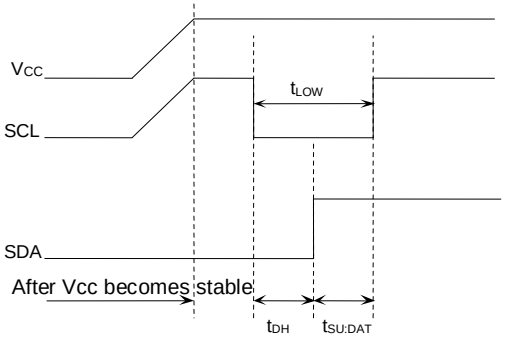


Figure 52. When SCL= 'H' and SDA= 'L'

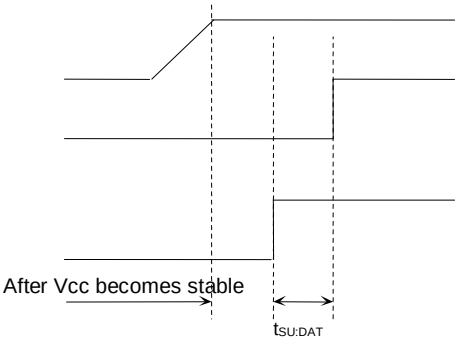


Figure 53. When SCL='L' and SDA='L'

(2) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(Page 16).
(3) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out (1), and then carry out (2).

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power and prevents write error. At LVCC voltage (Typ =1.2V) or below, data rewrite is prevented.

Noise Countermeasures

1. **Bypass Capacitor**
   When noise or surge gets in the power source line, malfunction may occur, therefore, it is recommended to connect a bypass capacitor (0.1µF) between the IC's Vcc and GND pins. Connect the capacitor as close to the IC as possible. In addition, it is also recommended to attach a bypass capacitor between the board's Vcc and GND.

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Operational Notes

1. Described numeric values and data are design representative values only and the values are not guaranteed.

2. We believe that the application circuit examples in this document are recommendable. However, in actual use, confirm characteristics further sufficiently. If changing the fixed number of external parts is desired, make your decision with sufficient margin in consideration of static characteristics, transient characteristics, and fluctuations of external parts and our LSI.

3. Absolute maximum ratings
   If the absolute maximum ratings such as supply voltage, operating temperature range, and so on are exceeded, LSI may be destroyed. Do not supply voltage or subject the IC to temperatures exceeding the absolute maximum ratings. In the case of fear of exceeding the absolute maximum ratings, take physical safety countermeasures such as adding fuses, and see to it that conditions exceeding the absolute maximum ratings should not be supplied to the LSI.

4. GND electric potential
   Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is not lower than that of GND terminal.

5. Thermal design
   Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

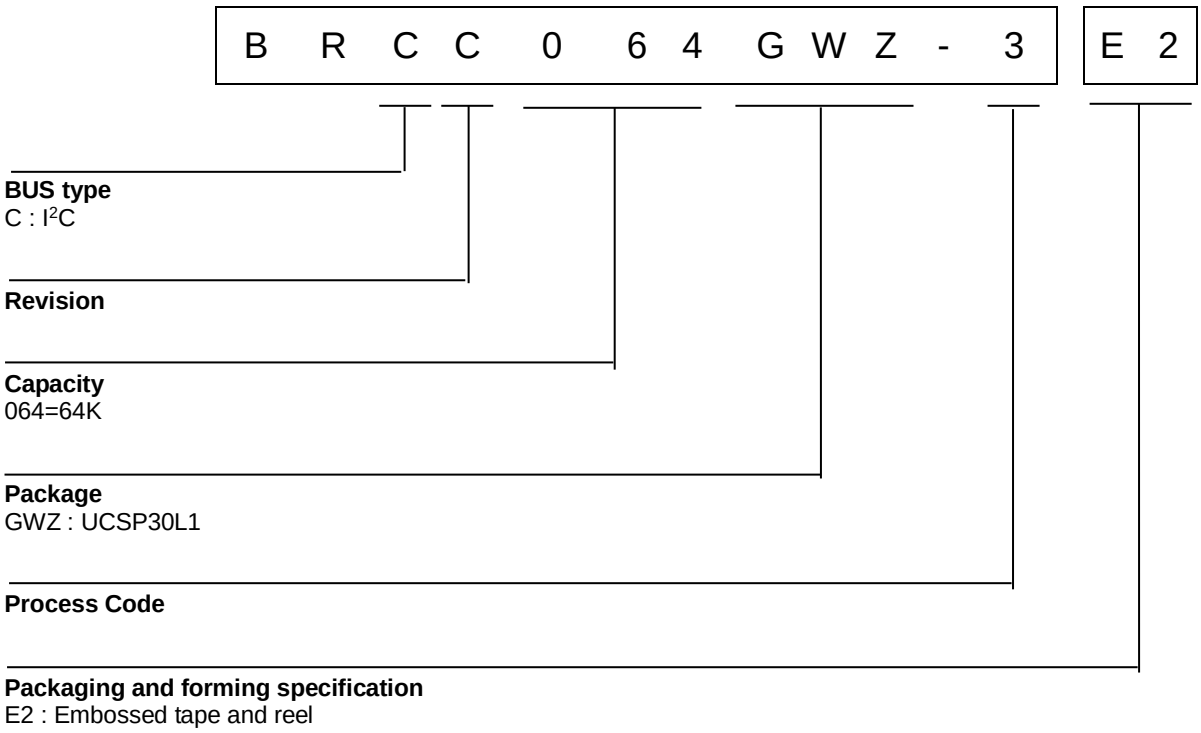
6. Short between pins and mounting errors
   Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

7. Operating the IC in the presence of strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

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Part Numbering

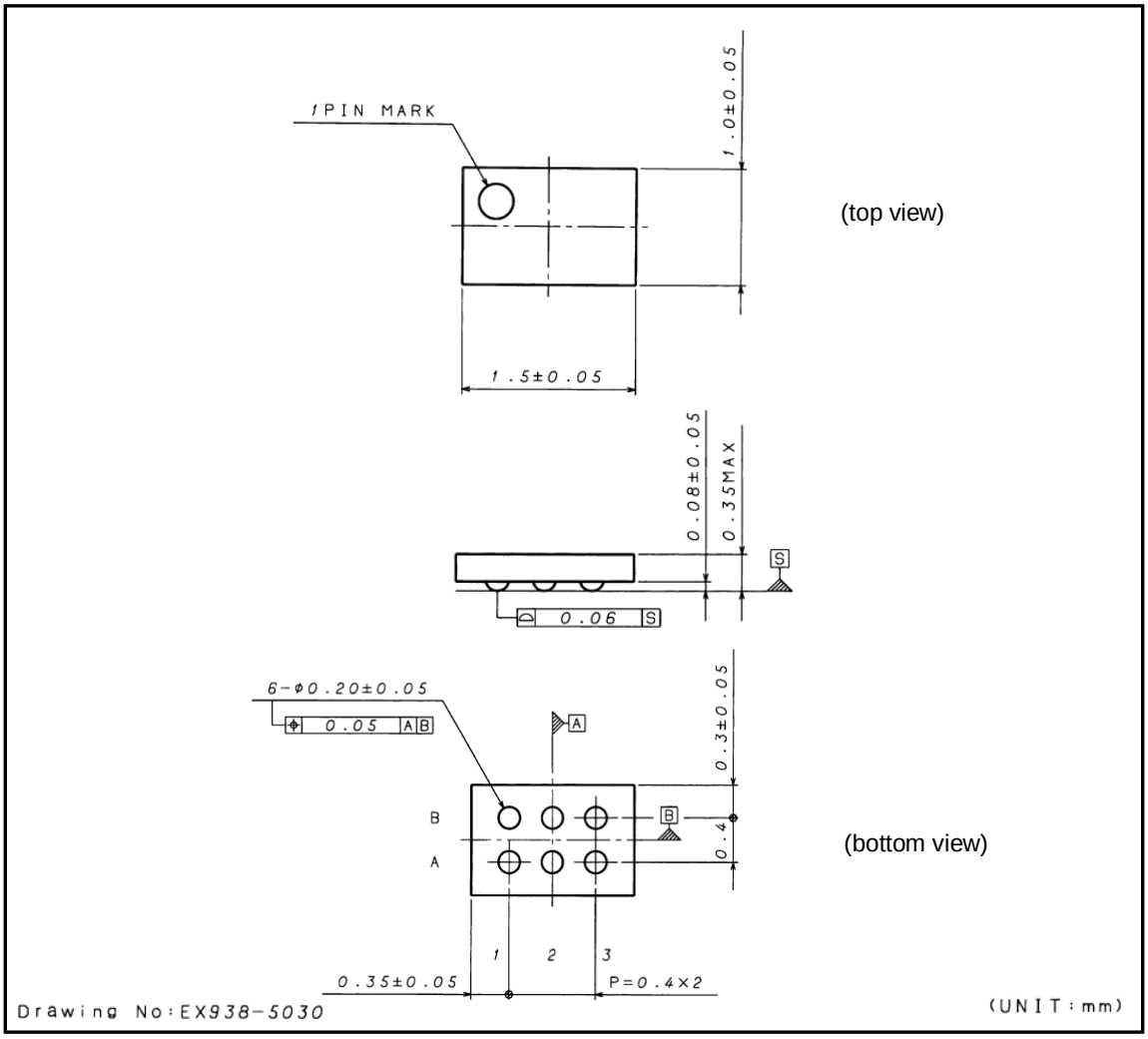


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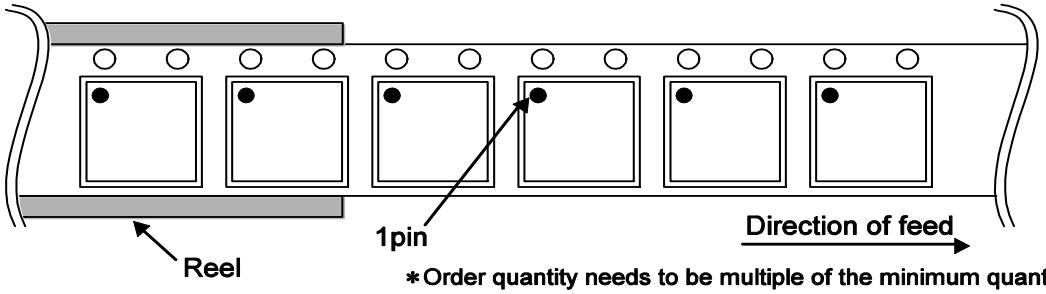
Physical Dimensions Tape and Reel Information

UCSP30L1



<Tape and Reel information>

Tape	Embossed carrier tape (heat sealing method)
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



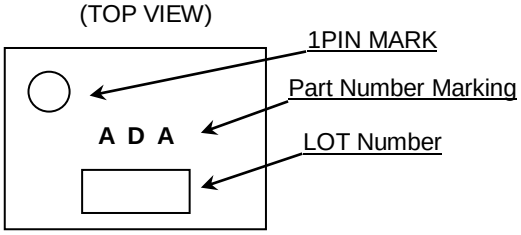
∗Order quantity needs to be multiple of the minimum quantity.

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Marking Diagram

UCSP30L1(BRCC064GWZ-3)
(TOP VIEW)



Revision History

Date	Revision	Changes
27.May.2013	001	New Release
21.Dec.2017	002	Change terminal name of slave address setting from TEST to A2
9.Nov.2018	003	Change terminal name of slave address setting from A2 to SLV P.13 Add the explanation of Device Addressing P.13 Add Table 1. The relationship of SLV Pin and Slave Address SLV Bit where EEPROM can operate

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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