LX7165

3V to 5.5V, 5A Constant Frequency Hysteretic Synchronous Buck Regulator with I²C Production Datasheet

Description

The LX7165 is a digitally controlled step-down regulator IC with an integrated 40mΩ high-side P-channel MOSFET and a 14mΩ low-side N-channel MOSFET. It features Microsemi's proprietary constant-frequency hysteretic control engine for near-instantaneous correction to line/load transients. It does not require high-ESR output capacitors and incorporates energy-saving "PSM" (Power Save or Pulse Skip Mode) at light loads, to extend battery life in mobile applications.

The LX7165 has an I²C serial interface port for output voltage margining and monitoring if required (it can also operate in default mode). In addition it includes robust fault monitoring functions.

The LX7165 will operate from 3V to 5.5V, and is readily available in 4 fixed output voltage options: 0.8, 0.9V, 0.95V, and 0.97V (no voltage divider is necessary). After start up, the reference voltage can be adjusted with I2C with a resolution 4.7mV between 0.6V and 1.2V. The output voltage can also be adjusted with an external voltage divider up to 3.3V.

Features

- Constant Frequency Hysteretic Control
- Extremely Fast Line/Load Transient Response
- I²C for Output Adjustment (3.4Mbps)
- 1.875 MHz Switching Frequency
- Extremely Low-R_{DSON} MOSFETS
- Input Voltage Rail 3.3V to 5V
- Greater than 5A Output Current
- I²C Selectable Power Save Mode for Light-Load Efficiency
- UVLO, OVP, OCP
- 0°C to +85°C Ambient Temperature
- Available in WLCSP-20 (0.4mm pitch)
- RoHS Compliant

Applications

- High Performance HDD
- Notebooks/Netbooks/Tablets/Slates

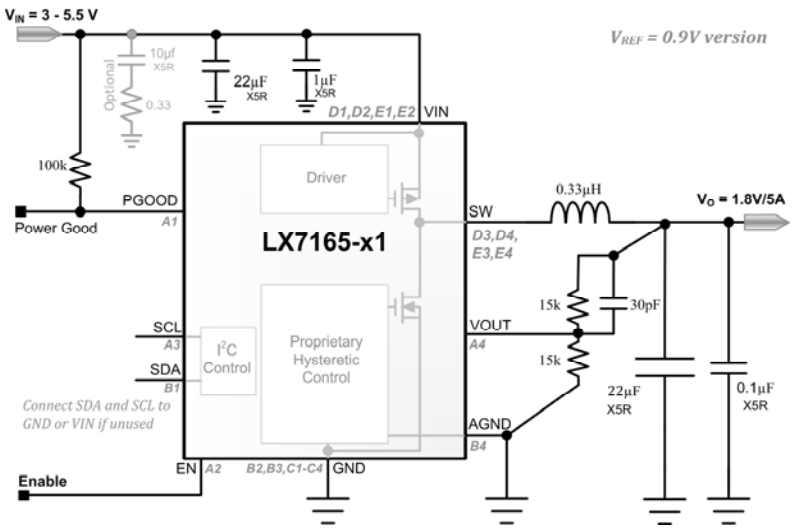


Figure 1: Typical 5V to 1.8V at 5A schematic with or without I²C implemented

Microsemi
Analog Mixed Signal Group
One Enterprise Aliso Viejo, CA 92656 USA, 1-800-713-4113, 949-380-6100, fax 949-215-4996

Other Typical Application Diagrams

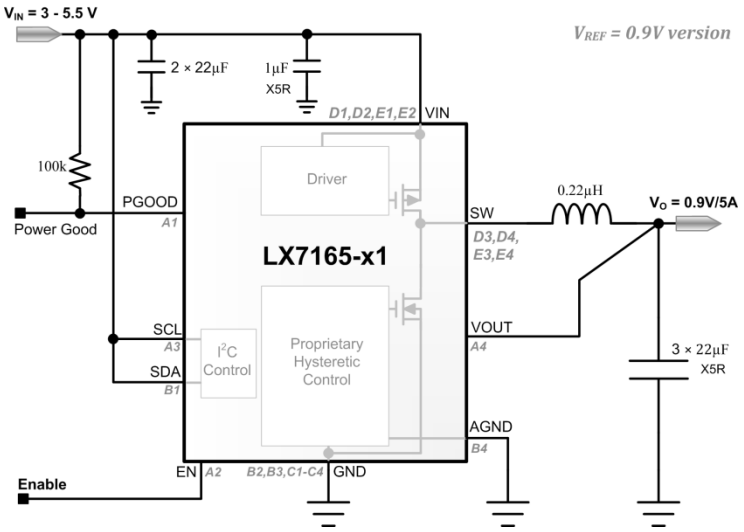


Figure 2: Typical 0.9V output schematic without I²C implemented

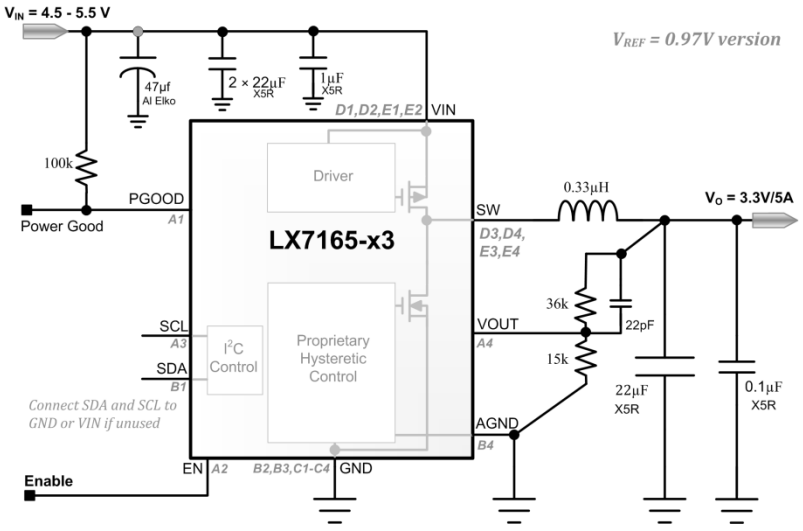
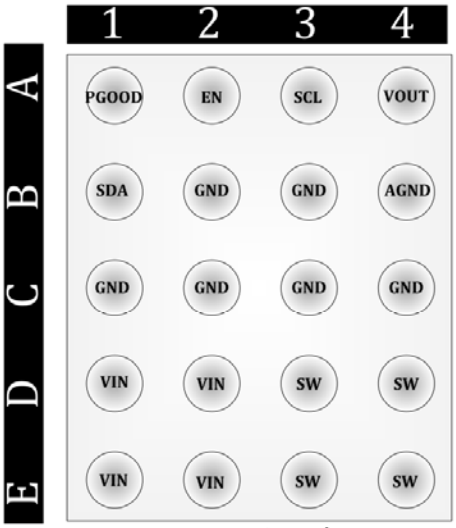
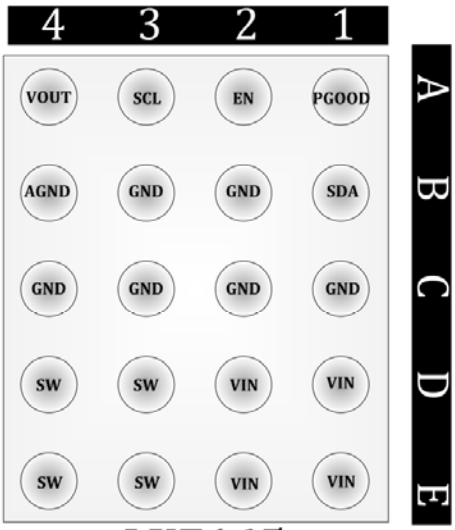


Figure 3: A typical 3.3V output schematic with or without I²C implemented

Pin/Ball Configuration



LX7165
Top View
(Ball Side Down)
20-ball Wafer Scale Package



LX7165
Bottom View
(Ball Side Up)
20-ball Wafer Scale Package

Part Marking:

MSC XXXX YWWA	XXXX=Device Number E.g.: 6501=LX7165-01CSP 6502=LX7165-02CSP	YWWA Year/Work Week/Lot Code

Figure 4: Pinout

Ordering Information

Ambient Temperature	Type	Package	Set Output Voltage	Part Number	Packaging Type
0°C to 85°C	RoHS compliant, Pb-free	WLCSP-20 (0.4mm pitch)	0.9V 0.95V 0.97V 0.8V 0.8V 0.8V 0.8V	LX7165-01CSP LX7165-02CSP LX7165-03CSP LX7165-05CSP LX7165-15CSP LX7165-25CSP LX7165-35CSP LX7165-xyCSP*	Bulk
			0.9V 0.95V 0.97V 0.8V	LX7165-01CSP-TR LX7165-02CSP-TR LX7165-03CSP-TR LX7165-05CSP-TR	Tape and Reel

			0.8V 0.8V 0.8V	LX7165-15CSP-TR LX7165-25CSP-TR LX7165-35CSP-TR LX7165-xyCSP-TR*	

* Consult factory for other I²C slave address and set output voltage options.
"x" is the 2 LSB bits of the binary I²C slave address valued 0 to 3;
"y" is the set output voltage (1 is 0.9V, 2 is 0.95V, 3 is 0.97V, 5 is 0.8V)

Pin/Ball Description

Pin/Ball Number	Pin/Ball Designator	Description
A1	**PGOOD**	Open Drain status output, requires external pull up resistor. This pin will go low when VOUT is outside the defined power good range, when the die is hotter than the thermal shutdown threshold, when PVIN is above the over voltage threshold, or when PVIN is below the under voltage threshold. PGOOD will go high 45ms after the last of these fault conditions clear.
A2	**EN**	Enable for switching regulator. Force high to enable, force low to disable the IC.
A3	**SCL**	Serial clock input for I²C. Connect directly to GND if unused.
A4	**VOUT**	Output voltage sense. Connect directly to output rail or resistive voltage divider output.
B1	**SDA**	Serial data bus (bidirectional) for I²C. Connect directly to GND if unused.
B2, B3, C1 – C4	**GND**	Ground. Connect to ground plane.
B4	**AGND**	Analog Ground. Connect to ground plane.
D1, D2 E1, E2	**VIN**	Input of IC and buck stage. Connect to input rail VIN (between 3V and 5.5V). A minimum input capacitance of one 1µF and one 22µF of X5R or better multilayer ceramic, should be placed very close to IC between this node and GND.
D3, D4 E3, E4	**SW**	Switching Node. Drives the external L-C low pass filter.

Functional Block Diagram

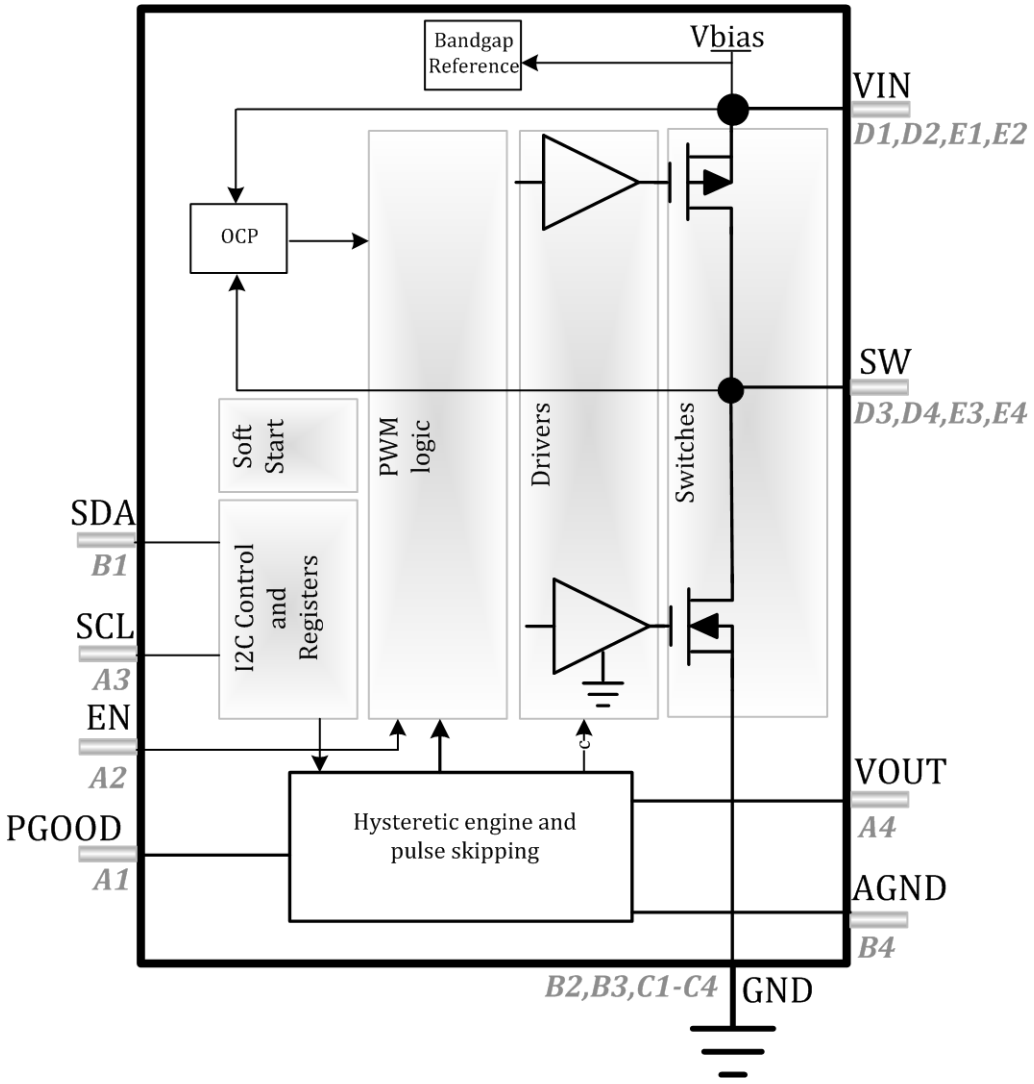


Figure 5: Block Diagram

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

	Min	Max	Units
VIN, SW to GND	-0.3	7	V
VOUT, SDA, SCL, EN, PGOOD to GND	-0.3	7	V
SW to GND (Shorter than 50ns)	-2	7	V
Maximum Junction Temperature		150	°C
Lead Soldering Temperature (40s, reflow)		260 (+0, -5)	°C
Storage Temperature	-65	150	°C

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

	Min	Max	Units
VIN	3	5.5	V
Ambient Temperature	0	85	°C
Output Current		5	A

Note: Corresponding Absolute Max Junction Temperature is 150°C.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	38	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

The following specifications apply over the operating ambient temperature of 0°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: VIN = 5V, EN = 5V, SCL = 5V, SDA = 5V, default register settings. Typical values stated, are either by design or by production testing at 25°C ambient.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Voltage						
I_Q	Input current	I_{LOAD} = 0, PSM enabled	200	440	600	µA
I_{IN}	Input current at shut down	EN = GND, T_A = 25°C		0.1	3	µA
$I_{IN\_I^2C}$	Input current I^2C shut down	VSEL(7) = low, EN = high		100	120	µA
UVLO	Under voltage rising threshold	VIN rising		2.6	2.8	V
$UVLO_{HYST}$	UVLO hysteresis			0.26		V
OVP_R	Over voltage rising threshold		6.25		6.75	V
OVP_F	Over voltage falling threshold		5.75		6.2	V
Reference Voltage						
V_{REFMIN}	Minimum reference voltage	VSEL(6:0) = 00h	0.588	0.6	0.612	V
$V_{REFMEAN}$	Mean reference voltage	VSEL(6:0) = 40h	0.888	0.9	0.912	V
V_{REFMAX}	Maximum reference voltage	VSEL(6:0) = 7Fh	1.184	1.195	1.206	V
T_{SS}	V_{REF} slew rate	SLEW: Ctrl2(2:0) = 011	3	4	5.5	mV/µs
T_{HICCUP}	Hiccup time	VOUT = 0.2V		1.5		ms
Output Voltage						
VOUT	Default VOUT	Target based on option: 00 = 0.8V, 01 = 0.9, 10 = 0.95, 11 = 0.97. Measured with respect to target voltage.	-1.5	0	1.5	%
	Line regulation	VIN from 3V to 5.5V, I_{LOAD} = 1A. Note 1		0.1		%
	Load regulation	I_{LOAD} = 0A to 5A. Note 1		-0.23		%/A
	VOUT input current			0	1	µA
V_{OUV}	VOUT under	VOUT below this threshold will	77	82	85	%V_{REF}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	voltage threshold	initiate a hiccup sequence				
SW						
R_{DSON_H}	High side on resistance	VIN = 5V		40		mΩ
R_{DSON_L}	Low side on resistance	VIN = 5V		14		mΩ
OCP	Current limit	Note 1	6.5	7.5	10.0	A
T_{SH}	Thermal shut down threshold	Note 1		150		°C
T_H	Hysteresis	Note 1		20		°C
F_{SW}	PWM switching frequency		1.5	1.875	2.25	MHz
R_{SWDISC}	SW discharge resistance	EN = low; Discharge: Ctrl2(4) = 1	80	200	1400	Ω
EN, SDA (as input), SCL						
V_{IH}	Input high		1.1			V
V_{IL}	Input low				0.4	V
V_H	Hysteresis			0.1		V
I_{II}	Input current			0	1	µA
PGOOD						
V_{PG90}	PGOOD VOUT lower threshold	VOUT rising, percentage of V_{REF}	85	90	95	$\%V_{REF}$
V_{PG110}	PGOOD VOUT upper threshold	VOUT falling, percentage of V_{REF}	105	110	115	$\%V_{REF}$
V_{PGHY}	Hysteresis	Percentage of V_{REF}		5		$\%V_{REF}$
PG_{RDSON}	PGOOD pull down resistance			100	300	Ω
	PGOOD leakage current			0	1	µA
	PGOOD delay	PGOOD rising edge delay	30	45	65	ms
7 Bit DAC						
	Differential linearity	Monotonicity assured by design			0.8	LSB

Note 1: Guaranteed by design.

Application Specifics

Efficiency	I_{OUT} = 2.0A, VCC = 5V, VOUT = 3.3V	95%
	I_{OUT} = 5.0A, VCC = 5V, VOUT = 3.3V	90%
VOUT Min Transient	0.5 A to 2.5 A load step slews in 660ns, C_{LOAD} = 3 x 22µF ceramic caps, 0.47µH inductor	27.2mV
VOUT Max transient	2.5 A to 0.5 A load step slews in 1.6µs, C_{LOAD} = 3 x 22µF ceramic caps, L = 0.47µH inductor	26.8mV
Typical Load Inductance	DCR = 6.7mΩ, IDC = 12.2A, ISAT = 16A	0.47µH
Typical Load Capacitance	6.3V, X5R	3x22µF

Layout Recommendations

The LX7165 EVAL Board is a 4-layer board, the thickness of the board is 63mil in total. The second layer to top layer is 7mil, the third layer to the bottom layer is 7mil. The recommended BGA PCB layout shown below requires no microvias or blind vias. Each signal trace can exit the LX7165 directly without any vias under the device. Also, with the bypass capacitors C2, C3 and C8 implemented as shown it can lower the ESL. Please see LX7165 User Guide for additional details.

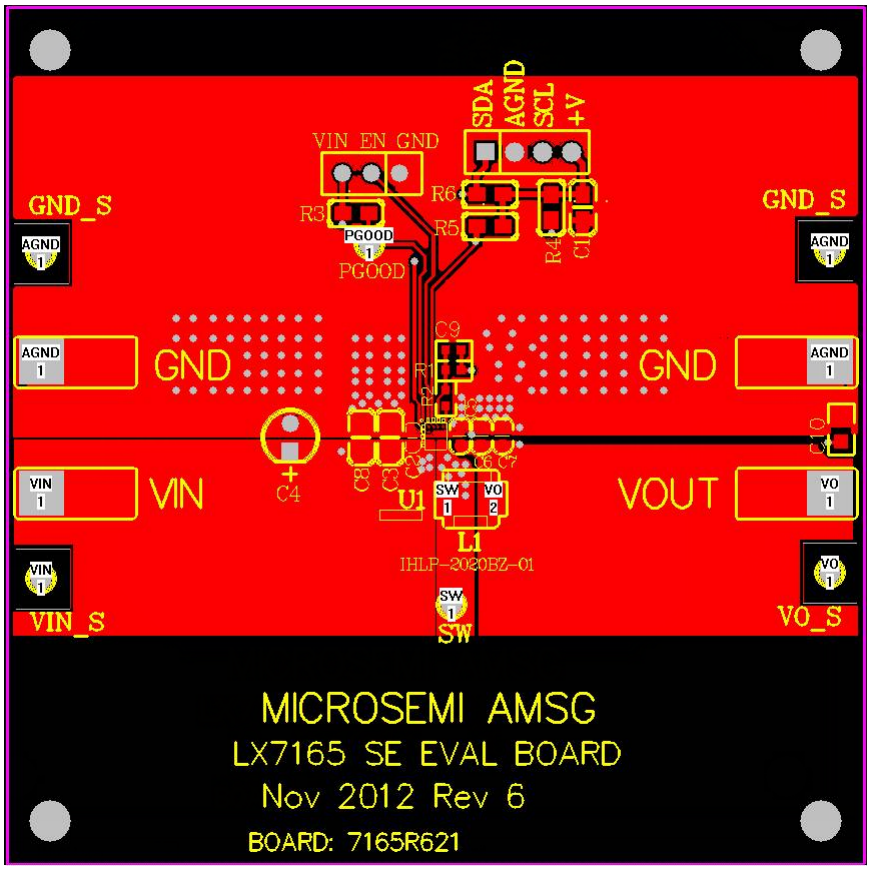


Figure 6: Layout recommendation (TOP layer)

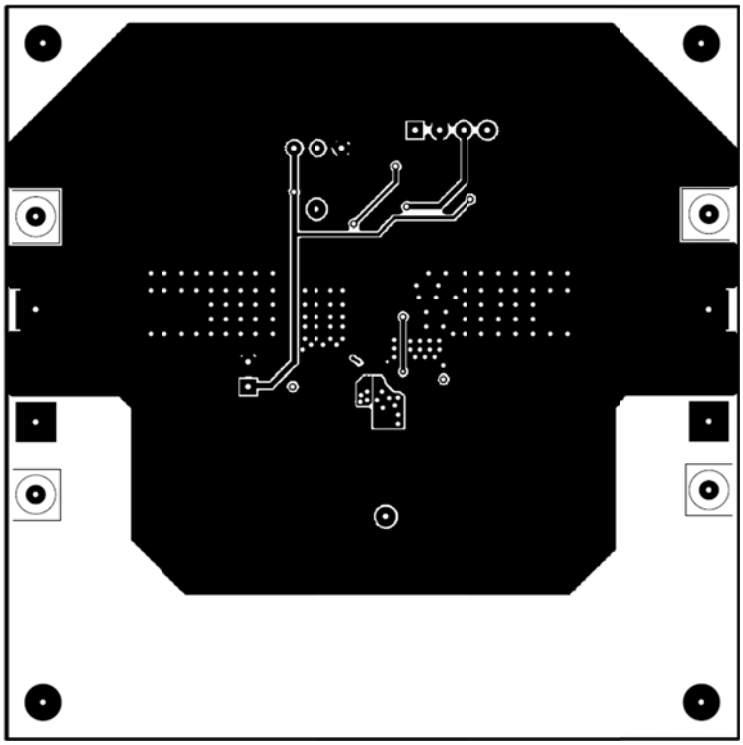


Figure 7: Layout recommendation (BOTTOM layer)

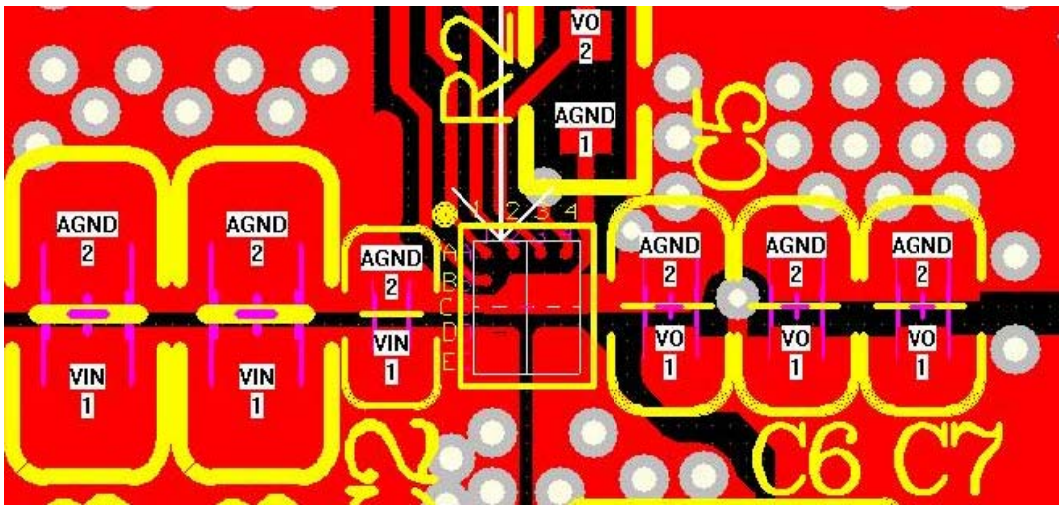


Figure 8: Closeup of Layout in Region of BGA (note Ground gull-wings and via Stitching to BOTTOM)

Typical Performance Curves

Dynamic Response

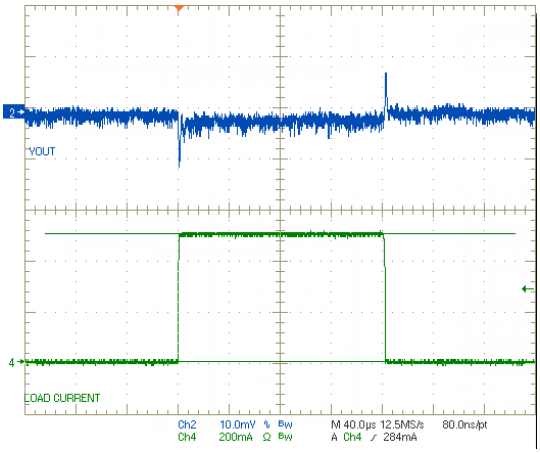


Figure 9: No load to 0.5A PWM
CH2: VOUT, CH4: I_{LOAD}

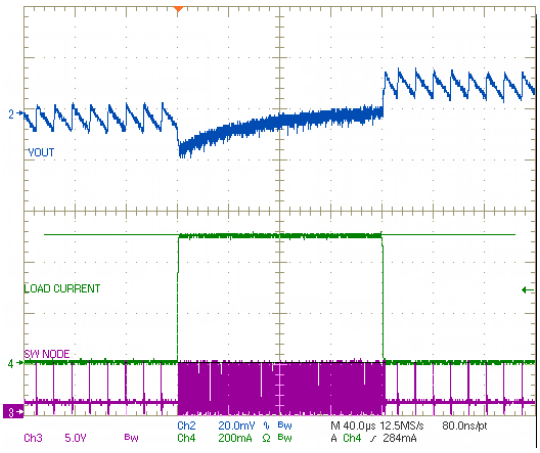


Figure 10: No load to 0.5A PSM
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

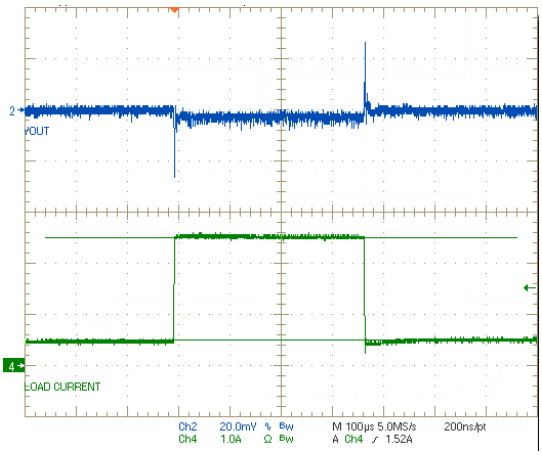


Figure 11: 0.5A to 2.5A PWM
CH2: VOUT, CH4: I_{LOAD}

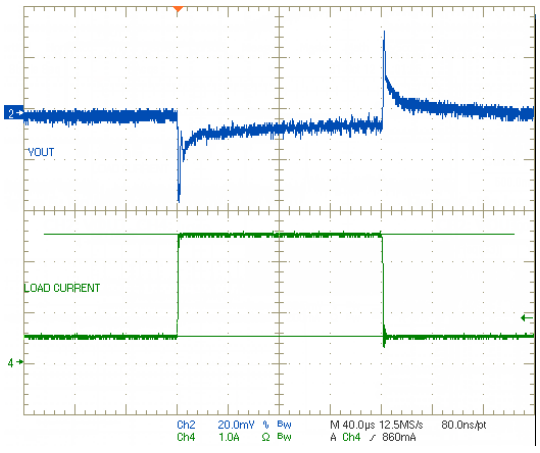


Figure 12: 0.5A to 2.5A PSM
CH2: VOUT, CH4: I_{LOAD}

Typical Performance Curves (Continued)

Dynamic Response (Continued)

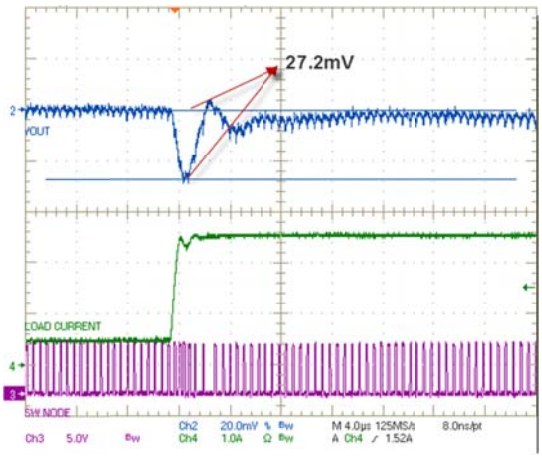


Figure 13: 0.5A to 2.5A PWM Rising Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

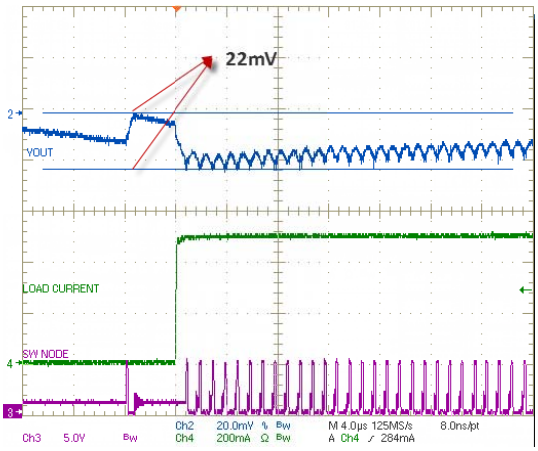


Figure 14: No load to 0.5A PSM Rising Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

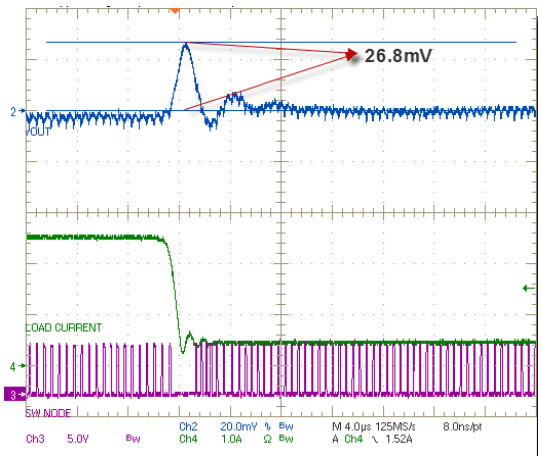


Figure 15: 0.5A to 2.5A PWM Falling Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

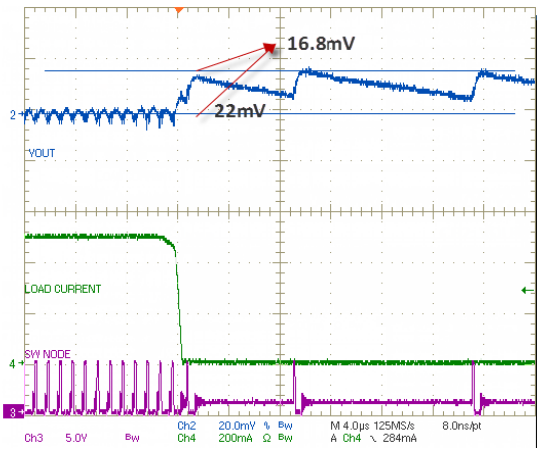


Figure 16: No load to 0.5A PSM Falling Edge
CH2: VOUT, CH3: SW, CH4: I_{LOAD}

Typical Performance Curves (Continued)

Efficiency

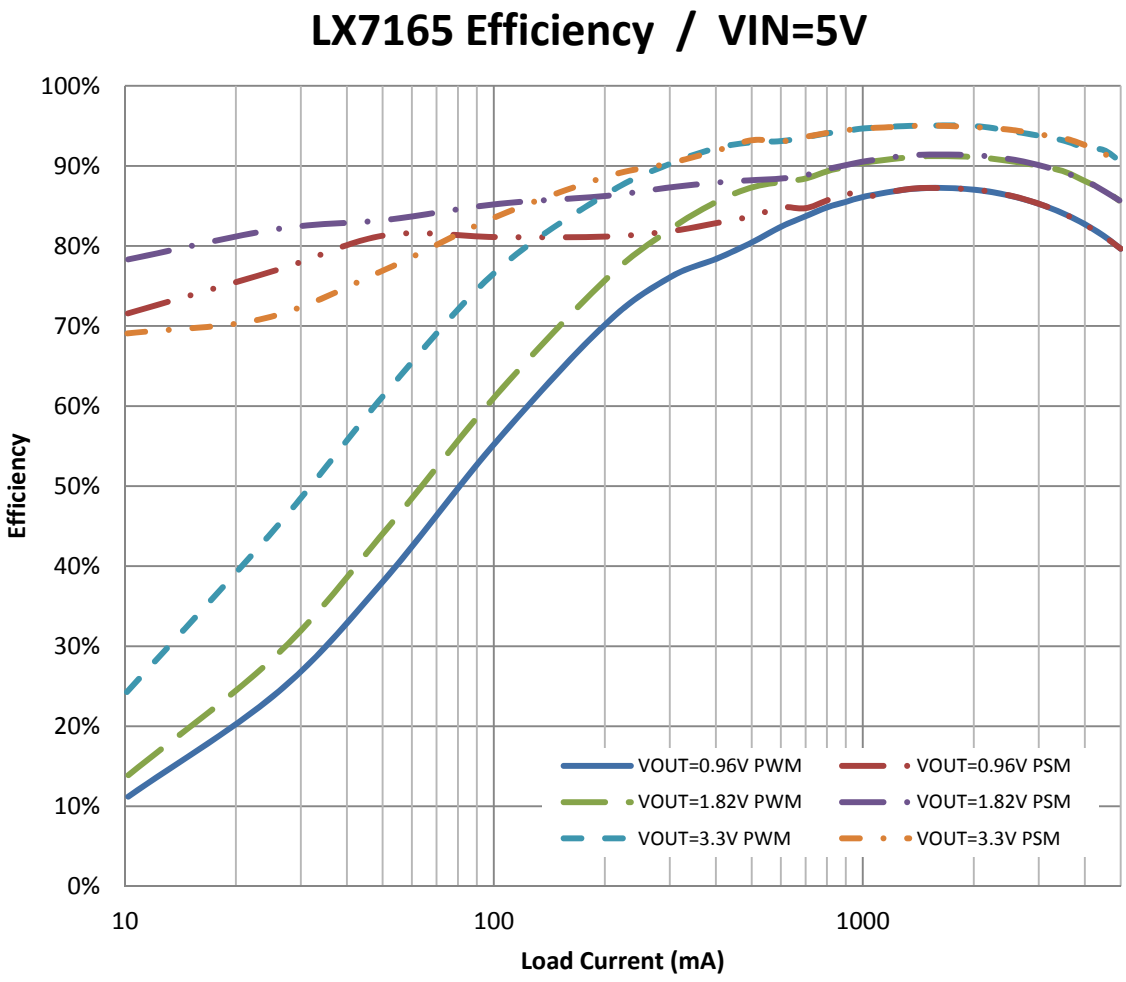


Figure 17: Efficiency Curves for 5V input

I²C Timing Specifications

Symbol	Parameter	Conditions	C_b = 100 pF (max) (*Note2)		C_b = 400 pF		Unit
			Min	Max	Min	Max	
f_{SCHL}	SCL clock frequency		0	3.4	0	0.4	MHz
$t_{SU;STA}$	Set-up time for a repeated START condition		160	-	600	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition		160	-	600	-	ns
t_{LOW}	LOW period of the SCL clock		160	-	1300	-	ns
t_{HIGH}	HIGH period of the SCL clock		60	-	600	-	ns
$t_{SU;DAT}$	Data set-up time		10	-	100	-	ns
$t_{HD;DAT}$	Data hold time		0	70	0	-	ns
t_{rCL}	Rise time of SCL signal		10	40	$20*0.1C_b$	300	ns
t_{rCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit		10	80	$20*0.1C_b$	300	ns
t_{fCL}	Fall time of SCL signal		10	40	$20*0.1C_b$	300	ns
t_{rDA}	Rise time of SDA signal		10	80	$20*0.1C_b$	300	ns
t_{fDA}	Fall time of SDA signal		10	80	$20*0.01C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		160	-	600	-	ns
t_{BUF}	Bus free time between a STOP and START condition		160	-	1300	-	ns
$t_{VD;DAT}$	Data valid time		-	160	-	900	ns
$t_{VD;ACK}$	Data valid acknowledge time		-	160	-	900	ns
C_b	Capacitive load for each bus line	SDA and SCL lines	-	100		400	pF

Note 1: All values referred to V_{IH}(min) and V_{IL}(max) levels of I/O stages table.
Note 2: Loads in excess of 100pF will restrict bus operation speed below 3.4MHz

Operation Theory

Basic Operation

The LX7165 compares VOUT voltage to an internal reference, V_{REF}. When VOUT is lower than V_{REF}, the upper switch turns on and the lower switch turns off. When VOUT is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp helps to keep the switching frequency constant over a wide range of output capacitor values and parasitic components (i.e. ESR, ESL). In addition, a frequency control loop keeps the switching frequency constant during continuous conduction mode.

At light loads, if enabled, the converter automatically reduces the switching frequency and enters discontinuous conduction to optimize efficiency while ensuring low VOUT ripple voltage.

An integrated I²C bus interface, operating up to 3.4Mbps, adds the following use programmability to the converter:

1. On the fly programming of the output voltage in 4.7mV increments.
2. Enable / Disable the regulator.
3. Allow PSM or limit operation to only PWM mode.
4. Set the V_{REF} slew rate.
5. Switch node slew rate control.

$$V_{REF} = 0.6V + N_{SEL} \cdot 0.0046875\ V$$

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right)$$

$$V_{OUT} = V_{REF}$$

Operation Theory (Continued)

Over Current Protection

The LX7165 protects against all types of short circuit conditions. Cycle by cycle over current protection turns off the upper switch when the current exceeds the OCP threshold. When this occurs, the upper switch is held off for at least 350ns before being allowed to turn on again. After startup, if VOUT drops below the VOUT under voltage threshold, a hiccup sequence will be initiated where both output switches are shut off for 1.5ms before initiating another soft start cycle. This protects against a crowbar short circuit. The VOUT under voltage detection is not active during start up.

Positive Voltage Transitions

After the initial start up sequence, the output voltage can be programmed to a new value by programming the VSEL register bits and then asserting the GO bit. V_{REF} will transition to the new value at the programmed slew rate. The PGOK monitor bit is deasserted during the V_{REF} ramp time, or when VOUT is outside the error envelope.

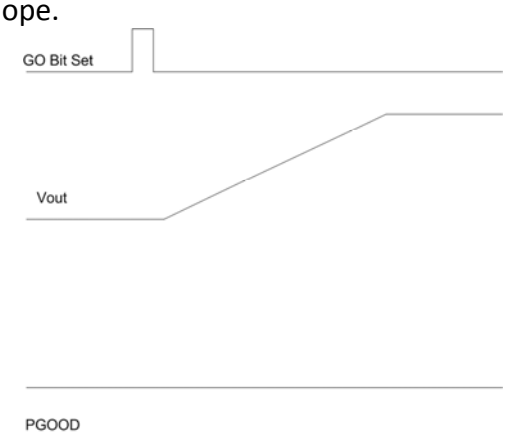


Figure 18: Positive Voltage Transition

Negative Voltage Transitions

A negative voltage transition occurs when a lower output voltage is programmed into the VSEL register, and initiated by asserting the GO bit. In PSM, the LX7165 will not discharge the output filter capacitor.

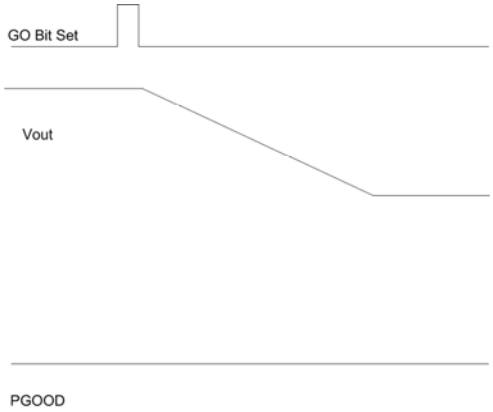


Figure 19: Negative Voltage Transition

Enabling Regulator from I²C Bus

In addition to the EN pin, the regulator can be enabled and disabled via the I²C bus by programming the control register. During disable, the regulator and most of the support circuitry is turned off. However, the I²C bus circuitry is still active and may be programmed.

Switch Node rise rate adjustment

The LX7165 can be programmed to operate in a lower emissions mode by slowing down the switch node rise rate. In this mode, the switch node rise rate will slow down 25%, reducing the switching frequency harmonic content.

I²C Interface

I²C Port Functional Description

- Simple two wire, bidirectional, serial communication port.
- Multiple devices on same bus speeds from 400Kbps (FS-Mode) to 3.4Mbps (HS-Mode).
- SOC Master controls bus.
- Device listens for the unique address that precedes data.

General I²C Port Description

The LX7165 includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage when they are not being controlled by a device on the bus. The LX7165 interface acts as a I²C slave that is clocked by the incoming SCL clock. The LX7165 I²C port will support both the Fast mode (400kHz max) and typically the High Speed mode(3.4MHz max). The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

Register Map

The LX7165 has four 8-bit user-accessible registers. See Control Register Bit Definition.

Slave Address

In the table below, the A1 and A0 are the binary value of the address given in the ordering information shown on page 3.

7	6	5	4	3	2	1	0
1	1	0	0	A2	A1	A0	R/W

A2=”0” for y=1-3, “1” for y=5

Table 1: I²C Slave Address

START and STOP Commands

When the bus is idle, both SCL and SDA must be high except in the power up case where they may be held high or low during the system power up sequence.

The STX SOC (bus master) signals START and STOP bits signify the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The STX SOC acts as the I²C master and always generates the START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transfer, STX SOC master can generate repeated START conditions. The START and the repeated START conditions are functionally equivalent.

I²C Interface (Continued)

Data Transfers

Data is transferred in 8 bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the master. The acknowledge occurs when the transmitter master releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver slave during the 9th clock pulse to signify acknowledgment. A receiver slave which has been addressed must generate an acknowledgement ("ACK") after each byte has been received.

After the START condition, the STX SOC (I^2C) master sends a chip address. The standard I^2C address is seven bits long. Making the eighth bit a data direction bit (R/W). For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

When a receiver slave doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP command to abort the transfer. If a slave receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow.

The slave leaves the data line HIGH and the master generates the STOP command. The data line is also left high by the slave and master after a slave has transmitted a byte of data to the master in a read operation, but this is a not acknowledge that indicates that the data transfer is successful.

Data Transfer Timing for Write Commands

In order to help assure that bad data is not written into the part, data from a write command is only stored after a valid STOP command has been performed.

I²C Electrical Characteristics

The minimum HIGH and LOW periods of the SCL clock specified the I^2C Timing Specification table determine the maximum bit transfer rates of, 400 kbit/s for Fast-mode devices, and 3.4 Mbits/s for HS-mode Plus. Devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the I^2C clock synchronization procedure, which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Figures 22 and Figure 23 show all timing parameters for the HS & FS-mode timing. The 'normal' START condition S does not exist in HS-mode. Timing parameters for Address bits, R/W bit, Acknowledge bit and DATA bits are all the same. Only the rising edge of the first SCL clock signal after an acknowledge bit has a larger value because the external Rp has to pull-up SCL without the help of the internal current-source.

I²C Interface (Continued)

The HS & FS-mode timing parameters for the bus lines are specified in the I²C Timing Specification Table. The minimum HIGH and LOW periods and the maximum rise and fall times of the SCL clock signal determine the highest bit rate.

With an internally generated SCL signal with LOW and HIGH level periods of 200ns and 100ns respectively, an HS-mode master fulfills the timing requirements for the external SCL clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4 Mbit/s. So a basic frequency of 10 MHz, or a multiple of 10 MHz, can be used by an HS-mode master to generate the SCL signal. There are no limits for maximum HIGH and LOW periods of the SCL clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load up to 100 pF for each bus line allowing the maximum possible bit rate of 3.4 Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400 pF are specified in I²C Timing Specification Table, allowing a maximum bit rate of 1.7 Mbit/s. For capacitive bus loads between 100 pF and 400 pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDA and SCL to prevent reflections of the open ends.

1	7	1	1	8	1	8	1	1
Start	xxxxxxx Device Address	0 Write	Ack	xxxxxxxx Register Address	Ack	xxxxxxxx Data	Ack	Stop

Figure 20: Write Protocol

1	7	1	1	8	1	1	7	1	1	8	1	1
Start	xxxxxxx Device Address	0 Write	Ack	xxxxxxxx Register Address	Ack	Repeated Start	xxxxxxx Device Address	1 Read	Ack	xxxxxxxx Data	Master Ack	Stop

Figure 21: Read Protocol

Microsemi

I²C Interface (Continued)

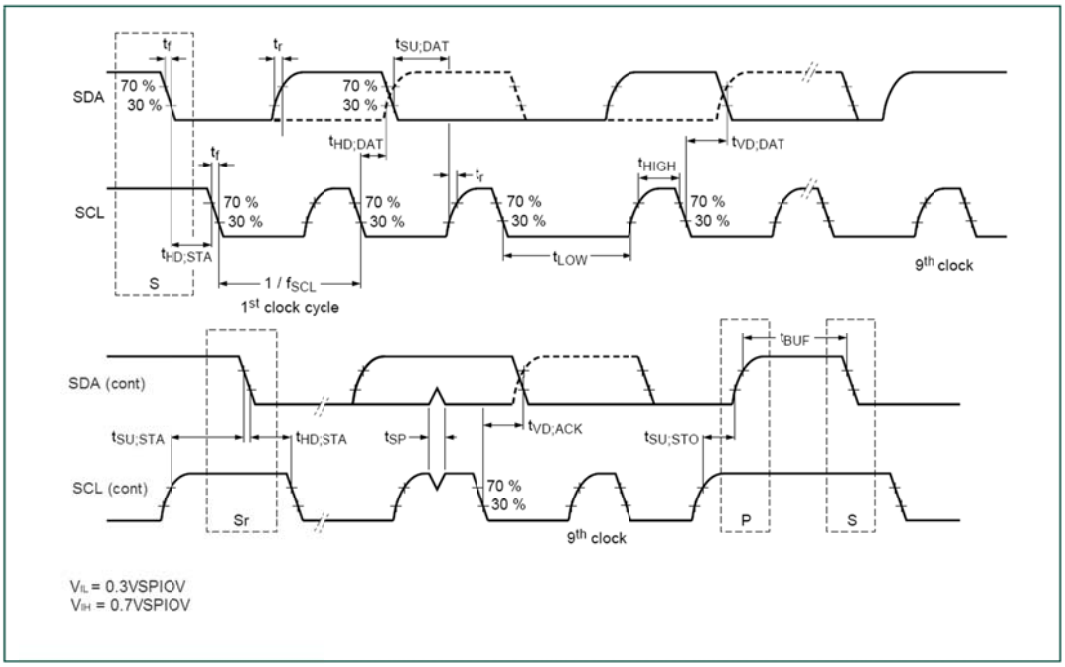


Figure 22: Definition for FS-Mode devices on the I²C Port

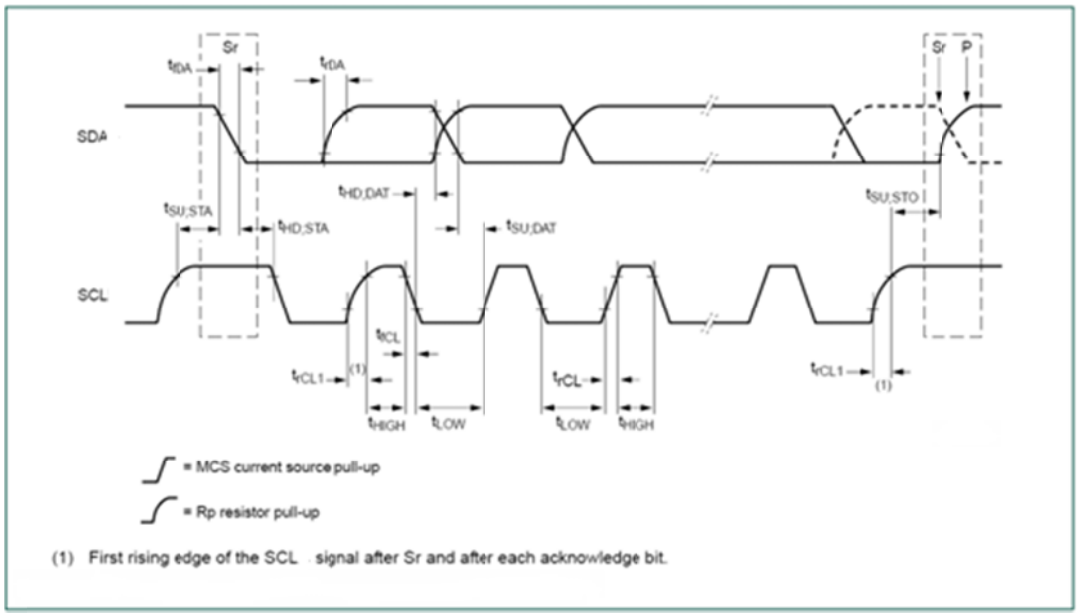


Figure 23: Timing definition for HS-mode devices on the I²C Port

I²C Interface (Continued)

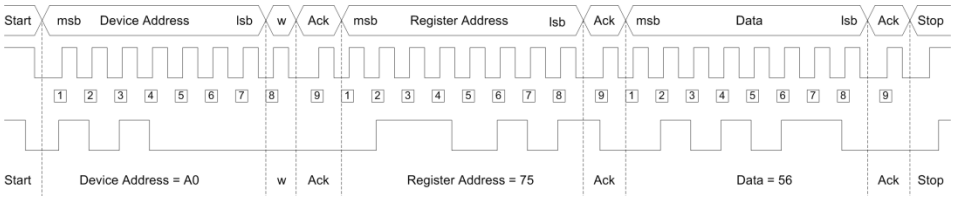


Figure 24: Write Cycle Diagram

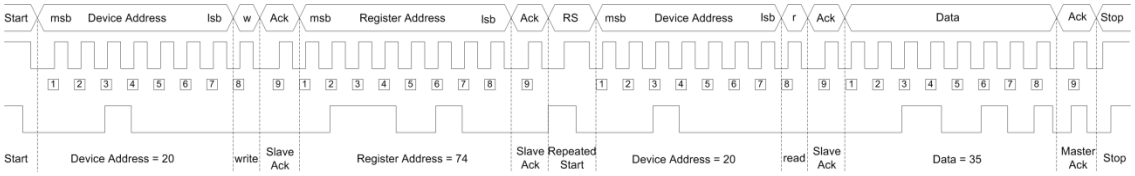


Figure 25: Read Cycle Diagram

Control Register Bit Definition

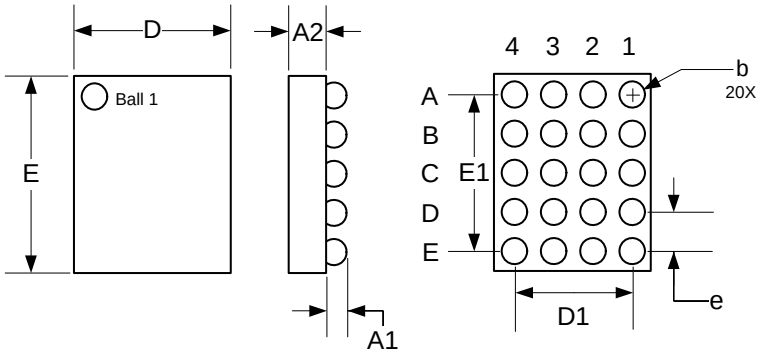
Bit	Name	Value	Description
Status, Address 00h			
7:3	Reserved		
2	OCP		Latched to 1 if the over current limit is reached. Write a "1" to reset the status flag.
1	OTP		Latched to 1 if an over temperature event occurs. Write a "1" to reset the status flag.
0	FB_UVLO		Latched to 1 if a FB_UVLO event occurs. Write a "1" to reset the status flag.
Vsel, Address 01h, (aka dac)			
7	EN	1-d	Device enabled.
		0	Device disabled.
6:0	VSEL[6:0]		7-bit DAC value to set V_{REF}. The default value is determined by the part ordering code.

Bit	Name	Value	Description
Ctrl1, Address 02h, (aka reg2)			
7:6	Reserved	00-d	
5	ctrl1	1-d	TBD
4	DLY_DIS	1	Disable 45ms delay on PGOOD.
		0-d	45ms delay on PGOOD is enabled.
3	SW_RATE	1-d	Normal high efficiency rise rate.
		0	Reduced switch node rise rate.
2	Reserved	1-d	
		0	
1	Reserved	1-d	
		0	
0	MODE	1-d	PWM mode only – NO PSM.
		0	Power Saving Mode – allows discontinuous conduction.
Vendor ID, Address 03h (Read Only)			
7:4	VID[3:0]	0010	Microsemi Vendor ID .
3:2	A1A0	00	Designates the slave address version. These bits will correspond to the two LSB bits.
1:0	VOUT	XX	Designates the default output voltage version, 00=0.8V, 01=0.9V, 10=0.95V, 11=0.97V.
Ctrl2, Address 04h, (aka reg4)			
7:6	Reserved		
5	GO	1	Writing to this bit starts a VOUT transition regardless of its initial value.
		0-d	The VOUT is ramped to the default VSEL Value.
4	Discharge	1	When the regulator is disabled, the output voltage is discharged through the SW pin.
		0-d	When the regulator is disabled, the output voltage Is not discharged.
3	PGOK (read only)	1	Is high when output is in regulation and V_{REF} has stabilized.
		0	Is low during a output voltage transition or when the output is not in regulation.
2:0	SLEW	000	Reserved.
		001	Reserved.
		010	V_{REF} slews at 2mV/µs.
		011-d	V_{REF} slews at 4mV/µs; this is the default setting.
		100	V_{REF} slews at 8mV/µs.
		101	V_{REF} slews at 16mV/µs.
		110	V_{REF} slews at 32mV/µs.
		111	V_{REF} slews at 64mV/µs.

Note: -d is the default value at startup.

Package Dimensions

WLCSP 20 Ball 0.4mm Pitch



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A1	0.186	0.226	0.0073	0.0089
A2	0.360	0.400	0.0142	0.0157
b	0.240	0.280	0.0094	0.0110
D1	1.20 BSC		0.0472 BSC	
D		1.630		0.0642
e	0.40 BSC		0.0157 BSC	
E1	1.60 BSC		0.0630 BSC	
E		2.045		0.0805

Note:
1.Solder ball composition SnAgCu

Recommended Footprint