

PH1330AL

N-channel 30 V 1.3 mΩ logic level MOSFET in LPAK

Rev. 01 — 14 October 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in LPAK package qualified to 150 °C. This product is designed for computing customers only

1.2 Features and benefits

- Advanced TrenchMOS provides low $R_{DS(on)}$ and low gate charge
- High efficiency gains in switching power convertors
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

1.3 Applications

- For computing customers only

1.4 Quick reference data

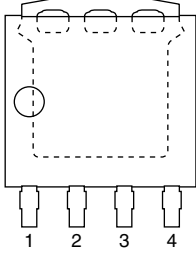
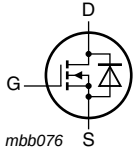
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	121	W
T_j	junction temperature		-55	-	150	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	-	383	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$;	-	9.3	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 12\text{ V}$; see Figure 13 and 14	-	46.6	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 100\text{ °C}$; see Figure 12	-	-	1.8	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; see Figure 17	-	1.04	1.3	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		
			SOT1023 (LPAK2)	

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PH1330AL	LPAK2	Plastic single-ended surface-mounted package (LPAK2); 4 leads	SOT1023

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1 ^[1]	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ^[1]	-	100	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	923	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	121	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C

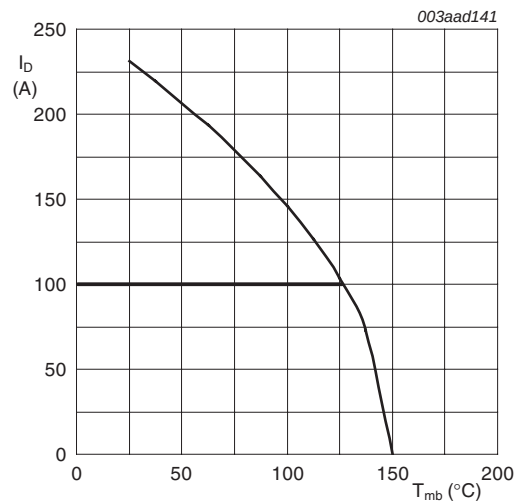
Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$; ^[1]	-	100	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	923	A

Avalanche ruggedness

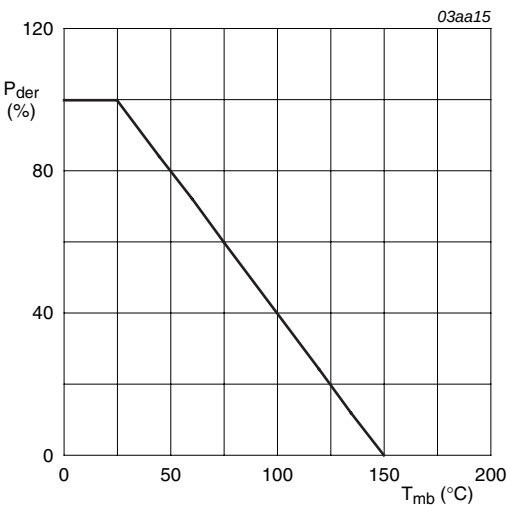
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	383	mJ
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[1] Continuous current is limited by package.



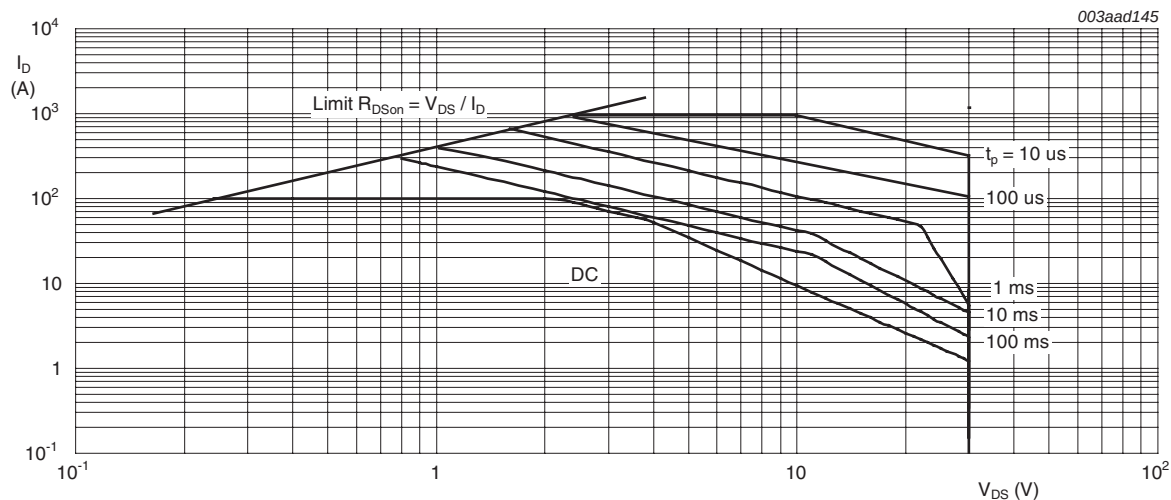
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.4	1.03	K/W

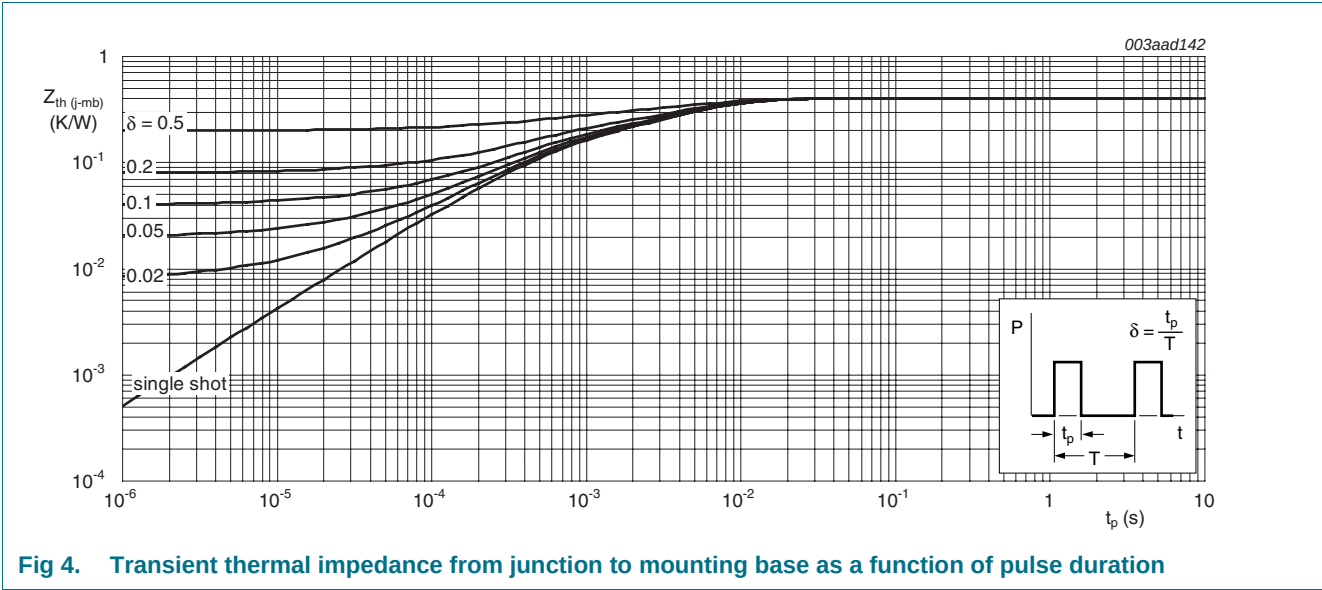


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

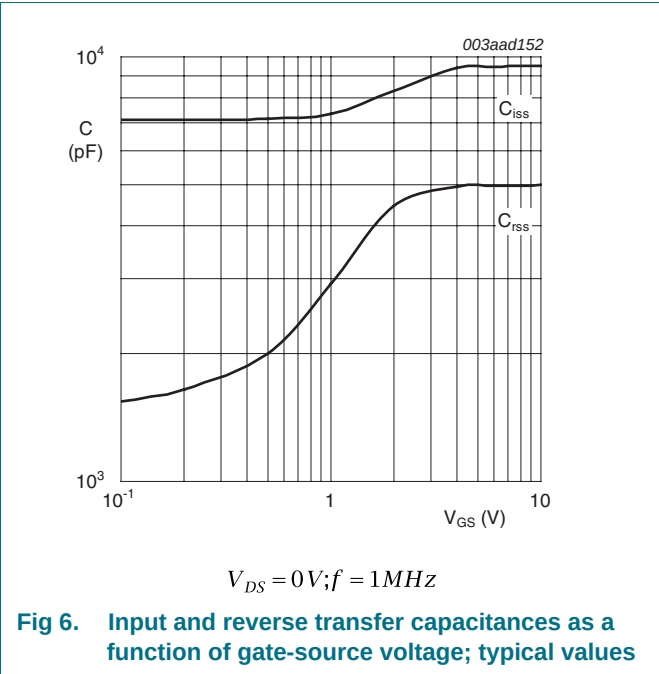
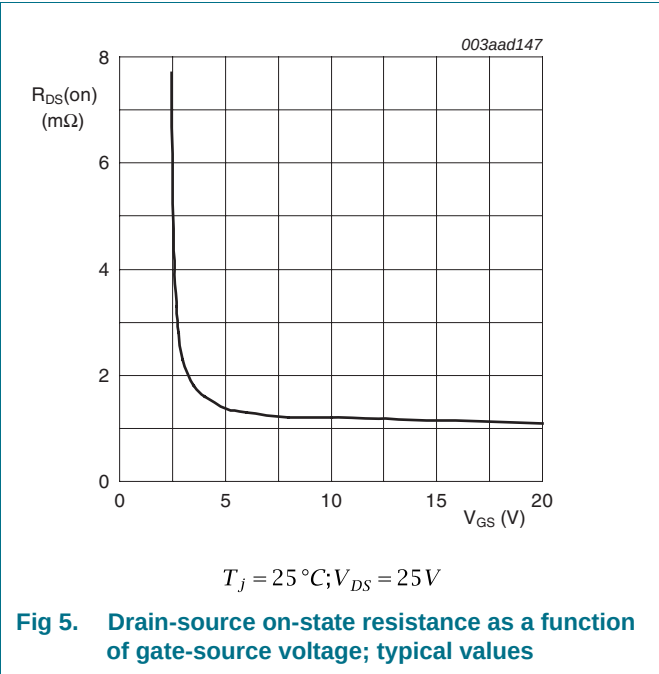
6. Characteristics

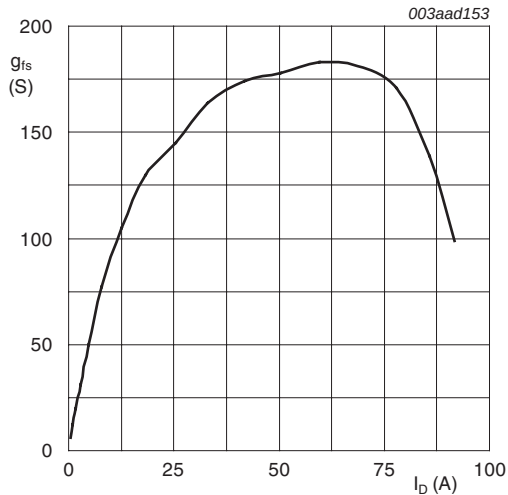
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	30	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 and 11	1.3	1.7	2.15	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ\text{C}$; see Figure 10	0.65	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$; see Figure 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1.5	μA
		$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 15\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -15\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 17	-	1.43	1.95	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 100\ ^\circ\text{C}$; see Figure 12	-	-	1.8	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12	-	1.9	2.8	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 15\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 17	-	1.04	1.3	mΩ
R_G	gate resistance		-	0.89	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 13 and 14	-	100	-	nC
		$I_D = 0\ \text{A}$; $V_{DS} = 0\ \text{V}$; $V_{GS} = 10\ \text{V}$	-	90	-	nC
		$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 13 and 14	-	46.6	-	nC
Q_{GS}	gate-source charge		-	17.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 13	-	11	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6.9	-	nC
Q_{GD}	gate-drain charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 13 and 14	-	9.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12\ \text{V}$; see Figure 13 and 14	-	2.53	-	V
C_{iss}	input capacitance	$V_{DS} = 12\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$;	-	6227	-	pF
C_{oss}	output capacitance	$T_j = 25\ ^\circ\text{C}$; see Figure 15	-	1415	-	pF
C_{rss}	reverse transfer capacitance		-	619	-	pF

Table 6. Characteristics ...continued

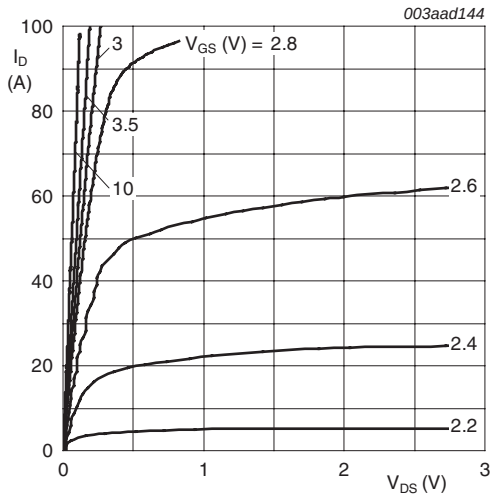
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 12 V; R _L = 0.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5.6 Ω	-	64	-	ns
t _r	rise time		-	108	-	ns
t _{d(off)}	turn-off delay time		-	106	-	ns
t _f	fall time		-	52	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.88	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/s; V _{GS} = 0 V;	-	46	-	ns
Q _r	recovered charge	V _{DS} = 20 V	-	53	-	nC





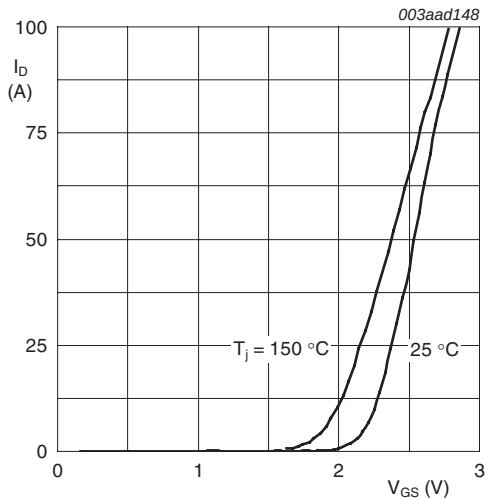
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 25\text{ V}$

Fig 7. Forward transconductance as a function of drain current; typical values



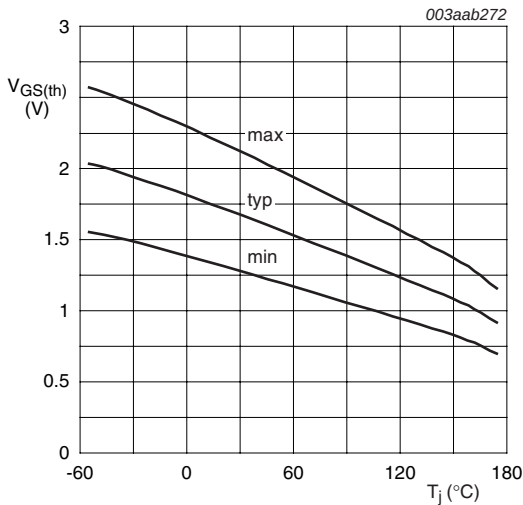
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



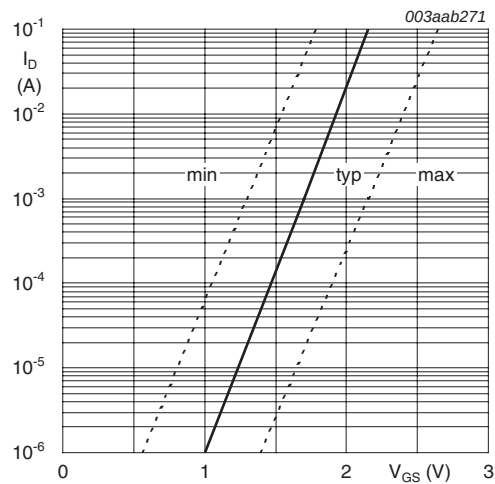
$V_{DS} > I_D \times R_{DSon}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical valuesvalues



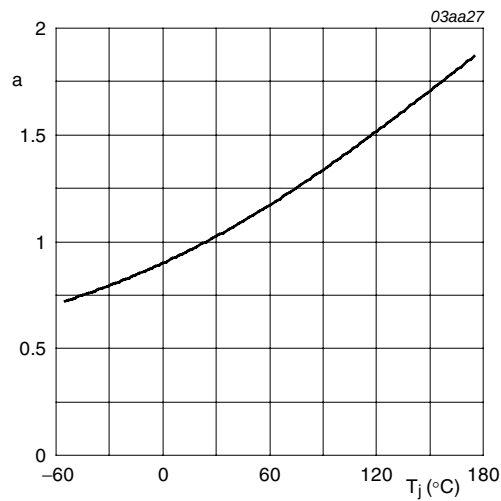
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

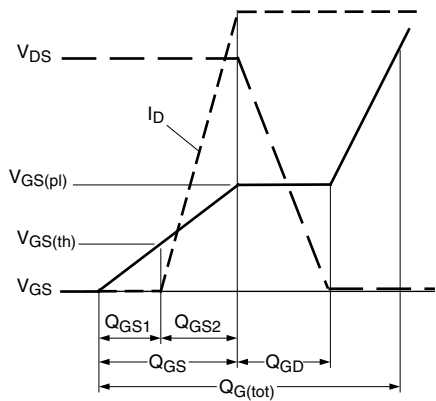
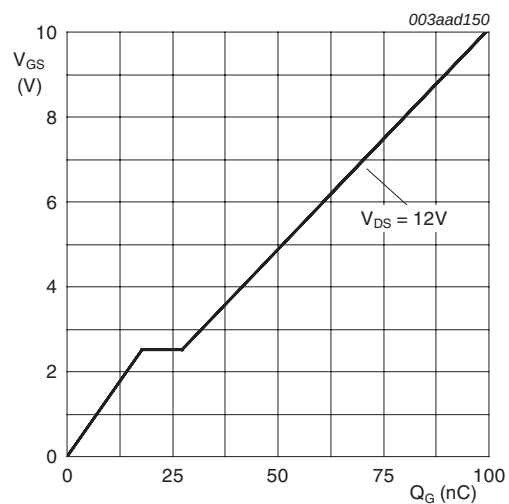
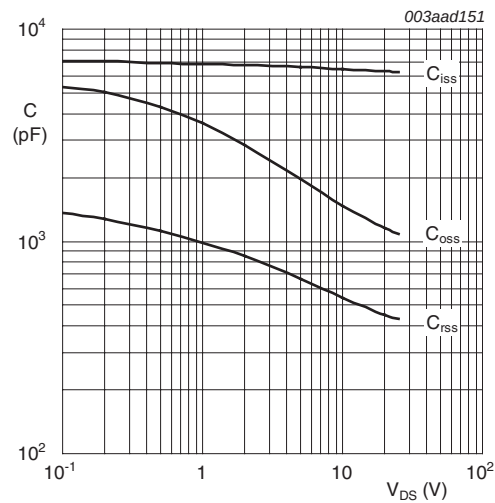


Fig 13. Gate charge waveform definitions



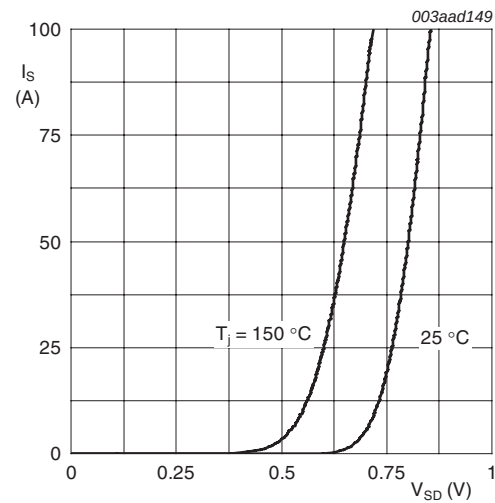
$I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



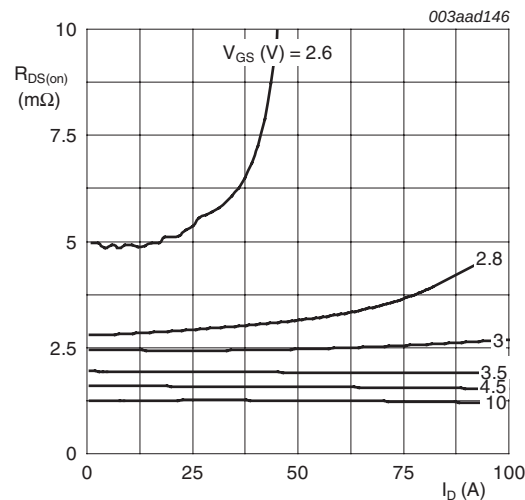
$V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 16. Source current as a function of source-drain voltage; typical values



$T_j = 25^\circ C$

Fig 17. Drain-source on-state resistance as a function of drain current; typical values

7. Package outline

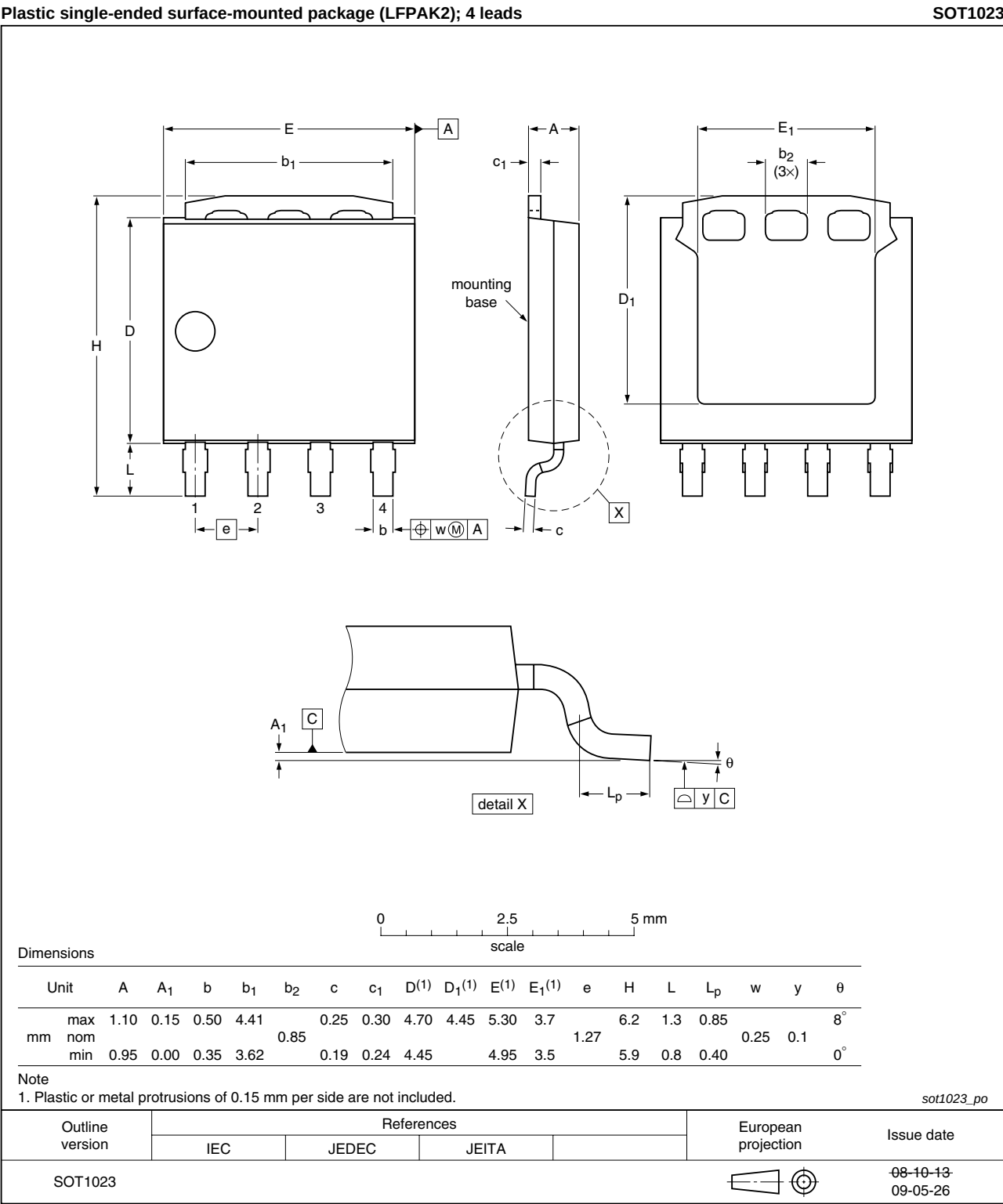


Fig 18. Package outline SOT1023 (LPAK2)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH1330AL_1	20091014	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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