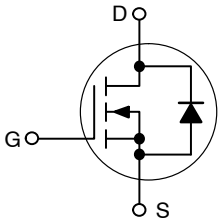
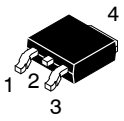
MOSFET - Power, N-Channel, Logic Level

100 V, 23 A, 56 mΩ

NTD6415ANL, NVD6415ANL

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	56 mΩ @ 4.5 V	23 A
	52 mΩ @ 10 V	





DPAK
CASE 369AA
STYLE 2

Features

- Low $R_{DS(on)}$d
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	100	V
Gate-to-Source Voltage – Continuous			V_{GS}	±20	V
Continuous Drain Current	Steady State	T_C = 25 °C	I_D	23	A
		T_C = 100 °C		16	
Power Dissipation	Steady State	T_C = 25 °C	P_D	83	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	80	A
Operating and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	23	A
Single Pulse Drain-to-Source Avalanche Energy (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, $I_{L(pk)}$ = 23 A, L = 0.3 mH, R_G = 25 Ω)			E_{AS}	79	mJ
Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds			T_L	260	°C

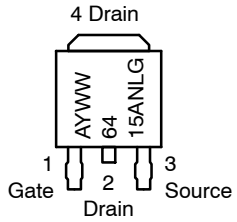
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	1.8	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	49	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location*
6415ANL = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 3.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = 250 μA, T_J = −40 °C		100 92			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				115		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25 °C			1.0	μA
			T_J = 125 °C			100	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		2.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.8		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 10 A			44	56	mΩ
		V_{GS} = 10 V, I_D = 10 A			43	52	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 10 A			24		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1024		pF
Output Capacitance	C_{OSS}				156		
Reverse Transfer Capacitance	C_{RSS}				70		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 80 V, I_D = 23 A			20		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.1		
Gate-to-Source Charge	Q_{GS}				3.1		
Gate-to-Drain Charge	Q_{GD}				14		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 80 V, I_D = 23 A			35		nC
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DD} = 80 V, I_D = 23 A, R_G = 6.1 Ω			11		ns
Rise Time	t_r				91		
Turn-Off Delay Time	$t_{d(off)}$				40		
Fall Time	t_f				71		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 23 A	T_J = 25 °C		0.87	1.2	V
			T_J = 125 °C		0.74		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 23 A			64		ns
Charge Time	T_a				40		
Discharge Time	T_b				24		
Reverse Recovery Charge	Q_{RR}				152		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

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ORDERING INFORMATION

Device	Package	Shipping†
NTD6415ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD6415ANLT4G-VF01		

DISCONTINUED (Note 4)

NVD6415ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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TYPICAL CHARACTERISTICS

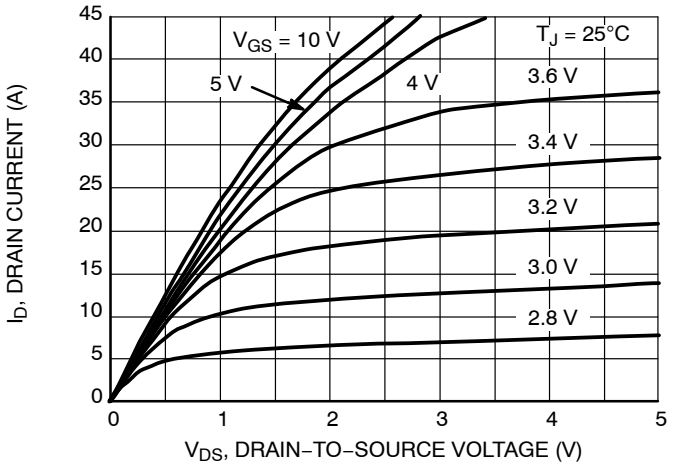


Figure 1. On−Region Characteristics

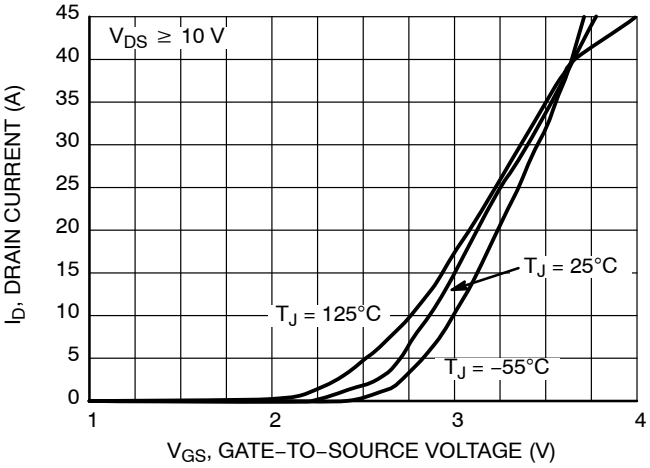


Figure 2. Transfer Characteristics

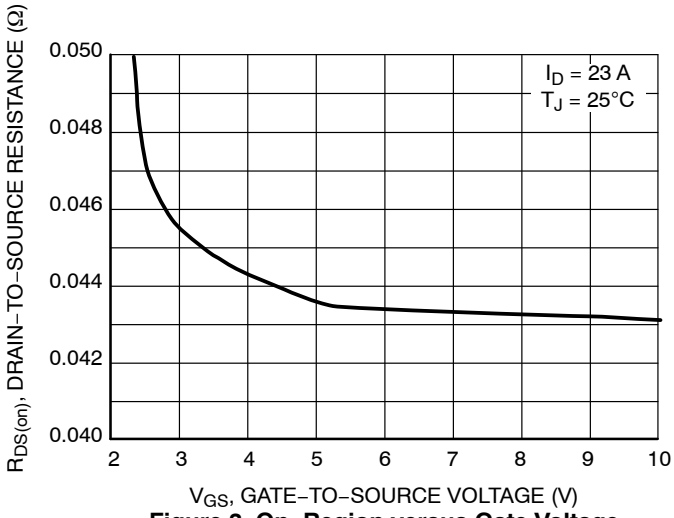


Figure 3. On−Region versus Gate Voltage

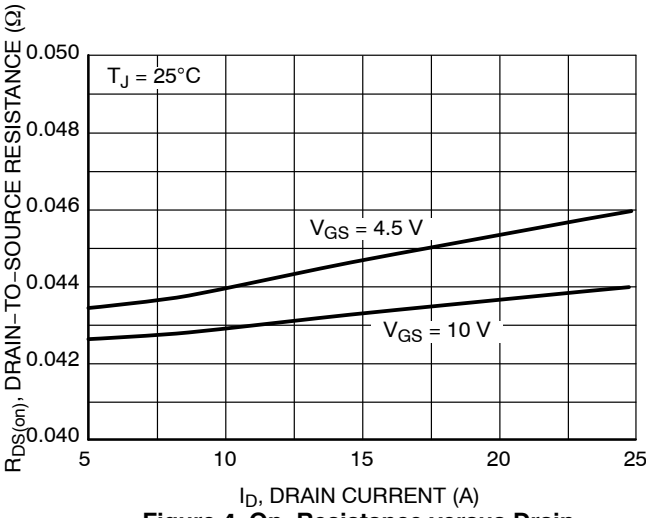


Figure 4. On−Resistance versus Drain Current and Gate Voltage

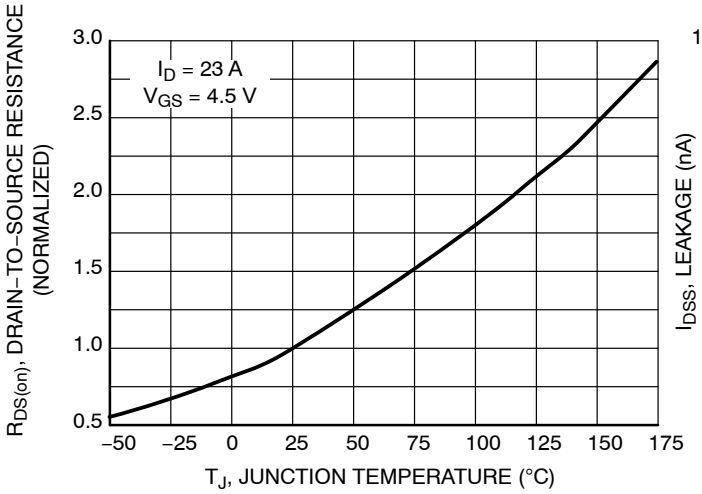


Figure 5. On−Resistance Variation with Temperature

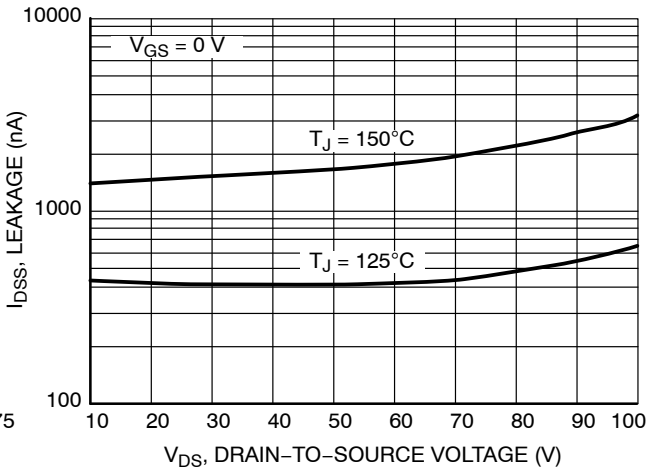


Figure 6. Drain−to−Source Leakage Current versus Voltage

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TYPICAL CHARACTERISTICS

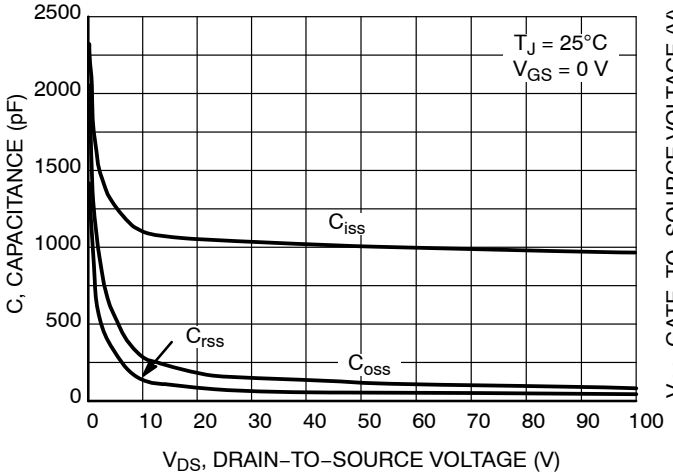


Figure 7. Capacitance Variation

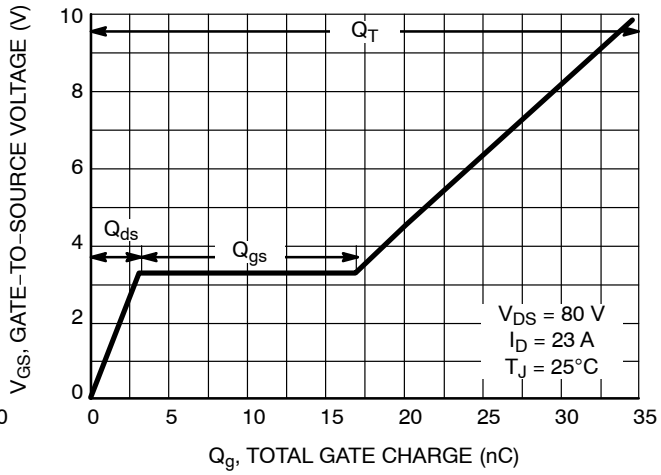


Figure 8. Gate−to−Source Voltage and Drain−to−Source Voltage versus Total Charge

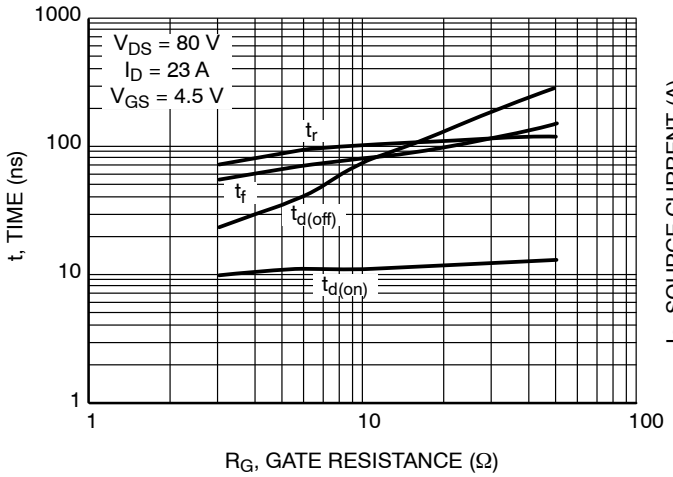


Figure 9. Resistive Switching Time Variation versus Gate Resistance

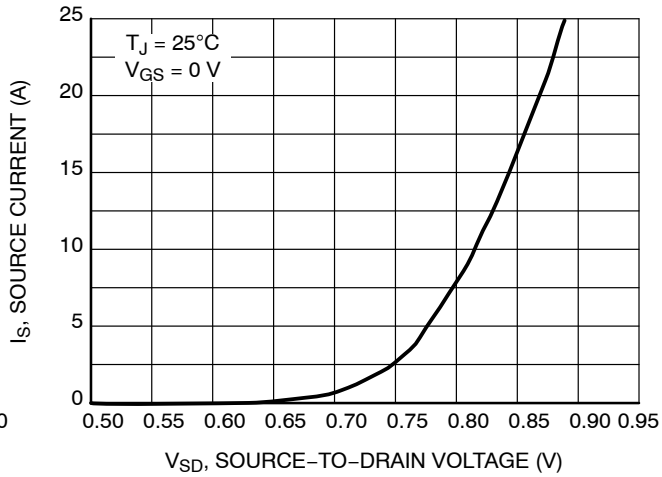


Figure 10. Diode Forward Voltage versus Current

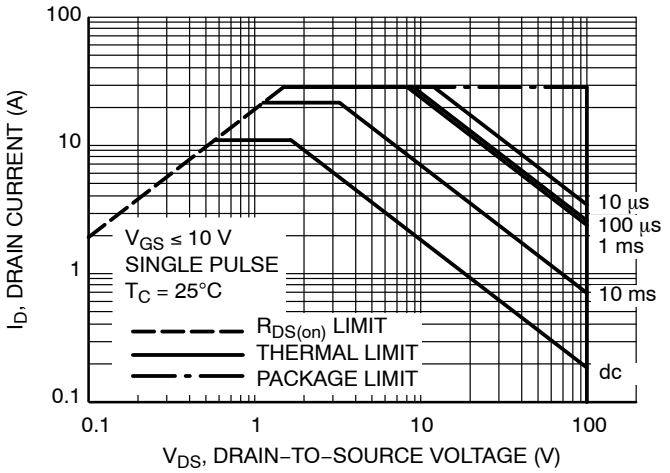


Figure 11. Maximum Rated Forward Biased Safe Operating Area

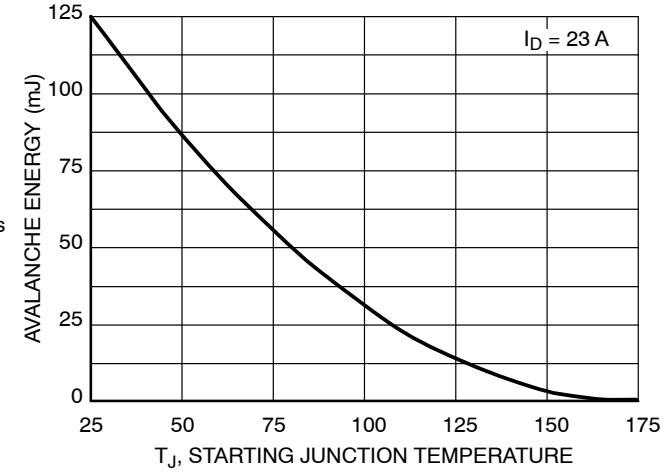


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL CHARACTERISTICS

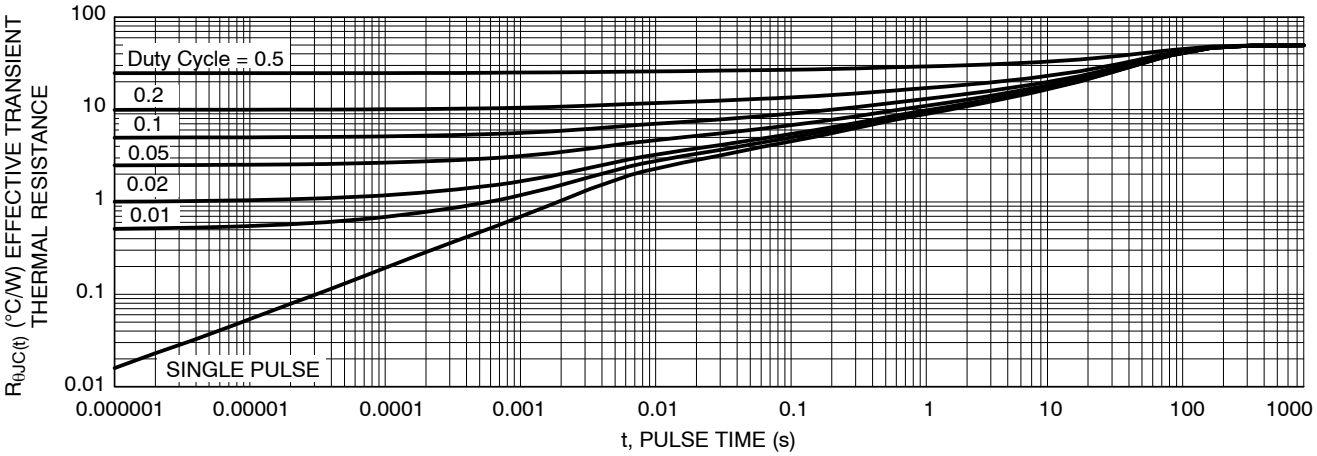
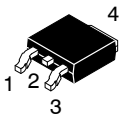


Figure 13. Thermal Response

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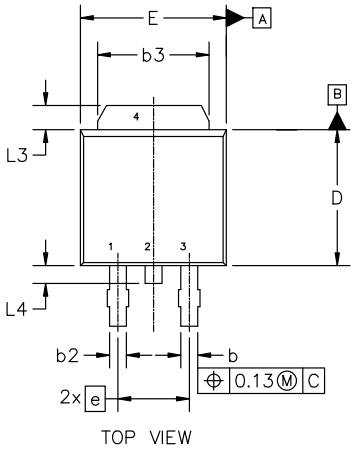
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DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369AA
ISSUE C

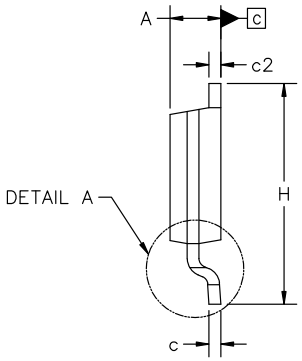
DATE 14 MAY 2026

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.76	0.95	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−

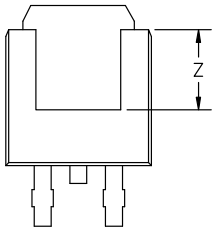
NOTES
1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H



TOP VIEW

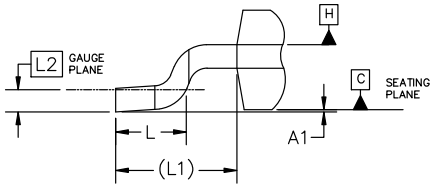


SIDE VIEW

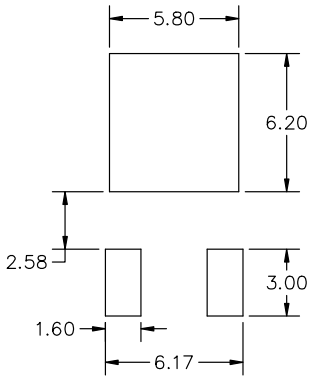


TOP VIEW

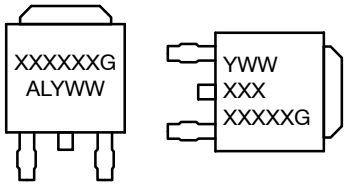
RECOMMENDED
MOUNTING FOOTPRINT



DETAIL A
ROTATED 90° CW



GENERIC
MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 1**

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