

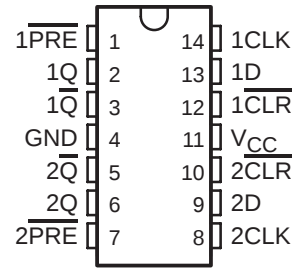
# 74AC11074

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (N)

D, N, OR PW PACKAGE  
(TOP VIEW)



### description

This device contains two independent positive-edge-triggered D-type flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) input sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input that meets the setup-time requirements are transferred to the outputs on the low-to-high transition of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The 74AC11074 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

| INPUTS           |                  |     |   | OUTPUT         |                  |
|------------------|------------------|-----|---|----------------|------------------|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q              | $\overline{Q}$   |
| L                | H                | X   | X | H              | L                |
| H                | L                | X   | X | L              | H                |
| L                | L                | X   | X | H <sup>†</sup> | H <sup>†</sup>   |
| H                | H                | ↑   | H | H              | L                |
| H                | H                | ↑   | L | L              | H                |
| H                | H                | L   | X | Q <sub>0</sub> | $\overline{Q}_0$ |

<sup>†</sup> This configuration is nonstable; that is, it does not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.



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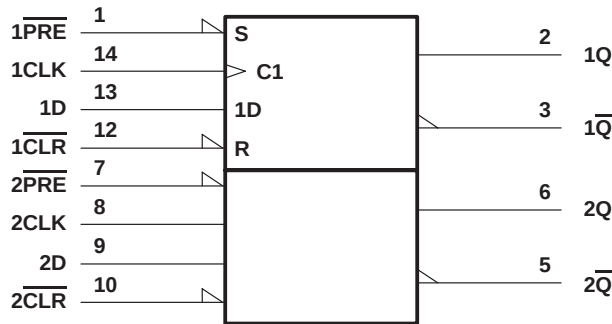
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Table with 2 columns: Parameter and Rating. Parameters include Supply voltage range, Input voltage range, Output voltage range, Input clamp current, Output clamp current, Continuous output current, Continuous current through VCC or GND, Maximum power dissipation at TA = 55°C, and Storage temperature range.

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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**recommended operating conditions**

|                     |                                    | MIN                     | NOM  | MAX      | UNIT |
|---------------------|------------------------------------|-------------------------|------|----------|------|
| $V_{CC}$            | Supply voltage                     | 3                       | 5    | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 3\text{ V}$   | 2.1  |          | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ | 3.15 |          |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ | 3.85 |          |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 3\text{ V}$   |      | 0.9      | V    |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | 1.35     |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | 1.65     |      |
| $V_I$               | Input voltage                      | 0                       |      | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                       |      | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 3\text{ V}$   |      | -4       | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | -24      |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | -24      |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 3\text{ V}$   |      | 12       | mA   |
|                     |                                    | $V_{CC} = 4.5\text{ V}$ |      | 24       |      |
|                     |                                    | $V_{CC} = 5.5\text{ V}$ |      | 24       |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0                       |      | 10       | ns/V |
| $T_A$               | Operating free-air temperature     | -40                     |      | 85       | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS                   | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |           | MIN     | MAX | UNIT          |
|-----------|-----------------------------------|----------|--------------------------|-----|-----------|---------|-----|---------------|
|           |                                   |          | MIN                      | TYP | MAX       |         |     |               |
| $V_{OH}$  | $I_{OH} = -50\text{ }\mu\text{A}$ | 3 V      | 2.9                      |     |           | 2.9     |     | V             |
|           |                                   | 4.5 V    | 4.4                      |     |           | 4.4     |     |               |
|           |                                   | 5.5 V    | 5.4                      |     |           | 5.4     |     |               |
|           | $I_{OH} = -4\text{ mA}$           | 3 V      | 2.58                     |     |           | 2.48    |     |               |
|           |                                   | 4.5 V    | 3.94                     |     |           | 3.8     |     |               |
|           |                                   | 5.5 V    | 4.94                     |     |           | 4.8     |     |               |
|           |                                   | 5.5 V    |                          |     |           | 3.85    |     |               |
| $V_{OL}$  | $I_{OL} = 50\text{ }\mu\text{A}$  | 3 V      |                          |     | 0.1       | 0.1     |     | V             |
|           |                                   | 4.5 V    |                          |     | 0.1       | 0.1     |     |               |
|           |                                   | 5.5 V    |                          |     | 0.1       | 0.1     |     |               |
|           | $I_{OL} = 12\text{ mA}$           | 3 V      |                          |     | 0.36      | 0.44    |     |               |
|           |                                   | 4.5 V    |                          |     | 0.36      | 0.44    |     |               |
|           | $I_{OL} = 24\text{ mA}$           | 5.5 V    |                          |     | 0.36      | 0.44    |     |               |
|           |                                   | 5.5 V    |                          |     |           | 1.65    |     |               |
| $I_I$     | $V_I = V_{CC}$ or GND             | 5.5 V    |                          |     | $\pm 0.1$ | $\pm 1$ |     | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$  | 5.5 V    |                          |     | 4         | 40      |     | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC}$ or GND             | 5 V      |                          | 3.5 |           |         |     | pF            |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see Figure 1)

|                    |                                  |                                                             | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|--------------------|----------------------------------|-------------------------------------------------------------|--------------------------|-----|-----|-----|------|
|                    |                                  |                                                             | MIN                      | MAX |     |     |      |
| $f_{\text{clock}}$ | Clock frequency                  |                                                             | 0                        | 100 | 0   | 100 | MHz  |
| $t_w$              | Pulse duration                   | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 4                        |     | 4   |     | ns   |
|                    |                                  | CLK low or high                                             | 5                        |     | 5   |     |      |
| $t_{\text{su}}$    | Setup time before CLK $\uparrow$ | Data high or low                                            | 5                        |     | 5   |     | ns   |
|                    |                                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 1                        |     | 1   |     |      |
| $t_h$              | Hold time after CLK $\uparrow$   |                                                             | 0                        |     | 0   |     | ns   |

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (see Figure 1)

|                    |                                  |                                                             | $T_A = 25^\circ\text{C}$ |     | MIN | MAX | UNIT |
|--------------------|----------------------------------|-------------------------------------------------------------|--------------------------|-----|-----|-----|------|
|                    |                                  |                                                             | MIN                      | MAX |     |     |      |
| $f_{\text{clock}}$ | Clock frequency                  |                                                             | 0                        | 125 | 0   | 125 | MHz  |
| $t_w$              | Pulse duration                   | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low      | 4                        |     | 4   |     | ns   |
|                    |                                  | CLK low or CLK high                                         | 4                        |     | 4   |     |      |
| $t_{\text{su}}$    | Setup time before CLK $\uparrow$ | Data high or low                                            | 3.5                      |     | 3.5 |     | ns   |
|                    |                                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | 1                        |     | 1   |     |      |
| $t_h$              | Hold time after CLK $\uparrow$   |                                                             | 0                        |     | 0   |     | ns   |

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)                                       | TO (OUTPUT)                | $T_A = 25^\circ\text{C}$ |     |      | MIN | MAX  | UNIT |
|------------------|----------------------------------------------------|----------------------------|--------------------------|-----|------|-----|------|------|
|                  |                                                    |                            | MIN                      | TYP | MAX  |     |      |      |
| $f_{\text{max}}$ |                                                    |                            | 100                      | 125 |      | 100 |      | MHz  |
| $t_{\text{PLH}}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 1.5                      | 5.8 | 9.3  | 1.5 | 10   | ns   |
| $t_{\text{PHL}}$ |                                                    |                            | 1.5                      | 6.5 | 11.4 | 1.5 | 12.2 |      |
| $t_{\text{PLH}}$ | CLK                                                | Q or $\overline{\text{Q}}$ | 1.5                      | 7.7 | 10.5 | 1.5 | 11.3 | ns   |
| $t_{\text{PHL}}$ |                                                    |                            | 1.5                      | 7.3 | 9.7  | 1.5 | 10.6 |      |

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)                                       | TO (OUTPUT)                | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|------------------|----------------------------------------------------|----------------------------|--------------------------|-----|-----|-----|-----|------|
|                  |                                                    |                            | MIN                      | TYP | MAX |     |     |      |
| $f_{\text{max}}$ |                                                    |                            | 125                      | 150 |     | 125 |     | MHz  |
| $t_{\text{PLH}}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 1.5                      | 4.2 | 6.6 | 1.5 | 7.1 | ns   |
| $t_{\text{PHL}}$ |                                                    |                            | 1.5                      | 4.7 | 8.2 | 1.5 | 9   |      |
| $t_{\text{PLH}}$ | CLK                                                | Q or $\overline{\text{Q}}$ | 1.5                      | 5.4 | 7.5 | 1.5 | 8.2 | ns   |
| $t_{\text{PHL}}$ |                                                    |                            | 1.5                      | 5   | 6.9 | 1.5 | 7.5 |      |

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER       |                               | TEST CONDITIONS         |                     | TYP | UNIT |
|-----------------|-------------------------------|-------------------------|---------------------|-----|------|
| $C_{\text{pd}}$ | Power dissipation capacitance | $C_L = 50 \text{ pF}$ , | $f = 1 \text{ MHz}$ | 30  | pF   |

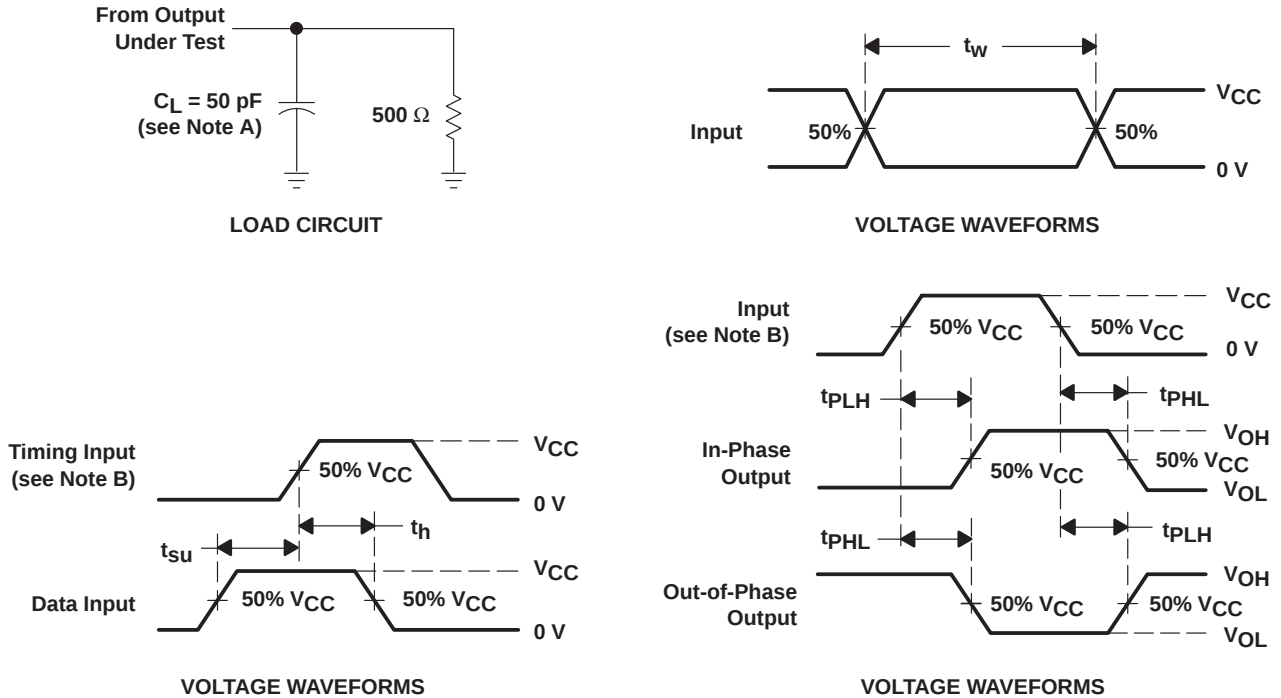


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**WITH CLEAR AND PRESET**

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**PARAMETER MEASUREMENT INFORMATION**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74AC11074D       | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AC11074                 | <a href="#">Samples</a> |
| 74AC11074DE4     | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AC11074                 | <a href="#">Samples</a> |
| 74AC11074DR      | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AC11074                 | <a href="#">Samples</a> |
| 74AC11074DRG4    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AC11074                 | <a href="#">Samples</a> |
| 74AC11074N       | ACTIVE        | PDIP         | N                  | 14   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | 74AC11074N              | <a href="#">Samples</a> |
| 74AC11074PWR     | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AE074                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**

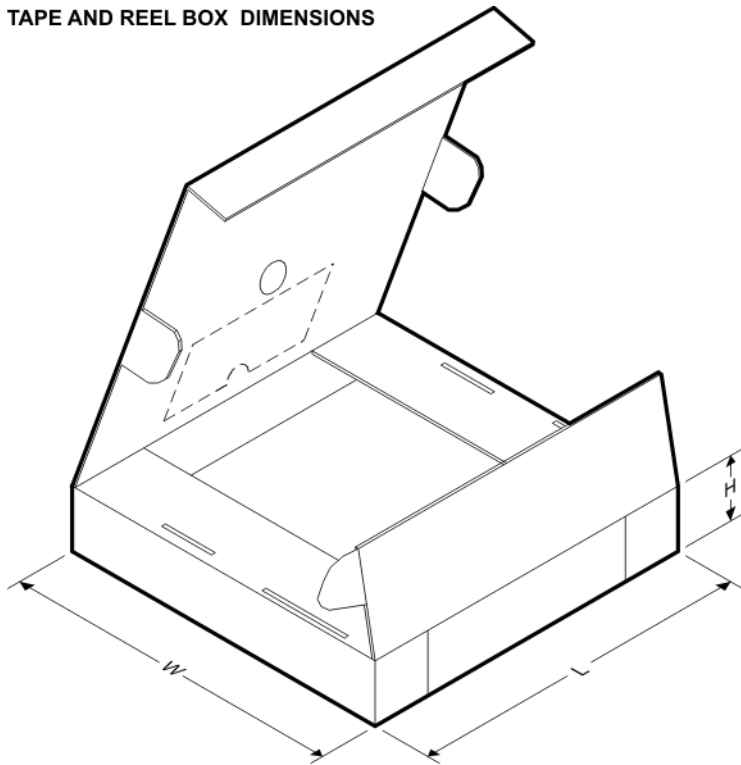

|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74AC11074DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| 74AC11074PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

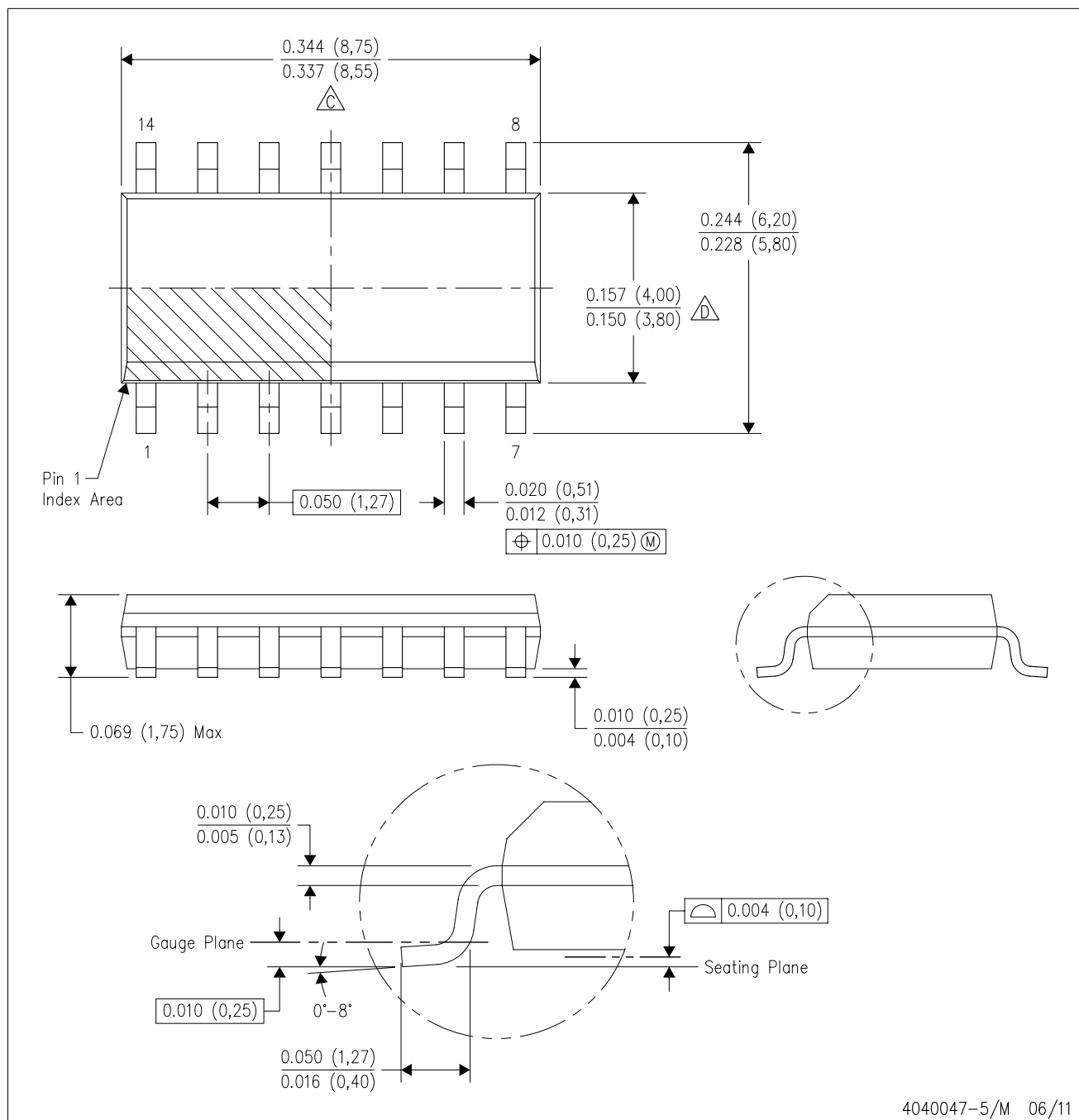


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74AC11074DR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| 74AC11074PWR | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

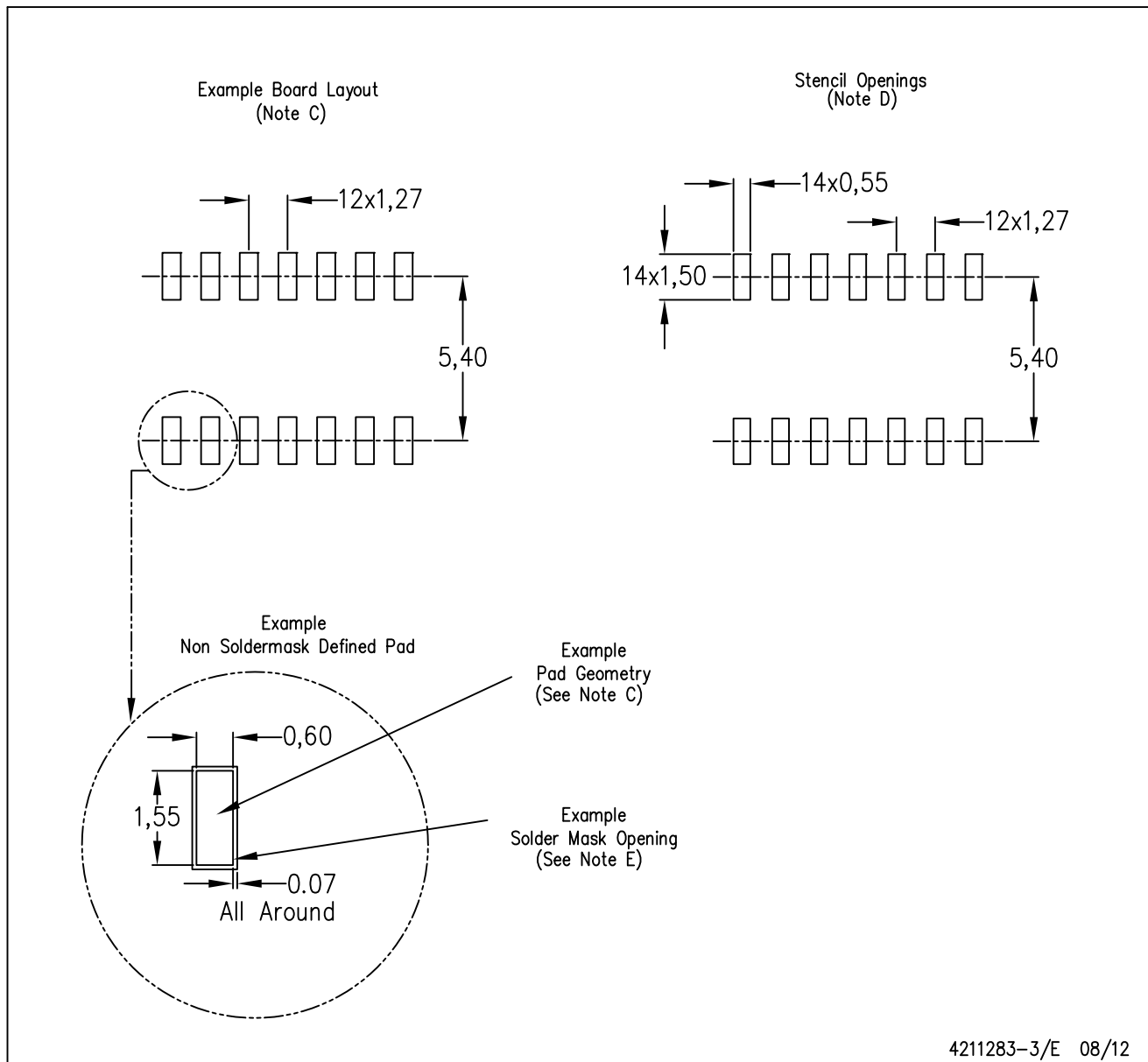


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

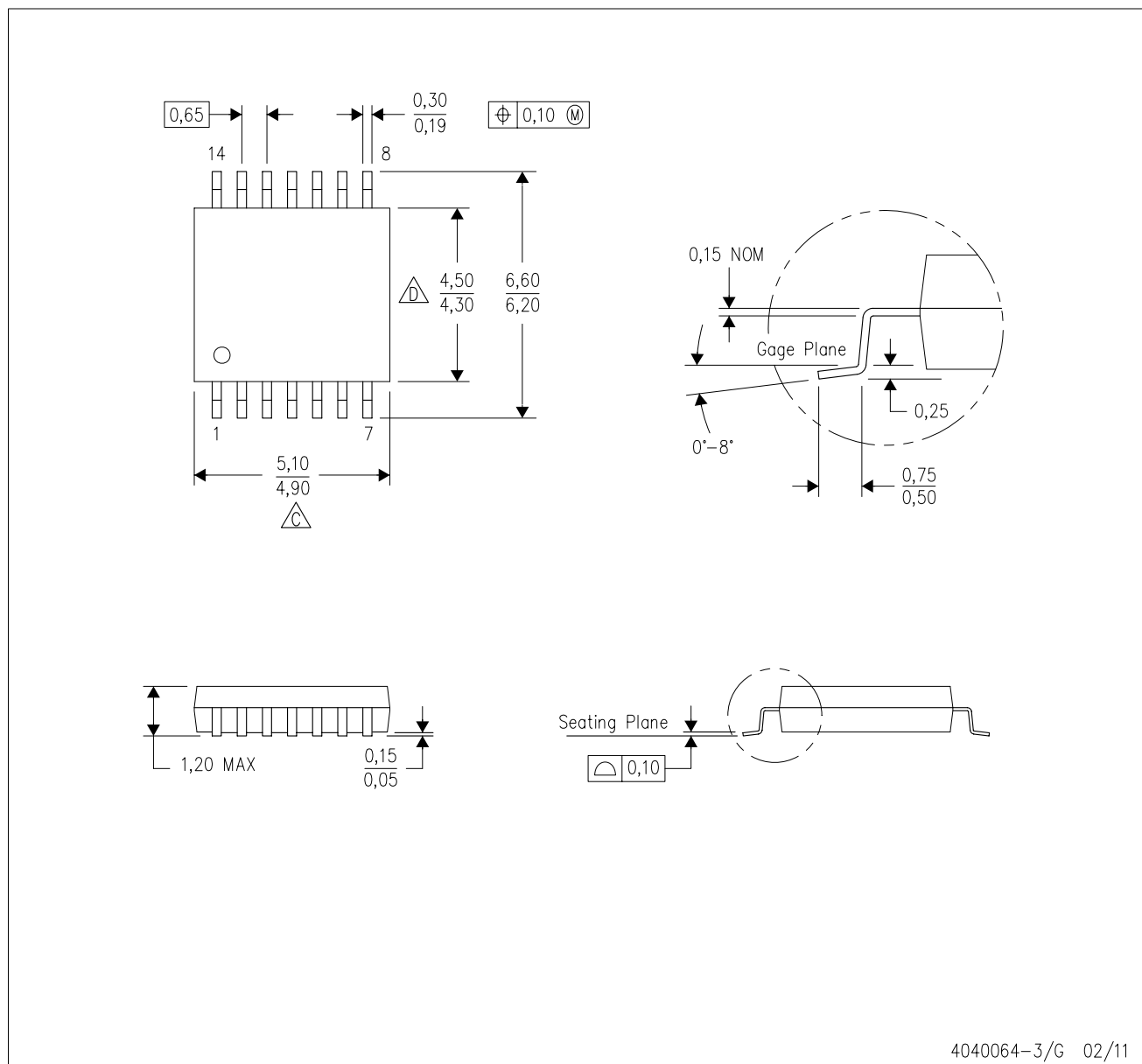
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

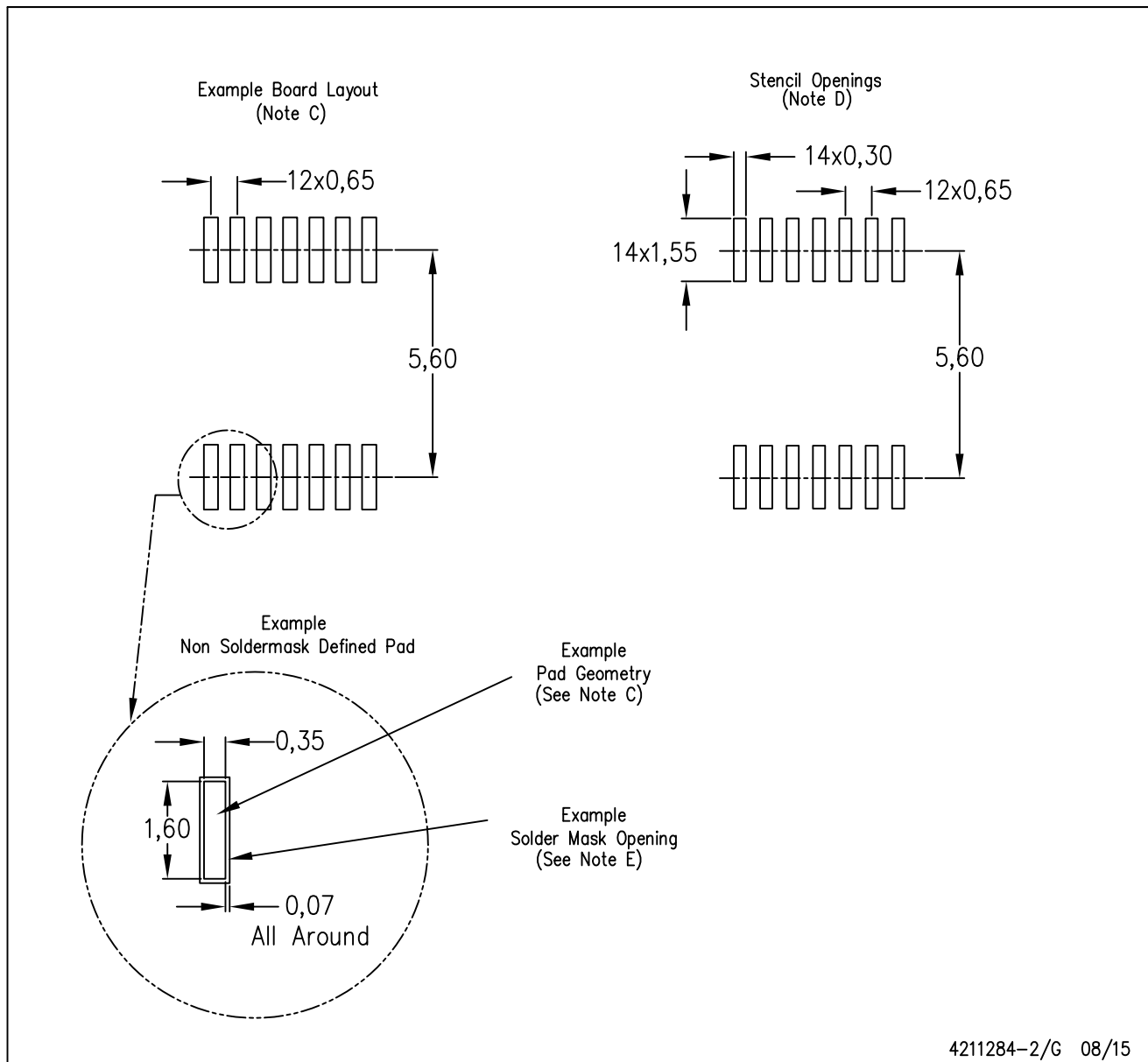
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

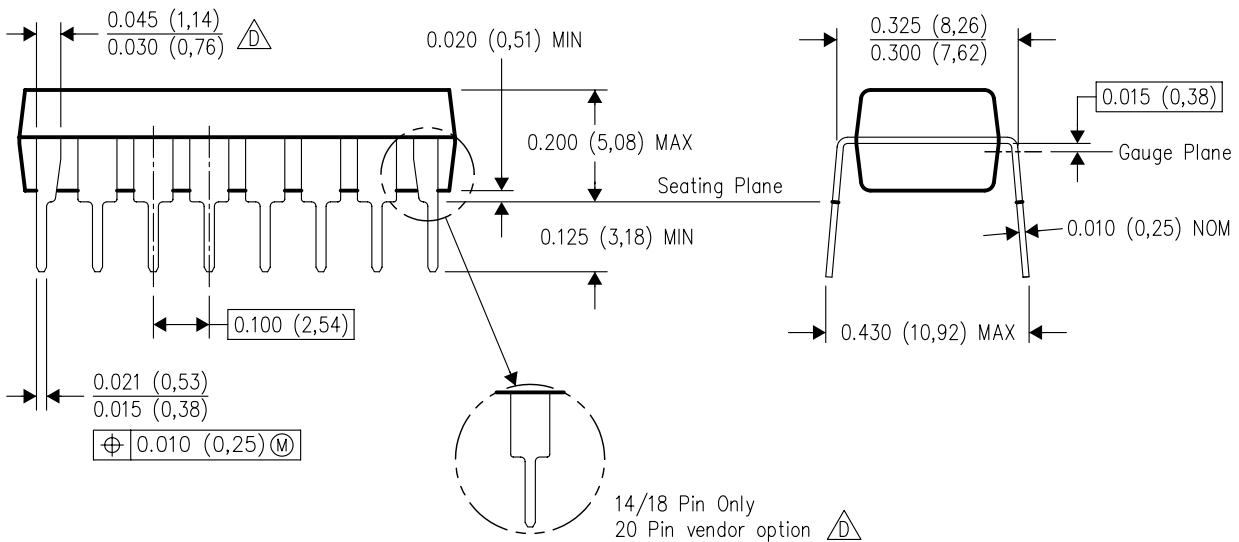
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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