ZL70103 Medical Implantable RF Transceiver

MICS-Band RF Telemetry

Features

- 402–405 MHz (10 MICS-band channels) and 433–434 MHz (2 ISM-band channels)
- Raw Data Rates: 800/400/200/40/18.18kbit/s
- High-Performance MAC with Automatic Error Handling and Flow Control
- Very Few External Components (crystal, decoupling, and antenna matching)
- Ultra-Low-Power Operation
  - Average TX/RX Current (typical 5mA)
  - Sleep/Sniff State Average Current (typical 290nA at 1-second sniff interval)
- Standards Compatible (MICS[1], ETSI, FCC, IEC)
- RoHS Compliant

Applications

- Implantable Medical Devices
  - Cardiac Rhythm Management
  - Neurostimulators
  - Drug Delivery, Sensors, and Diagnostics

Description

The ZL70103 is a high-performance, half-duplex, RF communications link for medical implantable applications.

The system is very flexible and supports two low-power wake-up options. Extremely low power is achievable using the 2.45-GHz ISM-band wake-up receiver option. The high level of integration includes a Media Access Controller, providing complete control of the device along with coding and decoding of RF messages. A standard SPI bus interface provides for easy access by the application.

Ordering Information

ZL70103LDG1 48-pin QFN (for base station applications only)

ZL70103UEJ2 49-pin CSP, SAC405 (for implant applications only)

ZL70103UBJ Bare die (for implant applications only)

Please see chapter "2 – Ordering and Package Overview" on page 2-1 for details.

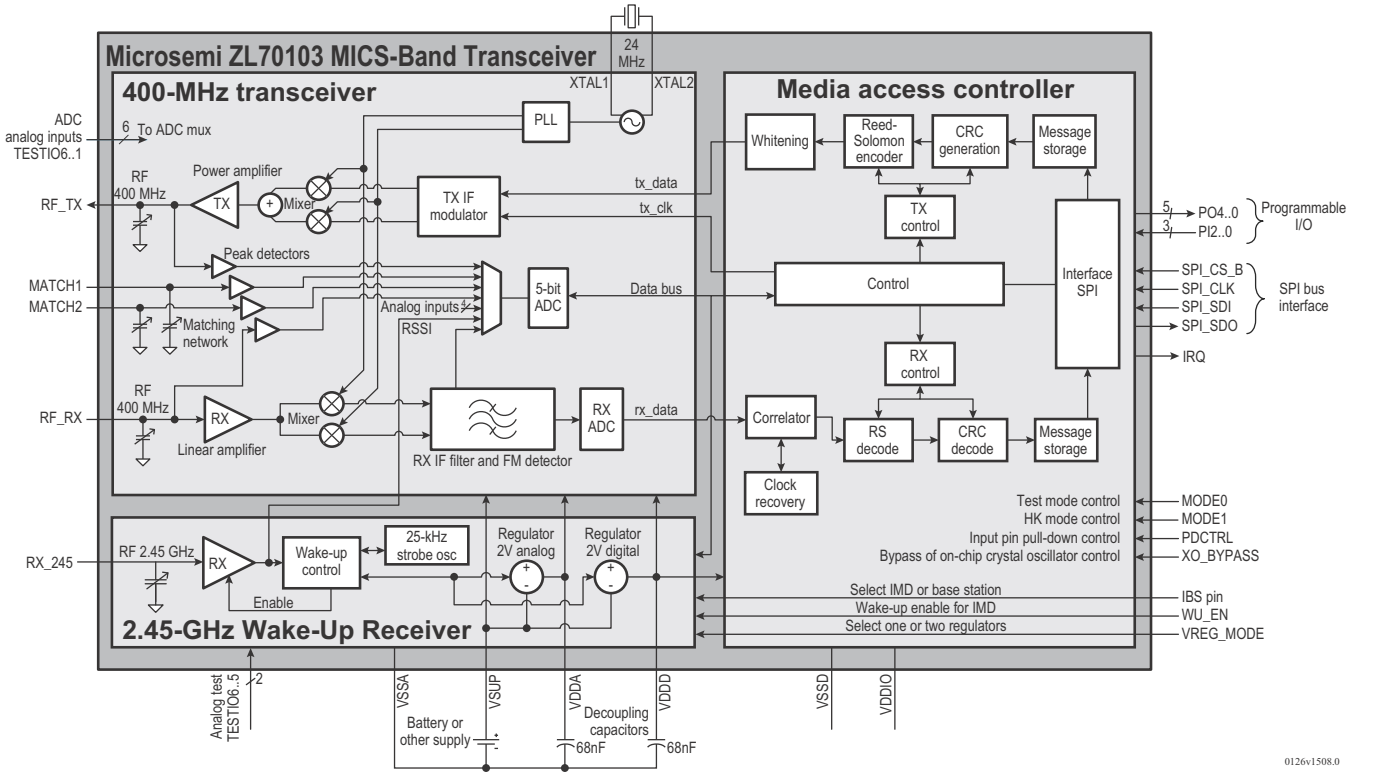

Figure 1 • **ZL70103 Block Diagram**

1 *The MICS band is a subset of the designated MedRadio frequency band.*

Schematic Interconnect Diagram of the ZL70103

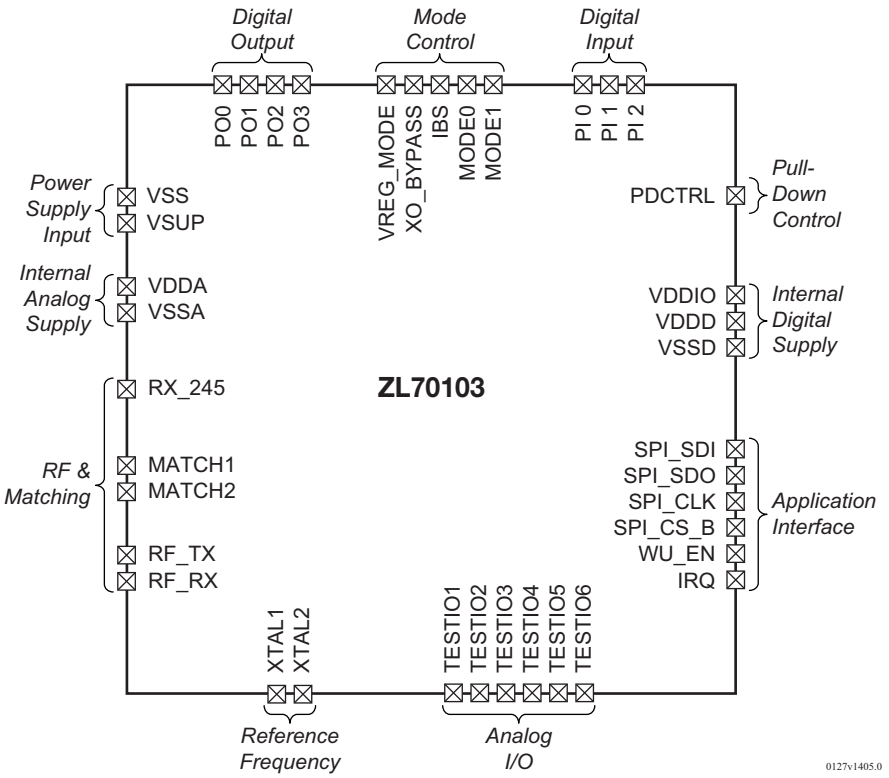

Figure 2 • **ZL70103 Schematic Interconnect Diagram**

The schematic interconnect diagram above shows all of the important connections that are available. Please note that the diagram does not show all connections (for example, ground connections) and that the available connections differ for each package option. Please see Table 8-1 on page 8-1 and chapter "9 – Mechanical Reference" on page 9-1 for details.

Table 1 • Schematic Overview of the ZL70103 Interconnects

Symbol	Description
Internal Analog Supply	
VSSA	Analog ground
VDDA	Analog on-chip voltage regulator output (internal analog 2-V domain); connects to an external 68- to 100-nF capacitor for voltage regulator stability
Power Supply Input	
VSS	Common chip ground
VSUP	Power supply input
RF and Matching	
RX_245	2.45-GHz wake-up receiver input
MATCH1 MATCH2	Antenna/matching network tuning capacitors
RF_TX	400-MHz RF transmitter output to matching network
RF_RX	400-MHz RF receiver input from matching network
Reference Frequency	
XTAL1 XTAL2	Connection to the reference frequency crystal. The chip can also use an external oscillator connected to XTAL1 (controlled by XO_BYPASS).
Analog I/O	
TESTIO1 to TESTIO6	Analog input/output. Mainly used during electrical testing in chip production.
Application Interface	
IRQ	Master interrupt request
WU_EN	Wake-up enable signal used to initiate the 2.45-GHz wake-up receiver to perform a sniff or for a direct wake-up of the device
SPI_CS_B	SPI chip select (active low)
SPI_CLK	SPI serial clock
SPI_SDO	SPI serial data out
SPI_SDI	SPI serial data in
Internal Digital Supply	
VDDIO	Digital I/O supply input to internal level shifters
VDDD	Digital on-chip voltage regulator output (internal digital 2-V domain); connects to an external 68- to 100-nF capacitor for voltage regulator stability
VSSD	Digital ground
Digital Input Mode	
PDCTRL	Digital input pull-down control for the following pins: MODE0, MODE1, IBS, XO_BYPASS, and PI0 to PI2. If PDCTRL = VDDIO, then these inputs are pulled low with a 90-kΩ internal resistor and do not need to be grounded externally.
Digital Input	
PI0 to PI2	Programmable digital inputs (three inputs)

Table 1 • Schematic Overview of the ZL70103 Interconnects (continued)

Symbol	Description
Mode Control	
MODE0	The MODE0 input selects normal operation mode or test mode (for Microsemi use only). Should be tied low for normal operation.
MODE1	Controls whether HK messages can write to registers. MODE1 = 0 disables HK writes (recommended).
IBS	Implant/base mode selection
XO_BYPASS	When high, the internal oscillator is bypassed and an external oscillator clock is fed to the XTAL1 pin
VREG_MODE	Voltage regulator selection of *either* VDDA *or* VDDA and VDDD (VREG_MODE = 0 for VDDA and VDDD, recommended). Note that this pin is not available on the QFN package and is hardwired to VSS internally.
Digital Output	
PO0 to PO3	Programmable digital outputs (four outputs).

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1 – Product Description

Introduction

The ZL70103 is an ultra-low-power RF transceiver for implantable medical applications. It operates in the Medical Implantable Communication Service[1] (MICS) band at 402–405 MHz and provides a complete radio modem enabling communication with a medical device in the body. The *wireless* RF telemetry link replaces the traditional inductively coupled wand and enables benefits including:

- Higher data rates
- Placement of the programmer further away from the body (outside the sterile area) during surgery
- Remote monitoring outside the medical clinic
- Body-worn applications allowing patient control and monitoring
- Link to other nonimplanted medical devices and sensors for more advanced applications

The ZL70103 RF transceiver provides a complete MICS-band solution and can be used in both ends of the link, that is, both in the Implantable Medical Device (IMD) and in the external device (base station, programmer, remote monitor, etc.).

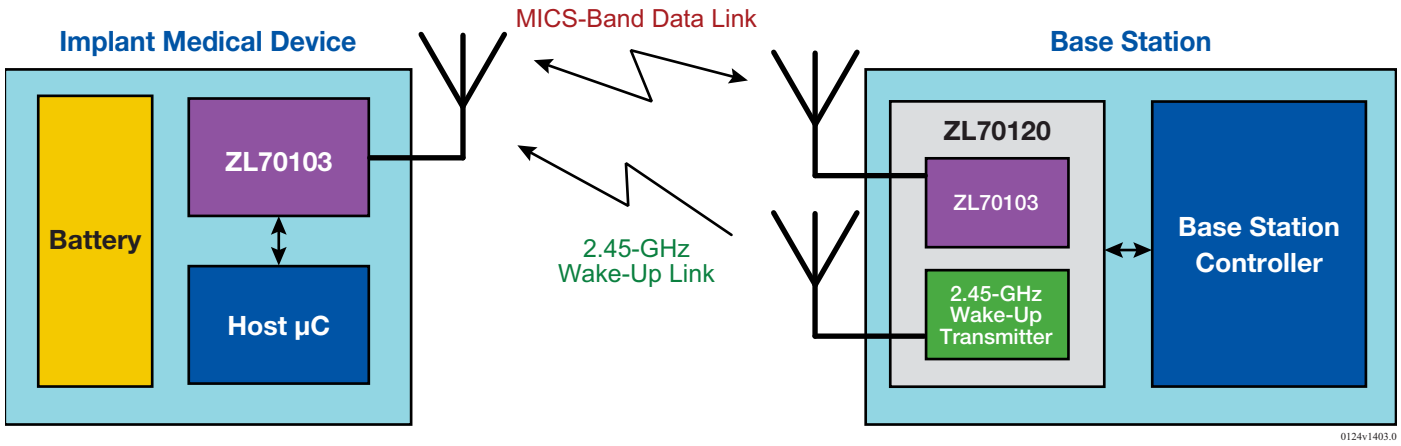


Figure 1-1 • **Application Example**

Dedicated for the Medical Implant Market

The ZL70103 has been developed specifically for the medical implant market and is optimized for the requirements driven by these types of products. Robustness, quality, and ultralow power have been cornerstones in the ZL70103 system definition.

The ZL70103 RF transceiver is designed, from the bottom up, to be a true ultra-low-power device. Implantable medical devices normally have very limited battery resources, and longevity is one of the core values of the application. The RF telemetry link is expected to use a fraction of the battery resources from the target treatment of the IMD.

Low current consumption during transmission is essential, but even more important is that the radio can be kept in a sleep state for as much time as possible while maintaining responsiveness. Every block of the ZL70103 has therefore been carefully designed with ultralow power consumption in mind, and advanced power management is implemented on all levels.

1 The MICS band is a dedicated band for nonaudio, implantable applications. One side of the link has to be implanted.

Innovative Wake-Up System

To conserve battery power it is essential to provide an ultra-low-power wake-up system. The ZL70103 is very versatile and supports three wake-up methods:

- 2.45-GHz wake-up receiver: Fully autonomous, ultra-low-power wake-up receiver, utilizing the higher transmitted power allowed for by the 2.45-GHz ISM band. Modulation and protocol are optimized for ultralow power and robustness.
- In-band (MICS-band) wake-up: Advanced support for in-band wake-up in the MICS band enables a simple hardware implementation (some support from the host required).
- Wake-up by host: Wake-up by the host controller, in combination with support for the low duty-cycle mode, enables scheduled communication schemes or ad hoc wake-up initiated by the implant.

High-Performance MAC and Autonomous Operation

The ZL70103 has a packet-level interface that is simple to use and supported by a high-performance MAC with automatic error correction and flow control. The host controller can concentrate on the treatment and delegate the communication to the ZL70103 transceiver. The radio can be controlled remotely through the link and could in principle operate with no host controller using the on-chip general purpose I/Os to control a simple application.

Self-Contained

The ZL70103 transceiver is highly integrated and self-contained. Very few external components are required to make a complete radio system:

- Antenna with suitable matching network
- SAW filter to suppress unwanted blockers
- Crystal for the reference frequency (on-chip oscillator)
- Decoupling capacitors for power supply (on-chip regulators)

Typical Applications

Three typical applications are presented below. Chapter "10 – Typical Application Examples" on page 10-1 provides schematics and more details. These three typical applications are intended as a starting point for the target application.

Ultra-Low-Power Implant Devices

This application area has been dominated by cardiac rhythm management products like pacemakers and Implantable Cardioverter Defibrillators (ICD) where low power and device longevity were very important characteristics of the device market long before RF telemetry was introduced. This means that the industry is willing to take extra efforts to save power even if this results in a moderate increase in complexity. There are other new applications that also fall into this category.

To address this need, the ZL70103 is equipped with an ultra-low-power 2.45-GHz wake-up system that provides by far the lowest power consumption. The 2.45-GHz wake-up system is also autonomous and fully integrated when the ZL70103 is used in an implant.

Low-Power Implant Devices

Many neurostimulators, drug delivery systems, sensors, and diagnostic applications are operated in a mode allowing higher power consumption since the core function itself consumes more power, requiring use of larger or rechargeable batteries. This allows alternative wake-up solutions to be used, like the in-band wake-up in the MICS band, that simplify the hardware design (the matching network and antenna use only the 400-MHz band).

External Devices

This is the other side of the MICS-band link with a higher allowed power budget in comparison with the implanted device. The external device, acting as a base station, also has to fulfill other requirements of the MICS standard such as Clear Channel Assessment (CCA), and it is required to transmit the 2.45-GHz wake-up packet if the 2.45-GHz wake-up option is used. Applications include:

- Programming base stations
- Home/remote monitoring devices
- Handheld, mobile, and belt-worn applications

2 – Ordering and Package Overview

The ZL70103 RF transceiver is available in several package options. Some of these packages are intended for implant devices and some for external devices (base stations). Depending on the application there are some differences in the electrical specifications, please refer to chapter "7 – Electrical Reference" on page 7-1 for details.

Table 2-1 • **Ordering and Package Overview**

Ordering Code	Temp Range (°C)	Package	Delivery Form	Pb Free	Implant Grade	Application Area	
						Implant Devices	External Devices [1]
ZL70103LDG1	0 to +55	48-pin QFN	trays, bake, and dry-pack	YES [2]	NO [3]		X
ZL70103UEJ2 (contact Microsemi for availability)	0 to +55	49-pin CSP	trays	YES [4]	YES	X	
ZL70103UBJ (contact Microsemi for availability)	0 to +55	bare die	trays	N/A	YES	X	

Notes:

1. *Conditions that are applicable only for external applications are marked with "EXTOP" or "EXT-3.3V"; please refer to the "Conditions" section on page 7-3 for details.*
2. *Matte tin.*
3. *The QFN device is intended **ONLY** for external devices that are configured as controllers, such as base stations, programmers, patient controllers, and bedside monitors. The QFN device is **NOT** intended to be used in implant applications inside or outside the body. Implant applications such as trial devices that are functionally equivalent to implants but are worn outside the body should use bare die, CSP, or Microsemi modules. Testing of the 2.45-GHz wake-up receiver (RX_245 pin) is limited on QFN devices and, therefore, its operation and/or specifications are not guaranteed.*
4. *SAC405.*

3 – Functional Description

General

The ZL70103 is an ultra-low-power, high-bandwidth, RF transceiver for medical implantable applications. It operates in the Medical Implantable Communication Service (MICS) band at 402–405 MHz. It uses a forward error correction scheme together with CRC error detection to achieve an extremely reliable link.

Basic Modes

The ZL70103 transceiver is designed for operation in either an implant or a base station application. These systems have different requirements, especially with regard to power consumption. Therefore the ZL70103 transceiver has two basic modes (the mode is selected at power-up by the IBS pin):

- IMD mode The device is asleep waiting for a wake-up event
- Base mode The device is powered up and idle

When configured in IMD mode, the transceiver is usually asleep and in an ultra-low-current state. The IMD may be woken up to initiate communications either by receipt of a specially coded 2.45-GHz wake-up message or directly by the IMD processor via the WU_EN pin. These two methods of starting a communication session with an IMD are summarized below.

Power-Up Sequence

To ensure proper operation, the device must be powered-up in the correct order:

1. VDDIO and all digital inputs should have a defined low state
2. Provide supply voltage on the VSUP pin
3. Provide supply for the digital interface on the VDDIO pin and define digital inputs according to the configuration used

It is OK to provide supply to VDDIO at the same time as VSUP when they are connected together; however, VDDIO must never exceed VSUP.

Wake-Up Method Using 2.45-GHz Sent from a Base Station

Figure 3-1 shows the steps in setting up communication between a base station and an IMD woken up by using the ultra-low-power 2.45-GHz wake-up method. Details of this wake-up method are available in the ZL70103 Design Manual.

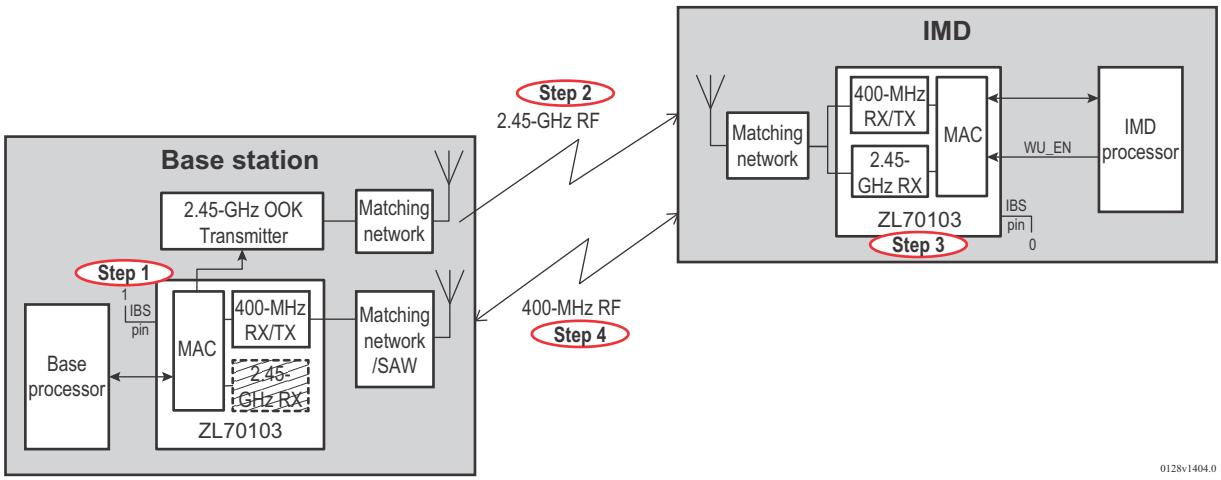


Figure 3-1 • **Wake-Up Method Using 2.45 GHz**

Steps:

1. START UP BASE STATION: Set the IBS pin equal to 1 and power up the base station. MAC starts and waits in IDLE state. Base station application performs Clear Channel Assessment (CCA) as described in the ZL70103 Design Manual. Base station application sets up important link parameters including registers for modulation mode, channel to use, IMD transceiver ID, and company ID as described in the "2.45-GHz Wake-Up Receiver" section on page 3-9 as well as in the ZL70103 Design Manual.
2. SEND 2.45-GHz WAKE-UP MESSAGE: The base station application initiates wake-up by writing to a communication control register in the ZL70103. This simultaneously provides the On-Off Keyed (OOK) pattern to the external 2.45-GHz transmitter and starts the 400-MHz transmitter and receiver to transmit 400-MHz wake-up messages and to receive 400-MHz wake-up responses, respectively.
3. IMD RECEIVES 2.45-GHz MESSAGE: The IMD's 2.45-GHz receiver is usually in a sleep state but is configured to periodically be powered up to look for a 2.45-GHz wake-up message. The interval between power-up strobes is user defined. The user may select one or both of the following two strobe mechanisms: (a) program a low-power oscillator available in the ZL70103 to generate the strobe, or (b) toggle the WU_EN pin to initiate a strobe.
4. IMD SENDS 400-MHz WAKE-UP RESPONSES: The IMD begins transmitting 400-MHz wake-up responses to the base station while listening for 400-MHz wake-up messages. The interval between response packets is randomized to minimize collisions between multiple IMDs and the base station. The base station may then begin a full MICS-band communication session with the desired IMD by writing to a communication control register in the ZL70103.

Wake-Up Method Using IMD Pin Control

Figure 3-2 shows the steps in setting up communication between a base station and an IMD woken up using the pin control in the IMD. This method is used for the following wake-up schemes:

- IMD woken up to sniff for a 400-MHz link. The ZL70103 supports such a mode of operation, although the 2.45-GHz wake-up system described in the previous "Wake-Up Method Using 2.45-GHz Sent from a Base Station" section on page 3-2 has a much lower power consumption.
- IMD woken to send an emergency message, in which case no CCA by the base station is required.
- IMD woken up by a low-frequency inductive link (as typically used in pacemakers/ICDs) or some other alternative mechanism.

In all these cases, the IMD transceiver is started by applying a positive pulse on WU_EN longer than 1.5 ms as described in the following steps.

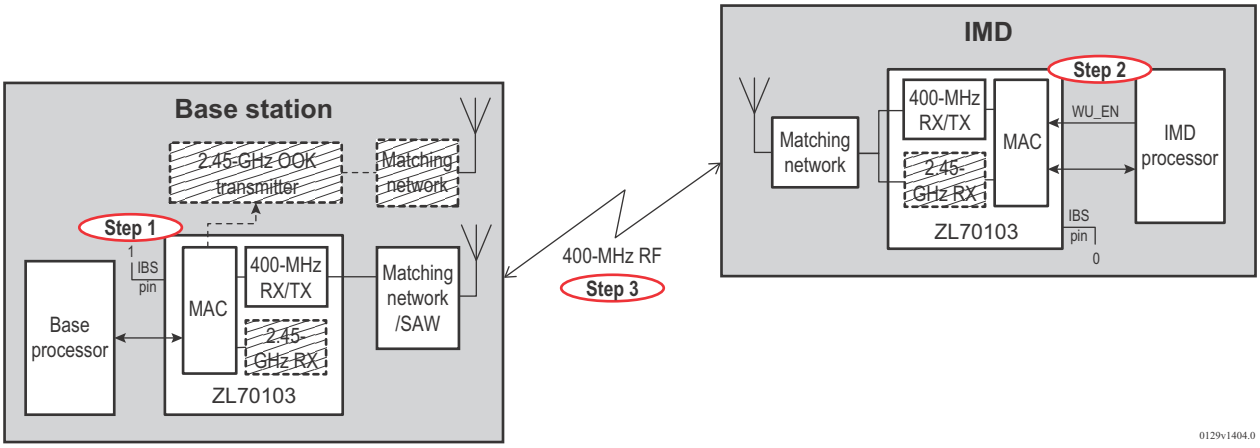


Figure 3-2 • **Wake-Up Method Using IMD Pin Control**

Steps:

1. START UP BASE STATION: Set the IBS pin equal to 1 and power up the base station. MAC starts and waits in the IDLE state. Base station application is set to monitor a channel selected by the application.
2. IMD PROCESSOR STARTS IMD TRANSCEIVER: IMD application sets the WU_EN pin high for greater than 1.5 ms and then low again (direct wake-up). The IMD transceiver wakes up and waits in the IDLE state. An important flag in the IMD transceiver called the IBS flag is set to 1 (IDLE). The IBS flag defines the operation of the transceiver after the MAC has woken up. The flag has two states (1 for IDLE, 0 to transmit wake-up responses).
3. IMD SENDS 400-MHz WAKE-UP NOTIFICATION: The IMD application then sets up the transceiver to use the desired modulation mode and channel, then changes the IBS flag to 0 (transmit wake-up responses) by writing to the appropriate control register in the IMD ZL70103. The IMD begins transmitting 400-MHz wake-up responses to the base station and the base station receives these responses. The base station may then begin a full MICS-band communication session with the desired IMD by writing to a communication control register in the ZL70103.

Details of the programming steps necessary for these steps and other operations is provided in the ZL70103 Design Manual.

Wake-Up Modes and Operational States

Wake-Up Modes

The IBS pin is used to define the normal operating mode. The IBS pin is low (0) to define that the ZL70103 is used in an implant and the IBS pin is high (1) to define that the device is used in an external device like a base station.

Operational States

During normal operation the device switches between the operational states depending on activity. Please refer to Figure 3-3 for an overview of the operating states.

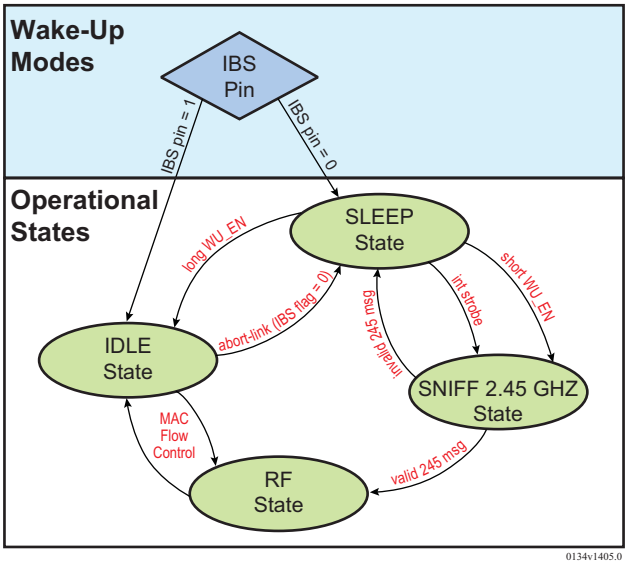


Figure 3-3 • **Operating Modes and States**

Current Consumption Overview

Table 3-1 summarizes the current consumption for the different operational states. Please also refer to Figure 3-6 on page 3-10.

Table 3-1 • **Current Consumption for Different Conditions of Each Operational State**

Operational State	Condition	Typical Current	Description
SLEEP	Standby	10nA	The device is in the ultra-low-power SLEEP (standby) state. In this condition, the ZL70103 can be woken up only by an external strobe to the WU_EN pin.
	25-kHz strobe oscillator (enabled)	320nA	Internal strobe pulse generator that can be used as an alternative to an external pulse on WU_EN. This current does include the SLEEP state current given for the Standby condition above.
IDLE	IDLE	0.95mA	The MAC is running but the RF and wake-up blocks are inactive.
RF	400-MHz receive	4.3mA	The device is running and in the 400-MHz receive state.
	400-MHz transmit	5.3mA	The device is running and in the 400-MHz transmit state (default configuration). Note that this current varies based on the transmitter output setting and based on the load on the transmitter.
	400-MHz RSSI sniff	4.0mA	The device is running in the receive state and sniffing for energy in the 400-MHz band as part of a 400-MHz wake-up mode.
SNIFF 245 GHZ	2.45-GHz RX sniff	1.4mA	The device is receiving on 2.45GHz to decode and identify valid wake-up messages from the base station (default configuration). The typical sniff period is 200µs. See Note 1.

Note:

1. *This feature is not tested on the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).*

Based on the wake-up method, Table 3-2 gives the typical average current consumption for each method.

Table 3-2 • **Average Sleep/Sniff Current Consumption While Sniffing**

Sniff Mode	Condition	Typical Average Current	Description
400-MHz	Direct wake-up with fast startup enabled	<5µA	Average sleep/sniff current consumption for a 400-MHz sniff based on a sniff interval of 5 seconds and a sniff period of 9.375ms.
2.45-GHz	External strobe of the WU_EN pin once a second	290nA	Average sleep/sniff current consumption based on a sniff interval of 1 second and a sniff period of 200µs. The sniff is triggered by a short pulse on the WU_EN pin. See Note 1.
	Internal strobe once a second by the 25-kHz strobe oscillator (strosc)	600nA	Average sleep/sniff current consumption based on a sniff interval 1 second and a sniff period of 200µs. The sniff is triggered by the internal 25-kHz strobe oscillator. See Note 1.

Note:

1. *This feature is not tested on the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).*

The communication protocol features a power-save timer, which allows the transceiver to enter the IDLE state for a user defined time (0 to 14 seconds) following the transmission of a packet. This is a very useful power saving feature in applications where the IMD does not immediately have data to send and the effective required data rate is lower than the high data rate provided by the ZL70103.

400-MHz Transceiver Subsystem

The transceiver uses a low-intermediate-frequency, superheterodyne architecture with image reject mixers. The low-IF architecture minimizes filter and modulator power consumption without the flicker noise issues associated with zero-IF architectures. An FSK modulation scheme reduces amplifier linearity requirements thereby reducing power consumption. In addition, FSK offers spectral efficiency by producing a high data rate given the MICS band spectrum mask requirements. Image rejection improves the adjacent channel rejection of the system.

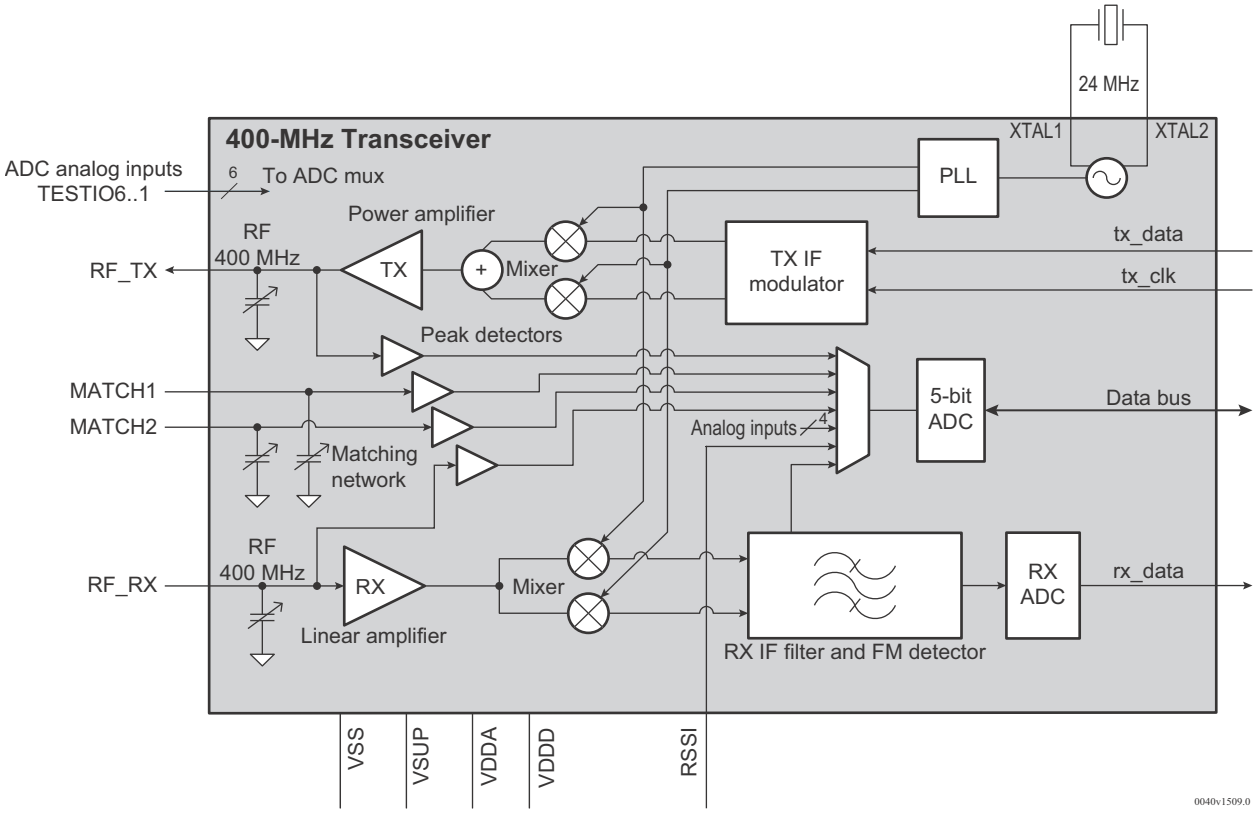


Figure 3-4 • **400-MHz Transceiver Subsystem**

Due to the relatively high RF path loss in implant applications, it is recommended that customers use the lowest possible data rate to ensure the best possible link quality. The sensitivity for different data rates can be seen in Table 3-3 on page 3-7.

The ZL70103 allows the user to select from a wide range of data rates (18.1818, 40, 200, 400, 800 kbit/s) with varying receiver sensitivity. To facilitate this flexibility, the system uses either 2FSK or 4FSK modulation with 200 or 400 kSymbols/s and varying frequency deviations and spreading factors. Table 3-3 on page 3-7 summarizes the allowable modulation modes, respective data rates, and corresponding receiver sensitivity. Please refer to the ZL70103 Design Manual for further information.

Table 3-3 • **Options for Modulation Modes, Data Rates, and Receiver Sensitivity**

Modulation Mode	Maximum Raw Radio Data Rate (kbit/s)	Maximum Effective Data Rate (kbit/s)	Typical Receiver Sensitivity (Note 1)
2FSK-Barker11	18.18	12.2	−110dBm
2FSK-Barker5	40	26.8	−107dBm
2FSK-fallback	200	134	−102dBm
2FSK	400	265	−91dBm
4FSK (Note 2)	800	515 (Note 3)	−79dBm

Notes:

1. *The sensitivity is based on the application circuit in Figure 10-1 on page 10-1, at the reference point of the dual-band antenna (50ohm). This value represents a packet error rate of 10%.*
2. *4FSK is an unevaluated mode for the ZL70103. Specifications for this mode are provided for guidance only. Contact Microsemi Application Support if use of this mode is required.*
3. *Requires calibration of the RX ADC. Refer to the ZL70103 Design Manual for the calibration procedure.*

Transmitter Section

The ZL70103 transmitter consists of an IF modulator, I and Q mixer, and power amplifier.

The IF modulator converts a one-bit (2FSK) or two-bit (4FSK) asynchronous digital input data stream to a 450-kHz FSK-modulated I and Q signal. The IF center frequency of 450kHz is automatically calibrated using a frequency locked loop (FLL) each time the transceiver is woken up.

An up-converting mixer transforms the IF to RF. Note that the local oscillator frequency is the same for both transmit and receive modes, facilitating a minimum dead time between receiving and transmitting packets. Both low- and high-side injection is used to always keep the image in the MICS band to relax the demands on phase and amplitude matching of the I and Q signals. When the RF is in the lower half of the MICS band, the LO frequency is higher than the transmitted radio frequency. When the RF is in the upper half of the MICS band, the LO frequency is lower than the transmitted radio frequency.

The output power of the TX power amplifier is register-programmable from approximately −3dBm to −30dBm (into a 500-ohm load, dependent on supply voltage). An antenna-matching capacitor bank is provided to fine tune the matching network for maximum delivered output power for a given power setting. The antenna tuning is an automatic calibration that uses a peak detector coupled to an ADC along with a state machine for calibration control.

Receiver Section

The ZL70103 400-MHz receiver amplifies the MICS-band signal and down-converts from the carrier frequency to the intermediate frequency (IF) using an I/Q image reject mixer. The LNA gain is programmable from 11 to 33dB in approximately 3-dB steps. The maximum gain settings are recommended for IMD transceivers, while the lower gain settings may be applicable to base station transceivers that choose to use an external LNA. Programmability of LNA and mixer bias currents provides further flexibility in optimizing for desired linearity (IIP3), power consumption, and noise figure.

An image-rejecting I/Q polyphase IF filter is used to suppress interference at the image frequency and adjacent channels and limit the noise bandwidth. The polyphase filter is followed by limiters and a Received Signal Strength Indicator (RSSI) block. The RSSI measurement is converted by a five-bit ADC and may be read by the SPI bus interface. To fulfill the regulatory requirements for performing the MICS-band clear channel assessment, the user has to port out the IF signal via the TESTIO pins. The RSSI measurement then uses off-chip components, available in the base station, to perform a measurement with higher resolution than the on-chip RSSI.

The RSSI block on the ZL70103 can be trimmed to obtain an optimum absolute accuracy. This is done once in production by applying a known external signal on RX and calibrating the RSSI offset with the trim bits.

An FM detector converts frequency deviation to voltage levels. The resulting baseband signal is subsequently low-pass filtered to remove the fourth harmonic of the IF and then digitized by a two-bit quantizer. The resulting data stream is provided to the MAC for correlation and clock recovery.

Before the packet, a sequence of training words are received. A DC removal circuit prior to the quantizer adjusts the DC level during the training phase. The purpose of this adjustment is to remove DC offset due to reference frequency differences between the base station and IMD transceivers.

Each packet begins with a 40-bit correlation sequence. If the frame sync match criteria is met, the DC level is fixed for the remainder of the packet. The value of the training and correlation word is programmable as well as the number of training bytes. A programmable capacitor bank is provided on RX to fine-tune the matching network. This function is intended to be used when RX and TX are separated in the matching network, as is typical in a base station.

Two additional programmable capacitor banks (MATCH1 and MATCH2) are provided to further facilitate tuning of the matching network. Refer to the ZL70103 Design Manual for further details.

Frequency Synthesizer

The frequency synthesizer is a PLL structure with an RF Voltage Controlled Oscillator (VCO) running at four times the LO frequency. The I/Q Local Oscillator (LO) signals are derived from the VCO signal and distributed to the receive and transmit front-end. The VCO is divided down and locked to the reference frequency, which is supplied by the crystal oscillator running at 24 MHz with an external crystal. The synthesizer uses both high- and low-side injection to ensure that the image frequency is always within the MICS band. The channel number is programmable from 0 to 9 for the 402- to 405-MHz MICS band and from 10 to 11 for 433.65 and 434.25 MHz in the ISM band; please refer to Table 3-4 for details.

Table 3-4 • **MICS/ISM Channel Table**

Channel Number	Center Frequency (MHz)	Frequency Band
0	402.15	MICS
1	402.45	MICS
2	402.75	MICS
3	403.05	MICS
4	403.35	MICS
5	403.65	MICS
6	403.95	MICS
7	404.25	MICS
8	404.55	MICS
9	404.85	MICS
10	433.65	ISM
11	434.25	ISM

Crystal Oscillator

The 24-MHz crystal oscillator (XO) is responsible for generating the system clock used by both the 400-MHz transceiver and the MAC. The required characteristics of the crystal are discussed in detail in the ZL70103 Design Manual. Microsemi has worked closely with leading IMD crystal manufacturers to ensure the availability of implant-grade 24-MHz crystals.

The required XO tolerance is determined by the transmitter and receiver frequency alignment requirements. Analysis of the ZL70103 indicates that the total frequency misalignment should be limited to 31 ppm. The ZL70103 XO has the facility for trimming a ±60-ppm oscillator to within ±10 ppm.

The oscillator may be bypassed by asserting the XO_BYPASS pin. This enables an external oscillator connected to XTAL1 to provide the 24-MHz frequency. Base stations may then choose to use a very accurate external crystal oscillator (XO) to provide engineering margin in the frequency budget and reduce on-chip frequency trimming requirements. When XO_BYPASS is asserted, the XO core is powered down and the signal from XTAL1 is provided directly to internal circuitry.

The 24-MHz clock divided by two (12MHz) and a variety of subfrequencies are available on the buffered programmable output pins PO3 and PO4 via register programming.

General-Purpose ADC

A five-bit general-purpose successive approximation ADC with a conversion time of 2µs is provided for the following purposes:

1. Measurement of the peak voltage at the 400-MHz PA output. This measurement is used for tuning the antenna matching network.
2. Measurement of the peak voltage at the MATCH1 capacitor bank. This is used for tuning the antenna matching network.
3. Measurement of the peak voltage at the MATCH2 capacitor bank. This is used for tuning the antenna matching network.
4. Measurement of the peak voltage at the 400-MHz RX input. This is used for tuning the antenna matching network.
5. Measurement of the internal 400-MHz RSSI signal. The application may find the RSSI measurement useful for automatic gain control or other system optimization methods that require a measurement of received 400-MHz signal strength.
6. Measurement of the internal 2.45-GHz RSSI signal. The application may also use this RSSI measurement for system optimization methods that require a measurement of received 2.45-GHz signal strength.
7. Supply voltage input. This is a useful system diagnostic measurement. The voltage on VSUP is divided by a resistive divider and measured using the ADC. The resistor divider is disconnected from the battery voltage when the ADC measurement is not selected or the ADC is disabled. Other ADC inputs do not have a resistor divider.
8. Measurement of inputs from analog TESTIO bus. One of four TESTIO pins, TESTIO4 to TESTIO1, may be selected for input into the ADC. This provides a useful general-purpose ADC function for the application. The ADC may be used to measure application specific physiological signals or system diagnostic signals.

A programmable multiplexer on the input of the ADC selects between the different measurements.

2.45-GHz Wake-Up Receiver

The 2.45-GHz receiver is used for a low-power wake-up system. The block diagram is shown as Figure 3-5, followed by a description of the basic operation.

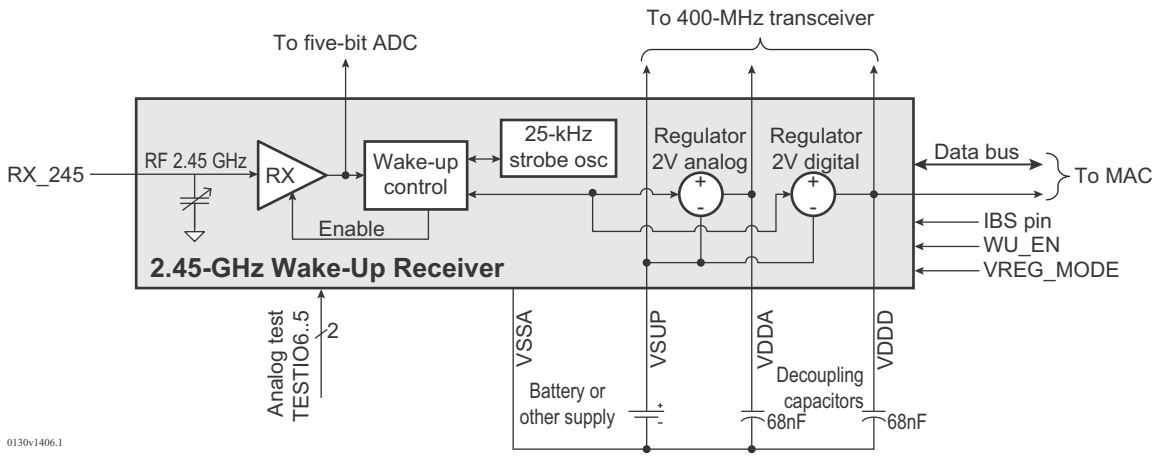


Figure 3-5 • **2.45-GHz Wake-Up Receiver Subsystem**

Note: This feature is not tested on the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).

Basic Operation

Most implant applications use the MICS-band RF link infrequently due to the overriding need to conserve battery power. In very low-power applications, the ZL70103 spends most of the time asleep in a very low-current state. Except for the sending of an emergency command in case of a medical event or using the low-duty-cycle mode, systems that use the MICS band must first wait for the base station to initiate communications following a CCA procedure in which the base station determines which channel to use.

Therefore, periodically, the IMD transceiver should listen for a base station that wants to begin communication. This sniffing operation should be frequent enough to provide reasonable startup latency, consume a very low current since it occurs regularly, and be immune to noise sources that invoke an erroneous startup.

For a very low-power receiver, an OOK modulation scheme is used since it removes the need for a local oscillator and synthesizer in the receiver. Further simplification, and hence power savings, is gained by using a frequency band that is of reasonable power for the startup process. The 2.45-GHz ISM band satisfies such a requirement by allowing up to 36 dBm (100 mW) or 26 dBm (10 mW) EIRP higher power than the MICS band, depending on each country's regulatory limits.

The wake-up system uses a novel ultra-low-power RF receiver, operating in the 2.45-GHz ISM band, to read OOK transmitted data. The main functions are: to detect and decode a specific data packet that is transmitted from a base station, and then to switch on the supply to the rest of the chip (the MAC block and the RF block, referred to collectively as the *core* in this document).

To reduce the average current consumption of the wake-up subsystem, the wake-up system is strobed by either:

1. An application-generated strobe pulse applied to the WU_EN pin to enable the wake-up circuitry. This minimizes the sleep current (I_{sleep} typically approximately 10 nA) to the leakage current.
2. An internally generated strobe pulse created using a low-power (typically 310-nA), internal, 25-kHz strobe oscillator. The total sleep current with the 25-kHz strobe oscillator is therefore typically 320 nA (I_{strosc}).

The average sleep/sniff current consumption for a system using an external strobe is:

$$I_{wu245\_ext} = I_{sleep} + I_{wu245} = 10 + 280 = 290 \text{ nA}$$

The average sleep/sniff current consumption for a system using the internal 25-kHz strobe oscillator is:

$$I_{wu245\_int} = I_{strosc} + I_{wu245} = 320 + 280 = 600 \text{ nA}$$

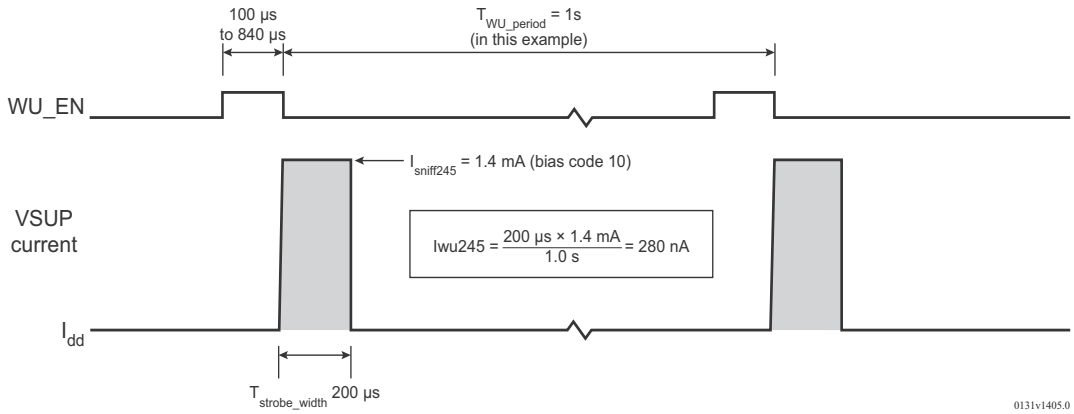


Figure 3-6 • **Strobing of Wake-Up System**

The actual current depends significantly on the timing of the strobe and the programming of the 2.45-GHz receiver. The power supply to both the digital and analog parts in the wake-up block is the VSUP voltage (2.05 V to 3.5 V).

The external strobe (WU_EN) and internal oscillator strobe are ORed such that either one (or both) may generate a wake-up strobe at any time when the device is asleep.

The data packet that is sent from the base station to the IMD transceiver is Manchester encoded and OOK modulated. The transmitted data packet is encoded with clock and data information. A simple decoder block is used to extract the clock information and sample the data using the recovered clock.

If an OOK-modulated signal with the correct timing is detected during the sniff period (T_{strobe_width}), the system continues to operate and searches for the start of the pattern indicated by a unique non-Manchester-encoded pattern of 11110000. After the start sequence is found, a complete packet of data is analyzed. If corrupted data is received, the wake-up controller terminates reception and powers down. Furthermore, if the received signal is lost during reception, a watchdog circuit terminates reception and powers down the wake-up receiver.

On successful detection and decoding of a valid packet of data, the wake-up receiver is turned off and the on-chip 2-V voltage regulators are enabled. Two voltage regulators are used (one for the analog core supply and one for the digital core supply) to separate the digital and analog supplies. The two voltage regulator outputs are available on two pins, VDDA and VDDD. Each voltage regulator requires one 68- to 200-nF capacitor for regulator stability.

After the regulators are fully on, the wake-up receiver is shut down and the crystal oscillator starts up, followed by the MAC. On successful core power up (where success is defined by whether the MAC is running) the MAC replies to the wake-up subsystem that it is ready and performs a CRC check of the wake-up memory, copies registers to the MAC, and performs calibrations. A communication session then occurs at 400 MHz. When the communication session is no longer required, the application puts the IMD into the SLEEP state via register control, thus powering down the core and returning the wake-up subsystem to periodic sniffing for a wake-up packet.

As mentioned in the "Basic Modes" section on page 3-1, there are various methods for waking up the transceiver. The wake-up controller, by monitoring the IBS and WU_EN pins, controls the selection of the various wake-up methods. Note that when the IBS pin is high (base-idle mode), the wake-up controller enables the regulated supply (VDDA and VDDD) throughout operation and the wake-up receiver remains disabled.

When the battery is connected for the first time, a POR block (wake_por) resets all digital registers and flip flops in the wake-up subsystem.

2.45-GHz Wake-Up Data Packet Definition

The data packet content is shown in Figure 3-7. The information is used by the IMD to set up the 400-MHz transceiver for communication on the appropriate channel and modulation mode.

The raw data is Manchester encoded (where a 0 is encoded as 01, a 1 is encoded as 10) since such a coding scheme can convey clock information, thus permitting the wake-up receiver to operate without a high-frequency clock and therefore save power. The OOK modulation pattern is provided on the PO0 pin by appropriately programming the output and writing a 1 to bit 0 of *reg_mac_initcom*. This OOK modulation pattern may be used by the external base station's 2.45-GHz transmitter. The contents of the wake-up pattern are set by programming various registers in the base station ZL70103 transceiver. The total wake-up packet length is typically 3.072 ms. Further details of the wake-up packet are described in the ZL70103 Design Manual.

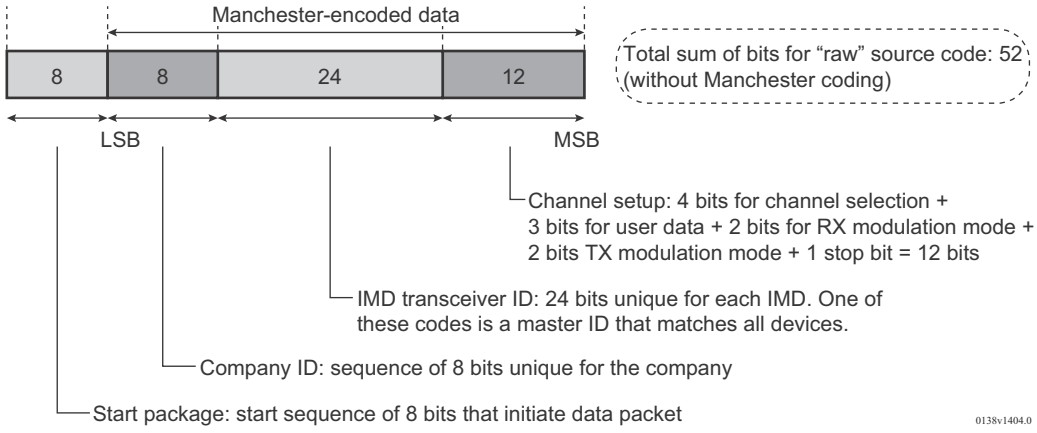


Figure 3-7 • **The Data Packet Definition**

The wake-up packet contains a company ID (assigned by Microsemi) and a IMD transceiver ID to identify the target IMD for communication.

The 12 bits after the IMD transceiver ID consist of channel setup information required to establish a 400-MHz communication session. This information is sent to the MAC if a correct company ID and IMD transceiver ID is detected.

The channel setup information is Manchester encoded as per the rest of the data packet and therefore no additional error checking is considered necessary. The probability is very low that these last 12 bits would be incorrectly detected following a correct company ID and IMD transceiver ID. Furthermore, any error would simply manifest as a delayed wake-up (it would need to be repeated).

Media Access Controller (MAC)

The MAC is a digital subsystem that controls the data communication and application interface. The block diagram in Figure 3-8 is followed by a description of the basic operation.

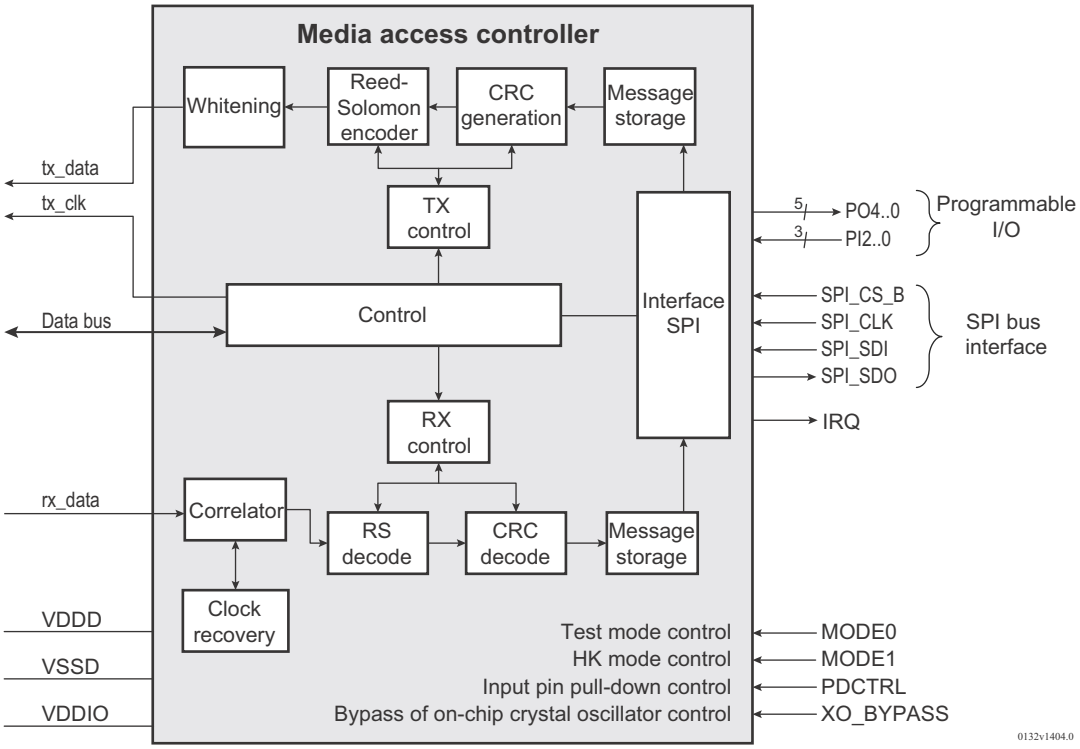


Figure 3-8 • **Media Access Controller Subsystem**

Basic Operation

The MAC consists of four main subsystems including:

1. Transmitter processing
2. Receiver processing
3. Communication control sequencer
4. Application interface

The transmit processing is fed by a 64×113-bit storage buffer capable of storing two maximally sized packets. The buffer is written through the SPI bus interface. The TX control constructs a data packet when more than one block of data exists in the transmit buffer. The definition of a data packet is contained in the "400-MHz Packet Definition" section on page 3-13. A cyclic redundancy code (CRC) is appended to the data and the result is passed through a Reed-Solomon (RS) block that provides extensive forward error correction. The final stage of transmission processing is to perform whitening using a pseudonoise (PN) method. Whitening ensures that the data has sufficient transitions for accurate operation of the clock recovery.

The receiver processing fills up a 64 × 113-bit storage buffer capable of storing two maximally sized packets. Again, the buffer is read through the SPI bus interface. The receiver performs clock recovery and identifies the correlation word signifying the start of a packet. Upon receipt of a packet, a Reed-Solomon decoder performs forward error correction on the header and each of the blocks that constitute a packet. The RS is capable of correcting up to 15 consecutive bit errors within a block. After error correction, a CRC decoder identifies blocks that contain uncorrectable errors and forwards the information on which blocks require retransmission to the transmit controller and main sequencer.

The communication control sequencer implements and controls the overall ZL70103 communication protocol. The features offered by the protocol include:

- Correction and detection of errors (FEC and CRC)
- Automatic retransmission of data blocks in error (ACK/NACK)
- Automatic flow control to prevent buffer overflow
- Automatic setup of modulation modes and reply to wake-up responses
- Facility to flush old data (which is useful when sending real-time ECG data in poor link conditions)
- Capable of sending MICS-band emergency command
- Minimization of collisions from multiple implants during wake-up responses
- Ability to send high-priority housekeeping messages
- Handling of link watchdog to ensure link is shut down after 5 seconds without successful communication
- Provision of link quality diagnostics
- Backup of important registers to wake-up block and CRC checking of memory
- Control of automatic calibrations
- Low-duty-cycle mode

The rich feature set of the ZL70103 communication protocol relieves the user application of many link maintenance activities. The communication link is simply viewed as a receive-and-transmit buffer accessible via the SPI bus interface. Buffer conditions that require user attention are flagged by interrupts, allowing the user to optimally maintain data flow. The user may also choose to poll buffer status registers as an alternative to handling interrupts.

The application interface is discussed in more detail in chapter "5 – Application Interface" on page 5-1.

400-MHz Packet Definition

The packet definition is chosen to enable a high effective data rate. The packet header should be kept as small as possible and the payload should be as large as possible. The same packet definition is used in both the uplink and downlink. The basis for the packet definition and the link protocol is fully described in the ZL70103 Design Manual.

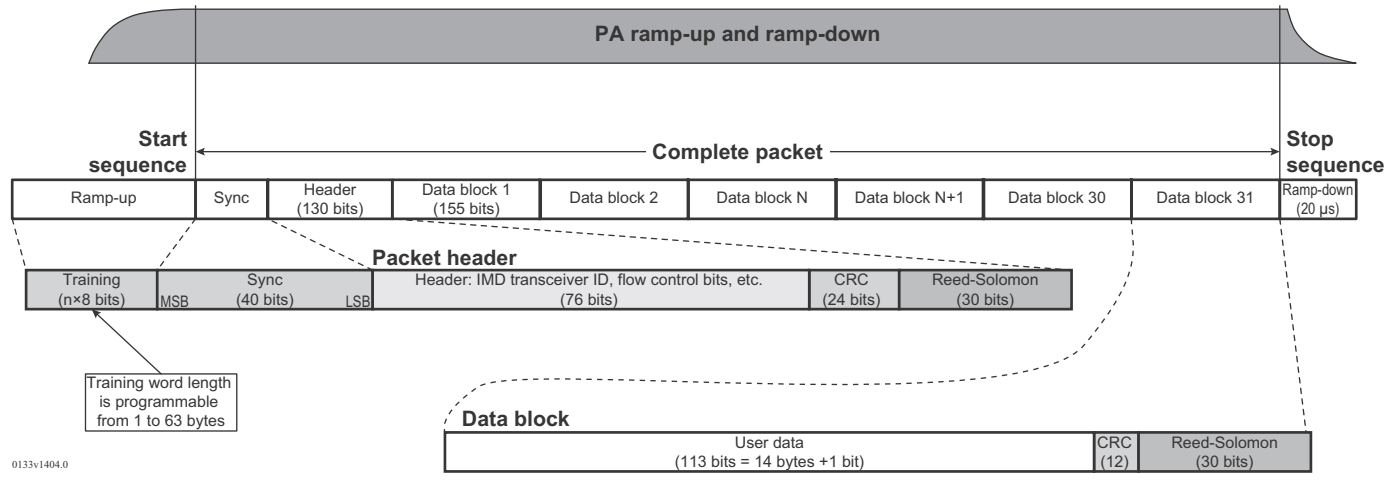


Figure 3-9 • **Packet Definition (first in time on the left side)**

Before the packet is transmitted a start sequence is applied to allow the PA to ramp up to full amplitude. During this period, training words are generated (and transmitted when the PA starts to ramp). The training words serve two purposes:

1. To form the signal during PA ramp
2. To provide the DC removal circuit with a training word for calibration after the PA is fully ramped

It is necessary to send sufficient training words so that the DC removal circuit can settle after the PA is fully ramped and before the packet is transmitted. The chip is preconfigured with default values for number of training words depending on chosen modulation.

The training sequence is followed by a 40-bit synchronization word defined by the registers *reg_mac_sync5..1*. The number of bits that must match in the synchronization word is specified by the register *reg_mac_syncmatch.* The default value of this register is 36 (8'h24), which allows a maximum of four errors in the synchronization word. The sliding correlator in the receiver checks against a known pattern. The synchronization word has been chosen so that its auto correlation is high only for zero lag.

The packet header contains flow control information that handles the automatic retransmissions of blocks in error, the prevention of receiver buffer overflow, packet acknowledgement, HK-related bits, channel info, and other protocol details. These are fully described in the ZL70103 Design Manual. The header also contains the IMD transceiver ID, which is a unique 24-bit code that identifies the implant, and the company ID, which is a code with eight bits that are unique to the company. The entire header is protected by a Reed-Solomon code and 24-bit CRC.

The header has a stronger CRC protection than the data since it is important that there are no undetected header errors. Undetected header errors would cause erroneous link operation depending on the header bits in error.

Each data block consists of 113 bits of effective data (14 bytes plus 1 bit). The single additional bit may be used by the application in a transport layer for indicating the start of the users packet. The data block is protected by a 12-bit CRC. The resulting bits are protected by 30 bits of RS error correcting code.

The maximum number of blocks in a data packet is programmable (1 to 31) via the register *reg_txbuff_maxpacksize.* The system sends less than the maximum number of blocks if data is available in the TX buffer. In other words, data is sent as soon as it is available, provided that at least one block exists in the TX buffer. The register *reg_txbuff_maxpacksize* only sets a limit on the *maximum* blocks in a packet.

The number of bytes in a TX or RX block that needs to be transferred from the SPI bus interface is programmable (*reg_rxbuff_bsize, reg_txbuff_bsize)* as described in the "Serial Peripheral Interface" section on page 5-1. There are always 113 bits sent in a data block but some of these bits are padded zeroes if the number of bytes in a block is set to less than the maximum value of 15. When using all 113 bits (14 bytes plus 1 bit, where block size set to 15) then the LSB of the first byte sent by the SPI bus interface is used for the additional single bit. This single bit is not used when the block size is less than 15.

4 – System Reliability Features

System Integrity — Watchdogs

The ZL70103 has three watchdogs that prevent the device from consuming power under fault conditions or during different operating states.

The system timing varies at different stages of the ZL70103 transceiver operation, which leads to three different watchdogs as described in Table 4-1. A watchdog of some type is always operating in the ZL70103.

Table 4-1 • **Summary of Watchdogs**

Watchdog	Purpose
Wake-up watchdog (IMD only)	Ensures that the wake-up block is not unnecessarily active. The block is shut down if: • a loss of the 2.45-GHz signal and clock is detected. • a wake-up signal with valid modulation and timing is received but no start pattern is found within a time longer than 2.5 times the wake-up packet width.
Transceiver initialization watchdog (base station and IMD)	Ensures that the system is put to sleep (IMD) or restarted (base station) in the event of failure of the 24-MHz crystal or in some other condition in which the MAC fails to start. This does not prevent the application from unwanted power consumption if the application firmware is trying to wake up the chip again.
Main watchdog (base station and IMD)	Ensures that the link is shut down after 5 seconds if no header is received. The MICS standard requires that a previously established link must cease transmission if no communication has occurred for a period of 5 seconds. This watchdog also ensures that a device in the IDLE state has serial interface communication with the application. The application is notified by an interrupt that occurs 0.6 second before the link is shutdown and the IMD is put to sleep. The application may override the shutdown by resetting the watchdog. During initial software development, it is very convenient to disable the watchdog. Methods of disabling the watchdog are discussed in the ZL70103 Design Manual.

Memory Integrity — CRC Check of Registers

The MAC or application can perform a CRC check of selected registers in the wake-up block. The MAC normally does this action automatically at startup and the user may also perform the CRC check anytime the MAC is powered. The CRC check includes all registers labelled in the memory map for CRC checking.

The CRC operation is controlled by the register *reg_wakeup_crcctrl*. The user may initiate a check of the CRC using a control bit, and status bits indicate whether the CRC check passed or failed. The user can also calculate a new CRC word using a control bit, and a status bit indicates that the calculation is complete. The application should control the copying of registers to the wake-up stack using the "copy registers" control bit in *reg_mac_ctrl*. It is recommended that such copying only occur following a successful communication session, since the register settings have been verified as operational; however, the application processor should always keep a duplicate copy of the registers in the wake-up block in case either a CRC error is detected at wake-up or a full chip reset is required. It is also possible to read and write to a single register in the wake-up stack since the stack is addressable using the register *reg_wakeup_stack_addr*. See the memory map in the ZL70103 Design Manual for more details and requirements regarding the operation of the CRC control register.

Communication Link Integrity

The following features of the ZL70103 contribute to a high communication link integrity:

- The RS forward error correction and CRC provide for excellent final BER performance.
- Individual acknowledgement and retransmission of data blocks is automatically handled.
- The variable receiver sensitivity obtained by different modulation modes is useful for poor link conditions.
- Link quality diagnostics are available including:
  - number of corrected blocks.
  - number of blocks with errors detected.
  - number of received blocks.
- A link quality interrupt is generated when either the block error or retransmission indicator exceeds programmable thresholds (evaluated per packet).

Details of these features are found in the ZL70103 Design Manual.

5 – Application Interface

This section describes the application interface including:

- Serial Peripheral Interface (SPI)
- Housekeeping messages
- Interrupts
- Programmable I/O

Serial Peripheral Interface

Registers and the TX/RX buffers are programmed via a standard SPI slave interface. The ZL70103 Design Manual contains the full memory map and programming details for the device.

The interface supports "MODE0 slave" operation where data is valid on the first rising edge of SPI_CLK; the idle state of SPI_CLK is low as shown in the basic timing diagrams in Figure 5-2 and Figure 5-3 on page 5-2. The default maximum SPI_CLK rate is 4MHz. A register (*reg_interface_mode)* may be programmed to decrease this operating speed down to 1 or 2MHz to reduce power consumption.

The ZL70103 supports both seven-bit addressing and eight-bit addressing for the SPI bus interface; however, seven-bit addressing is recommend for simplicity and consistency in the software. The default is seven-bit addressing for write operations. The register *reg_interface_mode* can be programmed to change the addressing for write operations to eight-bit addressing mode. Read can be done in either seven-bit or eight-bit addressing mode. The mode used for a read operation is defined in the protocol on SPI_SDI by the user and is not dependent on any register settings. See the ZL70103 Design Manual for a description of the eight-bit addressing mode.

A typical connection between the application and the ZL70103 transceiver SPI bus interface is shown in Figure 5-1. The application initiates the data transfer by driving the SPI_CS_B pin low. Data from the application is presented to SPI_SDI while data to the application is presented to SPI_SDO. Both input and output are clocked using the input SPI_CLK.

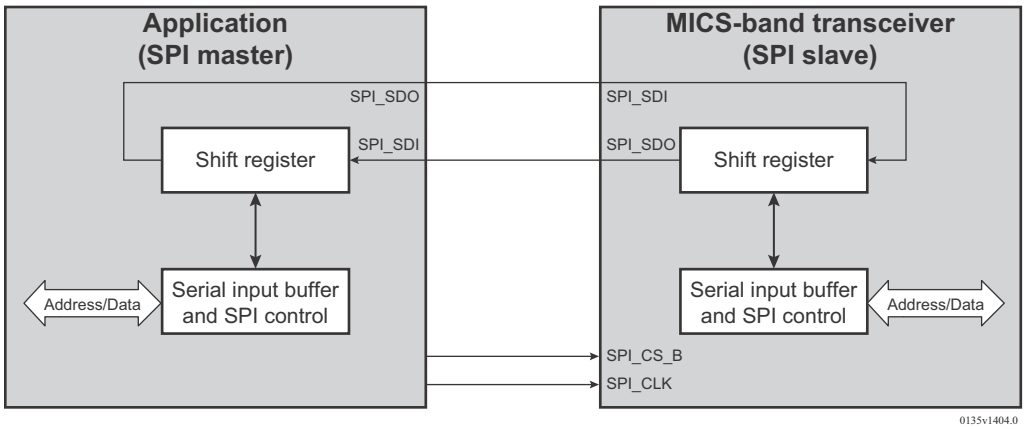


Figure 5-1 • **SPI Bus Interface**

Write Operation

For writing to a register using the default seven-bit addressing mode, SPI_CS_B is driven low to give access to the internal parallel bus in the ZL70103 transceiver. The application sends out address bits so data can be sampled on the rising edges of SPI_CLK. The write bit (where A7 is 0) and the seven address bits are shifted into the ZL70103 transceiver on the SPI_SDI pin. The eight address bits including the write bit are loaded into an address register. The address byte is followed by the data byte.

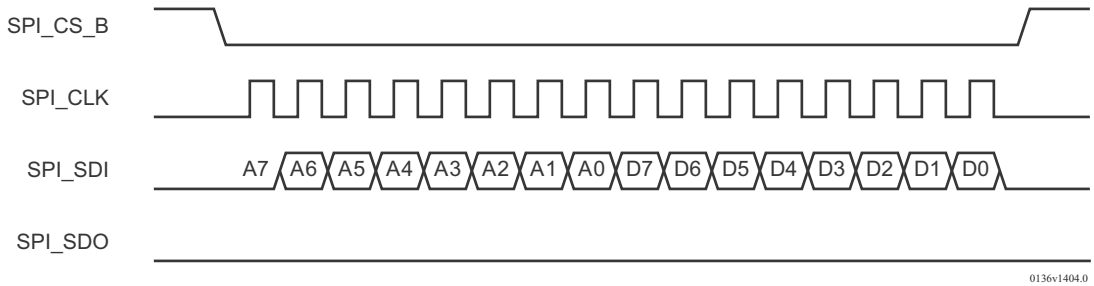


Figure 5-2 • **Timing for SPI Write of One Byte Using Seven-Bit Addressing Mode**

Read Operation

For reading a register using the seven-bit addressing mode, SPI_CS_B is driven low to give access to the internal parallel bus on the ZL70103 transceiver. Address or data changes can occur on the falling edge of SPI_CLK. Address and data bits, provided on the SPI_SDI pin, are sampled by the ZL70103 transceiver on the positive edge of SPI_CLK. The first bit indicates a read command (where A7 is 1). Read data is clocked out on the SPI_SDO pin on the falling edge of SPI_CLK. The application samples read data on the positive edge of SPI_CLK.

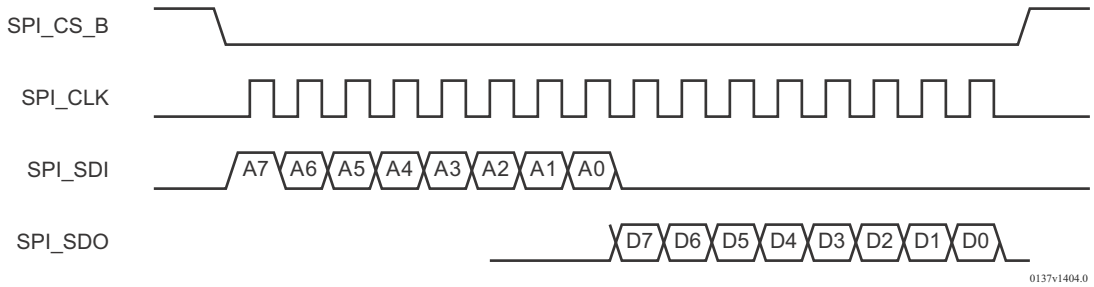


Figure 5-3 • **Timing for SPI Read of One Byte Using Seven-Bit Addressing Mode**

TX/RX Buffer Operation

The TX and RX buffers operate as a FIFO buffer occupying a single address (*reg_txrxbuff*) within the ZL70103 memory map. A read operation on *reg_txrxbuff* accesses the RX buffer and a write operation accesses the TX buffer.

TX and RX data is accessed in blocks. The internal block counters *reg_rxbuff_used* and *reg_txbuff_used* do not increment or decrement until a complete block is read or written. The number of bytes in a TX or RX data block that need to be transferred from the SPI bus interface for a block to be constructed into a TX packet or read from the RX buffer is programmable (*reg_rxbuff_bsize*, *reg_txbuff_bsize*). The value may range from 2 to 15 bytes per block.

Automatic SPI Address Increment

The SPI bus interface supports automatically incrementing the internal address, enabling reading and writing blocks of data without having to repeat the address for each byte. The first byte after assertion of SPI_CS_B is used to identify the address for the first byte that follows. When accessing registers other than *reg_txrxbuff*, the address subsequently automatically increments for each byte of data that follows. When accessing *reg_txrxbuff*, internal pointers within the TX and RX buffers automatically increment for each byte of data. The interface efficiency is improved since there is no need to send the address with each byte of data.

Housekeeping Messages

An HK message is a method of communicating directly with status and control registers in a remote transceiver in a manner similar to the local SPI bus interface. The data and address in the remote transceiver are sent in the radio packet header instead of via the SPI bus interface. There is one bit within the packet header (the HK bit) indicating that the header is an HK message. HK messages may be sent anytime by writing to the HK control registers. The HK messages do not contain the company ID or the channel info since these bits are used for the HK address and HK data.

HK messages have higher priority than packets containing data, so it is possible to send high-priority messages using HK. Eight-bit data can be sent to special registers (*reg_hk_userdata, reg_hk_userstatus*) in the receiving ZL70103 transceiver, and an IRQ alerts the receiving application that there is new HK data.

HK messages may be used to read from and write to remote registers, to transfer small amounts of data (one byte at a time), or to perform an action in the remote device that is initiated by a register write. Housekeeping messages are useful for downloading software, remotely performing calibrations such as a base station in production requesting calibrations in an implant, operating an implant transceiver without the need for an implant processor, and transferring small amounts of high-priority data with excellent CRC error detection.

HK messages feature a security mechanism that prevents unauthorized devices from remotely programming a transceiver. This feature is discussed in detail in the ZL70103 Design Manual.

Interrupts

The application may choose to develop software using an interrupt service routine or may simply use polling of various status registers within the device. Important status changes in the ZL70103 transceiver are signified by the assertion of an IRQ (interrupt request).

Interrupts are provided for the following purposes:

- Buffer control (for example, RX buffer not empty, TX buffer full)
- Housekeeping message control
- Radio and link status and quality indicators (for example, radio ready, link established)
- Radio operation error conditions (for example, backup memory CRC error)
- VREG (unintentional changes to the VREG trim register)

A maximum of three register reads are required to determine the interrupt source. These three registers have consecutive addresses and can therefore be read quickly using the automatic address increment function (refer to the ZL70103 Design Manual). The interrupt controller provides raw interrupt source status, interrupt status after masking, and an enable register. The enable register is used to determine if an active interrupt source should generate an interrupt request to the processor. The enable register has a dual mechanism for setting and clearing the enable bits. This allows enable bits to be set or cleared independently, with no knowledge of the other bits in the enable register. Such an approach simplifies interrupt software design. The control and clearing of interrupts is fully described in the ZL70103 Design Manual.

Programmable I/O

Programmable input/output pins are very useful for many applications. They provide polled outputs, direct access to status conditions within the ZL70103 transceiver, user-defined interrupt pins, user-defined general purpose outputs and clock signals, and access to specific base station outputs.

Programmable Output Sources

Four[1] output pins are available that may be programmable to directly display useful outputs. The programmable output sources include support for general purpose outputs, clock outputs, base station outputs, and interrupts.

One register is used for each programmable output pin (POx) to select the signals assigned to that pin. PO0 through PO3 are defined using registers called *reg_pox* (where x is the pin number 0, 1, 2, or 3), and PO4 is defined with the register *reg_mac_clkrecctrl,* giving a total of five registers. Several other registers control multiplexing of signals to these outputs and are detailed in the ZL70103 Design Manual, along with the available signals and register programming requirements.

Support for General-Purpose Outputs: The general-purpose outputs provide pin-constrained applications with some additional digital outputs. These outputs are set by writing the desired output value to the appropriate bit in *reg_gpo.* These general-purpose outputs may also be used by size-constrained implant applications in which removal of the implant application processor is desirable. In this case, the general-purpose outputs provide rudimentary digital control for the implant.

Support for Additional IRQ/Status Outputs: Most of the raw interrupt sources are available on the PO0, PO1, and PO2 pins. These sources support polled I/O processor communication or applications preferring multiple interrupts. The interrupts associated with PO0 and PO1 are mainly normal link and radio status conditions. The interrupts associated with are PO2 are mainly warning and error conditions.

Support for Selectable Clock Output: The PO3 pin may be used as a programmable clock. The values selected are extracted from a ripple counter operating from the 24-MHz system clock. Clock frequencies from 12MHz down to 150kHz are available.

Support for Base Station Controls: The programmable outputs provide several signals useful for supporting the base station operation. These signals are defined in Table 5-1.

Table 5-1 • **Summary of Base Station Control Signals**

Base Station Control Signal	Description
TX245	OOK digital modulation wake-up pattern produced by MAC power-up block.
TX_MODE	TX_MODE is high when both the TX_IF and TX_RF blocks are enabled. The transmitter does not begin transmitting until 15µs after the TX_MODE signal is asserted. The blocks are turned off less than 1µs after TX_MODE goes low. For convenience, some systems may prefer an active low variant of this signal; therefore,TX_MODE_B is equal to $\overline{\text{TX\_MODE}}$.
RX_MODE	RX_MODE is high when both the RX_IF and RX_RF blocks are enabled. The receiver blocks are not fully functional until 15µs after the RX_MODE signal is asserted. The blocks are turned off less than 1µs after RX_MODE goes low. For convenience, some systems may prefer an active low variant of this signal; therefore, RX_MODE_B is equal to $\overline{\text{RX\_MODE}}$.

Support for Bare Die: One of the programmable outputs (PO4) is placed on the right side of the chip to make it available also when the upper side of the chip is not bonded (typical on implants). This output can be programmed to provide the same signal as defined to any of the other four programmable outputs (PO0 to PO3). PO4 can also provide TX_MODE, TX_MODE_B, RX_MODE, or RX_MODE_B.

Programmable Input Sources

The programmable input pins (PI0, PI1, PI2) may be used as general-purpose inputs available as a register in the memory map. They are also used for various test purposes.

1 *Five output pads are available on the die option only.*

6 – Calibrations

Calibrations are needed for optimal transceiver performance. The majority of the calibrations may be performed very quickly (less than 10ms) and automatically by the ZL70103. These calibrations are started by a single register write to the calibration initiation bit in *reg_mac_ctrl*. Some calibrations need to be performed by the user and require more register writing and reading.

Some calibrations need to be performed only once in the factory, while other calibrations should be performed before each communication session; please see the ZL70103 Design Manual for more details.

The following parameters are automatically calibrated by the ZL70103 after each startup[1]:

- 25-kHz strobe oscillator tuning
- TX IF oscillator tuning
- FM detector and RX IF tuning
- RX ADC trimming

The following parameters can be automatically calibrated by the ZL70103. The following calibrations are optional, and the application has full control over initiation:

- Wake-up demodulator oscillator tuning
- 2.45-GHz LNA frequency tuning
- XO tuning
- 400-MHz TX antenna tuning
  - TX tuning capacitor and two additional antenna tuning capacitors (MATCH1 and MATCH2)
- 400-MHz RX antenna tuning capacitor

These calibrations are performed by writing and reading registers in the ZL70103 transceiver using the SPI or HK messages. At device power-up or wake-up, the MAC automatically performs calibrations defined by the register *reg_mac_calselect1*. The user may then perform calibrations anytime by first selecting the calibrations to perform (in *reg_mac_calselect1* or *reg_mac_calselect2*) and then writing to the calibration initiation bit in *reg_mac_ctrl* to initiate the calibrations.

The following parameters need to be calibrated by the user. There is no automatic calibration on the ZL70103 for these parameters. The procedures for these calibrations are described in the ZL70103 Design Manual.

- Voltage regulator trimming, if the ZL70103 is required to operate below 2.1 volts and at or above 2.05 volts
- 400-MHz RSSI offset trimming
- Spurious trimming (TX mixer and modulation spectrum)
- Output power trimming
- 2.45-GHz antenna tuning
- 2.45-GHz LNA gain trimming
- 2.45-GHz detector offset trimming

The majority of calibrations require no external equipment; the exceptions are:

- XO tuning requires a precise RF reference frequency
- 400-MHz RSSI trimming requires an external RF signal
- 2.45-GHz LNA frequency tuning and 2.45-GHz antenna tuning require an external 2.45-GHz RF signal
- Voltage regulator trimming requires an external voltmeter
- Output power trimming (external devices) requires an external power meter
- TX output spurious emissions trimming requires a spectrum analyzer

1 *Will be omitted if fast startup is used, please see the ZL70103 Design Manual for details.*

7 – Electrical Reference

Voltages are with respect to ground (VSS) unless otherwise stated.

Absolute Maximum Ratings

***Table 7-1* • Absolute Maximum Ratings**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.	Max.		
1.0	Supply voltage	V_{SUP}		−0.3		3.6	V	Note 1
1.1	Digital I/O supply voltage	V_{DDIO}		−0.3		V_{SUP}	V	Note 2
1.2	Digital I/O voltage	V_{IOD}		VSS−0.3		V_{DDIO}+0.3	V	Note 3
1.3	Analog I/O voltage	V_{IOA}		VSS−0.3		V_{SUP}+0.3	V	Note 4
1.4	XTAL I/O voltage	V_{XTAL}		VSS−0.3		V_{DDA}+0.3	V	Note 5
1.5	RF I/O voltage	V_{IORF}		VSS−0.3		V_{SUP}+0.3	V	Note 6
1.6	Storage temperature	T_{stg}	Unpowered	−40		+125	°C	
1.7	Burn-in temperature	T_{bi}	3.3V on VSUP and VDDIO			+125	°C	Notes 7, 8
1.8	Electrostatic discharge (human body model)	V_{ESD}	Any			500	V	Note 9

Notes:

1. *Application of voltage beyond the stated absolute maximum rating may cause permanent damage to the device or cause reduced reliability.*
2. *V_{DDIO} must never be higher than V_{SUP} even during system startup.*
3. *Applies to digital interface pins, including VREG_MODE, IBS, WU_EN, SPI_CS_B, SPI_CLK, SPI_SDI, PDCTRL, MODE0, MODE1, PI2..0, XO_BYPASS, SPI_SDO, PO3..0, PO4 (on bare die only), and IRQ.*
4. *Applies to analog interface pins, including TESTIO6..1.*
5. *Applies to reference frequency crystal interface pins, including XTAL1 and XTAL2.*
6. *Applies to RF interface pins, including RF_RX, RF_TX, MATCH1, MATCH2, and RX_245.*
7. *Device may be powered during burn-in but operation is not guaranteed.*
8. *Condition: 3.3V on VSUP and VDDIO.*
9. *Applied one at a time. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.*

Nominal Environment

The performance of several parameters is dependent on the matching network. Different applications require different matching networks, which impact the performance. The values specified in this chapter are valid based on an environment defined in Figure 7-1. This environment is intended for test and correlation only and is not suitable for a real application. Please see chapter "10 – Typical Application Examples" on page 10-1 for more information.

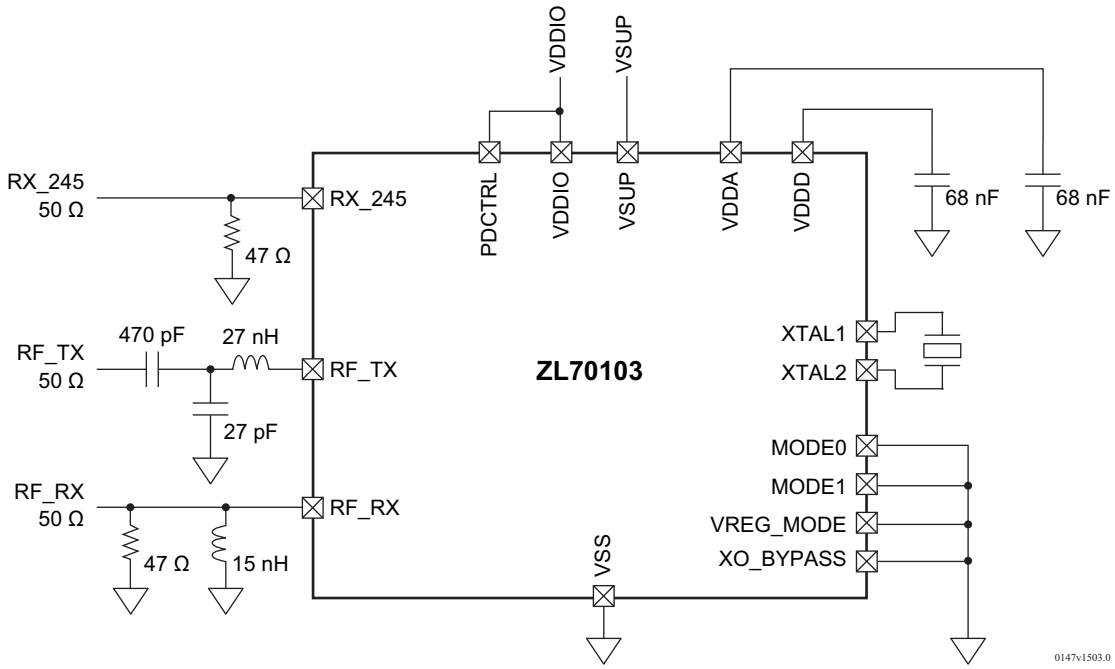


Figure 7-1 • **Nominal Environment Schematic**

Conditions

The ZL70103 transceiver can be used in different modes that impact the performance. Different applications also impose different requirements on the transceiver. An external application like a base station has much tougher requirements on out-of-band emissions compared to an implant, since the implant application is impacted by the transmission losses through the patient's body. Conversely, the wake-up receiver performance is only applicable to the implant application.

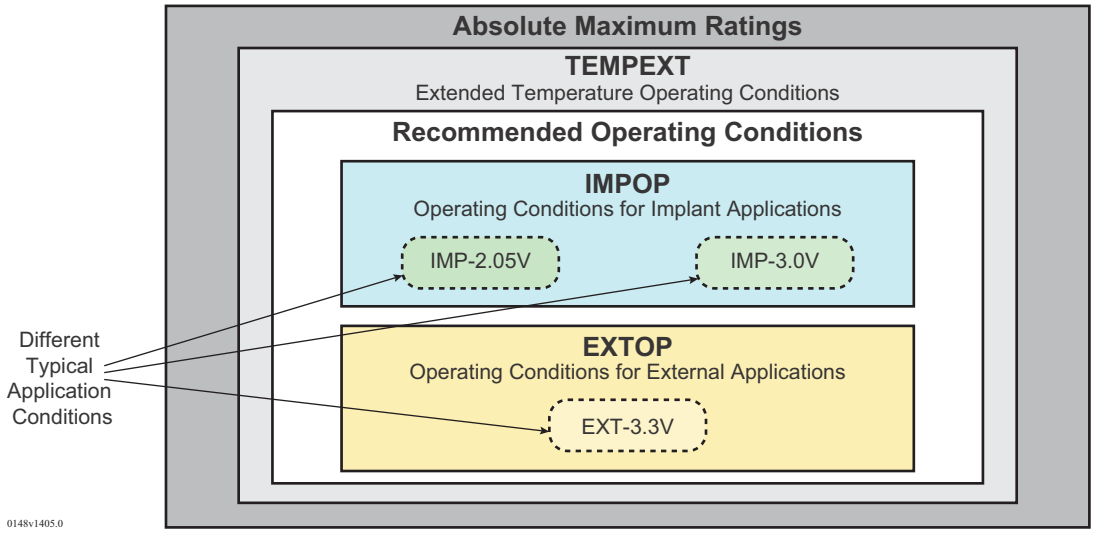


Figure 7-2 • **Operating Conditions Overview**

Figure 7-2 above provides an overview of the different operating conditions. Some performance parameters are more sensitive to conditions like supply voltage and temperature, and several typical application conditions like **IMP-2.05V** have been defined to allow more detailed performance characteristics. Please refer to the "Typical Application Conditions" section on page 7-5.

Operating Conditions

Recommended Operating Conditions

The recommended operating conditions define the nominal conditions for the device. This means that a specified parameter is valid for the recommended operating conditions stated in Table 7-2 unless otherwise noted.

Table 7-2 • **Recommended Operating Conditions**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
2.0	Supply voltage	V_{SUP}		2.05		3.50	V	
2.1	Input voltage (digital I/O)	V_{DDIO}		1.50		V_{SUP}	V	
2.2	Operating temperature	T_{op}		0		+55	°C	

Application-Dependent Operating Conditions

The ZL70103 transceiver power amplifier can operate in different modes:

- **Limited mode** suitable for implantable devices
- **Linear mode** suitable for external devices

The **limited mode** is optimized for ultralow power consumption at the cost of slightly higher unwanted emissions. This mode is intended for operation in the body, where the power losses due to the body reduce the unwanted emissions to levels compliant with the FCC CFR47.95 requirements.

Conditions valid only for implanted applications using the limited mode are marked with condition **IMPOP**.

The **linear mode** is optimized to minimize the unwanted emissions so that the maximum allowed output power can be used by an external device within the FCC CFR47.95 requirements. This impacts the supply voltage range that can be used as stated in Table 7-3. Parameters specified under the operating condition for external devices are marked with condition **EXTOP**.

Table 7-3 • **Operating Conditions for External Applications**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
3.0	Supply voltage	VSUP	EXTOP	2.80		3.50	V	Note 1

Note:

1. *The ZL70103 can also be used at lower supply voltages in linear mode, but this might require reduced output power to be compliant with the out-of-band emissions requirements.*

Extended Temperature Operating Conditions

The extended temperature operating conditions specify a temperature range where the chip is operating but has limited performance. Under extended temperature operating conditions, the chip does wake up at power-on. Communication and all digital functionality also work as expected. Parameters specified under the extended operating conditions are marked with condition **TEMPEXT**.

Table 7-4 • **Extended Temperature Operating Conditions**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
4.0	Operating temperature	T_{op}	TEMPEXT	−20		+60	°C	

Typical Application Conditions

Because the ZL70103 transceiver can be used in different modes that impact the performance, typical applications are referenced in the tables in "Electrical Characteristics" section on page 7-6, in the **Condition** column.

The device must be correctly configured, trimmed, and calibrated according to the ZL70103 Design Manual. The important register settings are listed in Table 7-6 and Table 7-8.

Implant Conditions

Table 7-5 • **Implant Conditions**

Condition ID	Supply Voltage	Temperature	Comment
IMP-2.05V	2.05V	37°C	Implies IMPOP
IMP-3.0V	3.0V		

Table 7-6 • **Register Settings for Implant Conditions**

Register	Description	Value	Comment
txrf_sel_ctrl	Set limit mode and power amplifier buffer amplitude	251	Default
txrfpwrdefaultset	Power amplifier output power code	48	Optimized maximum power

External Conditions

Table 7-7 • **External Device Conditions**

Condition ID	Supply Voltage	Temperature	Note
EXT-3.3V	3.3V	25°C	Implies EXTOP

Table 7-8 • **Register Settings for External Conditions**

Register	Description	Value	Comment
txrf_sel_ctrl	Set linear mode and power amplifier buffer amplitude	23	
txrfpwrdefaultset	Power amplifier output power code	240	The output power code is typically adjusted in the final application to provide the desired TX radiated power (e.g., maximum −16dBm EIRP for FCC)

Electrical Characteristics

General Notes on Limits

Default register and mode settings are assumed unless noted.

Electrical testing during production is used to ensure that delivered parts fulfill the limits defined under "Electrical Characteristics". In some cases it is not possible to perform electrical testing or the testing has been carried out in a different manner. If exceptions apply, these exceptions are tagged in the tables in this chapter as defined in Table 7-9.

Table 7-9 • **General Notes on Limits**

Tag	Definition
①	These parameters are guaranteed by production tests but with different limits than those specified in the datasheet. This is due to limitations in the capabilities of the automated test equipment. The production tests that are carried out have been correlated to tests carried out in the lab environment.
②	These parameters are guaranteed by production tests; however, these may be carried out in a different manner than that defined in the datasheet.
③	These parameters are tested during production testing, but the limits are provided for design guide only.
④	These parameters are provided for design aid only; they are not guaranteed and are not subject to production testing.
⑤	Typical values according to the specified condition. If no conditions are specified, the typical figures are at a temperature of 37°C and V_{SUP} equal to 3.0V. Typical values are for design aid only; they are not guaranteed and not subject to production testing.

On-Chip Voltage Regulators

Table 7-10 • **On-Chip Voltage Regulators**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
5.0	Analog on-chip regulated power (analog 2V domain)	V_{DDA}		1.9		2.0	V	Note 1
5.1	Digital on-chip regulated power (digital 2V domain)	V_{DDD}		1.9		2.0	V	

Note:

1. *Do not connect external circuits to this pin. VDDA is a regulated supply for the internal analog circuits of the ZL70103.*

Digital Interface

The digital interface parameters in Table 7-11 are valid for the following pins:

- Digital inputs: WU_EN, SPI_CS_B, SPI_CLK, SPI_SDI, PDCTRL, MODE0, MODE1, PI0, PI1, PI2, XO_BYPASS, VREG_MODE, IBS
- Digital outputs: SPI_SDO, PO0, PO1, PO2, PO3, PO4 (on bare die only), IRQ
- Crystal interface: XTAL1, XTAL2

Table 7-11 • **Digital Interface**

ID	Parameter	Symbol	Condition	Limits		Unit	Note
				Min.	Max.		
6.0	Digital interface voltage	V_{DDIO}	TEMPEXT	1.5	V_{SUP}	V	
6.1	Digital input low②	V_{IL}	TEMPEXT	0	$0.2 \times V_{DDIO}$	mV	Note 1
6.2	Digital input high②	V_{IH}	TEMPEXT	$0.8 \times V_{DDIO}$	V_{DDIO}	mV	Note 2
6.3	XTAL1 input low②	$V_{ILXTAL1}$	TEMPEXT	0	$0.2 \times V_{DDA}$	mV	Notes 1, 3
6.4	XTAL1 input high②	$V_{IHXTAL1}$	TEMPEXT	$0.8 \times V_{DDD}$	V_{DDA}	mV	Notes 2, 3
6.5	Digital output low	V_{OL}	TEMPEXT	0	150	mV	I_{load} = 1 mA
6.6	Digital output high	V_{OH}	TEMPEXT	V_{DDIO} − 150	V_{DDIO}	mV	I_{load} = −1 mA
6.7	Digital I/O input leakage	I_{DDIO_leak}	TEMPEXT	−10	10	nA	V_{out} = 0 V and 3.5 V
6.8	Maximum output frequency at 10-pF load	f_{max}			5	MHz	

Notes:

1. *V_{IL} is the required input voltage to ensure internal signal switching from high to low.*
2. *V_{IH} is the required input voltage to ensure internal signal switching from low to high.*
3. *A digital input to XTAL1 is applicable only when the XO is bypassed by connecting the XO_BYPASS pin to VDDIO.*

SPI Timing Requirements

The detailed timing requirements in Table 7-12 apply to all SPI operations with the ZL70103. The timing parameters are illustrated in Figure 7-3.

Table 7-12 • **SPI Timing Requirements**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
7.0	Data to SPI_CLK setup③	t_{DC}		50			ns	
7.1	SPI_CLK to data hold SPI_SDI③	t_{CDHI}		50			ns	
7.2	SPI_CLK to data hold SPI_SDO③	t_{CDHO}					ns	Note 1
7.3	SPI_CLK to data delay at 10-pF load③	t_{CDD}		0	20	50	ns	
7.4	SPI_CLK low time③	t_{CL}		125			ns	
7.5	SPI_CLK high time③	t_{CH}		125			ns	Note 2
7.6	SPI_CLK frequency③	f_{SPI_CLK}				4	MHz	Note 3
7.7	SPI_CLK rise and fall③	t_R, t_F				25	ns	
7.8	SPI_CS_B to SPI_CLK setup③	t_{CC}		125			ns	
7.9	SPI_CLK to SPI_CS_B hold③	t_{CCH}		125			ns	
7.10	SPI_CS_B inactive time③	t_{CWH}		250			ns	
7.11	SPI_CS_B to output high-Z③	t_{CDZ}				300	ns	

Notes:

1. *Depends on SPI_CLK frequency. Data is valid until new data is driven (see t_{CDD}) or until SPI_CS_B is inactive (high).*
2. *The minimum period for SPI clock high is based on a 4-MHz maximum SPI clock rate.*
3. *The maximum SPI clock rate is programmable to 1, 2, or 4MHz (refer to programming information for the reg_interface_mode register). The default is a 4-MHz maximum SPI clock rate. Lower maximum SPI clock rate settings allow for a reduction in power consumption.*

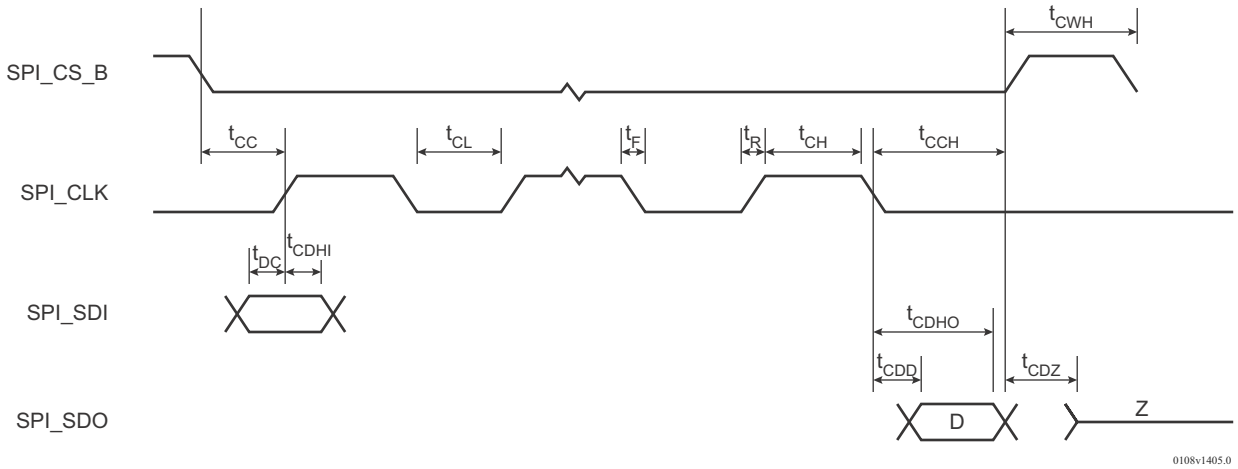


Figure 7-3 • **SPI Timing Parameters**

Performance Characteristics

General RF Parameters

Table 7-13 • **General RF Parameters**

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
8.0	Radio frequency (MICS band)	F_{RF_MICS}		402.0		405.0	MHz	
8.1	Radio frequency (ISM band)	F_{RF_ISM}		433.5		434.4	MHz	
8.2	Channel width	CW				300	kHz	
8.3	Raw data rate (4FSK)②	DR_{4FSK_raw}			800		kbit/s	Note 1
8.4	Maximum effective data rate (4FSK)④	DR_{4FSK_eff}				515	kbit/s	Notes 1, 2, 3
8.5	Raw data rate (2FSK)②	DR_{2FSK_raw}			400		kbit/s	
8.6	Maximum effective data rate (2FSK)④	DR_{2FSK_eff}				265	kbit/s	Note 2
8.7	Raw data rate (2FSK-fallback)②	DR_{2FSKfb_raw}			200		kbit/s	
8.8	Maximum effective data rate (2FSK-fallback)④	DR_{2FSKfb_eff}				134	kbit/s	Note 2
8.9	Raw data rate (2FSK-Barker5)	DR_{2FSKb5_raw}			40		kbit/s	
8.10	Maximum effective data rate (2FSK-Barker5)	DR_{2FSKb5_eff}				26.8	kbit/s	
8.11	Raw data rate (2FSK-Barker11)	$DR_{2FSKb11\_raw}$			18.18		kbit/s	
8.12	Maximum effective data rate (2FSK-Barker11)	$DR_{2FSKb11\_eff}$				12.2	kbit/s	

Notes:

1. *4FSK is an unevaluated mode for the ZL70103. Specifications for this mode are provided for guidance only. Contact Microsemi Application Support if use of this mode is required.*
2. *Maximum effective throughput assuming no errors in link, same raw data rate (mode) for TX and RX, maximum-sized packets for RX, and minimum-sized acknowledgment-only packet for TX (maximum-sized packets consist of 31 blocks per packet with 113 payload bits per block).*
3. *Requires calibration of the RX ADC. Refer to the ZL70103 Design Manual for the calibration procedure.*

Current Consumption

Table 7-14 • Current Consumption

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
9.0	SLEEP state current	I_{sleep}	IMPOP $T_{op} \leq 37°C$		10	50	nA	Note 1
			IMPOP $T_{op} \leq 55°C$		10	150	nA	
			TEMPEXT		10	200	nA	
			EXTOP		10	200	nA	
9.1	IDLE state current	I_{idle}			0.95	1.1	mA	
9.2	400-MHz receive state current	I_{RX400}			4.3	5.0	mA	
9.3	400-MHz transmit state current	I_{TX400}	IMP-2.05V		4.9	5.3	mA	
			IMP-3.0V		5.3	5.8	mA	
			EXT-3.3V		5.7	6.5	mA	
9.4	400-MHz RSSI sniff current	$I_{sniff400}$			4.0		mA	
9.5	400-MHz average wake-up current	I_{wu400}			<5		µA	Note 2
9.6	25-kHz strobe oscillator (strosc) current	I_{strosc}	IMP-2.05V		270	310	nA	Note 3
			IMP-3.0V		320	360		
			TEMPEXT			600		
9.7	2.45-GHz RX sniff current	$I_{sniff245}$	IMPOP		1.4	1.8	mA	Note 4
			TEMPEXT			2.1	mA	
9.8	Average wake-up current (external pulse on WU_EN)	I_{wu245_ext}	IMPOP $T_{op} \leq 37°C$		290	410	nA	Note 5
9.9	Average wake-up current (25-kHz strobe oscillator)③	I_{wu245_int}	IMPOP $T_{op} \leq 37°C$		600	810	nA	Note 5

Notes:

1. *WU_EN low between external strobe pulses*
2. *Average sleep/sniff current consumption for a 400-MHz sniff based on a sniff interval of 5seconds and a sniff duration of 9.375ms*
3. *WU_EN low between internal strobe pulses*
4. *Register settings for bias code: reg_wakeup_lnabias is 10, and reg_wakeup_wk_rx_lna_negrtrim1 is based on trimming*
5. *Wake up sniff interval is 1 second*

Synthesizer

Table 7-15 • Synthesizer

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
10.0	Composite transmit phase noise at Df = 250 kHz	Φ_{synth_250k}			−110		dBc/Hz	At mixer
10.1	Reference spurs	Ψ_{synth_clrs}				−45	dBc	At ±n × 300 kHz
10.2	PLL lock time	T_{synth_lock}			1.941 (Note 1)	4.35 (Note 2)	ms	To within 2 kHz.

Notes:

1. *Requires coarse tuning.*
2. *Without coarse tuning.*

400-MHz Transmitter

Table 7-16 • 400-MHz Transmitter

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
11.0	Frequency separation (4FSK, 800 kbit/s)	MOD_{F4}		33	36	42	kHz	
11.1	Frequency separation (2FSK, 400 kbit/s)	MOD_{F2}		77	80	83	kHz	
11.2	Frequency separation (2FSK-fallback, 200 kbit/s)	MOD_{F2_FB}		96	100	104	kHz	
11.3	Transmit power	$P_{TX400max}$	IMP-2.05V	−8.2	−6.5		dBm	
			IMP-3.0V	−5.2	−3.5		dBm	
			EXT-3.3V	−7.5	−4.0		dBm	
11.4	Minimum transmit power①	$P_{TX400min}$				−33	dBm	
11.5	Unwanted emissions outside the 402- to 405-MHz band	$E_{outband}$	EXTOP			−39	dBc	Note 1
			IMPOP			−30	dBc	Note 1
11.6	Unwanted emissions within the 402- to 405-MHz band	E_{inband}				−20	dBc	Note 2

Notes:

1. *Fulfills FCC CFR47.95. Requires trimming; please refer to the ZL70103 Design Manual for details.*
2. *Fulfills FCC CFR47.95*

400-MHz Receiver

Table 7-17 • 400-MHz Receiver

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
12.0	Minimum RF amplifier and mixer gain①	G_{RX}			11	16	dB	
12.1	Maximum RF amplifier and mixer gain①	G_{RX}		24	33		dB	
12.2	1-dB compression point referred to input①	ICP1		2.5	3		mV	Note 1
12.3	Third-order input intercept point④	IIP3			8		mV	Note 1
12.4	RX sensitivity (4FSK)①	P_{RX_4F}			−79		dBm	Note 2, 3
12.5	RX sensitivity (2FSK)①	P_{RX_2F}			−91		dBm	Note 2
12.6	RX sensitivity (2FSK-fallback)①	$P_{RX\_2F\_FB}$			−102		dBm	Note 2
12.7	RX sensitivity (2FSK-fallback with Barker5 spreading)	$P_{RX\_2F\_FB\_B5}$			−107		dBm	Note 2
12.8	RX sensitivity (2FSK-fallback with Barker11 spreading)	$P_{RX\_2F\_FB\_B11}$			−110		dBm	Note 2

1. *With an RX LNA gain setting of reg_rf_rxrflnagaintrim = 8'h7F (second highest gain).*
2. *The sensitivity is based on the application circuit in Figure 10-1 on page 10-1, at the reference point of the dual-band antenna (50ohm). This value represents a packet error rate of 10%.*
3. *4FSK is an unevaluated mode for the ZL70103. Specifications for this mode are provided for guidance only. Contact Microsemi Application Support if use of this mode is required.*

2.45-GHz Receiver

Table 7-18 • 2.45-GHz Receiver

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
13.0	RX_245 sensitivity (normal mode)②	P_{RX245}			−73		dBm	3 µs RF-on time; see Note 1
13.1	RX_245 sensitivity (sensitive mode)②	P_{RX245}			−75		dBm	6 µs RF-on time; see Note 1

Note:

1. *This feature is not tested on the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).*

Crystal Oscillator

Table 7-19 • Crystal Oscillator

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
14.0	Oscillator frequency	F_{xo_osc}			24		MHz	
14.1	Post-trim tolerance (frequency trim step)②	ΔF_{xo_post}				±10	ppm	Note 1

Note:

1. *Based on a pretrim tolerance = ±60 ppm.*

General-Purpose ADC

Table 7-20 • General-Purpose ADC

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
15.0	ADC conversion time	T_{con}			2.08		ms	T_{con} = 8 / 24 × N_{ADCr}
15.1	ADC resolution	n_{ADC}			5		bits	
15.2	Differential nonlinearity	DNL_{ADC}				0.5	LSB	
15.3	Integral nonlinearity	INL_{ADC}		−1		1	%FS	
15.4	Gain error	G_{ADCerr}		−2.5		2.5	%FS	at full scale
15.5	Offset error	V_{ADCerr}		−1		1	LSB	
15.6	Input voltage range	V_{ADC}		0		1.25	V	

Internal RSSI

Table 7-21 • Internal RSSI

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min	Typ⑤	Max		
16.0	Input voltage where n_{ADC} is 5'b00000 ②	V_{rssi_min}				5	µVrms	Note 1
16.1	Input voltage where n_{ADC} is 5'b11111 ②	V_{rssi_max}		4			mVrms	Note 1
16.2	Relative step size	DV_{rx_rssi}		1	2	3	dB	

Note:

1. *At LNA input, RSSI trimmed*

RF Ports

Table 7-22 • RF Ports

ID	Parameter	Symbol	Condition	Limits			Unit	Note
				Min.	Typ.⑤	Max.		
17.0	Tuning capacitor range (400-MHz TX)③	C_{400TX}		1.5		9	pF	0.1-pF step. Note 1
17.1	Tuning capacitor range (400-MHz RX)③	C_{400RX}		2		9	pF	0.1-pF step. Note 1
17.2	Tuning capacitor range MATCH1③	C_{M1}		2.5		15.5	pF	0.25-pF step. Note 1
17.3	Tuning capacitor range MATCH2③	C_{M2}		2		16	pF	0.25-pF step. Note 1
17.4	Tuning capacitor range (2.45-GHz)③	C_{245RX}		0.3		2	pF	0.1-pF step. Notes 1, 3
17.5	400-MHz receiver input impedance, reactive part	X_{400RX}			−j232		Ω	
17.6	400-MHz receiver input impedance, resistive part	R_{400RX}			4500		Ω	
17.7	2.45-GHz receiver input impedance, reactive part	X_{245RX}			−j64		Ω	Note 3
17.8	2.45-GHz receiver input impedance, resistive part	R_{245RX}			500		Ω	Note 3
17.9	Shunt resistive load presented to 400-MHz transmitter④	R_{400TX}		144	500		Ω	
17.10	Shunt reactive load presented to 400-MHz transmitter④	X_400TX		+j57	+j88	+j199	Ω	Note 2

Notes:

1. *Valid for bare die or CSP*
2. *The reactive load is set to provide resonance. It should be the conjugate of the tuning capacitor reactance. That is, $X_{L400tx} = j/(\omega C_{tune400})$. The range of tuning may be restricted by parasitic capacitance and inductance in a packaged device.*
3. *This specification does not apply to the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).*

Typical Performance

Typical performance graphs in Figure 7-4 show average device performance based on the test environment described earlier in this chapter. The typical performance is shown for design aid only.

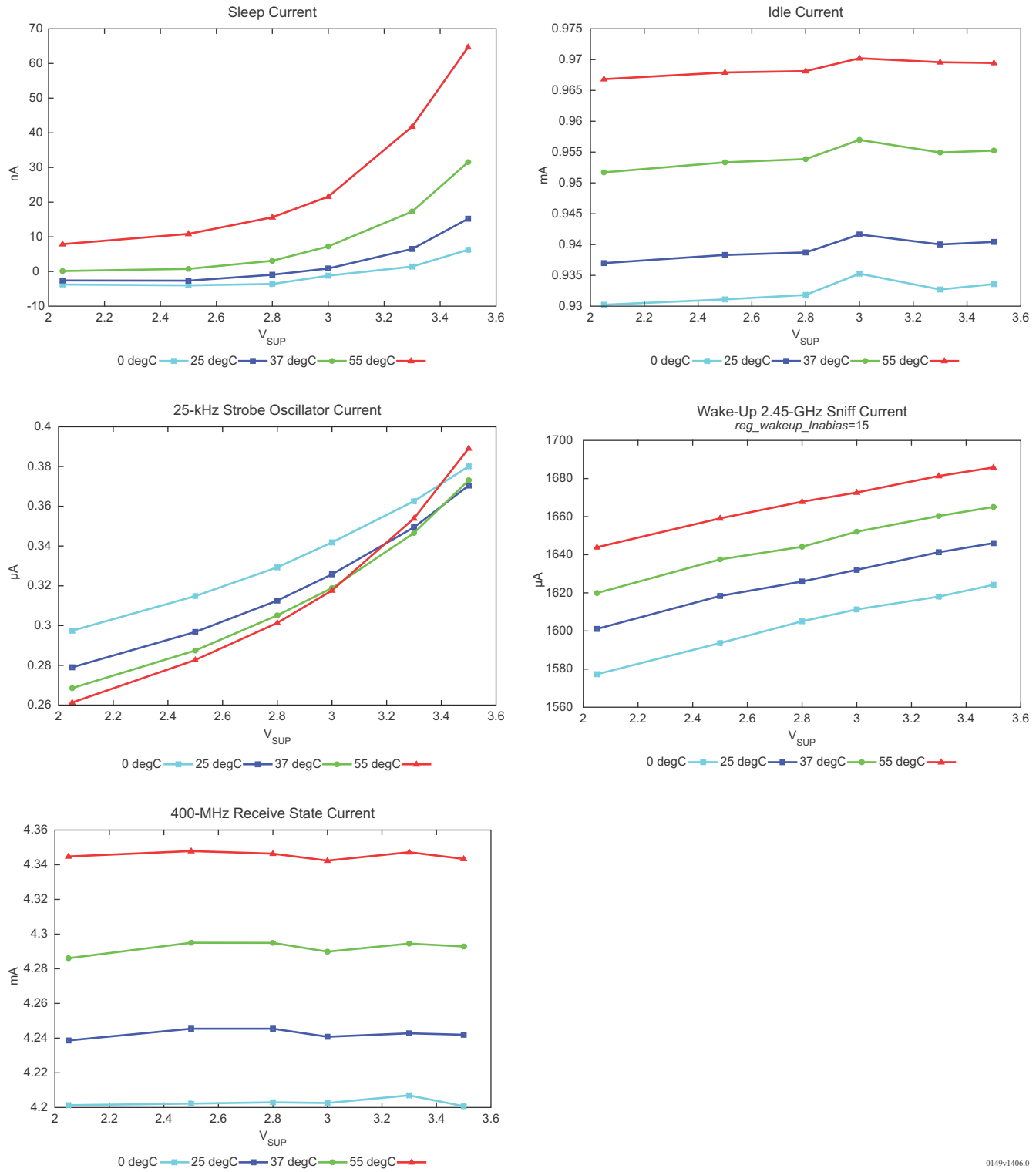


Figure 7-4 • **Typical Performance Graphs**

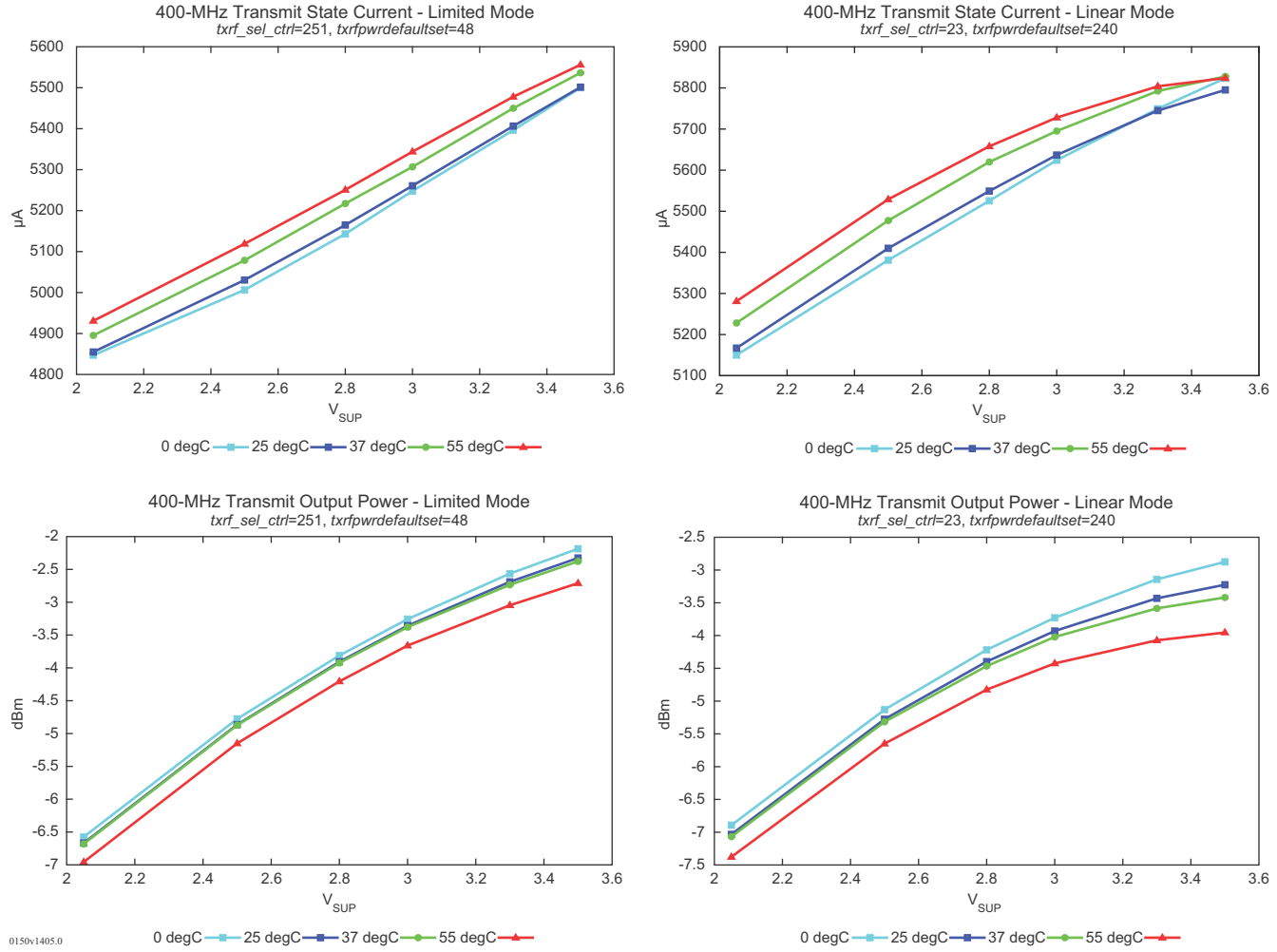


Figure 7-4 • **Typical Performance Graphs (continued)**

8 – Pin List

Proper ground is essential for good and stable performance. Please ensure all ground pins are connected.

Table 8-1 • **ZL70103 Pin List**

Symbol	Bare Die	QFN [1]	CSP	Description	Type	PD [2]	Notes
VSS	1	1, 4 ▣	D1	Common chip ground. Is connected to VSSA and VSSD.			
VDDA	2	2	A1	Analog on-chip regulated power (analog 2V domain)			Note 3
VSUP	3	3	D2	Power supply input (2.05 to 3.5 volts)			
RX_245	4	5	A2	2.45-GHz receiver input (wake-up messages)	5		Note 11
VSSA	5	▣	B3	RF ground for 2.45-GHz receiver			
MATCH1	6	6	A3	Tuning capacitor 1	3		
VSSA	7	7	B3	RF ground for MATCH1 and MATCH2 capacitors			
MATCH2	8	8	A4	Tuning capacitor 2	4		
VSSA	9	▣	C3	General analog ground			
RF_TX	10	10	B4	400-MHz transmitter output	1		
VSSA	11	9 ▣	C5	RF ground for 400-MHz transmitter output			
RF_RX	12	11	B5	400-MHz RF receive LNA input	2		
VSSA	13	12 ▣	C5	RF ground for 400-MHz receiver			
VSSA	14	▣	D4	General analog ground			
NC	15	▣		Reserved pin. Do not use. Do not connect.			
VSSD	16	▣	C6	Digital ground			
VSSD	17	▣	C6	Digital ground			

Notes:

1. *QFN pins denoted by a ▣ are connected to the bottom ground post of the package.*
2. *Pins marked in this column can be controlled by the PDCTRL pin; refer to Note 4 below for details.*
3. *VDDA and VDDD pins provide access to the regulated side of the analog and digital voltage regulators, respectively. These pins are needed to provide an external capacitor to the built-in regulator. These pins are sensitive to external noise.*
4. *Digital pins marked as PD are controlled by the PDCTRL pin. If PDCTRL is 1 these digital inputs are pulled low internally on the chip and have a LOW state. This feature allows for minimal connections for implant applications, thus reducing board space and routing requirements.*
5. *The SPI_SDO is tristated when the device is in the SLEEP state to ensure that other devices may use the SPI bus.*
6. *These output pins are defined low when the device is in the SLEEP state and when SPI_CS_B is 1. Please refer to the "Electrical Characteristics" section on page 7-6 for details on maximum frequency and load for the digital output pins.*
7. *When low, voltage regulators VDDA and VDDD are used (recommended). Use of only VDDA reduces receiver performance and is therefore NOT recommended.*
8. *This pad is available only on the bare-die version of the chip. The two VDDA pads are hardwired together on chip so only one of these pads is required to be bonded. It is recommended to bond only pad 2.*
9. *HK messages are by default disabled when MODE1 is 0 and enabled when MODE1 is 1. The default state can be changed with register settings.*
10. *MODE0 should be tied low for normal operation. Test modes (where MODE0 is 1) are intended only for Microsemi internal use.*
11. *Testing of the 2.45-GHz wake-up receiver (RX_245 pin) is limited on QFN devices and, therefore, its operation and/or specifications are not guaranteed.*

Table 8-1 • **ZL70103 Pin List (continued)**

Symbol	Bare Die	QFN [1]	CSP	Description	Type	PD [2]	Notes
VSSA	18	13 ▣	D6	RF ground for VCO			
TESTIO5	19	14	D7	Analog test bus pin 5	6		
TESTIO6	20	15	E6	Analog test bus pin 6	6		
NC	21	16	E7	Reserved pin. Do not use. Do not connect.			
NC	22			Reserved pin. Do not use. Do not connect.			
NC	23	17	F7	Reserved pin. Do not use. Do not connect.			
VSSA	24	▣	F6	General analog ground			
VSSA	25	▣	F6	General analog ground			
VSSA	26	18 ▣	G6	RF ground for crystal oscillator (XO)			
XTAL1	27	19	G7	Connection to the reference frequency crystal. The chip can also use an external XO connected to XTAL1 (controlled by XO_BYPASS).	12		
XTAL2	28	20	H7	Connection to the reference frequency crystal	12		
TESTIO1	29	21	H6	Analog test bus pin 1	6		
TESTIO2	30	22	I6	Analog test bus pin 2	6		
TESTIO3	31	23	I7	Analog test bus pin 3	6		
TESTIO4	32	24	F4	Analog test bus pin 4	6		
VSSD	33	▣	F3	Digital ground			
VSSD	34	▣	F3	Digital ground			
IRQ	35	25	J7	Interrupt request	11		
VSSD	36	▣	F3	Digital ground			
WU_EN	37	26	J6	Wake-up enable signal used for strobing the wake-up LNA	7		

Notes:

1. *QFN pins denoted by a ▣ are connected to the bottom ground post of the package.*
2. *Pins marked in this column can be controlled by the PDCTRL pin; refer to Note 4 below for details.*
3. *VDDA and VDDD pins provide access to the regulated side of the analog and digital voltage regulators, respectively. These pins are needed to provide an external capacitor to the built-in regulator. These pins are sensitive to external noise.*
4. *Digital pins marked as PD are controlled by the PDCTRL pin. If PDCTRL is 1 these digital inputs are pulled low internally on the chip and have a LOW state. This feature allows for minimal connections for implant applications, thus reducing board space and routing requirements.*
5. *The SPI_SDO is tristated when the device is in the SLEEP state to ensure that other devices may use the SPI bus.*
6. *These output pins are defined low when the device is in the SLEEP state and when SPI_CS_B is 1. Please refer to the "Electrical Characteristics" section on page 7-6 for details on maximum frequency and load for the digital output pins.*
7. *When low, voltage regulators VDDA and VDDD are used (recommended). Use of only VDDA reduces receiver performance and is therefore NOT recommended.*
8. *This pad is available only on the bare-die version of the chip. The two VDDA pads are hardwired together on chip so only one of these pads is required to be bonded. It is recommended to bond only pad 2.*
9. *HK messages are by default disabled when MODE1 is 0 and enabled when MODE1 is 1. The default state can be changed with register settings.*
10. *MODE0 should be tied low for normal operation. Test modes (where MODE0 is 1) are intended only for Microsemi internal use.*
11. *Testing of the 2.45-GHz wake-up receiver (RX_245 pin) is limited on QFN devices and, therefore, its operation and/or specifications are not guaranteed.*

Table 8-1 • **ZL70103 Pin List (continued)**

Symbol	Bare Die	QFN [1]	CSP	Description	Type	PD [2]	Notes
SPI_CS_B	38	27	I5	SPI chip select (active low)	9		
VSSD	39	28 ▣	F3	Digital ground			
PDCTRL	40	29	J5	Pull-down control for digital inputs marked with PD in this table	7		Note 4
VSSD	41	30 ▣	F3	Digital ground			
SPI_CLK	42	31	I4	SPI serial clock	9		
SPI_SDO	43	32	J4	SPI serial data out	10		Note 5
VSSD	44	▣	F3	Digital ground			
PO4	45			Programmable digital output 4	11		Note 6
SPI_SDI	46	33	J3	SPI serial data In	9		
VDDIO	47	34	I3	Digital I/O supply (acceptable range: 1.5V to VSUP)			
VSSD	48	▣	J2	Digital ground			
VREG_MODE	49	▣	G4	Voltage regulator selection of *either* VDDA *or* VDDA and VDDD (VREG_MODE = 0 for VDDA and VDDD, recommended)	7		Note 7
VDDD	50	35	J1	Digital on-chip regulated power (digital 2V domain)			Note 3
VSSD	51	36 ▣	F3	Digital ground			
VSSD	52	▣	F3	Digital ground			
MODE1	53	37	I2	Controls whether HK messages can write to registers (set low for normal operation)	8	X	Notes 4, 9
MODE0	54	38	I1	Test mode selection pin (set low for normal operation)	8	X	Notes 4, 10
VSSD	55	▣	F3	Digital ground			
PI2	56	39	H2	Programmable digital input 2	8	X	Note 4

Notes:

1. *QFN pins denoted by a ▣ are connected to the bottom ground post of the package.*
2. *Pins marked in this column can be controlled by the PDCTRL pin; refer to Note 4 below for details.*
3. *VDDA and VDDD pins provide access to the regulated side of the analog and digital voltage regulators, respectively. These pins are needed to provide an external capacitor to the built-in regulator. These pins are sensitive to external noise.*
4. *Digital pins marked as PD are controlled by the PDCTRL pin. If PDCTRL is 1 these digital inputs are pulled low internally on the chip and have a LOW state. This feature allows for minimal connections for implant applications, thus reducing board space and routing requirements.*
5. *The SPI_SDO is tristated when the device is in the SLEEP state to ensure that other devices may use the SPI bus.*
6. *These output pins are defined low when the device is in the SLEEP state and when SPI_CS_B is 1. Please refer to the "Electrical Characteristics" section on page 7-6 for details on maximum frequency and load for the digital output pins.*
7. *When low, voltage regulators VDDA and VDDD are used (recommended). Use of only VDDA reduces receiver performance and is therefore NOT recommended.*
8. *This pad is available only on the bare-die version of the chip. The two VDDA pads are hardwired together on chip so only one of these pads is required to be bonded. It is recommended to bond only pad 2.*
9. *HK messages are by default disabled when MODE1 is 0 and enabled when MODE1 is 1. The default state can be changed with register settings.*
10. *MODE0 should be tied low for normal operation. Test modes (where MODE0 is 1) are intended only for Microsemi internal use.*
11. *Testing of the 2.45-GHz wake-up receiver (RX_245 pin) is limited on QFN devices and, therefore, its operation and/or specifications are not guaranteed.*

Table 8-1 • **ZL70103 Pin List (continued)**

Symbol	Bare Die	QFN [1]	CSP	Description	Type	PD [2]	Notes
PI1	57	40	H1	Programmable digital input 1	8	X	Note 4
PI0	58	41	G3	Programmable digital input 0	8	X	Note 4
VSSD	59	42 ▣	D1	Digital ground			
PO3	60	43	G1	Programmable digital output 3	11		Note 6
PO2	61	44	G2	Programmable digital output 2	11		Note 6
VSSD	62	▣	D1	Digital ground			
PO1	63	45	F1	Programmable digital output 1	11		Note 6
PO0	64	46	F2	Programmable digital output 0	11		Note 6
VSSD	65	▣	D1	Digital ground			
XO_BYPASS	66	47	E1	Bypass on-chip crystal oscillator circuit and use external oscillator connected to XTAL1	8	X	Note 4
IBS	67	48	E2	Implant/base selection (0 for implant, 1 for base station)	8	X	Note 4
VSSD	68	▣	D1	Digital ground			
VDDA	69			Analog on-chip regulated power (analog 2V domain)			Notes 3, 8
VSSD	70	▣	D1	Digital ground			

Notes:

1. *QFN pins denoted by a ▣ are connected to the bottom ground post of the package.*
2. *Pins marked in this column can be controlled by the PDCTRL pin; refer to Note 4 below for details.*
3. *VDDA and VDDD pins provide access to the regulated side of the analog and digital voltage regulators, respectively. These pins are needed to provide an external capacitor to the built-in regulator. These pins are sensitive to external noise.*
4. *Digital pins marked as PD are controlled by the PDCTRL pin. If PDCTRL is 1 these digital inputs are pulled low internally on the chip and have a LOW state. This feature allows for minimal connections for implant applications, thus reducing board space and routing requirements.*
5. *The SPI_SDO is tristated when the device is in the SLEEP state to ensure that other devices may use the SPI bus.*
6. *These output pins are defined low when the device is in the SLEEP state and when SPI_CS_B is 1. Please refer to the "Electrical Characteristics" section on page 7-6 for details on maximum frequency and load for the digital output pins.*
7. *When low, voltage regulators VDDA and VDDD are used (recommended). Use of only VDDA reduces receiver performance and is therefore NOT recommended.*
8. *This pad is available only on the bare-die version of the chip. The two VDDA pads are hardwired together on chip so only one of these pads is required to be bonded. It is recommended to bond only pad 2.*
9. *HK messages are by default disabled when MODE1 is 0 and enabled when MODE1 is 1. The default state can be changed with register settings.*
10. *MODE0 should be tied low for normal operation. Test modes (where MODE0 is 1) are intended only for Microsemi internal use.*
11. *Testing of the 2.45-GHz wake-up receiver (RX_245 pin) is limited on QFN devices and, therefore, its operation and/or specifications are not guaranteed.*

Pin Types

Table 8-2 • **ZL70103 Pin Type Schematics**

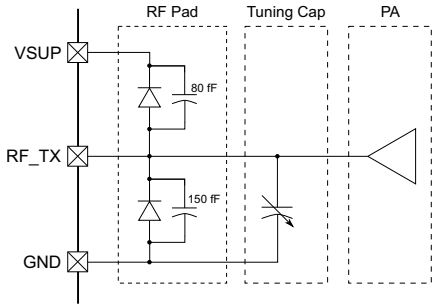
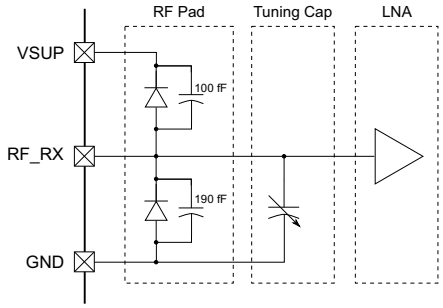
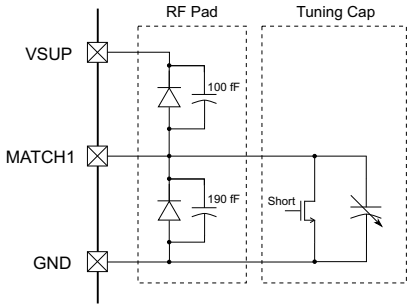
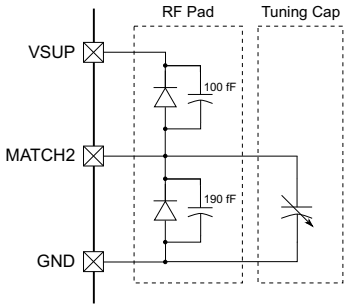
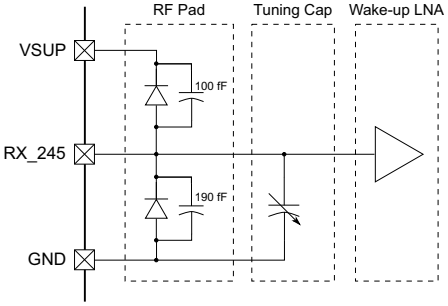
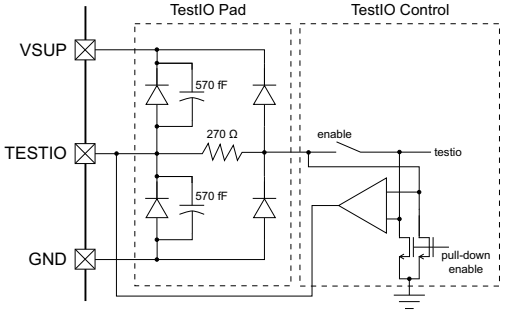
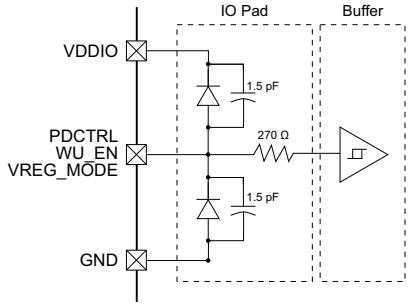
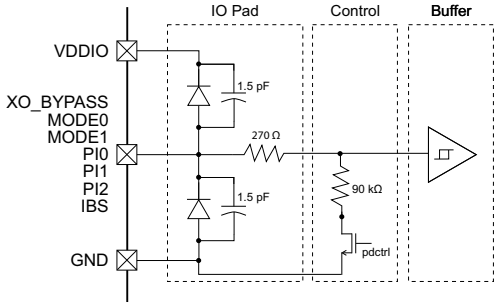
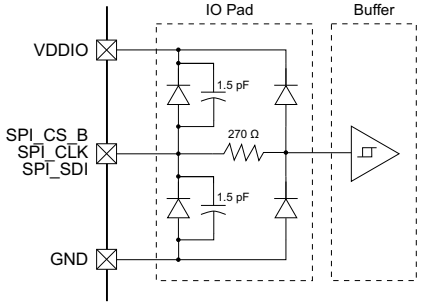
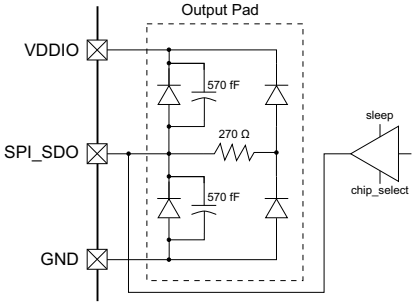
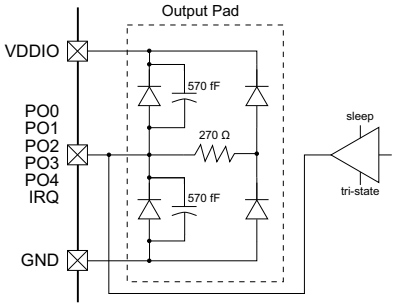
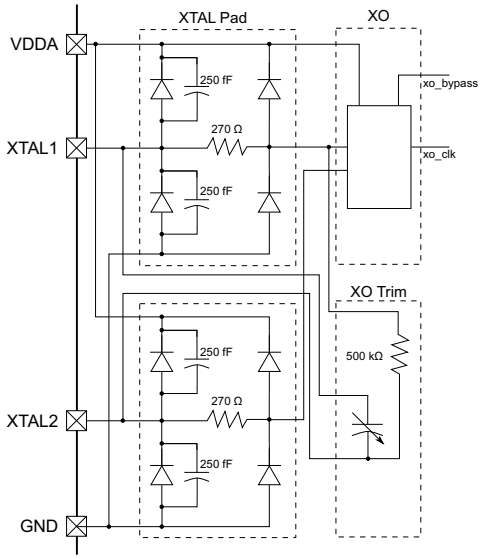
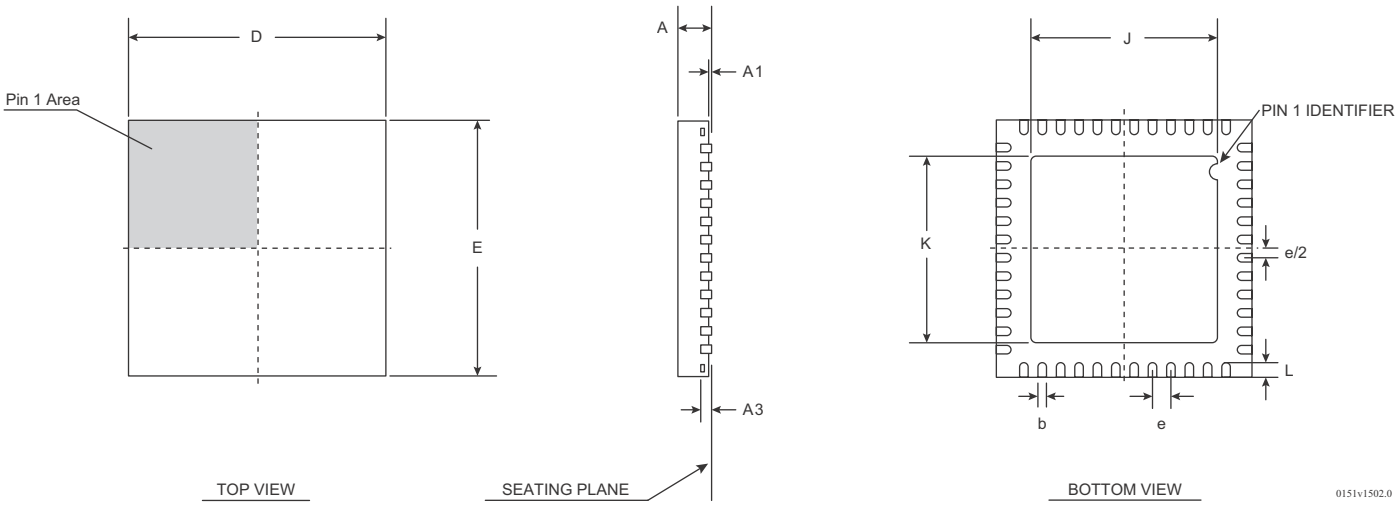
Type	Schematic	Type	Schematic
1		2	
3		4	
5		6	

Table 8-2 • **ZL70103 Pin Type Schematics (continued)**

Type	Schematic	Type	Schematic
7		8	
9		10	
11		12	

9 – Mechanical Reference

48-Pin QFN Package

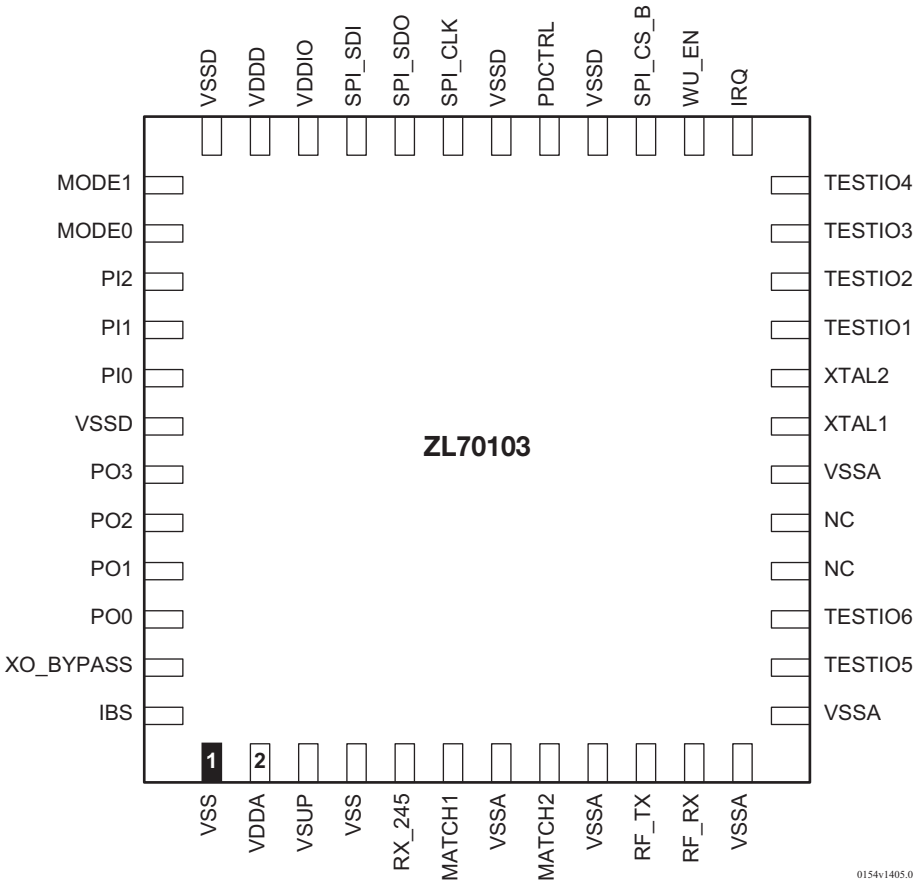


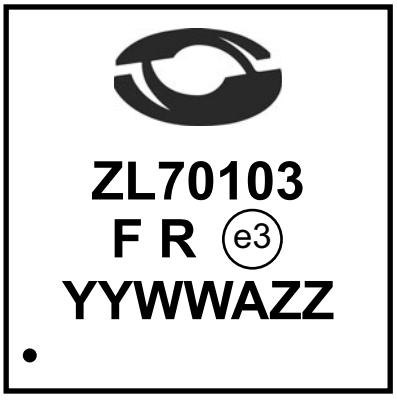
Symbol	Common Dimensions		
	Minimum	Nominal	Maximum
A	0.8	0.9	1.0
A1	0	0.02	0.05
A3		0.2	
b	0.18	0.20	0.30
D		7.00	
E		7.00	
e		0.5	
J	5.0	5.1	5.2
K	5.0	5.1	5.2
L	0.30	0.40	0.50

Notes:

1. *Dimensioning and tolerances conform to ASME Y14.5M. – 1994.*
2. *All dimensions are in millimeters.*
3. *Not to scale.*

Figure 9-1 • **Package Drawing and Package Dimensions for 48-Pin QFN**





Notes:

1. *YY = Last two digits of year of encapsulation*
2. *WW = Week number of encapsulation*
3. *ZZ = Assembly lot sequence code*
4. *A = Assigned Assembly Site Identifier*
5. *F = Fab code*
6. *R = Product revision code*
7. *e3 = Denotes Pb-free*

Figure 9-2 • **Footprint (top view) and Markings for 48-Pin QFN**

49-Pin CSP Package

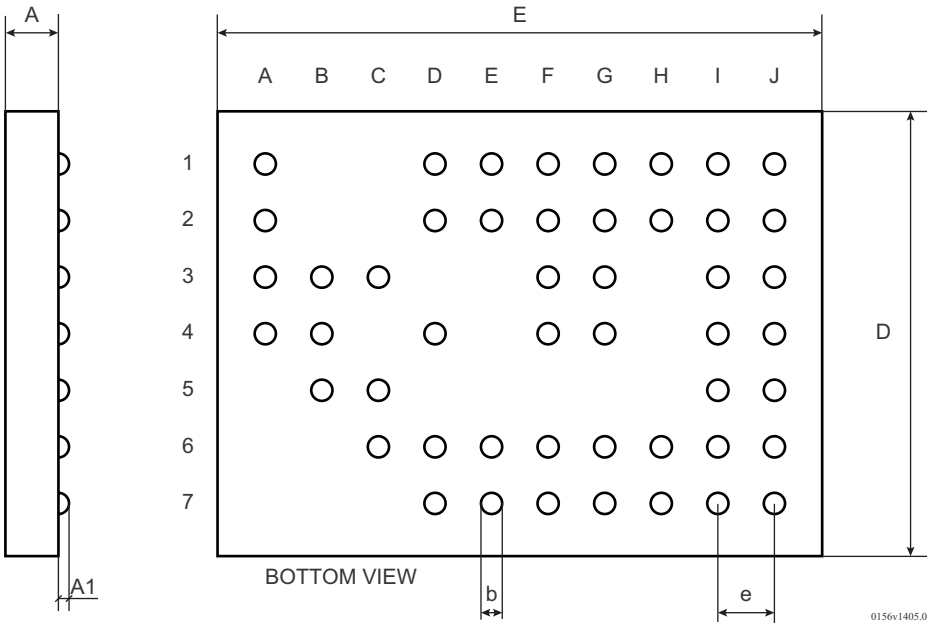


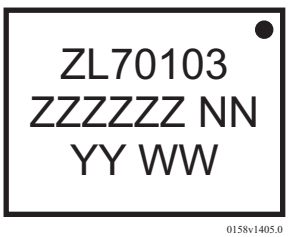
Figure 9-3 • **Package Drawing of 49-Pin CSP**

Table 9-1 • **Package Dimensions for 49-Pin CSP**

Symbol	Common Dimensions (mm)		
	Minimum	Nominal	Maximum
A	0.225	0.250	0.275
A1	0.115	0.130	0.145
b [1]		0.150	
D	3.025	3.040	3.075
E	4.155	4.170	4.205
N	49		
e	0.40 BSC		

Note:

1. UBM diameter



Notes:

1. *ZZZZZZ = Lot number*
2. *NN = Wafer ID*
3. *YY = Calendar year*
4. *WW = Calendar week*
5. *Orientation marker corresponds to pin A1*

Figure 9-4 • **Markings for 49-Pin CSP**

Bump Coordinates for 49-Pin CSP, Given in µm from Chip Center

Table 9-2 • Bump Locations for 49-Pin CSP

Bump	X	Y	Symbol	Bump	X	Y	Symbol
A1	−1791.87	1200	VDDA	G1	608.13	1200	PO3
A2	−1791.87	800	RX_245	G2	608.13	800	PO2
A3	−1791.87	400	MATCH1	G3	608.13	400	PI0
A4	−1791.87	0	MATCH2	G4	608.13	0	VREG_MODE
B3	−1391.87	400	VSSA	G6	608.13	−800	VSSA
B4	−1391.87	0	RF_TX	G7	608.13	−1200	XTAL1
B5	−1391.87	−400	RF_RX	H1	1008.13	1200	PI1
C3	−991.87	400	VSSA	H2	1008.13	800	PI2
C5	−991.87	−400	VSSA	H6	1008.13	−800	TESTIO1
C6	−991.87	−800	VSSD	H7	1008.13	−1200	XTAL2
D1	−591.87	1200	VSS	I1	1408.13	1200	MODE0
D2	−591.87	800	VSUP	I2	1408.13	800	MODE1
D4	−591.87	0	VSSA	I3	1408.13	400	VDDIO
D6	−591.87	−800	VSSA	I4	1408.13	0	SPI_CLK
D7	−591.87	−1200	TESTIO5	I5	1408.13	−400	SPI_CS_B
E1	−191.87	1200	XO_BYPASS	I6	1408.13	−800	TESTIO2
E2	−191.87	800	IBS	I7	1408.13	−1200	TESTIO3
E6	−191.87	−800	TESTIO6	J1	1808.13	1200	VDDD
E7	−191.87	−1200	NC	J2	1808.13	800	VSSD
F1	208.13	1200	PO1	J3	1808.13	400	SPI_SDI
F2	208.13	800	PO0	J4	1808.13	0	SPI_SDO
F3	208.13	400	VSSD	J5	1808.13	−400	PDCTRL
F4	208.13	0	TESTIO4	J6	1808.13	−800	WU_EN
F6	208.13	−800	VSSA	J7	1808.13	−1200	IRQ
F7	208.13	−1200	NC				

Bare Die

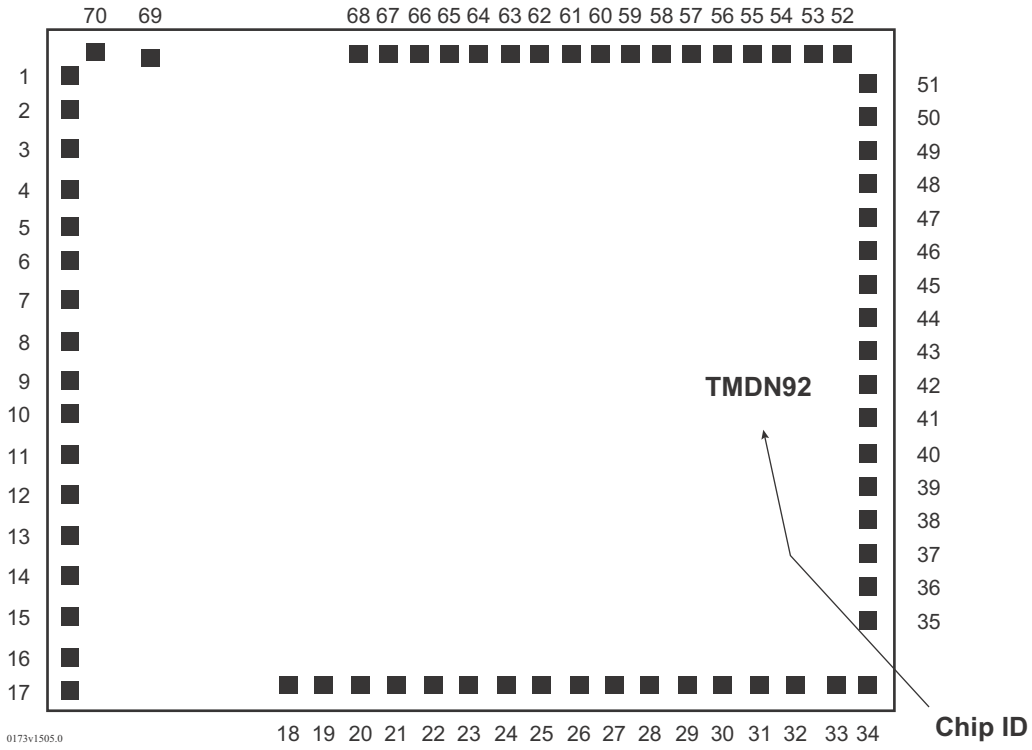


Figure 9-5 • **Pad Locations for Bare Die**

Table 9-3 • **Dimensions for Bare Die**

Parameter		Unit	Notes
Die area (x, y)	4205 × 3075	µm	Maximum size
Die thickness	250 ± 25	µm	
Pad size	80 × 80	µm	
Pad metal	Al/Cu		
Backside potential	GND		

Pad Coordinates for Bare Die, Given in µm from Chip Center

Table 9-4 • **Pad Coordinates for Bare Die**

Pad	X	Y	Bond Pad Name	Pad	X	Y	Bond Pad Name
1	−1971	1323	VSS	36	1986	−966	VSSD
2	−1971	1173	VDDA	37	1986	−816	WU_EN
3	−1971	993	VSUP	38	1986	−666	SPI_CS_B
4	−1971	813	RX_245	39	1986	−516	VSSD
5	−1971	644	VSSA	40	1986	−366	PDCTRL
6	−1971	494	MATCH1	41	1986	−216	VSSD
7	−1971	314	VSSA	42	1986	−66	SPI_CLK
8	−1971	134	MATCH2	43	1986	84	SPI_SDO
9	−1971	−46	VSSA	44	1986	234	VSSD
10	−1971	−197	RF_TX	45	1986	384	PO4
11	−1971	−377	VSSA	46	1986	534	SPI_SDI
12	−1971	−557	RF_RX	47	1986	684	VDDIO
13	−1971	−737	VSSA	48	1986	834	VSSD
14	−1971	−917	VSSA	49	1986	984	VREG_MODE
15	−1971	−1105	NC	50	1986	1134	VDDD
16	−1971	−1283	VSSD	51	1986	1284	VSSD
17	−1971	−1433	VSSD	52	1862	1421	VSSD
18	−890	−1406	VSSA	53	1712	1421	MODE1
19	−710	−1406	TESTIO5	54	1562	1421	MODE0
20	−530	−1406	TESTIO6	55	1412	1421	VSSD
21	−350	−1406	NC	56	1262	1421	PI2
22	−170	−1406	NC	57	1112	1421	PI1
23	10	−1406	NC	58	962	1421	PI0
24	190	−1406	VSSA	59	812	1421	VSSD
25	370	−1406	VSSA	60	662	1421	PO3
26	550	−1406	VSSA	61	512	1421	PO2
27	730	−1406	XTAL1	62	362	1421	VSSD
28	910	−1406	XTAL2	63	212	1421	PO1
29	1090	−1406	TESTIO1	64	62	1421	PO0
30	1270	−1406	TESTIO2	65	−88	1421	VSSD
31	1450	−1406	TESTIO3	66	−238	1421	XO_BYPASS
32	1630	−1406	TESTIO4	67	−388	1421	IBS
33	1832	−1406	VSSD	68	−538	1421	VSSD
34	1986	−1406	VSSD	69	−1570	1398	VDDA
35	1986	−1116	IRQ	70	−1845	1427	VSSD

10 – Typical Application Examples

Three typical application examples are presented in this chapter with schematics: two different examples using implants and one example using an external device (base station). Matching networks have to be adopted to the applicable antenna impedance. Please refer to the ZL70103 ADK for more information.

Ultra-Low-Power Implant Device

This implementation has full focus on reducing power consumption. This reduction is achieved by using the ultra-low-power 2.45-GHz wake-up system that provides by far the lowest power consumption. The 2.45-GHz wake-up system is also autonomous and fully integrated. Using the 2.45-GHz wake-up system requires a more complex implementation both on the implant side and on the base station side.

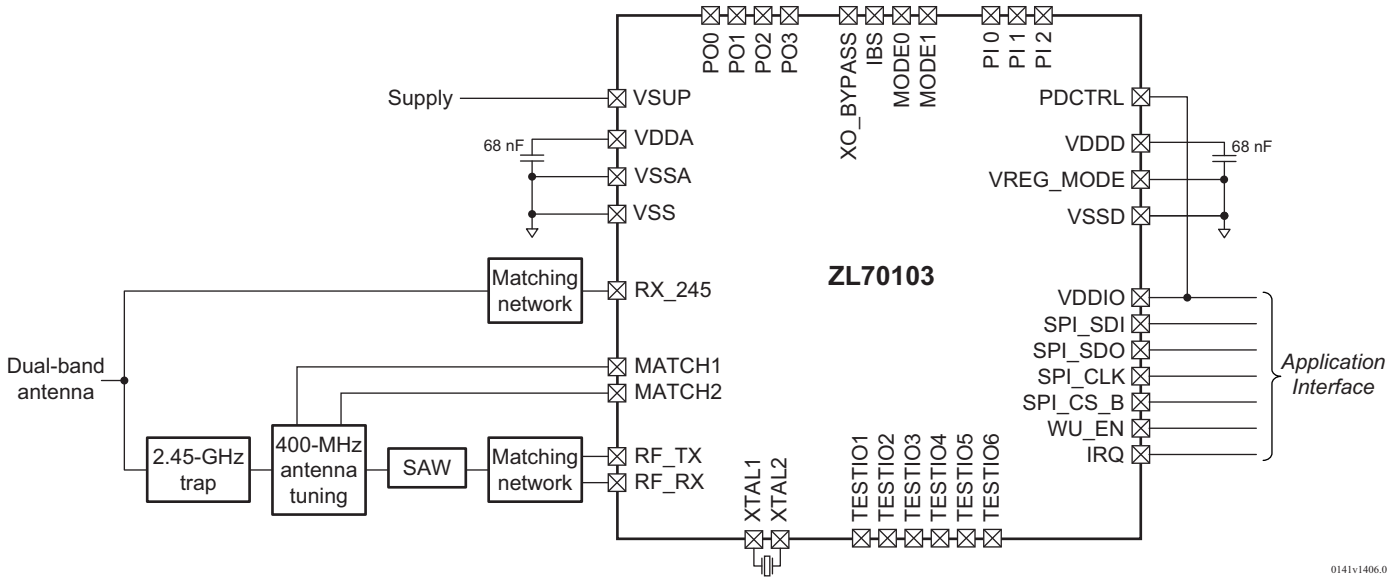


Figure 10-1 • **Ultra-Low-Power Implant Device**

Low-Power Implant Device

This implementation uses the in-band 400-MHz wake-up system to allow for a simpler hardware implementation but with the drawbacks of a higher average power consumption and of a higher burden on the implant host processor because parts of the wake-up control have to be implemented in the host processor firmware.

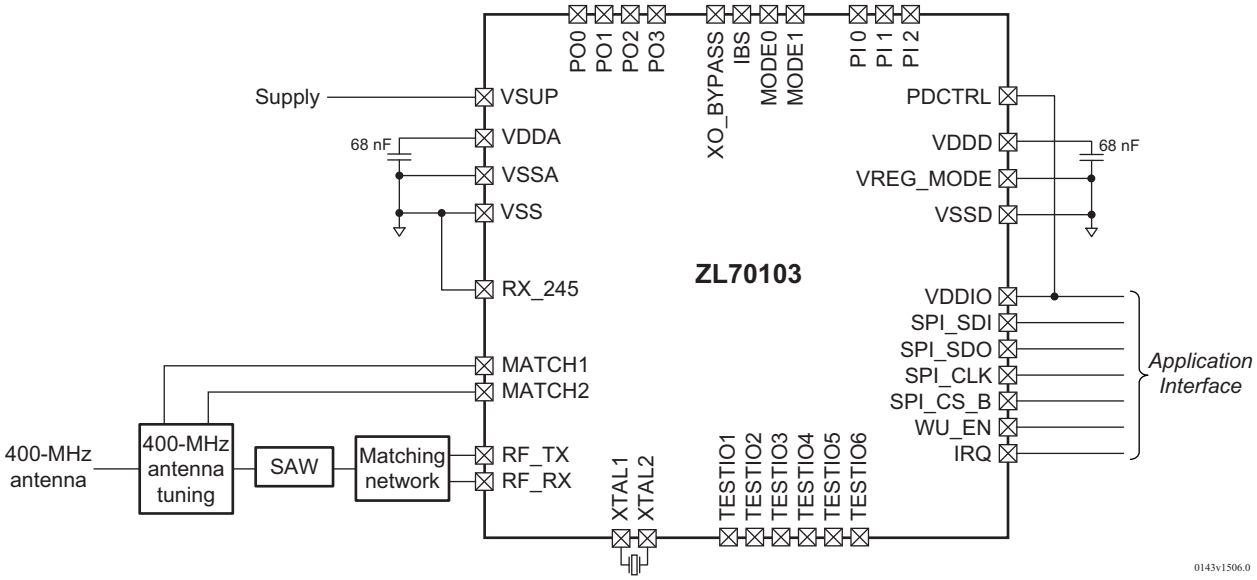


Figure 10-2 • **Low-Power Implant Device**

External Device

The external device (base station) has less stringent power supply requirements compared to the implant devices, but more effort is required regarding transmitter output power control and unwanted emissions to ensure that the regulatory requirements are met. The schematic in Figure 10-3 shows support for the use of the 2.45-GHz wake-up system. If the in-band 400-MHz wake-up system is used, the 2.45-GHz transmitter and antenna can be omitted.

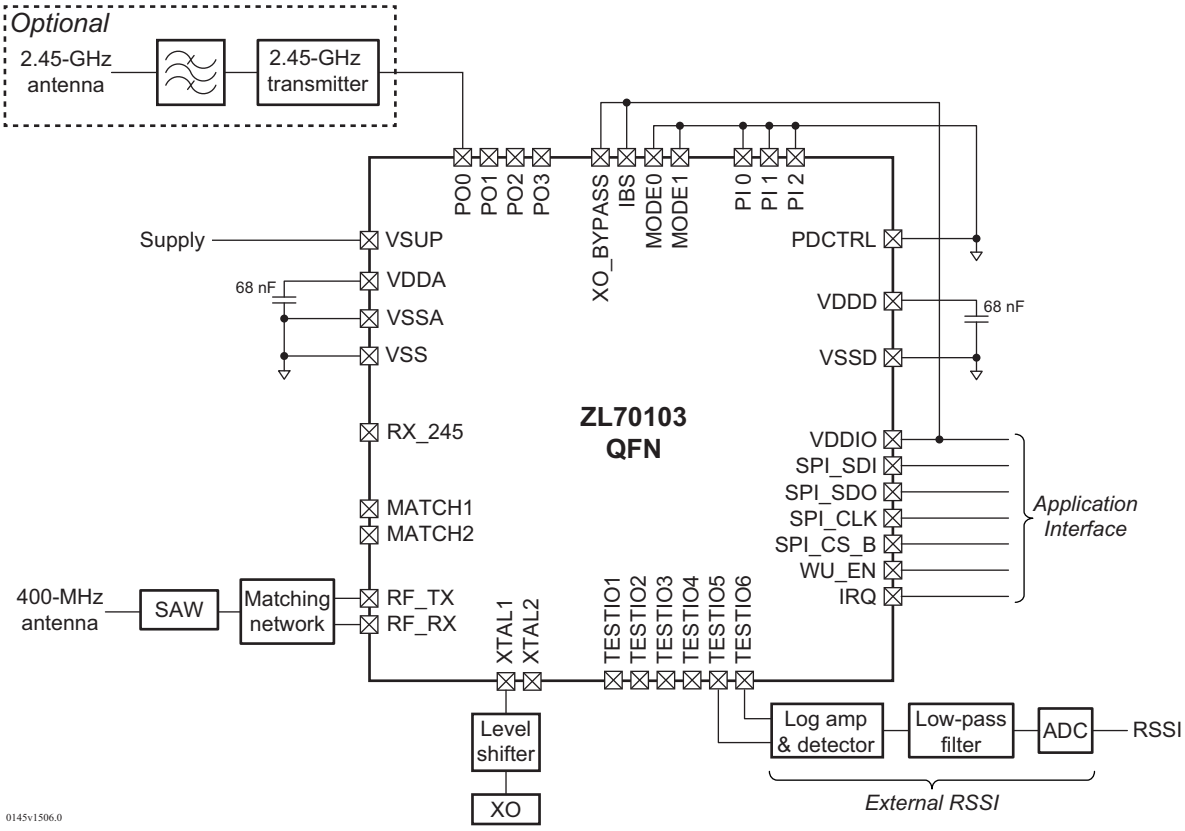


***Figure 10-3* • External Device**

Note: A crystal may be used with the internal oscillator with external load capacitors and then fine-tuned with the internal capacitor to achieve a very tight initial frequency tolerance.

Note: This feature is not tested on the QFN package for the ZL70103 since the QFN is intended for external applications only (for example, base station, programmer, patient controller, or bedside monitoring).

11 – Quality

The ZL70103 can be delivered in a bare-die, CSP, or QFN package; please refer to chapter "2 – Ordering and Package Overview" on page 2-1 for further details.

The bare die and CSP are intended for implantable applications. The QFN package is intended for base station applications and for nonimplantable applications. It is not approved for use in implantable products.

For all versions of the product, manufacturing processes are carried out in ISO9001-approved facilities and all products are fully tested and qualified to ensure conformance to this datasheet.

For the implantable products, the following additional stages are implemented among others:

- Enhanced change notification
  - A comprehensive system of change notification and approval is invoked. No major changes to the product will be made without notification to and/or approval from the customer.
- Wafer lot acceptance testing
  - Each wafer lot is individually assessed to ensure that it is capable of meeting the stringent quality requirements for implantable applications using established quality acceptance requirements and test methods based upon MIL-STD-883 and MIL-PRF-38535.
- Die acceptance testing
  - Every die is individually tested at 37 °C.
  - Every die is visually inspected.
- Enhanced record retention
  - Quality records are retained for the expected duration of production and use of end products.

12 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the ZL70103 Datasheet (149194).

Revision	Changes	Page
Revision 2 (September 2015)	Added RoHS bullet under "Features" heading and removed final bullet under "Applications" heading.	I
	Under "Ordering Information" added note for QFN and specified SAC405 for CSP and modified parenthetical information as to which products are intended for implants.	I
	Modified Figure 1 to correct number of analog inputs.	I
	Modified Table 1.	III
	Modified notes in Table 2-1.	2-1
	Modified Table 3-1 and Table 3-2 to add notes.	3-5
	Modified Figure 3-4 to correct number of TESTIO inputs.	3-6
	Modified Figure 3-5 to label bracket.	3-9
	Added note under "2.45-GHz Wake-Up Receiver".	3-9
	Modified Table 7-1 to: • Remove minimum limit for supply voltage. • Add rows for digital I/O voltage, analog I/O voltage, XTAL I/O voltage, RF I/O voltage, and electrostatic discharge. • Add and modify notes.	7-1
	Modified Table 7-10 to modify notes.	7-6
	Under "Digital Interface" added VREG_MODE, IBS, and XTAL2 to lists of valid pins.	7-7
	In Table 7-11 modified: • Parameter descriptions. • Digital input limits and XTAL1 input limits. • Notes.	7-7
	Modified Table 7-13 to: • Remove redundancies.	7-9
	Modified Table 7-14 to: • Add note related to 400-MHz average wake-up current.	7-10
	In Table 7-16, changed parameter descriptions for $P_{TX400max}$.	7-11
	In Table 7-17: • Changed parameter descriptions for RX sensitivity (4FSK, 2FSK, 2FSK-fallback, and 2FSK-fallback with Barker spreading).	7-12

Revision	Changes	Page
Revision 2, cont'd	In Table 7-18: • Changed parameter descriptions for RX_245 sensitivity (normal and sensitive modes) • Added note.	7-12
	Modified and added notes in Table 7-22.	7-14
	Added notes in Table 8-1.	8-1
	Replaced Figure 9-1 and Figure 9-2.	9-1 to 9-2
	Changed CSP length, width, and thickness in Table 9-1 and Table 9-3.	9-3 to 9-5
	Changed chip ID in Figure 9-5.	9-5
	Modified Figure 10-1, Figure 10-2, and Figure 10-3.	10-1 to 10-3
	Added "Note" paragraph under "External Device".	10-3
	Minor improvements throughout document to improve readability, clarity, and consistency.	Various
Revision 1 (July 2014)	Initial release	All

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com
Web: www.microsemi.com

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