CDCVF2310 2.5-V to 3.3-V High-Performance Clock Buffer

1 Features

- High-Performance 1:10 Clock Driver
- Operates up to 200 MHz at V_{DD} 3.3 V
- Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V
- V_{DD} Range: 2.3 V to 3.6 V
- Operating Temperature Range –40°C to 105°C
- Supports 105ºC Ambient Temperature (see *Thermal Considerations*)
- Output Enable Glitch Suppression
- Distributes One Clock Input to Two Banks of Five Outputs
- 25-Ω On-Chip Series Damping Resistors
- Packaged in 24-Pin TSSOP

2 Applications

- General-Purpose Applications

3 Description

The CDCVF2310 device is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

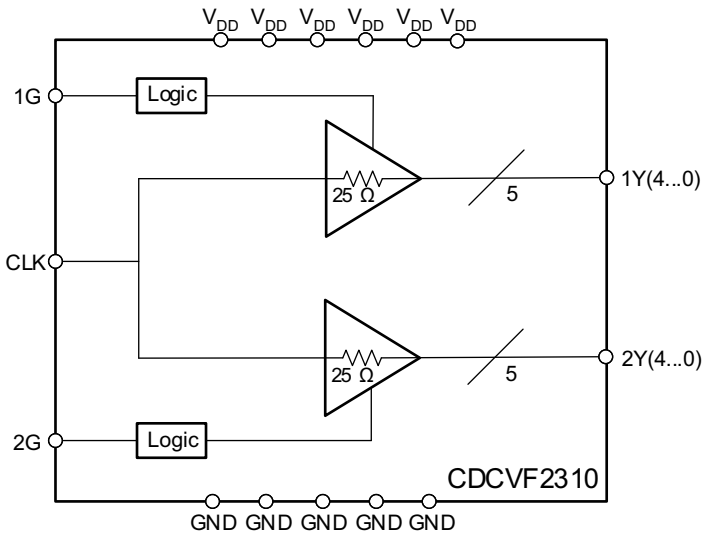
The CDCVF2310 is characterized for operation from –40°C to 85°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCVF2310	TSSOP (24)	4.40 mm × 7.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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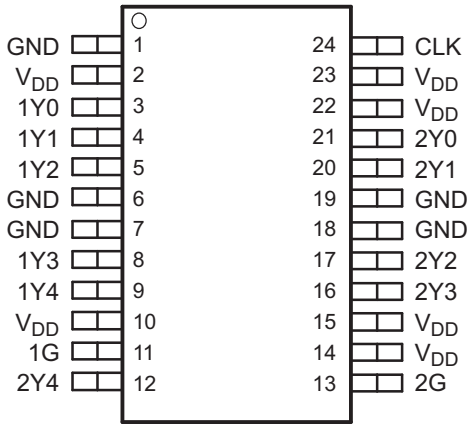
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2008) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19	—	Ground
V_{DD}	2, 10, 14, 15, 22, 23	—	DC power supply, 2.3 V – 3.6 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	4.6	V
V_I(2) (3)	Input voltage		–0.5	V_{DD} + 0.5	V
V_O(2) (3)	Output voltage		–0.5	V_{DD} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{DD}		±50	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{DD}		±50	mA
I_O	Continuous total output current	V_O = 0 to V_{DD}		±50	mA
T_J	Maximum junction temperature			125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.3	2.5		V
				3.3	3.6	
V_{IL}	Low-level input voltage	V_{DD} = 3 V to 3.6 V			0.8	V
		V_{DD} = 2.3 V to 2.7 V			0.7	
V_{IH}	High-level input voltage	V_{DD} = 3 V to 3.6 V	2			V
		V_{DD} = 2.3 V to 2.7 V	1.7			
V_I	Input voltage		0		V_{DD}	V
I_{OH}	High-level output current	V_{DD} = 3 V to 3.6 V			12	mA
		V_{DD} = 2.3 V to 2.7 V			6	
I_{OL}	Low-level output current	V_{DD} = 3 V to 3.6 V			12	mA
		V_{DD} = 2.3 V to 2.7 V			6	
T_A	Operating free-air temperature		–40		85	°C

(1) Unused inputs must be held high or low to prevent them from floating.

6.4 Thermal Information

THERMAL METRIC (1)		CDCVF2310 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V	I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	µA
I_{DD}	Static device current	CLK = 0 V or V_{DD} , I_O = 0 mA	-40°C to 85°C			80	µA
			≤105°C			100	µA
C_I	Input capacitance	V_{DD} = 2.3 V to 3.6 V	V_I = 0 V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3 V to 3.6 V	V_I = 0 V or V_{DD}		2.8		pF

(1) All typical values are at respective nominal V_{DD}.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD} = 3.3 V ±0.3 V							
V_{OH}	High-level output voltage	V_{DD} = min to max	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V	I_{OH} = –12 mA	2.1			
			I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max	I_{OL} = –100 µA			0.2	V
		V_{DD} = 3 V	I_{OL} = 12 mA			0.8	
			I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V	V_O = 1 V	–28			mA
		V_{DD} = 3.3 V	V_O = 1.65 V		–36		
		V_{DD} = 3.6 V	V_O = 3.135 V			–14	
I_{OL}	Low-level output current	V_{DD} = 3 V	V_O = 1.95 V	28			mA
		V_{DD} = 3.3 V	V_O = 1.65 V		36		
		V_{DD} = 3.6 V	V_O = 0.4 V			14	
V_{DD} = 2.5 V ±0.2 V							
V_{OH}	High-level output voltage	V_{DD} = min to max	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 2.3 V	I_{OH} = –6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = min to max	I_{OL} = 100 µA			0.2	V
		V_{DD} = 2.3 V	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 2.3 V	V_O = 1 V	–17			mA
		V_{DD} = 2.5 V	V_O = 1.25 V		–25		
		V_{DD} = 2.7 V	V_O = 2.375 V			–10	
I_{OL}	Low-level output current	V_{DD} = 2.3 V	V_O = 1.2 V	17			mA
		V_{DD} = 2.5 V	V_O = 1.25 V		25		
		V_{DD} = 2.7 V	V_O = 0.3 V			10	

6.6 Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clk}	Clock frequency	V_{DD} = 3 V to 3.6 V	0	200	MHz
		V_{DD} = 2.3 V to 2.7 V	0	170	

6.7 Jitter Characteristics

Characterized using CDCVF2310 Performance EVM when V_{DD}= 3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER		TEST CONDITIONS	TYP	UNIT
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f_{out} = 30.72 MHz	52	fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz	45	

6.8 Switching Characteristics

V_{DD}= 3.3V ±0.3V (see Figure 2) and over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} t_{PHL}	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.	1.3	2.8	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)			100	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)			250	ps
$t_{sk(pp)}$	Part-to-part skew			500	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 2 V	0.7	2	V/ns
t_f	Fall time (see Figure 3)	V_O = 2 V to 0.4 V	0.7	2	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1		ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1		ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4		ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4		ns

(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

6.9 Switching Characteristics

V_{DD}= 2.5V ±0.2V (see Figure 2) and over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH} t_{PHL}	CLK to Yn	f = 0 MHz to 170 MHz For circuit load, see Figure 2.	1.5	3.5	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)			170	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)			400	ps
$t_{sk(pp)}$	Part-to-part skew			600	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 1.7 V	0.5	1.4	V/ns
t_f	Fall time (see Figure 3)	V_O = 1.7 V to 0.4 V	0.5	1.4	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1		ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1		ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4		ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4		ns

(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

6.10 Typical Characteristics

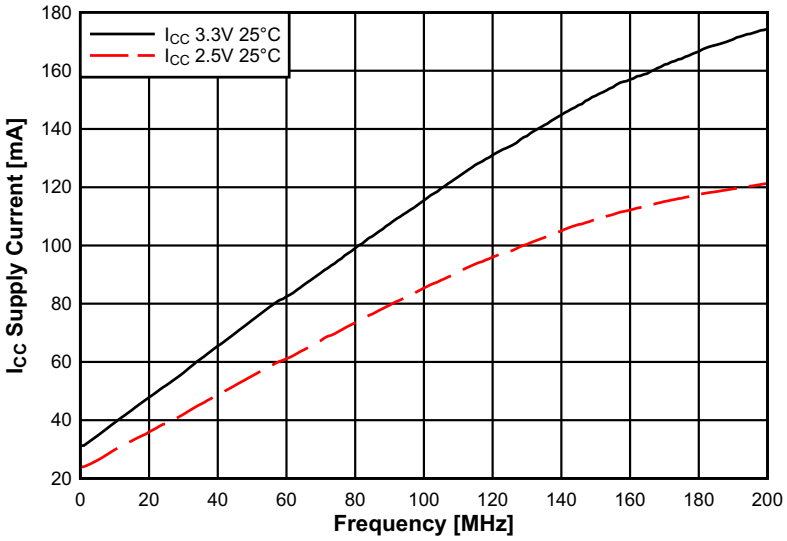
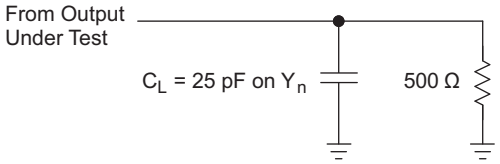


Figure 1. Supply Current vs Frequency

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

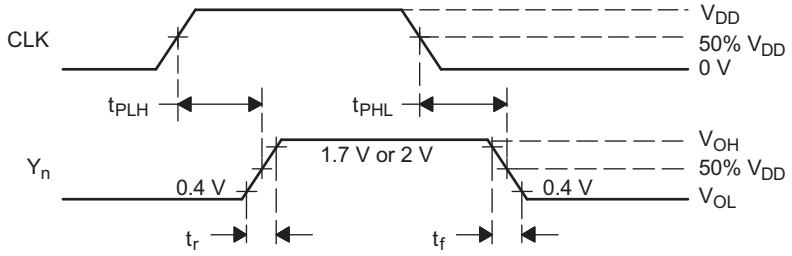


Figure 3. Voltage Waveforms Propagation Delay Times

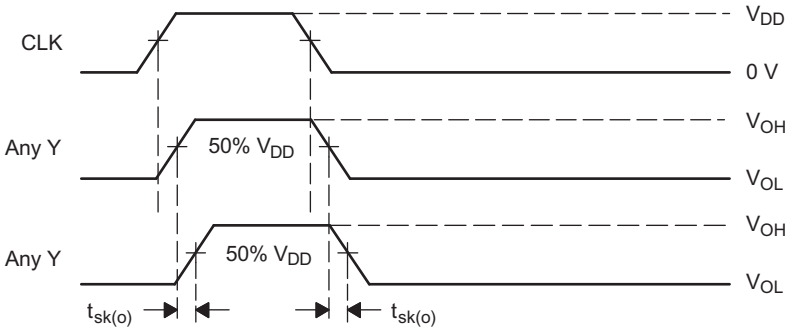
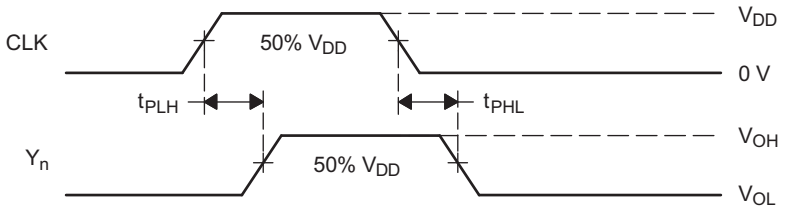


Figure 4. Output Skew



NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

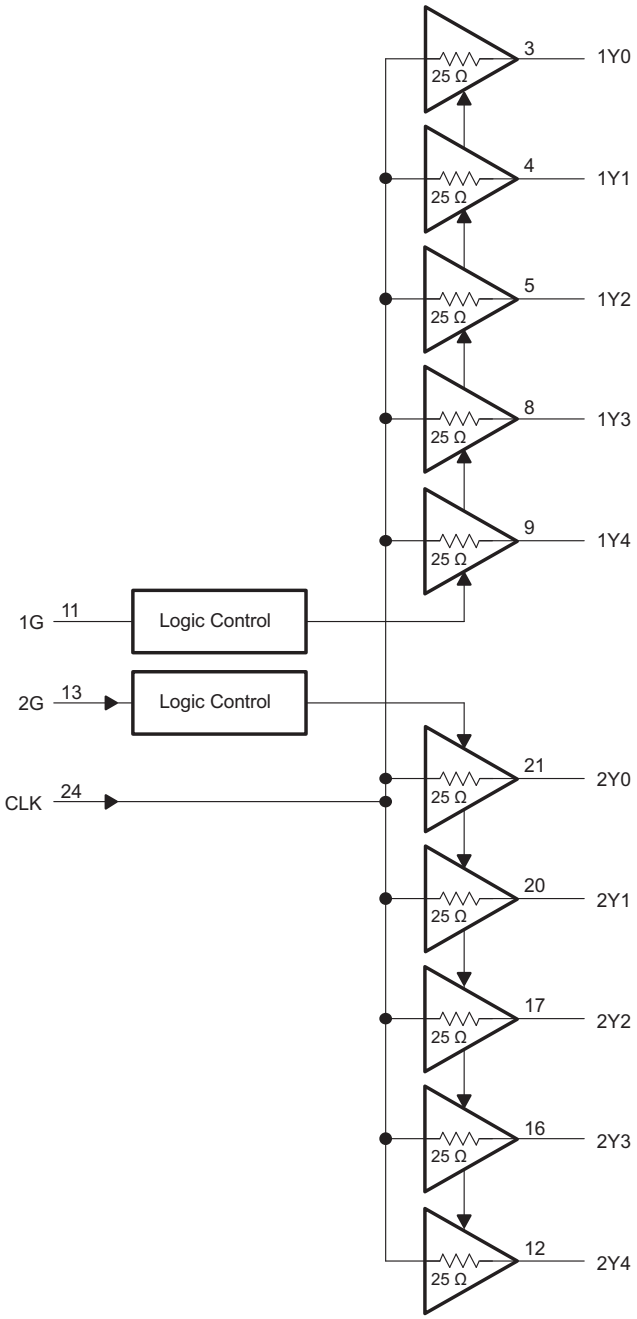
Figure 5. Pulse Skew

8 Detailed Description

8.1 Overview

The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

8.2 Functional Block Diagram

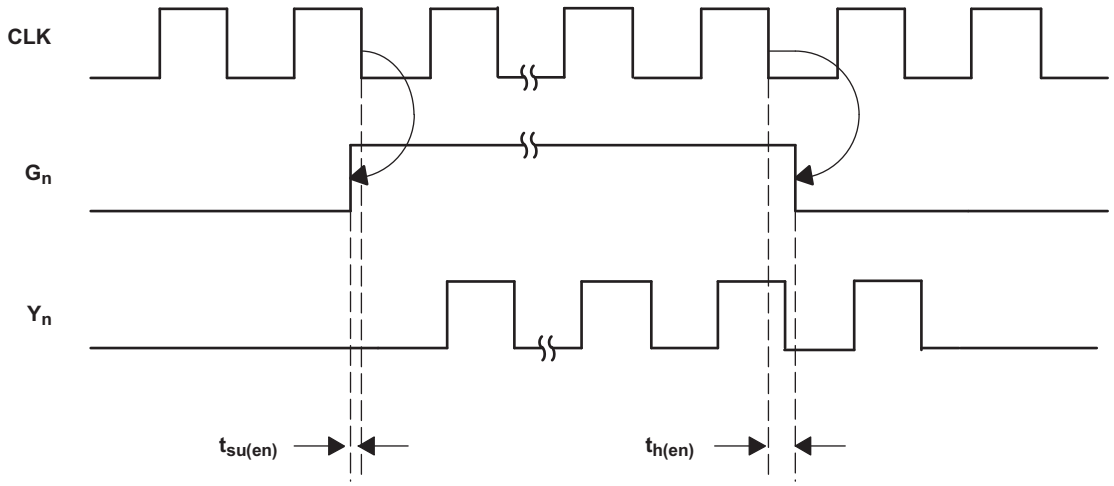


8.3 Feature Description

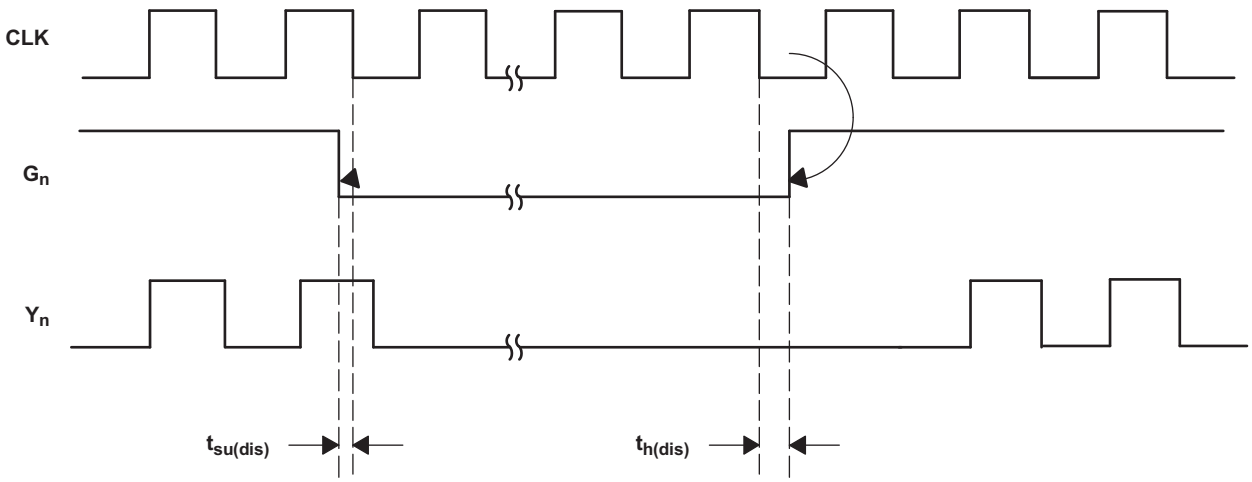
8.3.1 Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 6).

The G input must fulfill the timing requirements (t_{su}, t_h) according to the *Switching Characteristics* table for predictable operation.



a) Enable Mode



b) Disable Mode

Figure 6. Enable and Disable Mode Relative to CLK↓

8.4 Device Functional Modes

Table 1 lists the functional modes for the CDCVF2310.

Table 1. Function Table

INPUT			OUTPUT	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK(1)	L
L	H	↓	L	CLK(1)
H	H	↓	CLK(1)	CLK(1)

(1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCVF2310 is a LVCMOS buffer solution that can operate up to 200 MHz. Low output skew as well as the ability for glitchless output enable and disable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

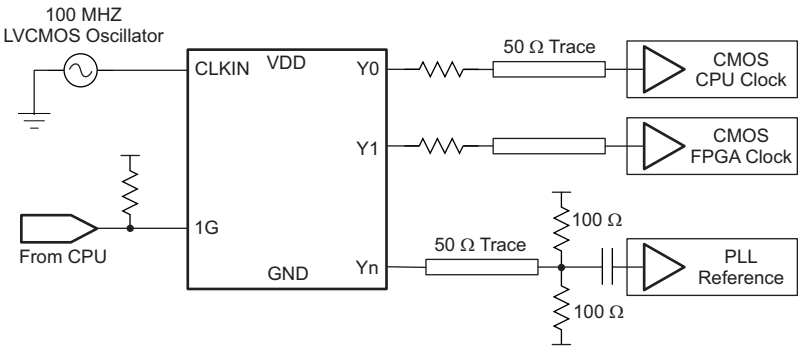


Figure 7. Example System Configuration

9.2.1 Design Requirements

The CDCVF2310 shown in Figure 7 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G.

The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the CDCVF2310 to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the CDCVF2310.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC-coupling can be used when common-mode voltage is mismatched.

9.2.2 Detailed Design Procedure

Refer to *Electrical Characteristics* table to determine the appropriate series resistance needed for matching the output impedance of the CDCVF2310 to that of the characteristic impedance of the transmission line.

Typical Application (continued)

9.2.3 Application Curves

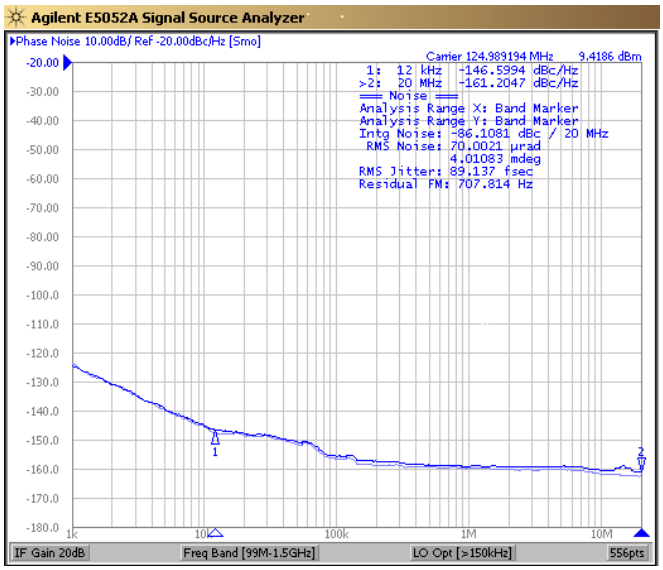


Figure 8. CDCVF2310 Output Phase Noise 89.1 fs (12 kHz to 20 MHz), Reference Phase Noise 76.9 fs, Output Frequency 125 MHz

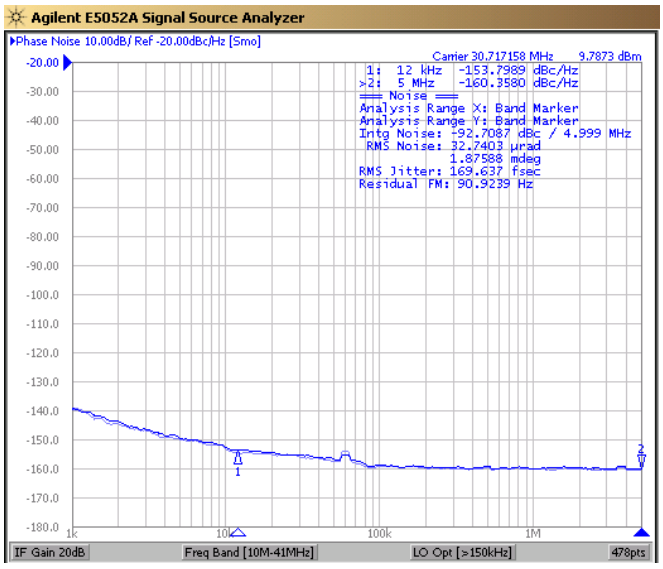


Figure 9. CDCVF2310 Output Phase Noise 169.6 fs (12kHz to 5MHz), Reference Phase Noise 161.5 fs, Frequency 30.72 MHz

The low-additive jitter of the CDCVF2310 can be seen in the previous application plots. The low-noise, 125-MHz input source drives the CDCVF2310, resulting in 45-fs RMS additive jitter when integrated from 12 kHz to 20 MHz for this configuration. The low-noise 30.72-MHz input source drives the CDCVF2310, resulting in 52-fs RMS additive jitter when integrated from 12 kHz to 5 MHz for this configuration.

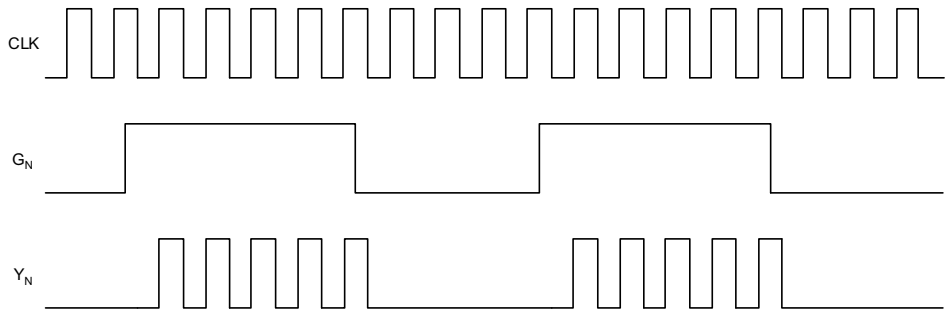


Figure 10. CDCVF2310 Configured as Gate Function for Output Clock

The CDCVF2310 can be configured to generate a gated clock using the G_N Please refer to *Output Enable Glitch Suppression Circuit* for required timings.

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1 µF) bypass capacitors, as there are supply terminals in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 12 shows this recommended power supply decoupling method.

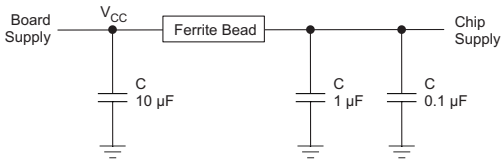


Figure 11. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

Figure 12 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example

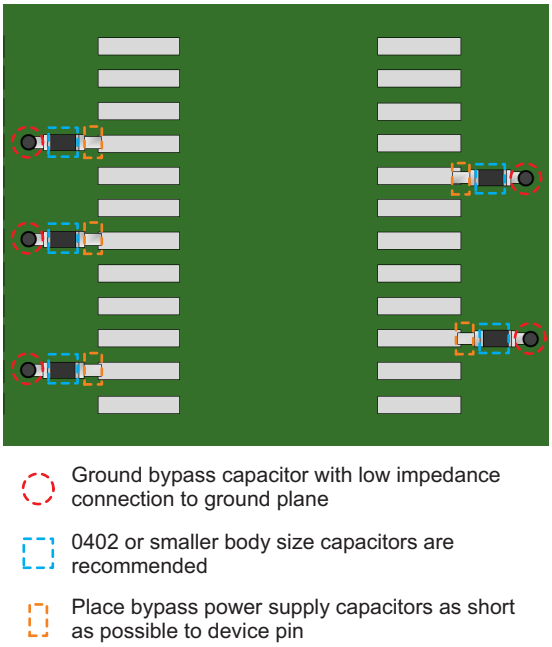


Figure 12. PCB Conceptual Layout

11.3 Thermal Considerations

CDCVF2310 supports high ambient temperature up to 105°C. The system designer needs to ensure that the maximum junction temperature is not exceeded. Following Equation 1 can be used to calculate the junction temperature based on the measured case temperature. The case temperature is defined as the hottest temperature on the top of the device. The case temperature measurement can be performed with (in order of accuracy) an IR camera, a fluor-optic probe, a thermocouple, or IR gun with a maximum field view of 4-mm diameter just to name a few techniques. Further information can be found at SPRA953 and SLUA566

$$T_{junction} = T_{case} + (\psi_{tj} \times Power) \quad (1)$$

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Using Thermal Calculation Tools for Analog Components, SLUA566

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2310PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV2310	Samples
CDCVF2310PWG4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV2310	Samples
CDCVF2310PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV2310	Samples
CDCVF2310PWRG4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV2310	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CDCVF2310 :

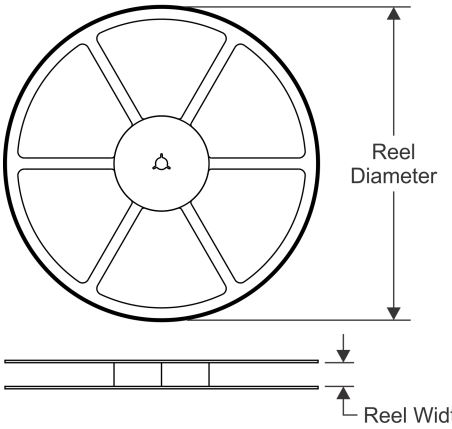
- Enhanced Product: CDCVF2310-EP

NOTE: Qualified Version Definitions:

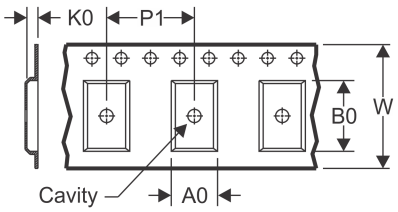
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

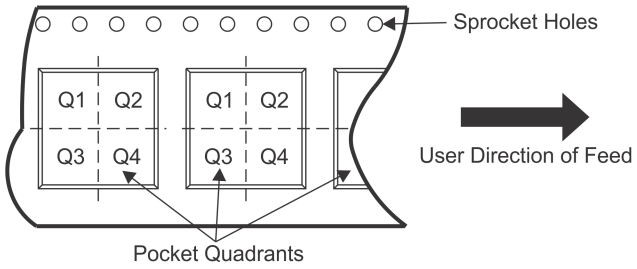


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

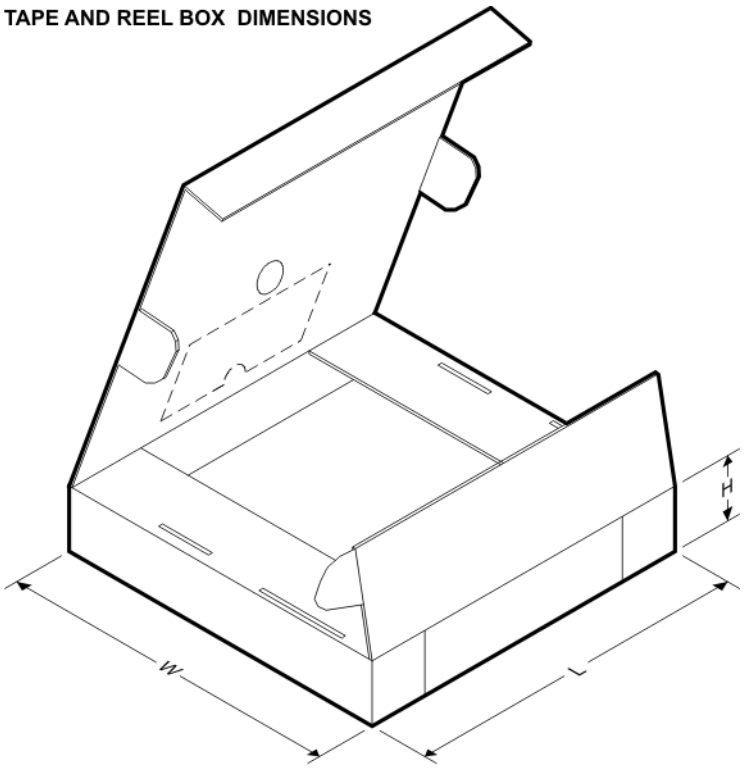
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2310PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

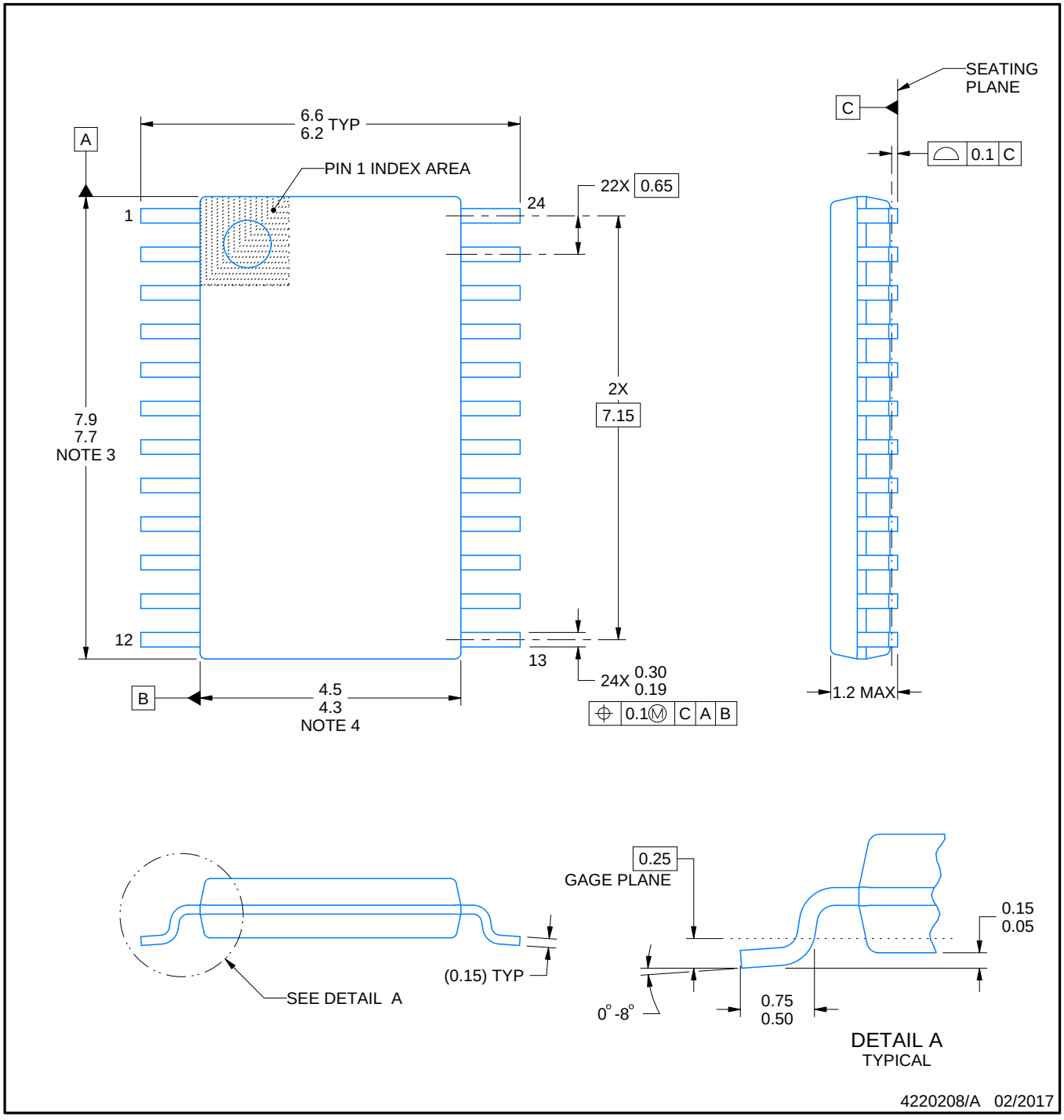
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2310PWR	TSSOP	PW	24	2000	853.0	449.0	35.0

PACKAGE OUTLINE

PW0024A

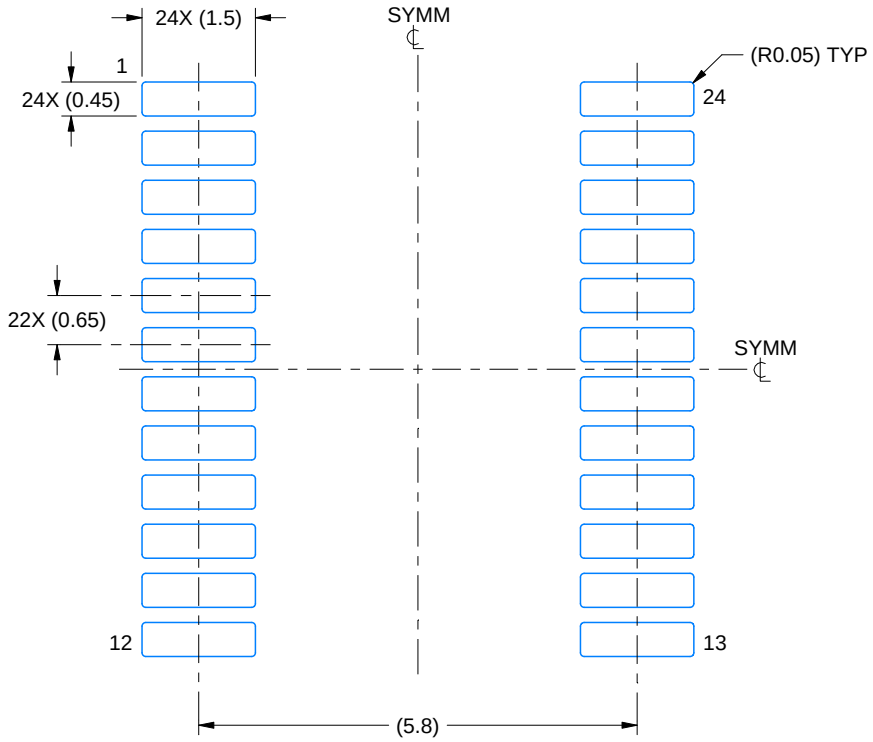
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

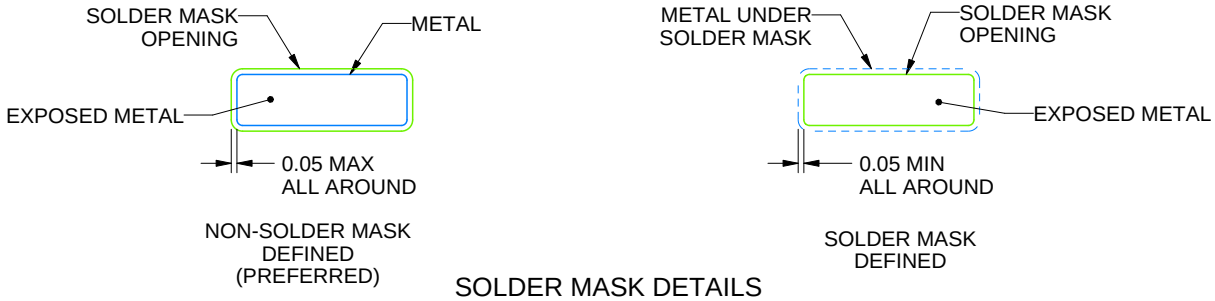


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

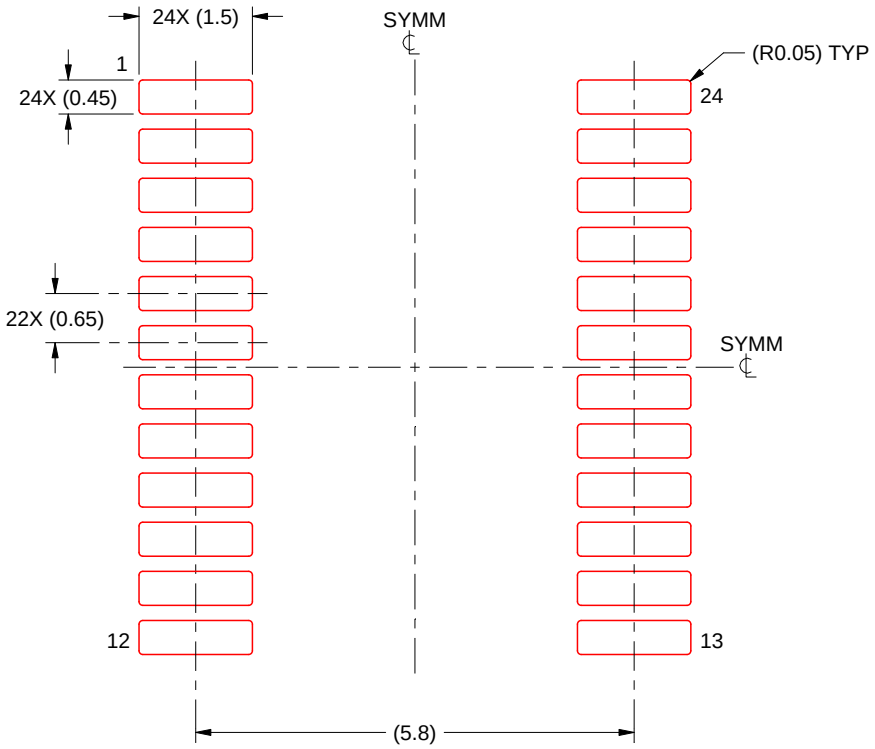


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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