P3S0210BQ

Dual bidirectional I3C-bus, 1:2 and 2:1 switch, and voltage level translator

Rev. 1.0 — 15 December 2023 Product data sheet

1 General description

The P3S0210BQ is a dual bidirectional I3C-bus 1:2 (one controller to two targets) and 2:1 (two controllers to one target) switch and voltage level translator. It includes a reference supply (V_{CCR}), supplies for ports 1, 2, and S (V_{CCP1}, V_{CCP2}, and V_{CCS} respectively), and a supply for OE and SEL pins (V_{CCE}).

The supply voltage of V_{CCP1}, V_{CCP2}, V_{CCS}, and V_{CCE} is between 0.72 V to 3.63 V. The reference supply V_{CCR} is between 1.62 V to 3.63 V and should be greater or equal to V_{CCP1}, V_{CCP2}, V_{CCS} and V_{CCE}.

Pins A1 and B1 are referenced to V_{CCP1}, pins A2 and B2 are referenced to V_{CCP2}, and pins A and B are referenced to V_{CCS}. The OE and SEL pins are defined for enable and port selection that are referenced to V_{CCE}.

P3S0210BQ can be used for both open-drain as well as push-pull application which allows for I3C-bus and other applications like I^2C-bus, SMBus and SPI protocols.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- I3C switch and voltage level translation
  - 2:1; two controllers ⇔ one target
  - 1:2; one controller ⇔ two targets
- Wide supply voltage range:
- V_{CCP1}: 0.72 V to 3.63 V (port 1)
- V_{CCP2}: 0.72 V to 3.63 V (port 2)
- V_{CCS}: 0.72 V to 3.63 V (port S)
- V_{CCE}: 0.72 V to 3.63 V (OE and SEL pins)
- V_{CCR}: 1.62 V to 3.63 V (reference)
- V_{CCP1}, V_{CCP2}, V_{CCS} and $V_{CCE} \leq V_{CCR}$
- Auto direction sensing, bidirectional voltage level translation
- Support both open-drain and push-pull application
  - I3C, I^2C and SPI protocols
  - Data rate up to 52 Mbps
- IOFF circuitry provides partial Power-down mode operation
- Provided voltage level translation for I3C, I^2C-bus, SMBus and SPI devices
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78F Class II
- Available in DHVQFN14 package (2.5 mm x 3 mm x 0.85 mm body)
- Specified from and -40 °C to +125 °C

3 Applications

- Server and data center
- Networking
- Desktop and laptop computers
- Smart phone and mobile devices

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3S0210BQ	S0210	DHVQFN14	plastic, dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 mm x 3 mm x 0.85 mm, 0.5 mm pitch	SOT762-1

4.1 Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3S0210BQ	P3S0210BQAZ	DHVQFN14	REEL 7" Q1 NDP SSB	3000	T_{amb} = -40 °C to +125 °C

5 Block diagram

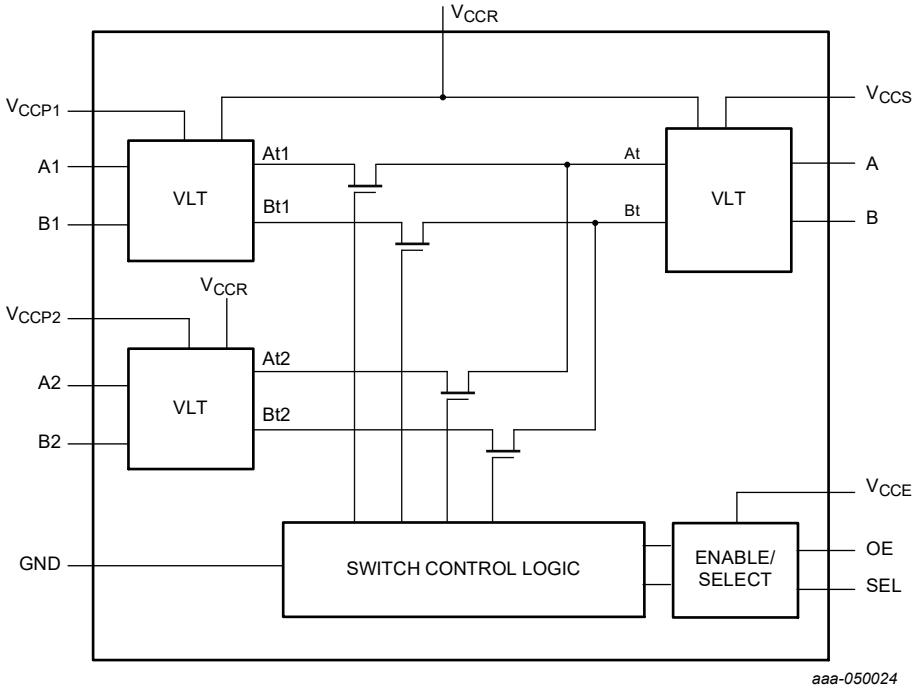
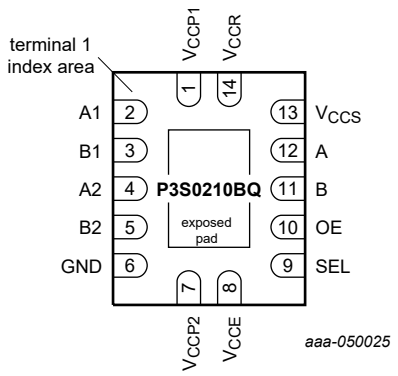


Figure 1. Block diagram

6 Pinning information

6.1 Pinning



Transparent top view

Transparent top view, terminal side down

Figure 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
V_{CCP1}	1	S	supply voltage for port 1
A1	2	I/O	input or output of port 1 (referenced to V_{CCP1})
B1	3	I/O	input or output of port 1 (referenced to V_{CCP1})
A2	4	I/O	input or output of port 2 (referenced to V_{CCP2})
B2	5	I/O	input or output of port 2 (referenced to V_{CCP2})
GND	6	S	supply ground
V_{CCP2}	7	S	supply voltage for port 2
V_{CCE}	8	S	supply voltage for EN & SEL
SEL	9	I	port 1 or 2 selection (referenced to V_{CCE})
OE	10	I	enable pin, active HIGH (referenced to V_{CCE})
B	11	I/O	common input or output of port S (referenced to V_{CCS})
A	12	I/O	common input or output of port S (referenced to V_{CCS})
V_{CCS}	13	S	supply voltage for port S
V_{CCR}	14	S	reference supply voltage
Exposed pad	-	-	connect to PCB GND

[1] I = input, O = output, I/O = input and output, S = power supply

7 Functional description

7.1 Architecture

The architecture is DPDT (Double Pole Double Throw) switch with VLT (Voltage Level Translation) to achieve 2:1 or 1:2 I3C-bus switch function. The VLT uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-channel Pass gate transistor and a 10 kΩ pullup resistor (to provide DC-bias and drive capabilities) to meet these requirements. All of the ports (A/A1/A2 and B/B1/B2) have pullup resistors when enabled and the I/O status is HIGH. When I/O status is LOW or is disabled, the pullup resistors are disconnected

The design is directionless and does not need direction control signal. The implementation supports both low-speed Open-drain operation (I^2C-bus) as well as high speed push-pull operation (I3C-bus or SPI-bus). The N-channel Pass device is on only during LOW input cycle and off during HIGH input cycle.

P3S0210BQ can be enabled/disabled by OE pin when all the power rails (V_{CCP1}, V_{CCP2}, $V_{CCS,}$, V_{CCE}, and V_{CCR}) are available.

The SEL pin provides the port select function.

- SEL = L, the port 1 is connected to port S. The port 2 is disconnected.
- SEL = H, the port 2 is connected to port S. The port 1 is disconnected.

See Table 3 function table for port status vs V_{CCP1}, V_{CCP1}, V_{CCS}, V_{CCR}, OE and SEL.

Table 3. Function table[1]

H = HIGH voltage level; L = LOW voltage level; X = don't care

Supply voltage			Input		Input/output
V_{CCR} = 1.62 V to 3.63 V and V_{CCE} = 0.72 to V_{CCR}					
V_{CCP1}	**V_{CCP2}**	**V_{CCS}**	**OE[2]**	**SEL[2]**	
0.72 to V_{CCR}	0.72 to V_{CCR}	0.72 to V_{CCR}	L	X	disconnected
0.72 to V_{CCR}	0.72 to V_{CCR}	0.72 to V_{CCR}	H	L	port 1 = port S[3] A1 = A B1 = B
0.72 to V_{CCR}	0.72 to V_{CCR}	0.72 to V_{CCR}	H	H	port 2 = port S[3] A2 = A B2 = B
GND	X	X	X	X	disconnected
x	GND	X	X	X	disconnected
x	X	GND	X	X	disconnected
V_{CCR} = GND or V_{CCE} = GND[4]					
V_{CCP1}	**V_{CCP2}**	**V_{CCS}**	**OE**	**SEL**	
X	X	X	X	X	disconnected

[1] At disconnected condition, port 1, port 2 and port S. (i.e. A1/A2/A & B1/B2/B pins) are high-Z.
[2] V_{IL} max = 0.35V_{CCE} and V_{IH} min = 0.65 V_{CCE}. The V_{CCE} can be connected to an external device that is powered by either V_{CCP1} , $V_{CCP2,}$ V_{CCS} or V_{CCR}.
[3] At this condition, there are internal 10 kΩ pullup resistors for port 1, port 2 and port S. (i.e. A1/A2/A & B1/B2/B pins)
[4] When V_{CCR} is at GND level, the device goes into Power-down mode.

7.2 Input driver requirements

The continuous DC- current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the P3S0210BQ IO pins.

The high bandwidth of these IO circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pullup resistor.

The fall time of a signal depends on the edge-rate and output impedance of the external driving the P3S0210BQ data IOs, as well as the capacitive loading at the data lines.

7.3 Power-up/power-down and enable/disable

It requires all the power rails ready and OE pin ready to power up P3S0210BQ.

If any power rail or OE are not ready, this part is disabled, and all the ports are disconnected. There is no special power sequence requirement between V_{CCP1}, V_{CCP2}, V_{CCS}, V_{CCR}, V_{CCE}, and OE pin. After power up, V_{CCR} should be greater or equal to the maximum value of V_{CCP1}, V_{CCP2}, V_{CCS}, V_{CCE}, and 1.62 V.

Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (tdis with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND, OE pin should not be left floating in any condition.

OE ($V_{IL(max)}$ = 0.35V_{CCE} and $V_{IH(min)}$ = 0.65V_{CCE}) allows the control signal by the device Vcc range from 0.72 V to V_{CCR}.

7.4 Pullup or pulldown resistors on I/O lines

Each I/O pin of port 1, port 2 and port S has an internal 10 kΩ pullup resistor to V_{CCP1}, V_{CCP2} and V_{CCS}, respectively.

The pullup resistors are connected only when P3S0210BQ is enabled and the I/O status is HIGH. When I/O status is low or P3S0210BQ is disabled, the pullup resistors are disconnected.

When SEL is set LOW, A2 and B2 are pulled up HIGH (V_{CCP2}) due to internal 10 kΩ pullup resistance. When SEL is set HIGH under V_{CCE} domain, A1 and B1 are tied to V_{CCP1} by internal pullup resistance.

If a smaller pullup resistor is required, add an external resistor in parallel to the internal 10 kΩ. The smaller value affects the V_{OL} level.

If an external pulldown resistor is required, the V_{OH} level is decreased by the voltage divider from the internal 10 kΩ pullup R and the external pulldown R. The pulldown resistor value is recommended to be greater than 200 kΩ. It ensures V_{OH} level drops less than 5 % of the associated supply voltage.

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCR}	reference supply voltage			-0.5	+4.2	V
V_{CCP1}	supply voltage for port 1			-0.5	+4.2	V
V_{CCP2}	supply voltage for port 2			-0.5	+4.2	V

Table 4. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCS}	supply voltage for port S			-0.5	+4.2	V
V_{CCE}	supply voltage for OE and SEL			-0.5	+4.2	V
V_I	input voltage	at I/O pins supplied by V_{CCP1}	[1]	-0.5	+4.2	V
		at I/O pins supplied by V_{CCP2}	[1] [2] [3]	-0.5	+4.2	V
		at I/O pins supplied by V_{CCS}	[1]	-0.5	+4.2	V
		OE, SEL		-0.5	+4.2	V
V_O	output voltage	Active mode		-0.5	V_{CCO}+0.25	V
		Power-down[4]		-0.5	+4.2	V
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C		-	125	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] V_{CCO} + 0.25 V should not exceed 4.2 V.
[4] V_{CCR} = GND or V_{CCE} = GND

9 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCR}	supply voltage	at V_{CCR} supply pin	1.62	3.63	V
V_{CCP1}		at V_{CCP1} supply pin	0.72	V_{CCR}	V
V_{CCP2}		at V_{CCP2} supply pin	0.72	V_{CCR}	V
V_{CCS}		at V_{CCS} supply pin	0.72	V_{CCR}	V
V_{CCE}		at V_{CCE} supply pin	0.72	V_{CCR}	V
V_I	input voltage	at I/O pins supplied by V_{CCP1}	-0.3	V_{CCP1}	V
		at I/O pins supplied by V_{CCP2}	-0.3	V_{CCP2}	V
		at I/O pins supplied by V_{CCS}	-0.3	V_{CCS}	V
		OE, SEL	-0.3	V_{CCE}	V
V_O	ouput voltage	at I/O pins supplied by V_{CCP1}	-0.3	V_{CCP1}	V
		at I/O pins supplied by V_{CCP2}	-0.3	V_{CCP2}	V
		at I/O pins supplied by V_{CCS}	-0.3	V_{CCS}	V
T_{amb}	ambient temperature		-40	+125	°C
T_j	junction temperature[1]		-40	+150	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CCO} = 0.72 V to V_{CCR}	-	<5.3	ns/V

[1] The T_j limits shall be supported by proper thermal PCB design.

10 Static characteristics

Table 6. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	port 1, 2 and S; I_O = -10 µA	[2]	0.8xV_{CCO}	-	-	V
V_{OL}	LOW-level output voltage	port 1, 2 and S; I_O = 10 µA; V_I = 0.1 V	[3]	-	-	0.25xV_{CCO}	V
I_i	input leakage current	OE input; V_I = 0 V or 1.98 V; V_{CCI} = 0.72 V to V_{CCR}; V_{CCR} = 1.62 V to 3.63 V		-	-	±1	µA
I_{OZ}	OFF-state output current	OE = 0; V_O = 0 V or V_{CCO}; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	±1	µA
I_{OFF}	power-off leakage current	port 1, 2; V_I or V_O = 0 V or V_{CCR}; V_{CCP1} = 0 V; V_{CCP2} = 0 V; V_{CCS} = 0 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	±1	µA
		port S; V_I or V_O = 0 V or 1 .98V; V_{CCS} = 0 V; V_{CCP1} = 0 V to V_{CCR}; V_{CCP2} = 0 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	±1	µA
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A; I_{CC1}, I_{CC2}, I_{CCS}, I_{CCR}; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[4]	-	5	-	µA
C_I	input capacitance	OE, SEL input; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	1.5	-	pF
$C_{I/O}$	input/output capacitance	I/O of port 1, 2 and S; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	4.0	-	pF

[1] The typical value is V_{CCI} = 1.0 V, V_{CCO} = 1.8 V, V_{CCR} = 1.8 V or 3.3 V
[2] V_{CCO} is the supply voltage associated with the output.
[3] The resistance between input and output at low stage. R_{on} max = 370 Ω at min (V_{CCI}, V_{CCO}) < 0.9 V. R_{on} max = 220 Ω at min (V_{CCI}, V_{CCO}) ≥ 0.9 V.
[4] V_{CCI} is the supply voltage associated with the input.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	port 1,2 and S; V_{CCI} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[1]	0.65 x V_{CCI}	-	-	V
		OE, SEL input		0.65 x V_{CCE}	-		V
V_{IL}	LOW-level input voltage	port 1,2 and S; V_{CCI} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[2]	-	-	0.35 V_{CCX}	V
		OE, SEL input		-	-	0.35 V_{CCE}	V
V_{OH}	HIGH-level output voltage	I_O = -10 µA; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[3]	0.75 x V_{CCO}	-	-	V

Table 7. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	V_I = 0 V; I_O = 10 µA; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[3] [4]	-	-	0.25 x V_{CCO}	V
L_I	input leakage current	OE,SEL input; V_I = 0 V to V_{CCI}; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	±5	µA
I_{OZ}	OFF-state output current	port 1,2 and S; V_O = 0 V or V_{CCO}; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V	[3]	-	-	±10	µA
I_{OFF}	power-off leakage current	port 1,2; V_I or V_O = 0 V or V_{CCR}; V_{CCP1} = 0 V; V_{CCP2} = 0 V; V_{CCS} = 0 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	10	µA
		port S; V_I or V_O = 0 V or 1.98 V; V_{CCS} = 0 V; V_{CCP1} = 0 V to V_{CCR}; V_{CCP2} = 0 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	10	µA
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[1]		-		
		I_{CC1}, I_{CC2}			-		
		OE = LOW; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	15	µA
		OE = HIGH; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	20	µA
		V_{CCP1} = V_{CCP2} = 1.98 V; V_{CCS} = 0 V		-	-	15	µA
		V_{CCP1} = V_{CCP2} = 0 V; V_{CCS} = 1.98 V		-	-	-15	µA
		I_{CCS}			-		
		OE = LOW; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	29	µA
		OE = HIGH; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	36	µA
		V_{CCP1} = V_{CCP2} = 1.98 V; V_{CCS} = 0 V		-	-	-15	µA
		V_{CCP1} = V_{CCP2} = 0 V; V_{CCS} = 1.98 V		-	-	20	µA
		I_{CC1} + I_{CC2} + I_{CCS}			-		
		OE = LOW; V_{CCO} = 0.72 V to V_{CCR}; V_{CCR}= 1.62 V to 3.63 V		-	-	56	µA

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCX} is the minimum of V_{CCPI} and V_{CCS}, where V_{CCPI} is the selected port of V_{CCP1} and V_{CCP2}.
[3] V_{CCO} is the supply voltage associated with the output.
[4] The resistance between input and output at low stage. R_{on} max = 370 Ω at min (V_{CCI}, V_{CCO}) < 0.9 V. R_{on} max = 220 Ω at min (V_{CCI}, V_{CCO}) ≥ 0.9 V.

11 Dynamic characteristics

Table 8. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

V_{CCR} = 1.62 V to 3.63 V, voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V_{CCS}			V_{CCS}			Unit
			1 V, 1.2 V ± 10 %			1.8 V ± 10 %			
			Min	Typ	Max	Min	Typ	Max	
V_{CCP1} = V_{CCP2} = 1 V ± 10 %									
t_{pd}[1]	propagation delay	port1,2 to port S; C_L = 68 pF	-	5.5	8	-	5.5	8	ns
		port S to port1,2; C_L = 68 pF	-	6	9	-	4	6	ns
t_{en}[2]	enable time	OE to port1,2 and S; C_L = 68 pF	-	1.4	1.8	-	1.4	1.8	µs
t_{dis}[2]	disable time	OE to port1,2; no external C_L[3]	-	190	220	-	180	210	ns
		OE to port S; no external C_L[3]	-	190	220	-	180	210	ns
		OE to port1,2; C_L = 68 pF	-	460	600	-	450	540	ns
		OE to port S; C_L = 68 pF	-	460	600	-	450	540	ns
t_{sel_en}	SEL enable time	OE = HIGH, V_I = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C_L = 68 pF	-	1.5	1.9	-	1.5	1.9	µs
t_{sel_dis}	SEL disable time	OE = HIGH, V_I = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C_L = 68 pF	-	140	210	-	130	200	ns
t_t	transition time	port1,2 ; C_L = 68 pF	1.1	4	6.5	0.7	3	5	ns
		port S; C_L = 68 pF	1.1	4	7	0.7	2.5	4	ns
$t_{sk(o)}$	output skew time	delta between channels[4]	0	0.2	0.4	0	0.2	0.4	ns
t_W	pulse width	data inputs	15	-	-	13.5	-	-	ns
f_{data}	data rate		0.064	-	52	0.064	-	52	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
[2] Guaranteed by design.
[3] Delay between OE going LOW and when the outputs are actually disabled (R_L = 50 kΩ and no C_L).
[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

V_{CCR} = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V_{CCS}			V_{CCS}			Unit
			1.2 V ± 10 %			1.62 V to V_{CCR}			
			Min	Typ	Max	Min	Typ	Max	
V_{CCP1} = 0.9 V to V_{CCR}; V_{CCP2} = 0.9 V to V_{CCR}									
t_{pd}	propagation delay	port1,2 to port S; C_L = 68 pF	-	5.5	8	-	5.5	8	ns
		port S to port1,2; C_L = 68 pF	-	5.5	6.9	-	5.5	6	ns
		port1,2 to port S; C_L = 80 pF	-	7.5	10	-	5.4	7	ns
		port S to port1,2; C_L = 30 pF	-	5	9	-	4	6	ns
t_{en}[2]	enable time	OE to port1,2 and S; C_L = 15 pF	-	1.4	1.8	-	1.4	1.8	µs
t_{dis}[2]	disable time	OE to port1,2; no external C_L[3]	-	180	210	-	180	210	ns
		OE to port S; no external C_L[3]	-	180	210	-	180	210	ns
		OE to port1,2; C_L = 68 pF	-	450	580	-	450	540	ns
		OE to port S; C_L = 68 pF	-	450	580	-	450	540	ns
t_{sel_en}	SEL enable time	OE = HIGH, V_I = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C_L = 68 pF	-	1.5	1.9	-	1.5	1.9	µs
t_{sel_dis}	SEL disable time	OE = HIGH, V_I = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C_L = 68 pF	-	140	210	-	130	200	ns
t_t	transition time	port1,2; C_L = 68 pF	0.8	1.8	5	0.6	3	5	ns
		port S; C_L = 68 pF	1.1	4	7	0.6	2.5	4	ns
t_{tc}	transition time	port1,2; C_L = 30 pF	-	3.5	7	-	2	3	ns
		port S; C_L = 80 pF	-	5	10	-	4	5	ns
$t_{sk(o)}$	output skew time	delta between channels[4]	0	0.1	0.5	0	0.3	0.4	ns
t_W	pulse width	data inputs	15	-	-	13.5	-	-	ns
f_{data}	data rate		0.064	-	52	0.064	-	52	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
[2] Guaranteed by design.
[3] Delay between OE going LOW and when the outputs are actually disabled (R_L = 50 kΩ and no C_L).
[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Table 10. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

V_{CCR} = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V_{CCS}			Unit
			1.8 V ± 10 %			
V_{CCP1} = V_{CCP2} = 1.8 V ± 10 %						
t_{pd}	propagation delay	port1,2 to port S; C_L = 68 pF	-	4	6	ns
		port S to port1,2; C_L = 68 pF	-	4	6	ns
t_{en}[2]	enable time	OE to port1,2 and S; C_L = 68 pF	-	1.4	1.8	µs
t_{dis}[2]	disable time	OE to port1,2; no external C_L[3]	-	180	210	ns
		OE to port S; no external C_L[3]	-	180	210	ns
		OE to port1,2; C_L = 68 pF	-	440	540	ns
		OE to port S; C_L = 68 pF	-	440	540	ns
t_{sel_en}	SEL enable time	OE = HIGH, V_I = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C_L = 68 pF	-	1.5	1.9	µs
t_{sel_dis}	SEL disable time	OE = HIGH, V_I = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C_L = 68 pF	-	130	200	ns
t_t	transition time	port1,2; C_L = 68 pF	0.5	1.5	2	ns
		port S; C_L = 68 pF	0.7	2.5	4	ns
$t_{sk(o)}$	output skew time	delta between channels[4]	0	0.2	0.3	ns
t_W	pulse width	data inputs	13.5	-	-	ns
f_{data}	data rate		0.064	-	52	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
[2] Guaranteed by design.
[3] Delay between OE going LOW and when the outputs are actually disabled (R_L = 50 kΩ and no C_L).
[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

V_{CCR} = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V_{CCS}			V_{CCS}			Unit
			0.72 V to 0.9V			0.9 V to V_{CCR}			
			Min	Typ	Max	Min	Typ	Max	
V_{CCP1} = 0.72 V to 0.9 V; V_{CCP2} = 0.72 V to 0.9 V									
t_{pd}	propagation delay	port1,2 to port S; C_L = 68 pF	-	7	13	-	7.5	8.5	ns

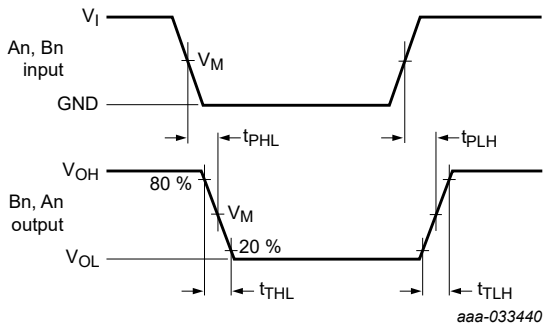
Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1]*...continued*

V_{CCR} = 1.62 V to 3.63 V, Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5; for waveform see Figure 3

Symbol	Parameter	Conditions	V_{CCS}			V_{CCS}			Unit
			0.72 V to 0.9V			0.9 V to V_{CCR}			
			Min	Typ	Max	Min	Typ	Max	
		port S to port1,2; C_L = 68 pF	-	8	14	-	8	9	ns
t_{en}[2]	enable time	OE to port1,2 and S; C_L = 15 pF	-	1.4	12	-	1.4	1.8	µs
t_{dis}[2]	disable time	OE to port1,2; no external C_L[3]	-	240	270	-	230	260	ns
		OE to port S; no external C_L[3]	-	240	270	-	230	260	ns
		OE to port1,2; C_L = 68 pF	-	490	650	-	470	620	ns
		OE to port S; C_L = 68 pF	-	490	650	-	470	620	ns
t_{sel_en}	SEL enable time	OE = HIGH, V_I = L or H SEL: H→L (or L→H) Port 1 (or port 2) connect to port S, C_L = 68 pF	-	1.5	1.9	-	1.5	1.9	µs
t_{sel_dis}	SEL disable time	OE = HIGH, V_I = L or H SEL: L→H (or H→L) Port 1 (or port 2) disconnect to port S, C_L = 68 pF	-	150	220	-	140	210	ns
t_t	transition time	port1,2 ; C_L = 68 pF	-	3	16	0.75	2.5	9	ns
		port S; C_L = 68 pF	-	6.5	16	0.8	6.5	9	ns
$t_{sk(o)}$	output skew time	delta between channels[4]	0	0.2	0.3	0	0.2	0.7	ns
t_W	pulse width	data inputs	37	-	-	17	-	-	ns
f_{data}	data rate		0.064	-	26	0.064	-	40	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_t is the same as t_{THL} and t_{TLH}.
[2] Guaranteed by design.
[3] Delay between OE going LOW and when the outputs are actually disabled (R_L = 50 kΩ and no C_L).
[4] Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

12 Waveforms



Measurement points are given in Table 12

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

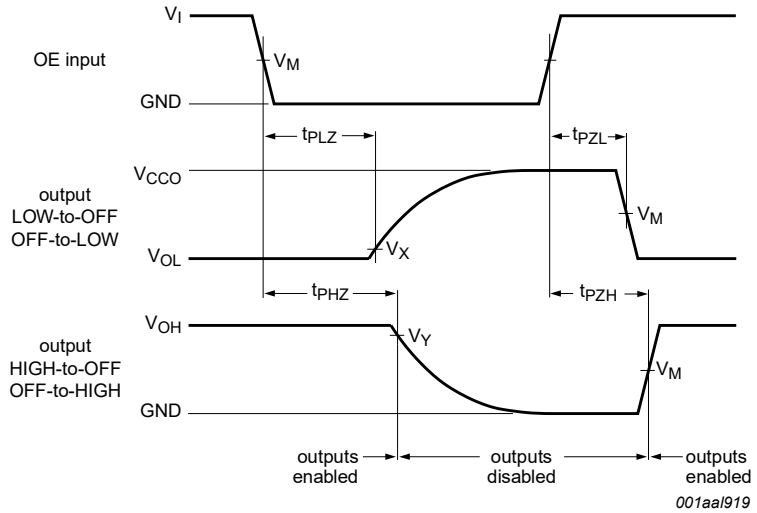
Figure 3. Data input (port 1/2, port S) to data output (port S, port 1/2) propagation delay times

Table 12. Measurement points

V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

Supply voltage	Input[1]	Output[2]		
V_{CCO}	V_M	V_M	V_X	V_Y
0.8V ± 10%	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.08V	V_{OH}-0.08V
1.0V ±10%	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.10V	V_{OH}-0.10V
1.2V ± 10%	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.12V	V_{OH}-0.12V
1.8V ± 10%	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.18V	V_{OH}-0.18V

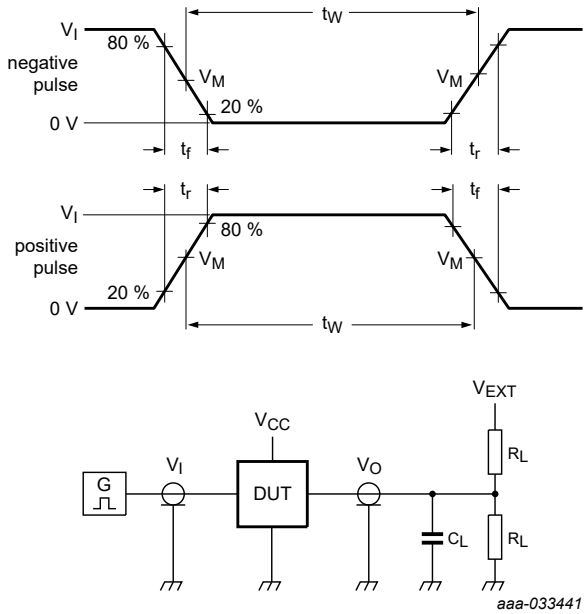
[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Measurement points are given in Table 12

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and disable times



Test data is given in Table 13

All input pulses are supplied by generators having the following characteristics: PRR ≤ 26 MHz; ZO = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 5. Test circuit for measuring switching times

Table 13. Test data

Supply voltage (V_{CCR} = 1.62 V to 3.6 V)			Input		Load		V_{EXT}		
V_{CCP1}	V_{CCP2}	V_{CCS}	V_I	Δt/ΔV	C_L[1]	R_L[2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.72 to V_{CCR}	0.72 to V_{CCR}	0.72 to V_{CCR}	V_{CCI}[3]	≤ 1.0 ns/V	68 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$[4]

[1] Different C_L values are specified in Dynamic characteristics.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.

[3] V_{CCI} is the supply voltage associated with the input.

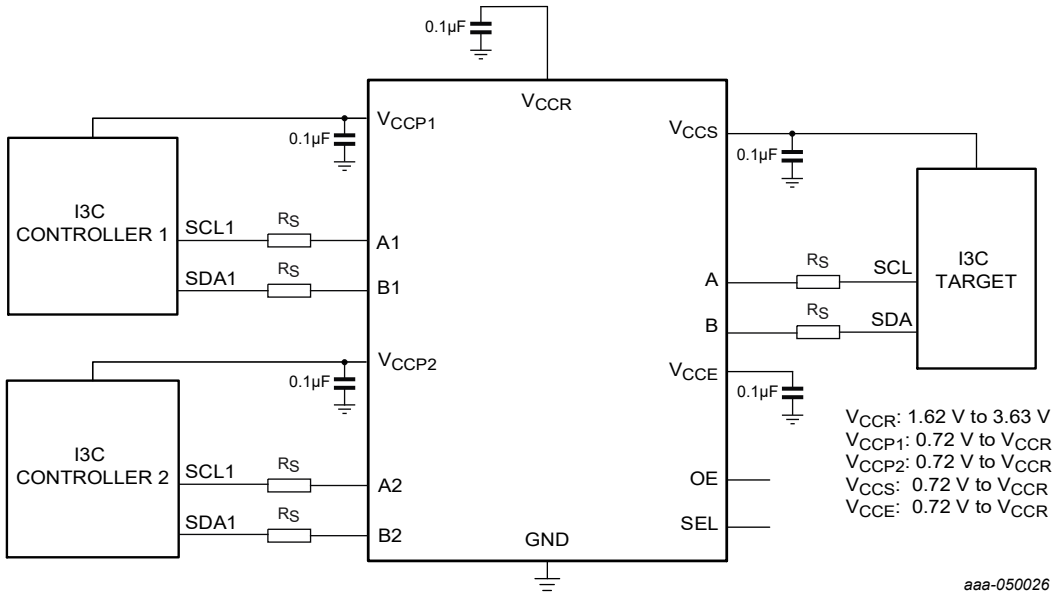
[4] V_{CCO} is the supply voltage associated with the output.

13 Application information

The P3S0210BQ can be used to interface between two I3C controllers to one target or one I3C controller to two targets at different supply voltages on port 1, port 2 and port S.

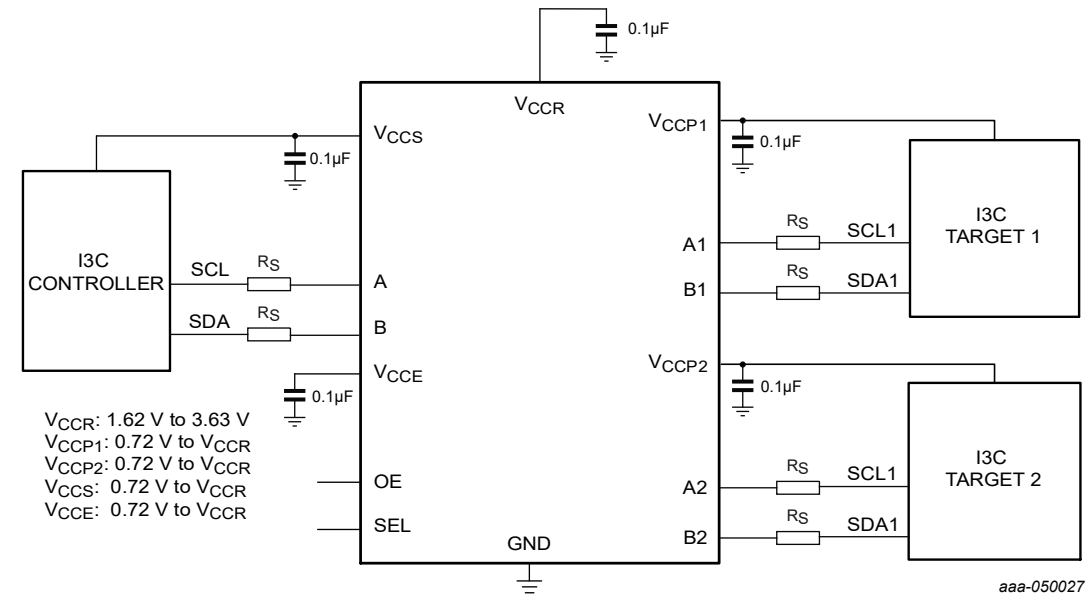
A series resistor Rs on each I/O pin is required to reduce the overshoot/undershoot. The recommended value is 30 Ω. Adjust the Rs value for optimized signal integrity is needed with different wire lengths, parasitic inductance and capacitance. Please ensure the Rs should not be too high to affect the V_{OL} level.

See Figure 6 and Figure 7 for I3C and Figure 8 and Figure 9 for I^2C typical operating circuit.



Assume the I3C controller has integrated pull up resistors for SCL/SDA at open drain mode. If not, the external pull up resistors on the I3C controller side are required.

Figure 6. I3C 2:1 application diagram (2 controllers, 1 target)



Assume the I3C controller has integrated pull up resistors for SCL/SDA at open drain mode. If not, the external pull up resistors on the I3C controller side are required.

Figure 7. I3C 1:2 application diagram (1 controller, 2 targets)

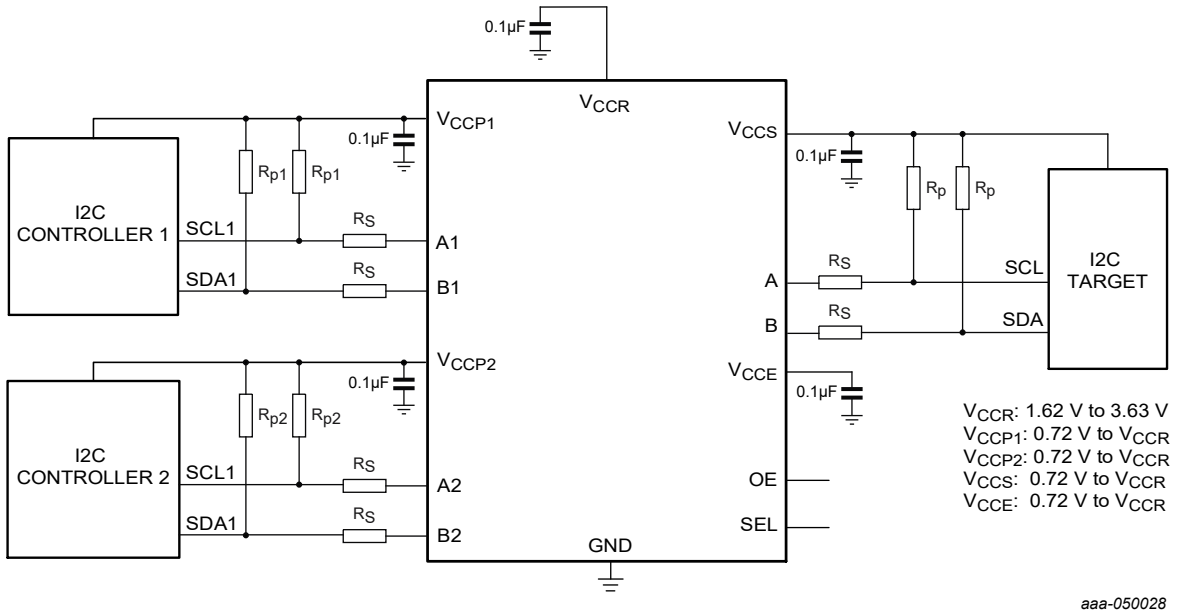


Figure 8. I^2C 2:1 application diagram (2 controllers, 1 target)

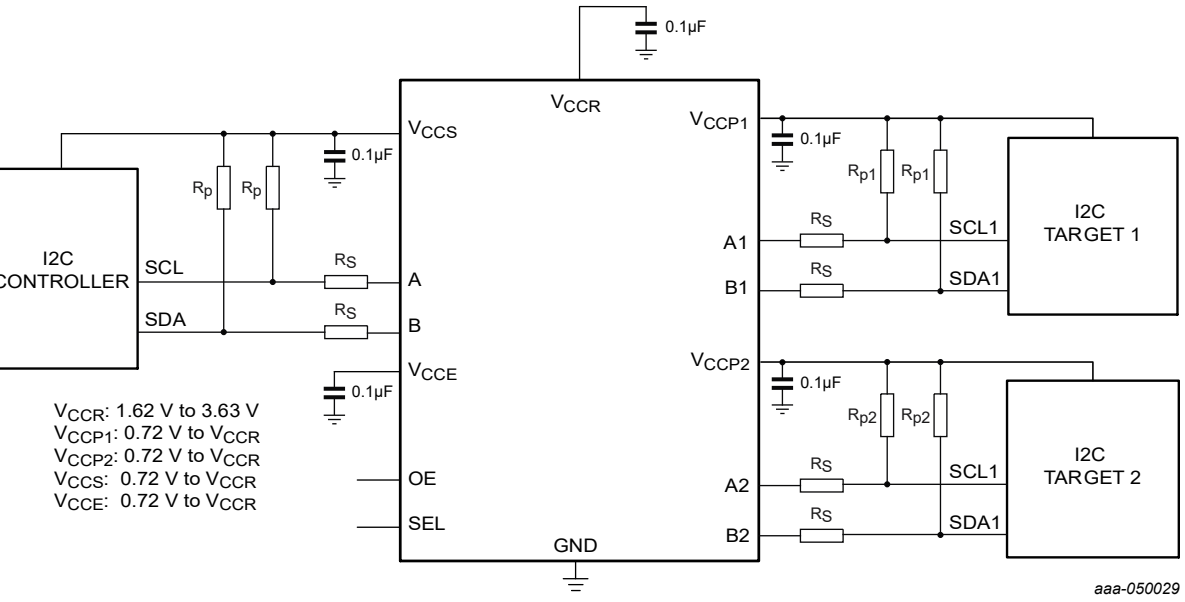
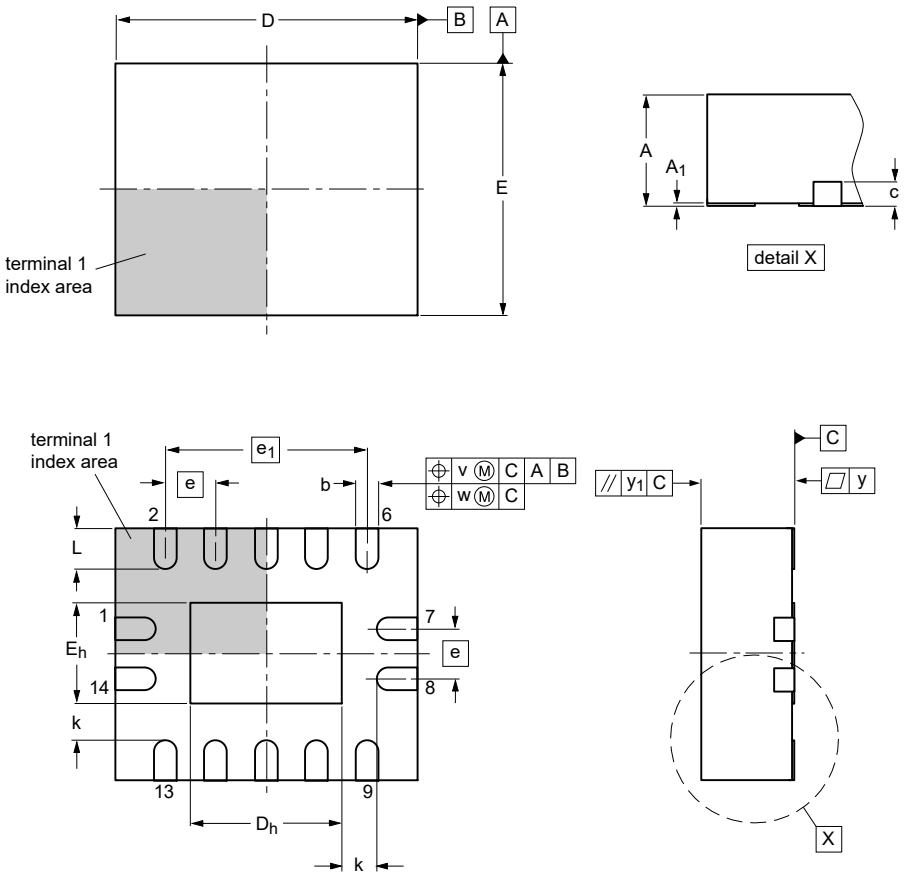


Figure 9. I^2C 1:2 application diagram (1 controller, 2 targets)

14 Package outline

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Figure 10. Package outline DHVQFN14 (SOT762-1)

15 Soldering PCB footprints

Footprint information for reflow soldering of DHVQFN14 package **SOT762-1**

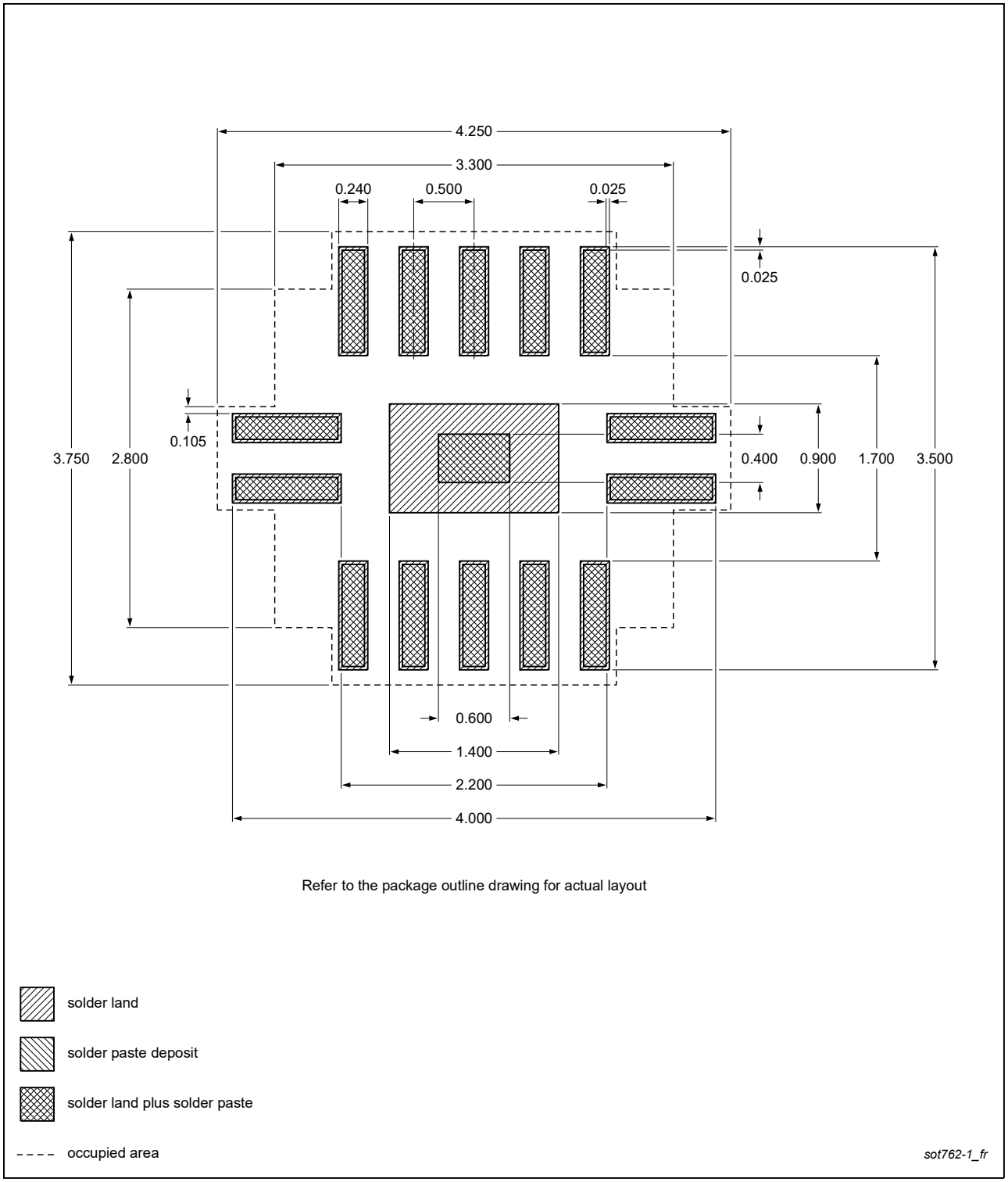


Figure 11. Reflow soldering footprint for DHVQFN14 (SOT762-1)

16 Revision history

Table 14. Revision history

Document ID	Release date	Description
P3S0210BQ v.1.0	15 December 2023	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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