Data Sheet

A New Direction in Mixed-Signal

COMLINEAR® CLC1001
Ultra-Low Noise Amplifier

FEATURES

- 0.6 nV/√Hz input voltage noise
- 1mV maximum input offset voltage
- 2.1GHz gain bandwidth product
- Minimum stable gain of 10
- 410V/μs slew rate
- 130mA output current
- -40°C to +125°C operating temperature range
- Fully specified at 5V and ±5V supplies
- CLC1001: Lead-free SOT23-6, SOIC-8

APPLICATIONS

- Transimpedance amplifiers
- Pre-amplifier
- Low noise signal processing
- Medical instrumentation
- Probe equipment
- Test equipment
- Ultrasound channel amplifier

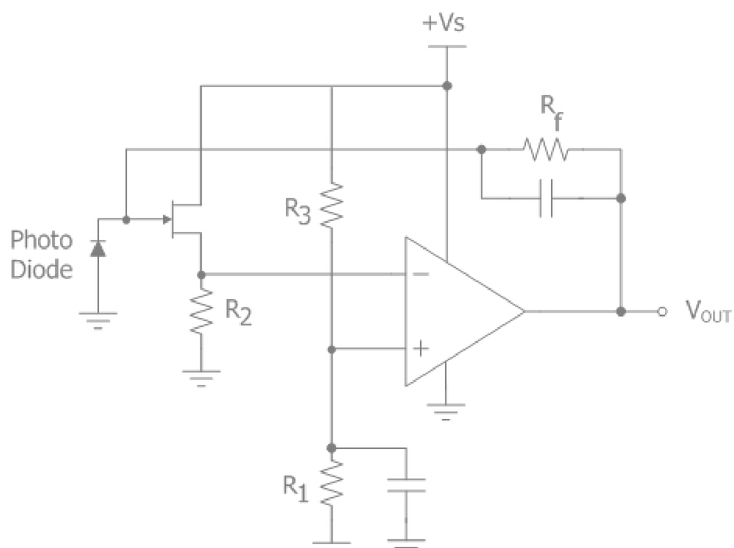
General Description

The COMLINEAR CLC1001(single) is a high-performance, voltage feedback amplifier with ultra-low input voltage noise, 0.6nV/√Hz. The CLC1001 provides 2.1GHz gain bandwidth product and 410V/μs slew rate making it well suited for high-speed data acquisition systems requiring high levels of sensitivity and signal integrity. This COMLINEAR high-performance amplifier also offers low input offset voltage.

The COMLINEAR CLC1001 is designed to operate from 4V to 12V supplies. It consumes only 12.5mA of supply current per channel and offers a power saving disable pin that disables the amplifier and decreases the supply current to below 225μA. The CLC1001 amplifier operates over the extended temperature range of -40°C to +125°C.

If a lower minimum stable gain is required, the CLC1002 offers a minimum stable gain of 5.

Typical Application - Single Supply Photodiode Amplifier



Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1001IST6X	SOT23-6	Yes	Yes	-40°C to +125°C	Reel
CLC1001ISO8X	SOIC-8	Yes	Yes	-40°C to +125°C	Reel
CLC1001ISO8	SOIC-8	Yes	Yes	-40°C to +125°C	Rail

Moisture sensitivity level for all parts is MSL-1.

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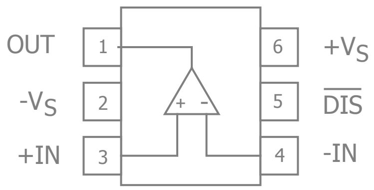
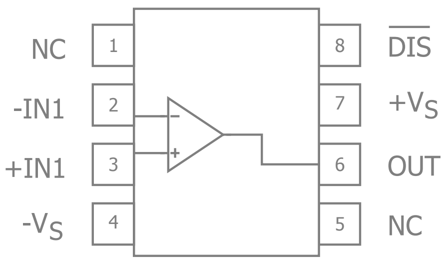
SOT23 Pin Configuration



SOT23 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.
6	$+V_S$	Positive supply

SOIC Pin Configuration



SOIC Pin Assignments

Pin No.	Pin Name	Description
1	NC	No connect
2	-IN1	Negative input
3	+IN1	Positive input
4	$-V_S$	Negative supply
5	NC	No connect
6	OUT	Output
7	$+V_S$	Positive supply
8	$\overline{DIS}$	Disable. Enabled if pin is left floating or pulled above V_{ON}, disabled if pin is grounded or pulled below V_{OFF}.

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
6-Lead SOT23		177		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOT23-6
Human Body Model (HBM)	2kV
Charged Device Model (CDM)	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+125	°C
Supply Voltage Range	4		12	V

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Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = 200Ω, R_L = 500Ω to V_S/2, G = 10; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +40, V_{OUT} = 0.2V_{pp}		2000		MHz
BW_{SS}	-3dB Bandwidth	G = +10, V_{OUT} = 0.2V_{pp}		265		MHz
BW_{LS}	Large Signal Bandwidth	G = +10, V_{OUT} = 2V_{pp}		105		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness Small Signal	G = +10, V_{OUT} = 0.2V_{pp}		37		MHz
$BW_{0.1dBLS}$	0.1dB Gain Flatness Large Signal	G = +10, V_{OUT} = 2V_{pp}		36		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		2.4		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		11		ns
OS	Overshoot	V_{OUT} = 1V step		6		%
SR	Slew Rate	4V step		360		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	1V_{pp}, 10MHz		-80		dBc
HD3	3rd Harmonic Distortion	1V_{pp}, 10MHz		-83		dBc
THD	Total Harmonic Distortion	1V_{pp}, 10MHz		-79		dB
e_n	Input Voltage Noise	> 100kHz		0.6		nV/√Hz
i_n	Input Current Noise	> 100kHz		4.2		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			0.1		mV
dV_{IO}	Average Drift			2.7		µV/°C
I_b	Input Bias Current			28		µA
dI_b	Average Drift			45		nA/°C
I_o	Input Offset Current			0.5		µA
PSRR	Power Supply Rejection Ratio	DC		83		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		82		dB
I_S	Supply Current	per channel		12		mA
Disable Characteristics						
t_{ON}	Turn On Time	1V step, 1% settling		100		ns
t_{OFF}	Turn Off Time			900		ns
OFF_{ISO}	Off Isolation	2V_{pp}, 5MHz		80		dB
$OFFC_{OUT}$	Off Output Capacitance			5.7		pF
V_{OFF}	Power Down Voltage	Disabled if $\overline{DIS}$ pin is grounded or pulled below V_{OFF}		Disabled if $\overline{DIS}$ < 1.5		V
V_{ON}	Enable Voltage	Enabled if $\overline{DIS}$ pin is floating or pulled above V_{ON}		Enabled if $\overline{DIS}$ > 3		V
I_{SD}	Disable Supply Current	No Load, $\overline{DIS}$ pin tied to ground		130		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		2.6		MΩ
C_{IN}	Input Capacitance			1.6		pF
CMIR	Common Mode Input Range			0.8 to 5.1		V
CMRR	Common Mode Rejection Ratio	DC , V_{cm}=1.5V to 4V		85		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 500Ω		0.93 to 4		V
		R_L = 2kΩ		0.9 to 4.1		V
I_{OUT}	Output Current			±130		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±150		mA

Notes:

1. 100% tested at 25°C

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Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_f = 200Ω, R_L = 500Ω , G = 10; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +40, V_{OUT} = 0.2V_{pp}		2100		MHz
BW_{SS}	-3dB Bandwidth	G = +10, V_{OUT} = 0.2V_{pp}		284		MHz
BW_{LS}	Large Signal Bandwidth	G = +10, V_{OUT} = 2V_{pp}		117		MHz
$BW_{0.1dBSS}$	0.1dB Gain Flatness Small Signal	G = +10, V_{OUT} = 0.2V_{pp}		42		MHz
$BW_{0.1dBLS}$	0.1dB Gain Flatness Large Signal	G = +10, V_{OUT} = 2V_{pp}		47		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		2.2		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		11		ns
OS	Overshoot	V_{OUT} = 1V step		3		%
SR	Slew Rate	4V step		410		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 10MHz		-81		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 10MHz		-75		dBc
THD	Total Harmonic Distortion	2V_{pp}, 5MHz		-74		dB
e_n	Input Voltage Noise	> 100kHz		0.6		nV/√Hz
i_n	Input Current Noise	> 100kHz		4.2		pA/√Hz
DC Performance						
V_{IO}	Input Offset Voltage (1)		-1	0.35	1	mV
dV_{IO}	Average Drift			4.4		µV/°C
I_b	Input Bias Current (1)		-60	30	60	µA
dI_b	Average Drift			44		nA/°C
I_o	Input Offset Current			0.8	6	µA
PSRR	Power Supply Rejection Ratio (1)	DC	78	83		dB
A_{OL}	Open-Loop Gain (1)	V_{OUT} = V_S / 2	74	83		dB
I_S	Supply Current (1)	per channel		12.5	16	mA
Disable Characteristics						
t_{ON}	Turn On Time	1V step, 1% settling		125		ns
t_{OFF}	Turn Off Time			840		ns
OFF_{ISO}	Off Isolation	2V_{pp}, 5MHz		80		dB
$OFFC_{OUT}$	Off Output Capacitance			5.6		pF
V_{OFF}	Power Down Voltage	Disabled if $\overline{DIS}$ pin is grounded or pulled below V_{OFF}	Disabled if $\overline{DIS}$ < 1.3			V
V_{ON}	Enable Voltage	Enabled if $\overline{DIS}$ pin is floating or pulled above V_{ON}	Enabled if $\overline{DIS}$ > 3			V
I_{SD}	Disable Supply Current (1)	No Load, $\overline{DIS}$ pin tied to ground		180	225	µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		4		MΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Common Mode Input Range			-4.3 to 5.1		V
CMRR	Common Mode Rejection Ratio (1)	DC , V_{cm}=-3.5V to 4V	75	90		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 500Ω (1)	-3.8	±4	3.8	V
		R_L = 2kΩ		±4		V
I_{OUT}	Output Current			±130		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±160		mA

Notes:

1. 100% tested at 25°C

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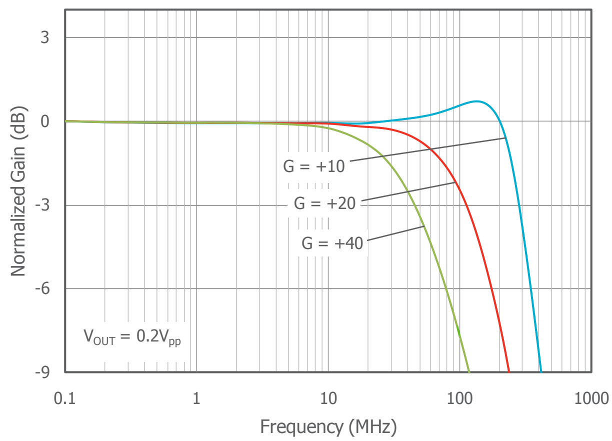
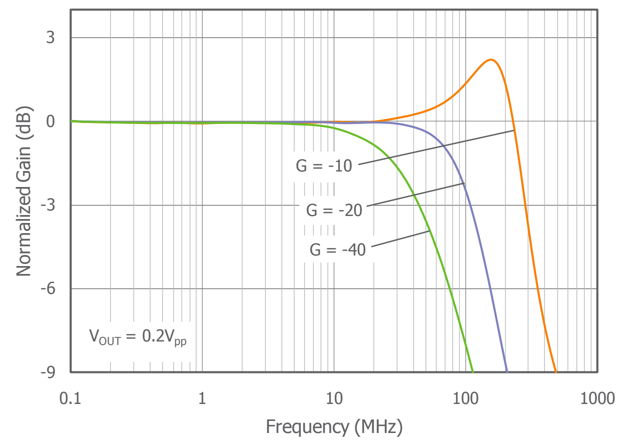
Typical Performance Characteristics

$T_A = 25°C$, $V_S = ±5V$, $R_f = 200Ω$, $R_L = 500Ω$, $G = 10$; unless otherwise noted.

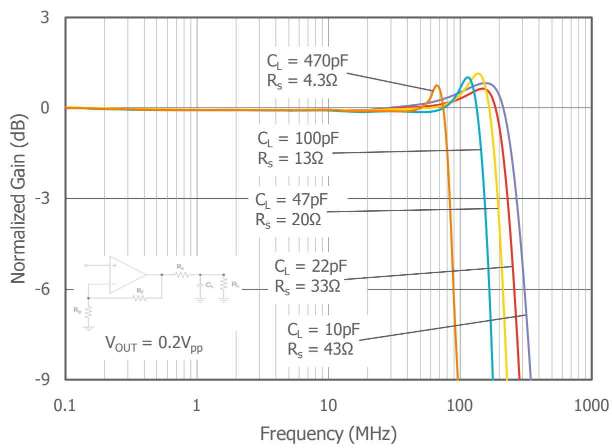
Non-Inverting Frequency Response



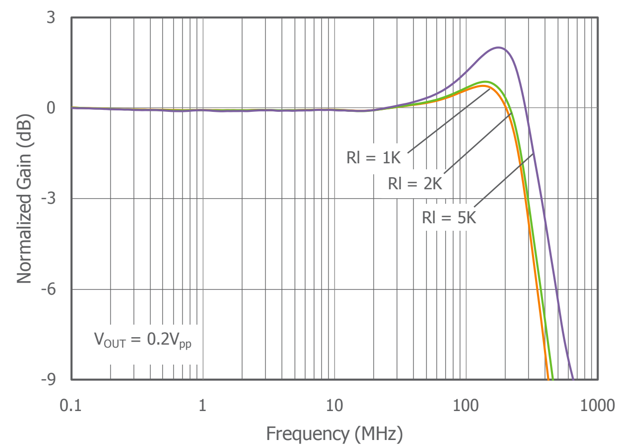
Inverting Frequency Response



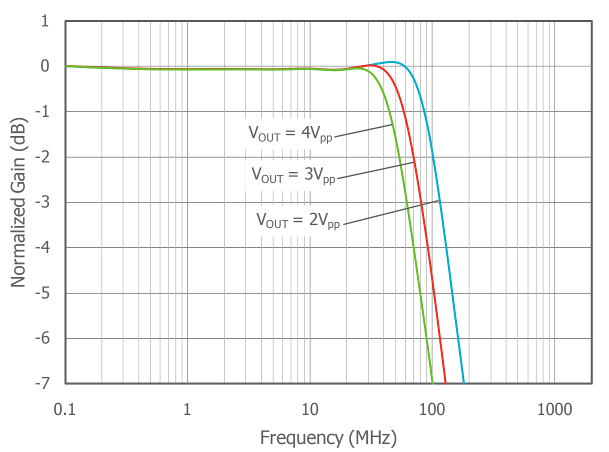
Frequency Response vs. C_L



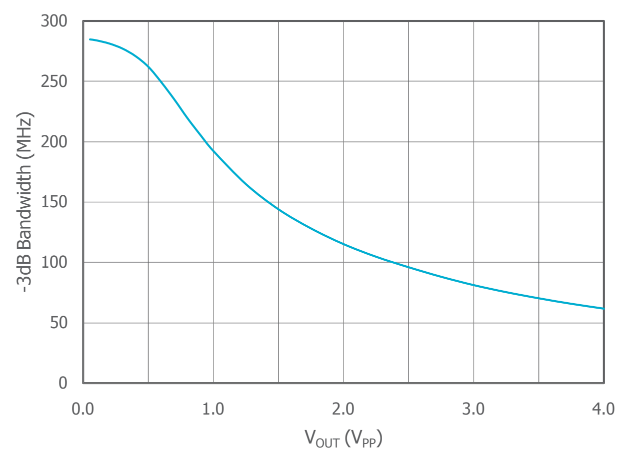
Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



-3dB Bandwidth vs. Output Voltage



COMLINEAR CLC1001 Ultra-Low Noise Amplifier Rev 1G

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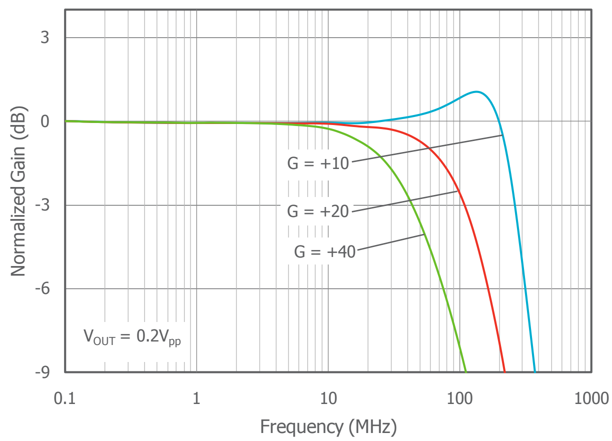
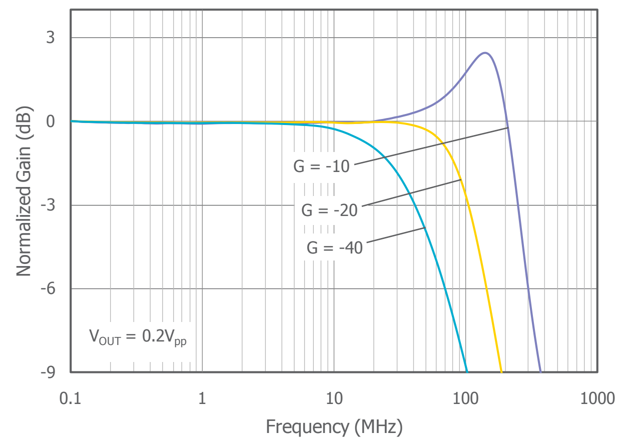
Typical Performance Characteristics

$T_A = 25°C$, $V_s = \pm5V$, $R_f = 200\Omega$, $R_L = 500\Omega$, $G = 10$; unless otherwise noted.

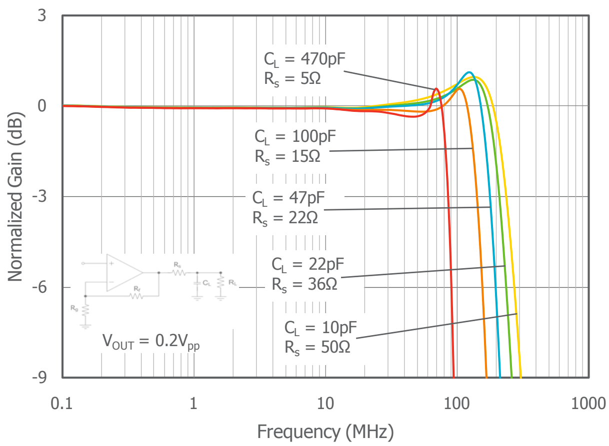
Non-Inverting Frequency Response at V_S = 5V



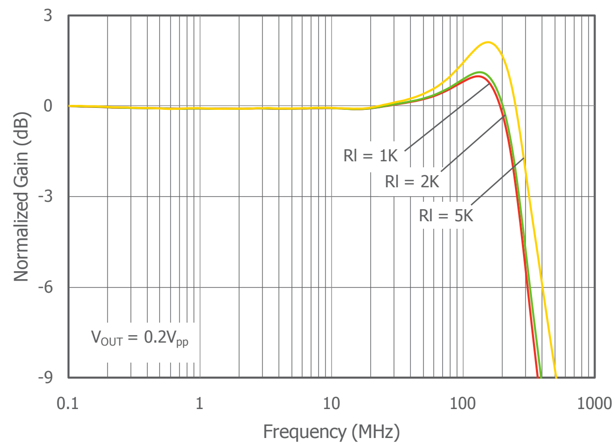
Inverting Frequency Response at V_S = 5V



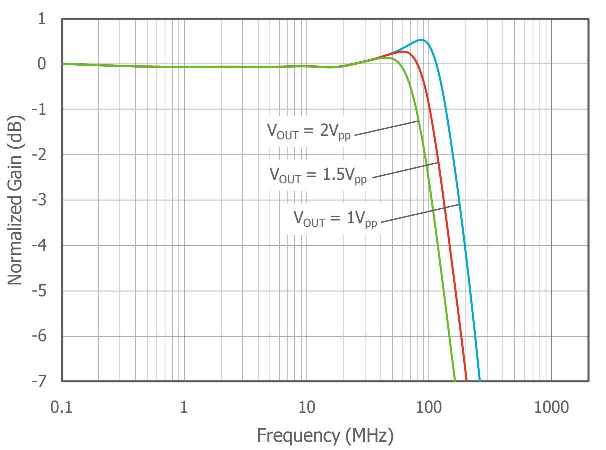
Frequency Response vs. C_L at V_S = 5V



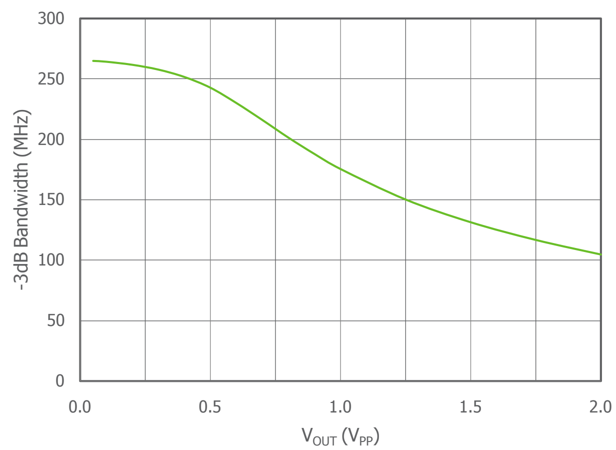
Frequency Response vs. R_L at V_S = 5V



Frequency Response vs. V_{OUT} at V_S = 5V



-3dB Bandwidth vs. Output Voltage at V_S = 5V



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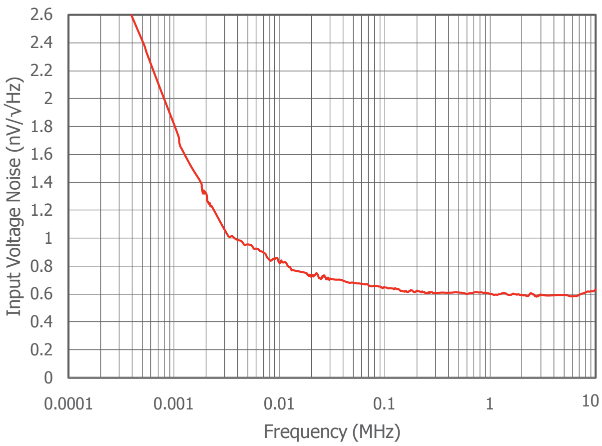
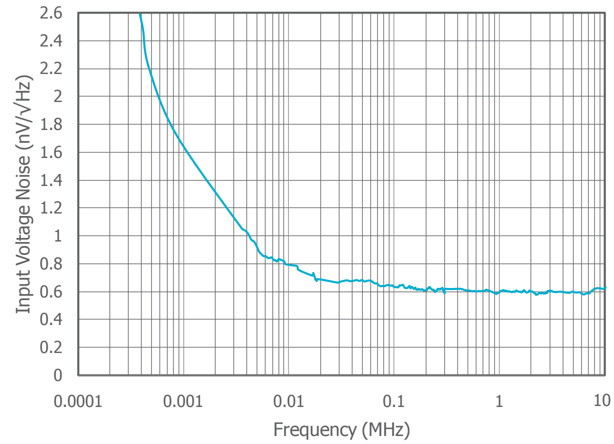
Typical Performance Characteristics - Continued

$T_A = 25°C$, $V_s = \pm 5V$, $R_f = 200\Omega$, $R_L = 500\Omega$, G = 10; unless otherwise noted.

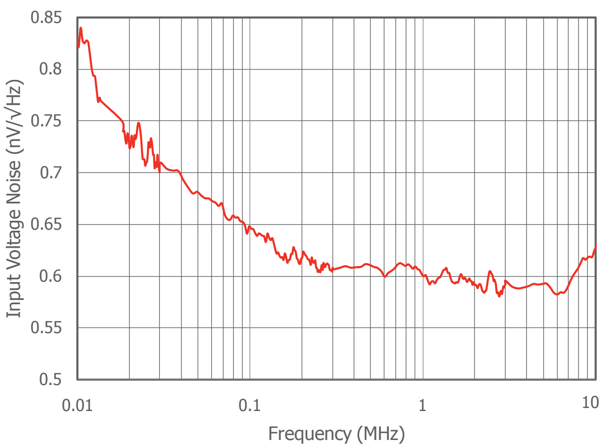
Input Voltage Noise



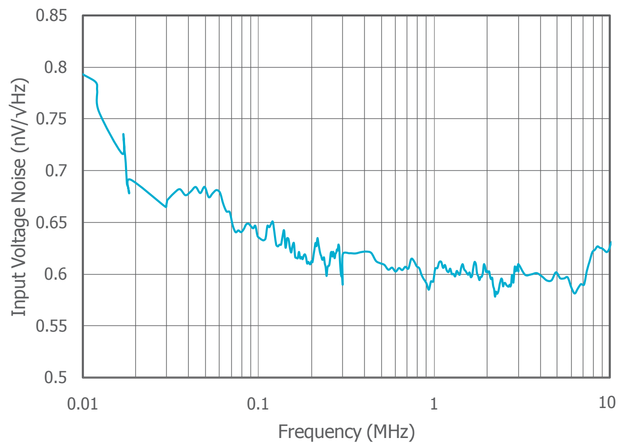
Input Voltage Noise at V_S = 5V



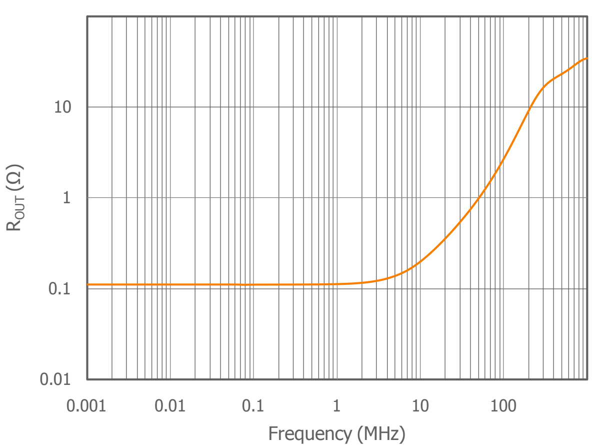
Input Voltage Noise (>10kHz)



Input Voltage Noise at V_S = 5V (>10kHz)



R_{OUT} vs. Frequency



COMLINEAR CLC1001 Ultra-Low Noise Amplifier Rev 1G

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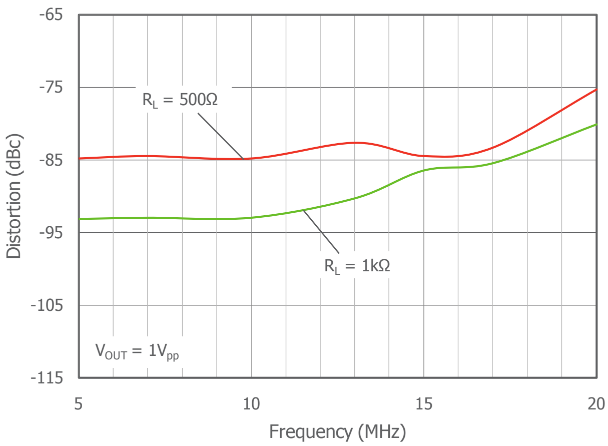
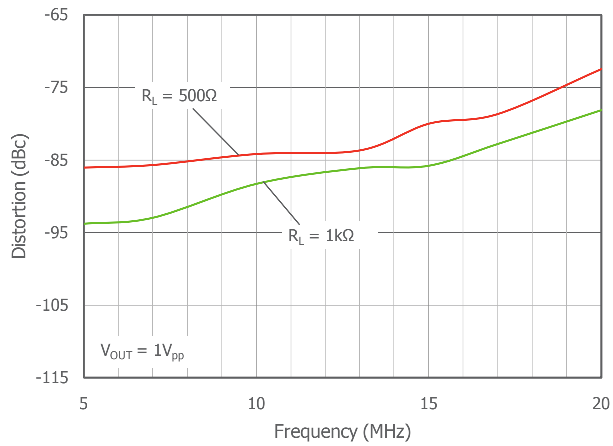
Typical Performance Characteristics - Continued

T_A = 25°C, V_s = ±5V, R_f = 200Ω, R_L = 500Ω, G = 10; unless otherwise noted.

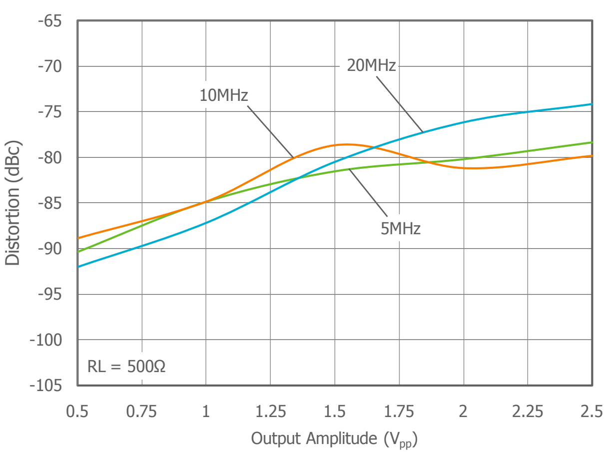
2nd Harmonic Distortion vs. R_L



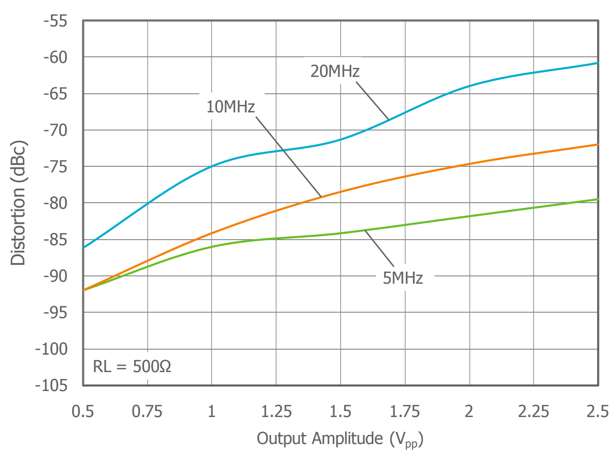
3rd Harmonic Distortion vs. R_L



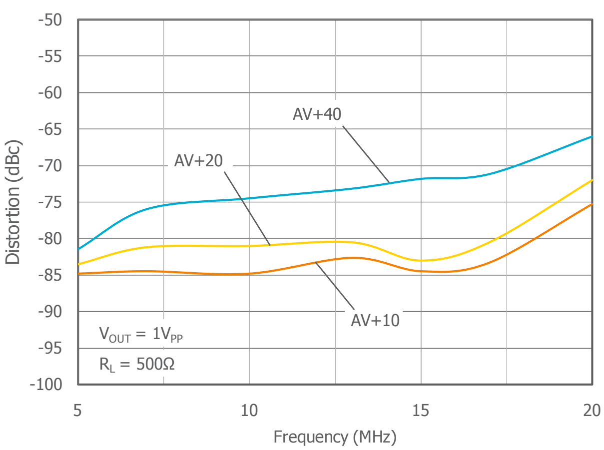
2nd Harmonic Distortion vs. V_{OUT}



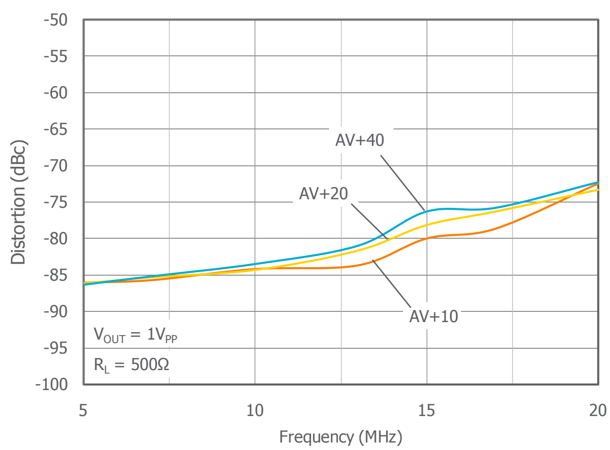
3rd Harmonic Distortion vs. V_{OUT}



2nd Harmonic Distortion vs. Gain



3rd Harmonic Distortion vs. Gain



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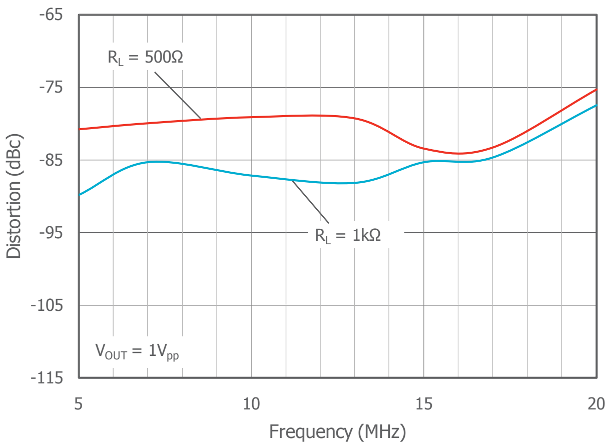
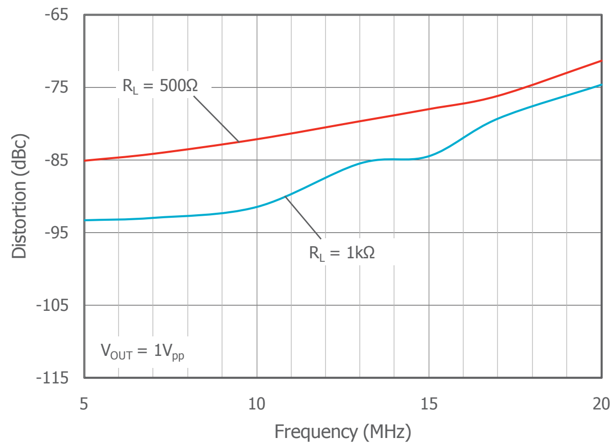
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = ±5V, R_f = 200Ω, R_L = 500Ω, G = 10; unless otherwise noted.

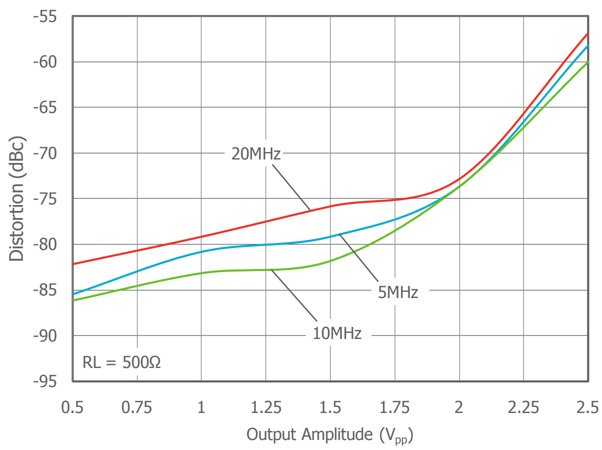
2nd Harmonic Distortion vs. R_L at V_S = 5V



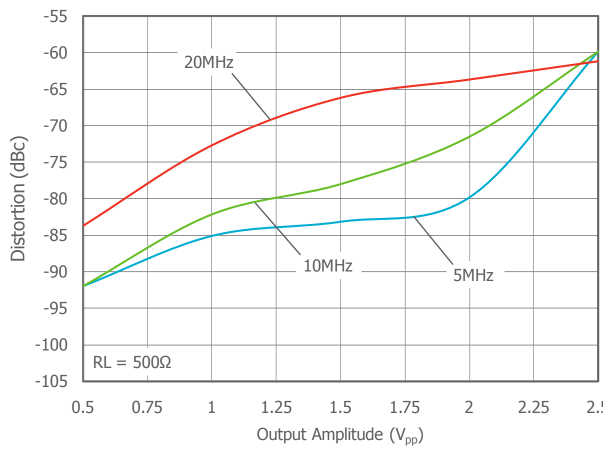
3rd Harmonic Distortion vs. R_L at V_S = 5V



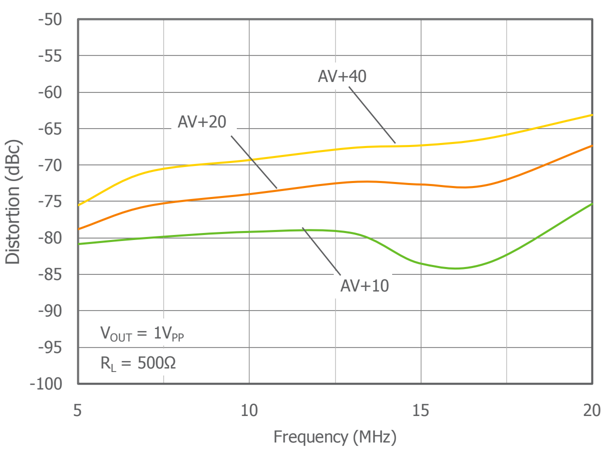
2nd Harmonic Distortion vs. V_{OUT} at V_S = 5V



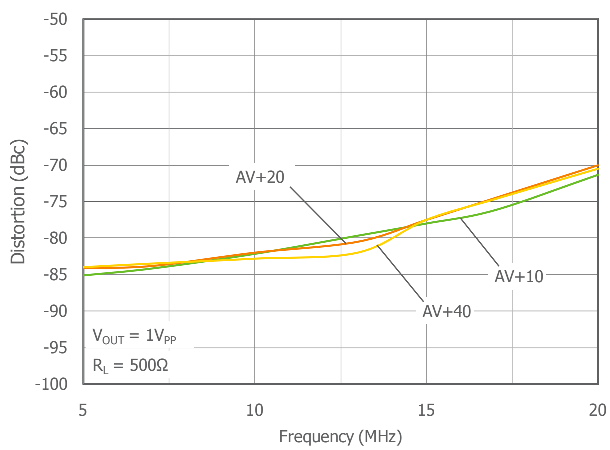
3rd Harmonic Distortion vs. V_{OUT} at V_S = 5V



2nd Harmonic Distortion vs. Gain at V_S = 5V



3rd Harmonic Distortion vs. Gain at V_S = 5V



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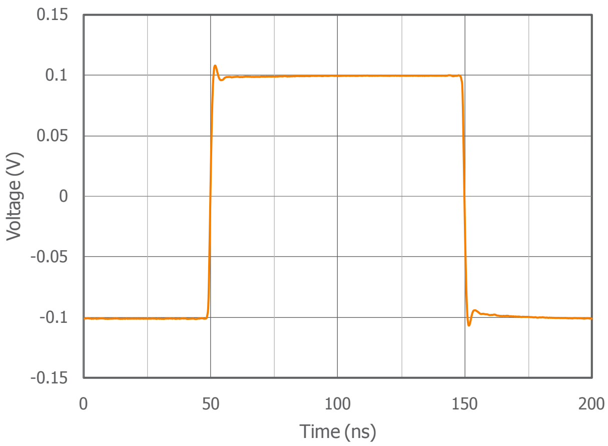
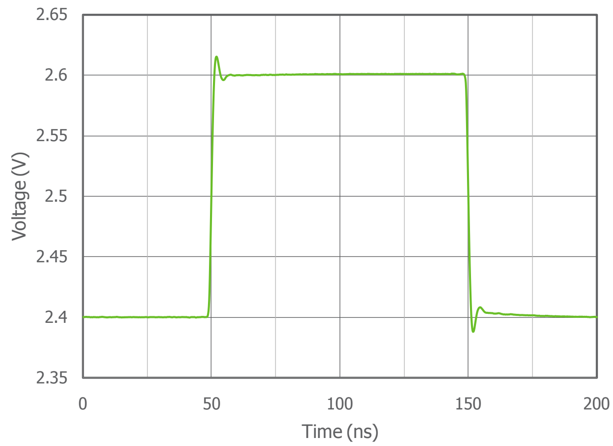
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = ±5V, R_f = 200Ω, R_L = 500Ω, G = 10; unless otherwise noted.

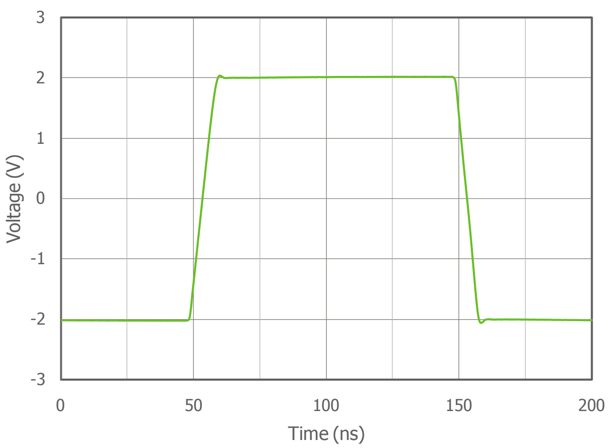
Small Signal Pulse Response



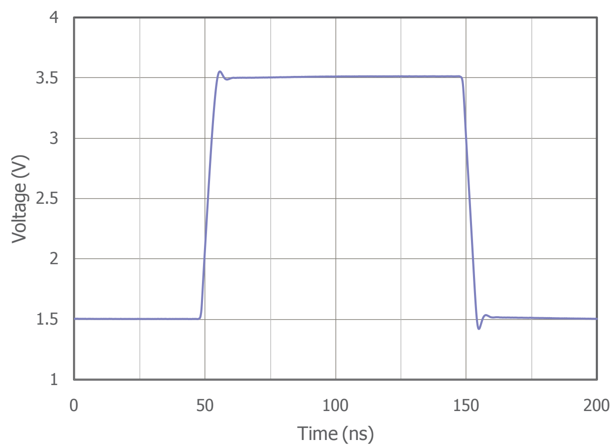
Small Signal Pulse Response at V_S = 5V



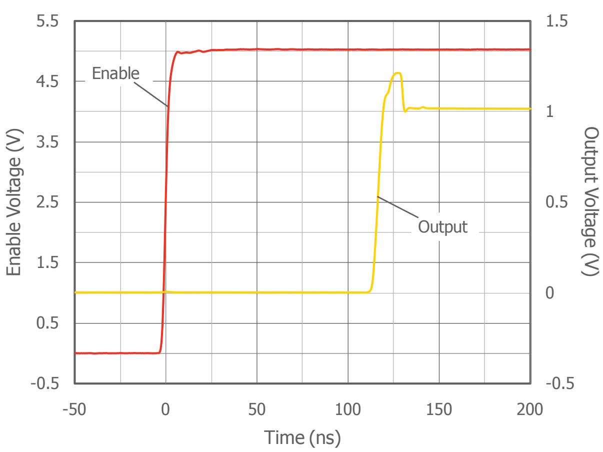
Large Signal Pulse Response



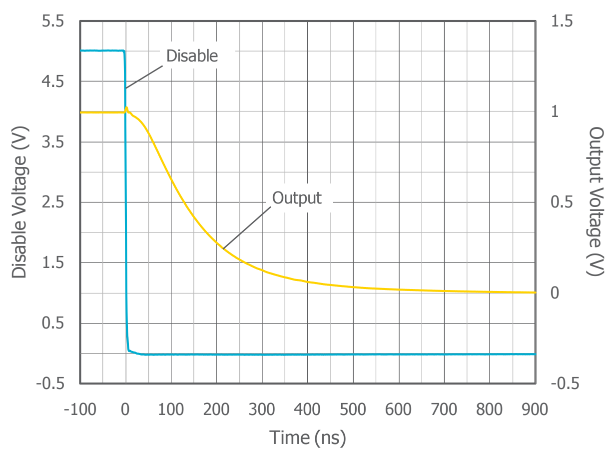
Large Signal Pulse Response at V_S = 5V



Enable Response



Disable Response



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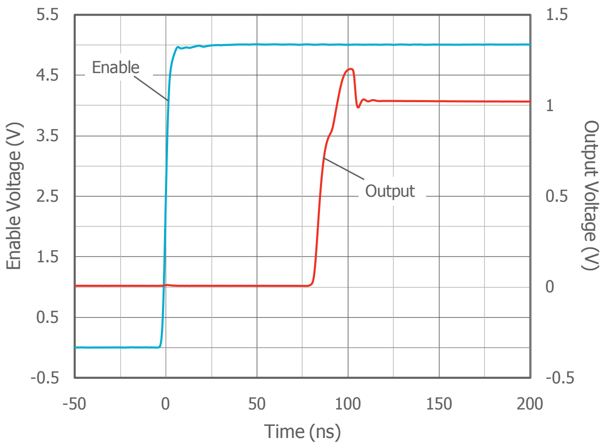
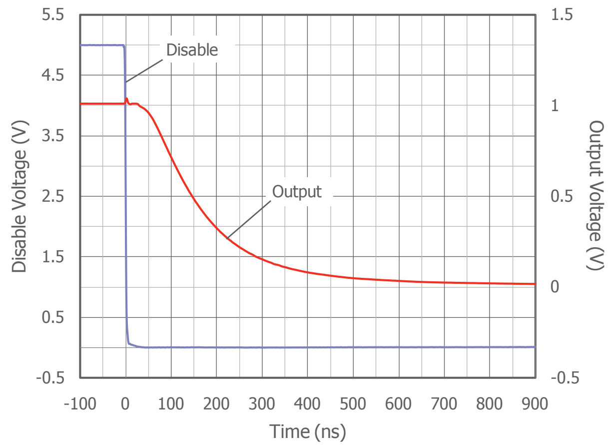
Typical Performance Characteristics - Continued

$T_A = 25°C$, $V_S = \pm5V$, $R_f = 200\Omega$, $R_L = 500\Omega$, G = 10; unless otherwise noted.

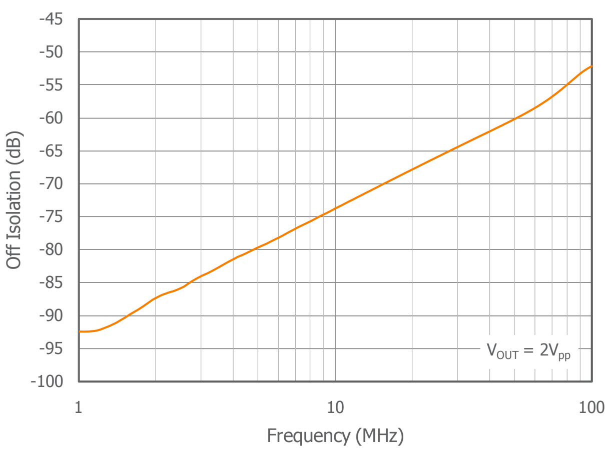
Enable Response at V_S = 5V



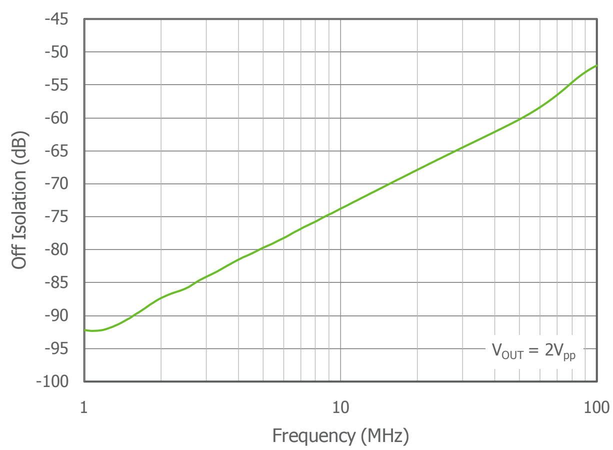
Disable Response at V_S = 5V



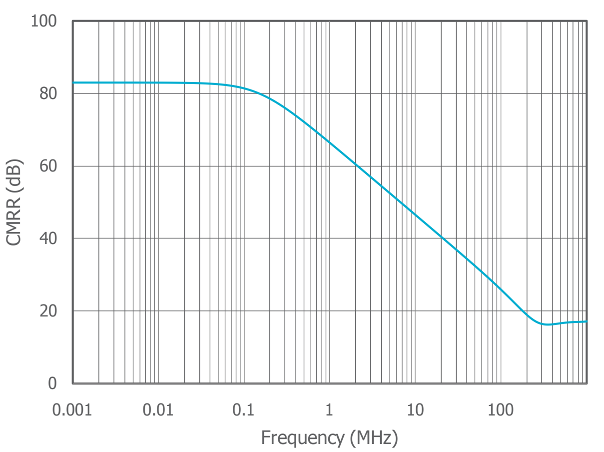
Off Isolation



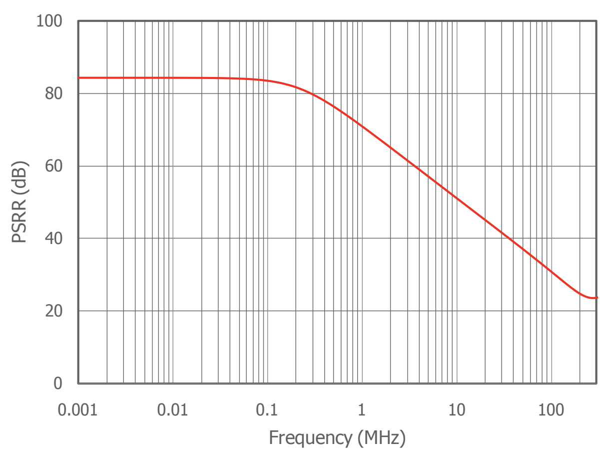
Off Isolation at V_S = 5V



CMRR vs. Frequency



PSRR vs. Frequency



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Application Information

Basic Operation

Figures 1 and 2 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

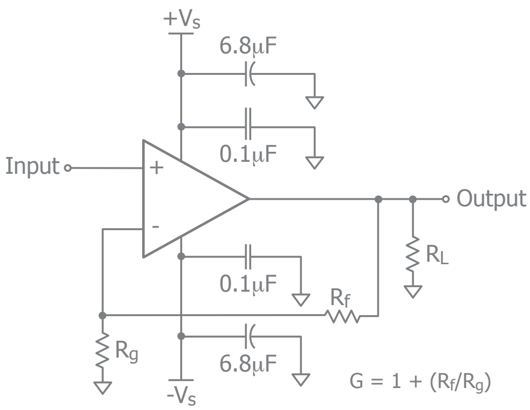

Figure 1. Typical Non-Inverting Gain Circuit

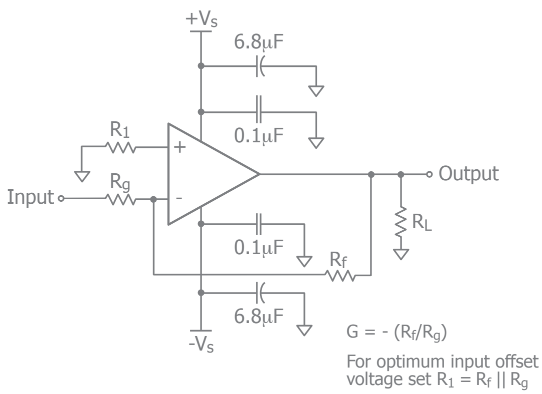

Figure 2. Typical Inverting Gain Circuit

Achieving Low Noise in an Application

Making full use of the low noise of the CLC1001 requires careful consideration of resistor values. The feedback and gain set resistors (R_f and R_g) and the non-inverting source impedance (R_{source}) all contribute noise to the circuit and can easily dominate the overall noise if their values are too high. The datasheet is specified with an R_g of 22.1Ω, at which point the noise from R_f and R_g is about equal to the noise from the CLC1001. Lower value resistors could be used at the expense of more distortion. Figure 3 shows total input voltage noise (amp+resistors) versus R_f and R_g. As the value of R_f increases, the total input referred noise also increases.

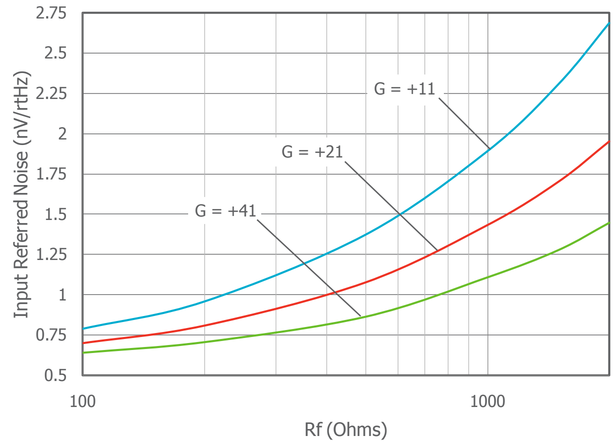

Figure 3: Input Referred Voltage Noise vs. R_f and R_g

The noise caused by a resistor is modeled with either a voltage source in series with the resistance:

$$\sqrt{4kTR}$$

Or a current source in parallel with it:

$$i_R = \sqrt{\frac{4kT}{R}}$$

Op amp noise is modeled with three noise sources, e_n, i_n and i_i. These three sources are analogous to the DC input voltage and current errors V_{os}, I_{bn} and I_{bi}.

The noise models must be analyzed in-circuit to determine the effect on the op amp output noise.

Since noise is statistical in nature rather than a continuous signal, the set of noise sources in circuit add in an RMS (root mean square) fashion rather than in a linear fashion. For uncorrelated noise sources, this means you add the squares of the noise voltages. A typical non-inverting application (see figure 1) results in the following noise at the output of the op amp:

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$$e_o^2 = e_n^2\left(1+\frac{R_f}{R_g}\right)^2 + in^2R_s{}^2\left(1+\frac{R_f}{R_g}\right)^2 + i_i^2R_f^2$$

op amp noise terms e_n, i_n and i_i

$$+\ e_{Rs}^2\left(1+\frac{R_f}{R_g}\right)^2 + e_{Rg}^2\left(\frac{R_f}{R_g}\right)^2 + e_{Rf}^2$$

external resistor noise terms for R_S, R_g and R_f

High source impedances are sometimes unavoidable, but they increase noise from the source impedance and also make the circuit more sensitive to the op amp current noise. Analyze all noise sources in the circuit, not just the op amp itself, to achieve low noise in your application.

Power Dissipation

Power dissipation should not be a factor when operating under the stated 500Ω load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$$R_L \ || \ (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

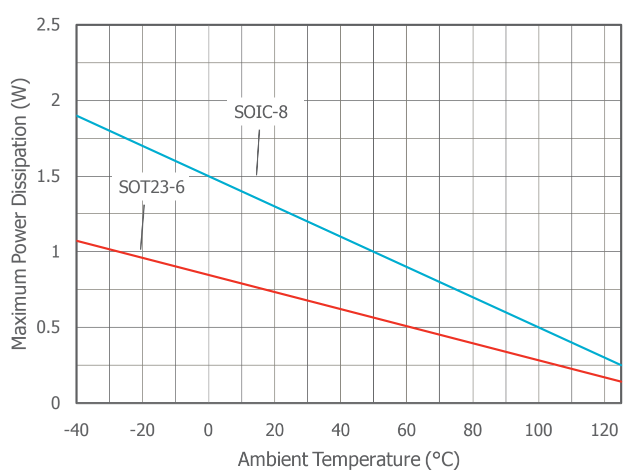

Figure 4. Maximum Power Derating

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Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

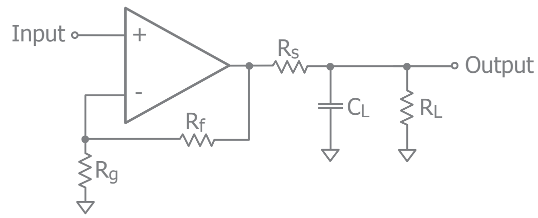

Figure 5. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in <=1dB peaking in the frequency response. The Frequency Response vs. C_L plots, on page 7, illustrates the response of the CLC1001.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10	43	266
22	33	228
47	20	192
100	13	155
470	4.3	84

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1001 will typically recover in less than 25ns from an overdrive condition. Figure 6 shows the CLC1001 in an overdriven condition.

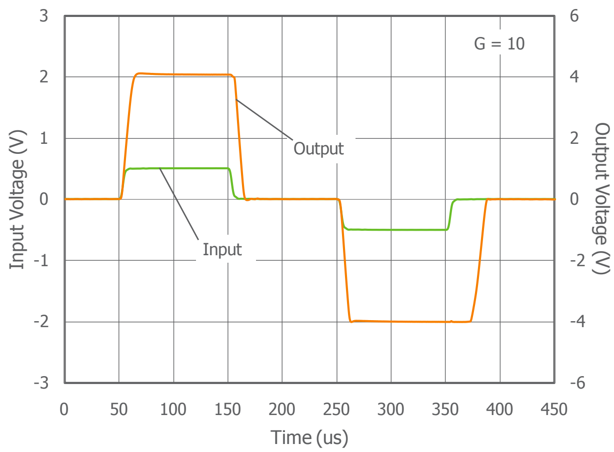

Figure 6. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1001 in SOT23-5
CEB003	CLC1001 in SOIC-8

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Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-11. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -V_S pin of the amplifier is not directly connected to the ground plane.

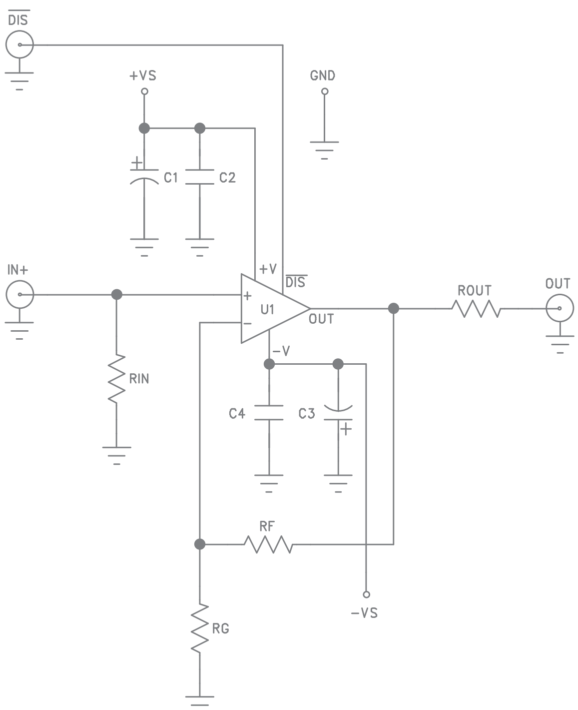

Figure 7. CEB002/CEB003 Schematic

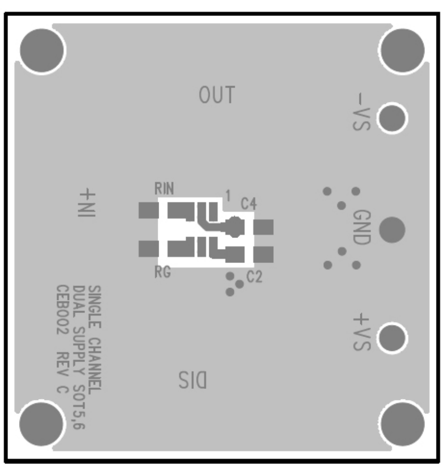

Figure 8. CEB002 Top View

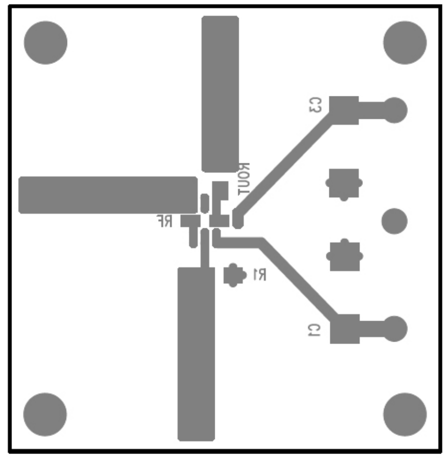

Figure 9. CEB002 Bottom View

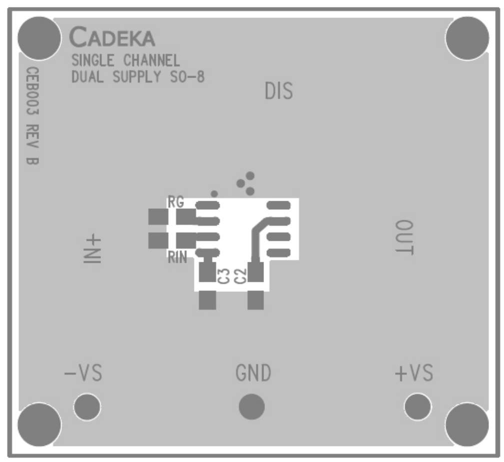

Figure 10. CEB003 Top View

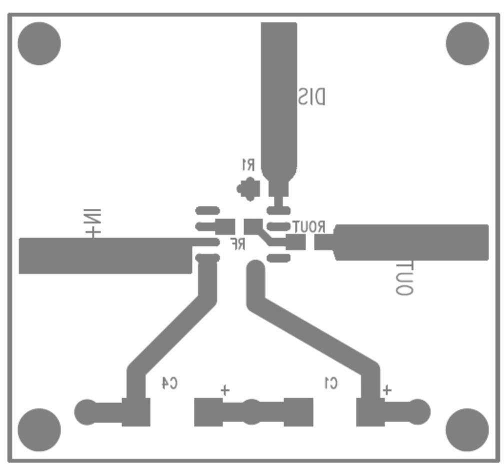

Figure 11. CEB003 Bottom View

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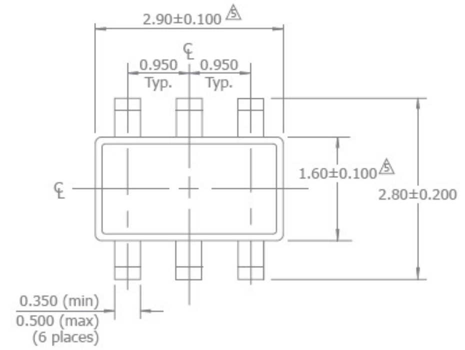
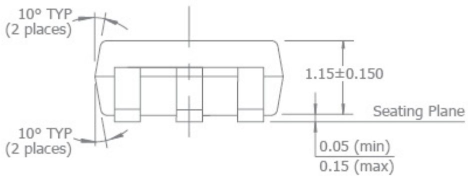
Mechanical Dimensions

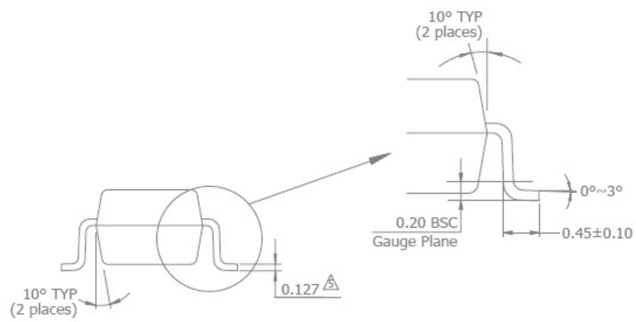
SOT23-6 Package



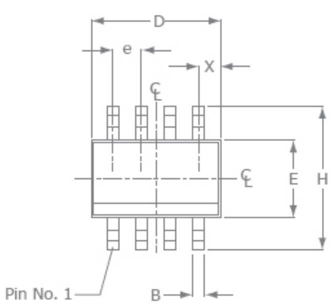
NOTES:

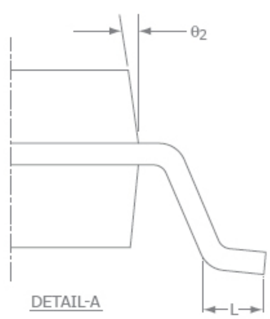
1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.
5. Dimension are exclusive of mold flash and gate burr.
6. Dimension are exclusive of solder plating.



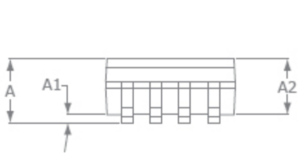


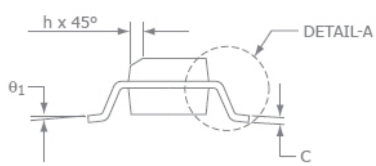
SOIC-8 Package





SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	





NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

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