

# N5 ANT SoC Module Series

## ANT<sup>®</sup> Operation (when loaded with the latest S210 or S310 SoftDevice)

- 79 selectable RF channels (2402 to 2480 MHz)
- Simple to complex network topologies: peer-to-peer, star, tree, star-to-star and more
- Broadcast, acknowledged, and burst data communication modes
- Built-in device search and pairing
- Built-in interference handling and radio coexistence management with application radio disable requests and application flash write/erase requests
- Enhanced ANT features
  - Supports up to 15 logical channels each with configurable channel periods (5.2ms - 2s)
  - Advanced burst data transfer modes (up to 60kbps)
  - Optional channel encryption mode (AES-128)
  - Supports up to 8 public, private and/or managed networks
  - Advanced power management features to optimize application power consumption including Event Filtering and Selective data updates
  - Asynchronous transmit channel
  - Fast channel initiation

## ANT/BLUETOOTH<sup>®</sup> Low Energy Peripheral Operation (when loaded with the latest S310 SoftDevice)

- ANT operation functions as S210
- BLUETOOTH 4.2 compliant low energy single-mode protocol stack
  - Link Layer
  - L2CAP, ATT, and SM protocols
  - GATT, GAP, and L2CAP APIs
  - Peripheral and Central roles
  - GATT Client and Server
  - Full SMP support including MITM protection and OOB pairing



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## Module Hardware

- Integrated PCB meander antenna
- On-board 32 kHz and 16 MHz crystal clocks
- 1.8V to 3.6V supply voltage range
- DC/DC converter
- Operating temperature:
  - -25°C to +75°C (N5150 and N548)
  - -40°C to +85°C (N550)
- 24 GPIOs (LGA package)
- Programmable output per channel from -20dBm up to +4dBm
- Excellent receiver sensitivity -90dBm ANT mode
- -93dBm BLE mode
  - 1dBm resolution RSSI
  - Total 256kB embedded flash memory and 16kB/32kB RAM
  - SPI, I2C and UART interface
  - ARM SWD interface
  - 14.0x9.8x2.0mm (LGA package)
  - Drop-in compatible options with AP2/C7 modules
  - Radio regulatory approval for major markets
  - BLUETOOTH SIG qualification
  - RoHS compliant

## Series Members

- N5150M8CD, N5150M4CD, N5150M5CD
- N550M8CC, N550M4CC
- N548M8CB, N548M4CB, N548M5CB

All these modules are pre-loaded with the S210 SoftDevice, the ANT-WP bootloader and an ANT network processor application code

D00001598 Rev 2.3

## Contents

|          |                                                            |           |
|----------|------------------------------------------------------------|-----------|
| <b>1</b> | <b>N5 ANT SoC Module Series</b>                            | <b>8</b>  |
| 1.1      | Nomenclature                                               | 8         |
| 1.2      | Production Tracking Code                                   | 9         |
| 1.3      | Models                                                     | 9         |
| 1.4      | N5 ANT SoC Module Starter Kit                              | 10        |
| <b>2</b> | <b>Product Overview</b>                                    | <b>11</b> |
| 2.1      | Block Diagram                                              | 11        |
| 2.2      | Pin-outs                                                   | 11        |
| 2.3      | N5 Module Preloaded Software                               | 13        |
| 2.4      | N5 Module Programming                                      | 13        |
| 2.4.1    | Programming via SWD Interface                              | 14        |
| 2.4.2    | Programming Over the Air                                   | 14        |
| 2.4.3    | Initializing the SoftDevice                                | 14        |
| 2.4.4    | Configuring the DC/DC Converter                            | 14        |
| 2.5      | Design Considerations                                      | 14        |
| 2.5.1    | M8 Module Mounting                                         | 14        |
| 2.5.2    | M4 Module Mounting                                         | 15        |
| 2.5.3    | M5 Module Mounting                                         | 15        |
| 2.6      | Assembly Considerations                                    | 15        |
| 2.6.1    | Moisture Control                                           | 15        |
| 2.6.2    | Solder Stencil Design of M8 Module                         | 16        |
| 2.6.3    | Cleaning Process                                           | 16        |
| <b>3</b> | <b>Regulatory Approvals and Compliances</b>                | <b>17</b> |
| 3.1      | United States                                              | 17        |
| 3.2      | Canada                                                     | 17        |
| 3.3      | European Economic Area and Great Britain                   | 18        |
| 3.4      | Australia & New Zealand                                    | 18        |
| 3.5      | Japan                                                      | 18        |
| 3.6      | BLUETOOTH Qualification                                    | 18        |
| <b>4</b> | <b>Electrical Specifications</b>                           | <b>19</b> |
| 4.1      | Absolute Maximum Ratings                                   | 19        |
| 4.2      | Recommended Operating Conditions                           | 19        |
| 4.3      | Industrial Temperature Range                               | 19        |
| 4.4      | Radio Operation Specifications and Antenna Characteristics | 19        |
| 4.5      | Electrical Specifications                                  | 20        |
| <b>5</b> | <b>Mechanical Drawings</b>                                 | <b>21</b> |
| <b>6</b> | <b>Support</b>                                             | <b>24</b> |
| 6.1      | ANT Forum                                                  | 24        |
| 6.2      | Technical References                                       | 24        |

|                                                                           |                                                                  |           |
|---------------------------------------------------------------------------|------------------------------------------------------------------|-----------|
| 6.3                                                                       | ANT Developer’s Zone .....                                       | 24        |
| 6.4                                                                       | ANT and ANT+ Social Media .....                                  | 25        |
| <b>Appendix A: Using the ANT Network Processor Configuration .....</b>    |                                                                  | <b>26</b> |
| 1.                                                                        | Pin Assignments in the ANT Network Processor Configuration ..... | 26        |
| 2.                                                                        | Asynchronous Serial Mode .....                                   | 27        |
| 3.                                                                        | Byte Synchronous Serial Mode .....                               | 29        |
| 4.                                                                        | ANT-WP Bootloader Activation .....                               | 29        |
|                                                                           | Using BOOT Pin .....                                             | 30        |
|                                                                           | Using Serial Command .....                                       | 30        |
| 5.                                                                        | DC/DC Configuration .....                                        | 31        |
| <b>Appendix B: Using the ANT Bootloader for OTA Firmware Update .....</b> |                                                                  | <b>32</b> |
| 1.                                                                        | Operational Memory Layout .....                                  | 32        |
| 2.                                                                        | Entering Bootloader Mode .....                                   | 33        |
| 3.                                                                        | Bootloader ANT-FS Functionality .....                            | 33        |
|                                                                           | ANT-FS Configuration .....                                       | 34        |
| 4.                                                                        | OTA Firmware Update Procedure .....                              | 34        |
|                                                                           | Example Usage .....                                              | 34        |
|                                                                           | Image Activation .....                                           | 36        |
| <b>Appendix C: N5 Module Pre-Loaded Software Versions .....</b>           |                                                                  | <b>37</b> |
| 1.                                                                        | Key functional changes in N550 and N5150 .....                   | 37        |
| 2.                                                                        | Key functional changes in rev B over rev A .....                 | 37        |

## Figures

|                                                                    |    |
|--------------------------------------------------------------------|----|
| Figure 1: N5 ANT SoC Module Series Nomenclature.....               | 8  |
| Figure 2: Production Tracking Code .....                           | 9  |
| Figure 3: N5 ANT SoC Module Series Block Diagram .....             | 11 |
| Figure 4: N5 M8 LGA Bottom View.....                               | 11 |
| Figure 5: N5 M4 Bottom View .....                                  | 11 |
| Figure 6: N5 M5 Module Bottom View .....                           | 12 |
| Figure 7: Memory Map of the Preloaded Software .....               | 13 |
| Figure 8: N5 M8 Module Mounting (all dimensions in mm) .....       | 15 |
| Figure 9: N5 M4 Module Mounting .....                              | 15 |
| Figure 10: Solder Stencil Reference .....                          | 16 |
| Figure 11: N5 M4 Module Typical Antenna Gain (dBi) .....           | 20 |
| Figure 12: N5 M8 Mechanical Drawing .....                          | 21 |
| Figure 13: N5 M4 Mechanical Drawing .....                          | 22 |
| Figure 14: N5 M5 Mechanical Drawing .....                          | 23 |
| Figure 15: Using ANT Network Processor .....                       | 26 |
| Figure 16: N5 M4 ANT NP Configuration Async Serial Connection..... | 28 |
| Figure 17: N5 M4 ANT NP Configuration Byte Sync Connection.....    | 29 |
| Figure 18: ANT-WP Bootloader Operational Memory Layout .....       | 32 |
| Figure 19: ANT Bootloader Topology .....                           | 34 |
| Figure 20: OTA Updater to PC Application .....                     | 35 |

## Tables

|                                                                            |    |
|----------------------------------------------------------------------------|----|
| Table 1: N5 ANT SoC Module Series Offerings .....                          | 9  |
| Table 2: N5 ANT SoC Module Starter Kit .....                               | 10 |
| Table 3: N5 ANT SoC Module Pin-Outs.....                                   | 12 |
| Table 4: Absolute Maximum Ratings .....                                    | 19 |
| Table 5: Recommended Operating Conditions.....                             | 19 |
| Table 6: N5 Module Antenna Gain .....                                      | 19 |
| Table 7: Current Consumption of Radio Operation.....                       | 20 |
| Table 8: Pin Assignments in ANT Network Processor Configuration .....      | 27 |
| Table 9: Asynchronous Serial Mode Baud Rate Select .....                   | 27 |
| Table 10 Byte-Sync Mode Speed Selection .....                              | 29 |
| Table 11: ANT OTA Update Enable Command.....                               | 30 |
| Table 12: ANT OTA Update Enable Response .....                             | 30 |
| Table 11: ANT DC/DC Configuration Command .....                            | 31 |
| Table 12: ANT DC/DC Configuration Response.....                            | 31 |
| Table 13: Summary of the ANT-WP Bootloader Operational Memory Layout ..... | 33 |
| Table 14: ANT-WP Bootloader Default ANT Channel Parameters .....           | 34 |
| Table 15: ANT-WP Bootloader ANT-FS Device Identification Parameters .....  | 34 |
| Table 16: N5 Module Versions and Factory Loaded Software .....             | 37 |

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## 1 N5 ANT SoC Module Series

Based on Nordic Semiconductor's nRF51422 SoC, the N5 ANT SoC module series offers support for both ANT® and Bluetooth® low energy and enables both protocols to run concurrently, depending on the loaded protocol stack.

The N5 ANT SoC module series starts with the M8 model in a 14.0mm x 9.8mm x 2.0mm LGA (Land Array Grid) package. A compact design meeting the market requirements for small, light and wearable, the M8 model is a turnkey system hardware solution including antenna, onboard 32 kHz and 16 MHz crystal clocks, DC/DC converter and 24 GPIOs with 6 analogue inputs.

The N5 modules are pre-programmed with the following software components:

- S210 SoftDevice (scalable ANT protocol stack with max. 15 channels)
- ANT network processor application
- ANT-WP (Wireless Programming) bootloader

SoftDevices are protocol stack solutions from Nordic Semiconductor for the nRF51 SoCs. There are multiple SoftDevice choices available from the Nordic Semiconductor's web site. The ANT network processor application provides the standard ANT serial interface front-end that is connectable to an external application controller. The ANT-WP bootloader allows over-the-air updates of any software components on the N5 module.

The N5 module's pre-programmed image can be easily replaced via the onboard SWD interface pins using off-the-shelf ARM programming tools or over the air using the pre-loaded ANT-WP bootloader.

Pin compatible options for the 20mm x 20mm AP2 or C7 modules from Garmin Canada Inc. (formerly Dynastream) are also available. In these M4 and M5 model options, N5 M8 models are soldered on carrier boards that are pin compatible to the previous modules. Current AP2 or C7 module customers can easily use these models to evaluate the hardware and upgrade their products.

The N5 module series, if loaded with the ANT and/or BLUETOOTH low energy stack has been certified to comply with radio regulation or standards covering major markets include North America, Europe, Great Britain, Australia, New Zealand and Japan. The N5 ANT SoC modules series has also been qualified by the BLUETOOTH SIG.

### 1.1 Nomenclature

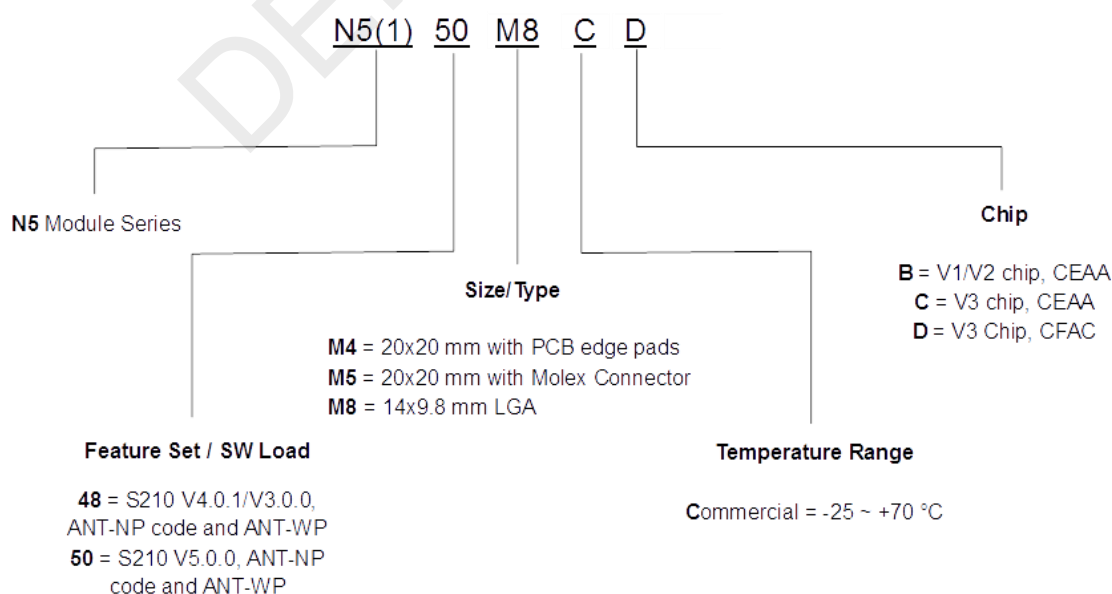
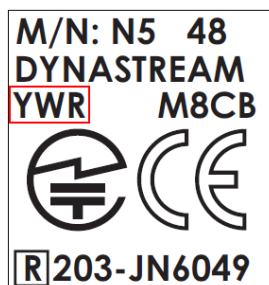


Figure 1: N5 ANT SoC Module Series Nomenclature



## 1.2 Production Tracking Code

For technical support and customer service purposes, a production code of three characters is laser marked on the RF shield as illustrated below. In the code, YW denotes production date code and R denotes module version.

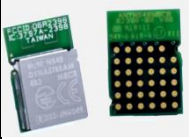


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Figure 2: Production Tracking Code

Please refer to Appendix C: N5 Module Pre-Loaded Software Versions for differences and important notes of each version.

## 1.3 Models

|                                                                                     | Part Number             | Size (mm)        | Connection                                                           | Chip              | RAM Size | Preloaded Software |             |             |
|-------------------------------------------------------------------------------------|-------------------------|------------------|----------------------------------------------------------------------|-------------------|----------|--------------------|-------------|-------------|
|                                                                                     |                         |                  |                                                                      |                   |          | SoftDevice         | ANT-NP      | ANT-WP      |
|  | N5150M8CD               | 14.0 x 9.8 x 2.0 | LGA package, 31 pads, 24 GPIOs.                                      | nRF51422-CFAC, V3 | 32k      | S210 V5.0.0        | BAW4.0 0B00 | BFD2.00 B00 |
|                                                                                     | N550M8CC                |                  |                                                                      | nRF51422-CEAA, V3 | 16k      |                    |             |             |
|                                                                                     | N548M8CB <sup>(1)</sup> |                  |                                                                      | nRF51422-CEAA, V2 | 16k      | S210 V4.0.1        | BAW3.0 0B00 | BFD1.00 B00 |
|  | N5150M4CD               | 20.0 x 20.0      | 17 pins, SMT mount, 13 GPIOs                                         | nRF51422-CFAC, V3 | 32k      | S210 V5.0.0        | BAW4.0 0B00 | BFD2.00 B00 |
|                                                                                     | N550M4CC                |                  |                                                                      | nRF51422-CEAA, V3 | 16k      |                    |             |             |
|                                                                                     | N548M4CB <sup>(1)</sup> |                  |                                                                      | nRF51422-CEAA, V2 | 16k      | S210 V4.0.1        | BAW3.0 0B00 | BFD1.00 B00 |
|  | N5150M5CD               | 20.0 x 20.0      | 20 pin Molex connector. Onboard JTAG programming connector. 13 GPIOs | nRF51422-CFAC, V3 | 32k      | S210 V5.0.0        | BAW4.0 0B00 | BFD2.00 B00 |
|                                                                                     | N548M5CB <sup>(1)</sup> |                  |                                                                      | nRF51422-CEAA, V2 | 16k      | S210 V4.0.1        | BAW3.0 0B00 | BFD1.00 B00 |

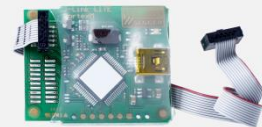
Note 1: Applies to rev B. Rev A module are pre-loaded with S210 V3.0.0 and BAW2.02B00 ANT NP code.

Table 1: N5 ANT SoC Module Series Model List

## 1.4 N5 ANT SoC Module Starter Kit

The N5 ANT SoC Module Starter Kit, ordering number “N5DK1”, contains all the pieces you need to start evaluation and development using the N5 ANT SoC module, as well as the nRF51422 IC.

The kit contains the following hardware pieces as described in Table 2, with a pre-loaded application ready to be demonstrated when opening the box. Additional reference application code is available on <https://www.thisisant.com/developer/components/n5/>. Most of the parts are orderable individually to create a more complex network.

| Order Number | Part Description                                                                 | Quantity |                                                                                       |
|--------------|----------------------------------------------------------------------------------|----------|---------------------------------------------------------------------------------------|
| N5150M5CD*   | Module with 20-pin Molex connector                                               | 2        |    |
| ANTBAT2      | Battery board with a Molex socket, a reset button and a five-position dip switch | 1        |    |
| ANTIO1       | I/O board with a Molex connector, a Molex socket, 4 LEDs and 4 buttons           | 1        |    |
| ANTUIF1      | USB Interface Board with a Molex socket                                          | 1        |   |
|              | Segger J-Link Lite Programmer                                                    | 1        |  |

Note: Starter kits before the release of N5150M5CD contain N548M5CB instead.

**Table 2: N5 ANT SoC Module Starter Kit**

## 2 Product Overview

### 2.1 Block Diagram

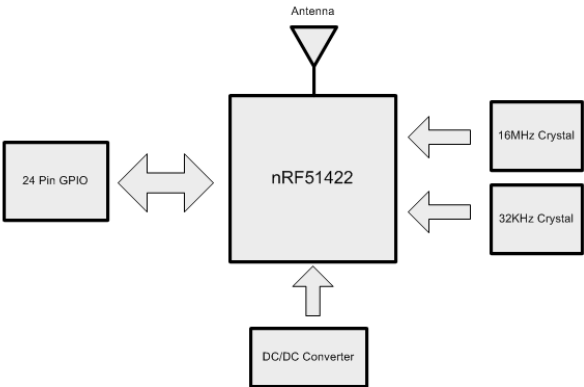


Figure 3: N5 ANT SoC Module Series Block Diagram

### 2.2 Pin-outs

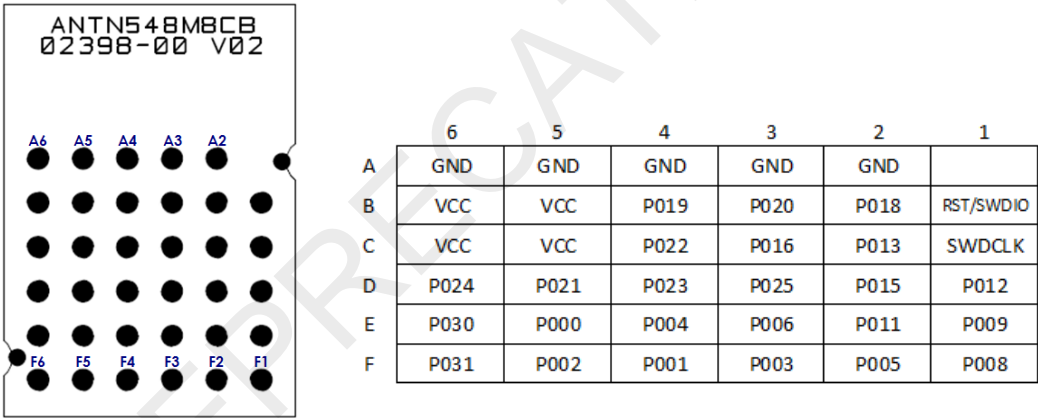


Figure 4: N5 M8 LGA Bottom View

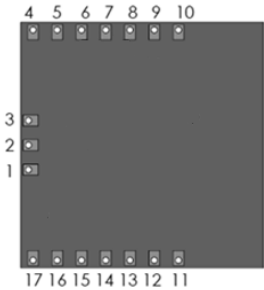


Figure 5: N5 M4 Bottom View

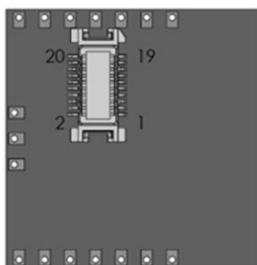


Figure 6: N5 M5 Module Bottom View

| N5 M8 LGA Pad | N5 M4 Pin | N5 M5 Molex Connector | nRF51422 Pin Name | Description                                           |
|---------------|-----------|-----------------------|-------------------|-------------------------------------------------------|
| A2-6          | 4         | 19                    | GND               | Power supply ground                                   |
| B1            | 2         | 10                    | RST<br>/SWDIO     | System reset. Also HW debug and flash programming I/O |
| B2            |           |                       | P018              | GPIO                                                  |
| B3            |           |                       | P020              | GPIO                                                  |
| B4            |           |                       | P019              | GPIO                                                  |
| B5, B6        | 3         | 1                     | Vcc               | Power supply source                                   |
| C1            | 5         | 6                     | SWDCLK            | HW debug and flash programming I/O                    |
| C2            |           |                       | P013              | GPIO                                                  |
| C3            |           |                       | P016              | GPIO                                                  |
| C4            |           |                       | P022              | GPIO                                                  |
| C5, C6        | 3         | 1                     | Vcc               | Power supply source                                   |
| D1            | 12        | 3                     | P012              | GPIO                                                  |
| D2            | 11        | 4                     | P015              | GPIO                                                  |
| D3            |           |                       | P025              | GPIO                                                  |
| D4            | 6         | 17                    | P023              | GPIO                                                  |
| D5            |           | 16                    | P021              | GPIO                                                  |
| D6            | 10        | 7                     | P024              | GPIO                                                  |
| E1            | 14        | 9                     | P009              | GPIO                                                  |
| E2            | 15        | 14                    | P011              | GPIO                                                  |
| E3            | 13        | 5                     | P006              | GPIO / ADC input 7/ ADC reference voltage 1           |
| E4            |           | 20                    | P004              | GPIO / ADC input 5                                    |
| E5            | 9         | 11                    | P000              | GPIO / ADC reference voltage 0                        |
| E6            | 8         | 13                    | P030              | GPIO                                                  |
| F1            | 16        | 12                    | P008              | GPIO                                                  |
| F2            | 17        | 2                     | P005              | GPIO / ADC input 6                                    |
| F3            | 1         | 8                     | P003              | GPIO / ADC input 4                                    |
| F4            |           | 18                    | P001              | GPIO / ADC input 2                                    |
| F5            | 7         | 15                    | P002              | GPIO / ADC input 3                                    |
| F6            |           |                       | P031              | GPIO                                                  |

Table 3: N5 ANT SoC Module Pin-Outs

## 2.3 N5 Module Preloaded Software

The N5 module is preloaded with the S210 SoftDevice, the ANT-WP bootloader, and the ANT Network Processor (NP) code as illustrated in Figure 7: Memory Map of the Preloaded Software. Depending on the module revision, the preloaded code varies. Please refer to Appendix C: N5 Module Pre-Loaded Software Versions.

- **S210 SoftDevice** - Refer to nRF51422 S210 SoftDevice Specification
- **ANT-WP Bootloader** - Refer to Appendix B: Using the ANT Bootloader for OTA Firmware Update
- **ANT Network Processor Application** - Refer to Appendix A: Using the ANT Network Processor Configuration

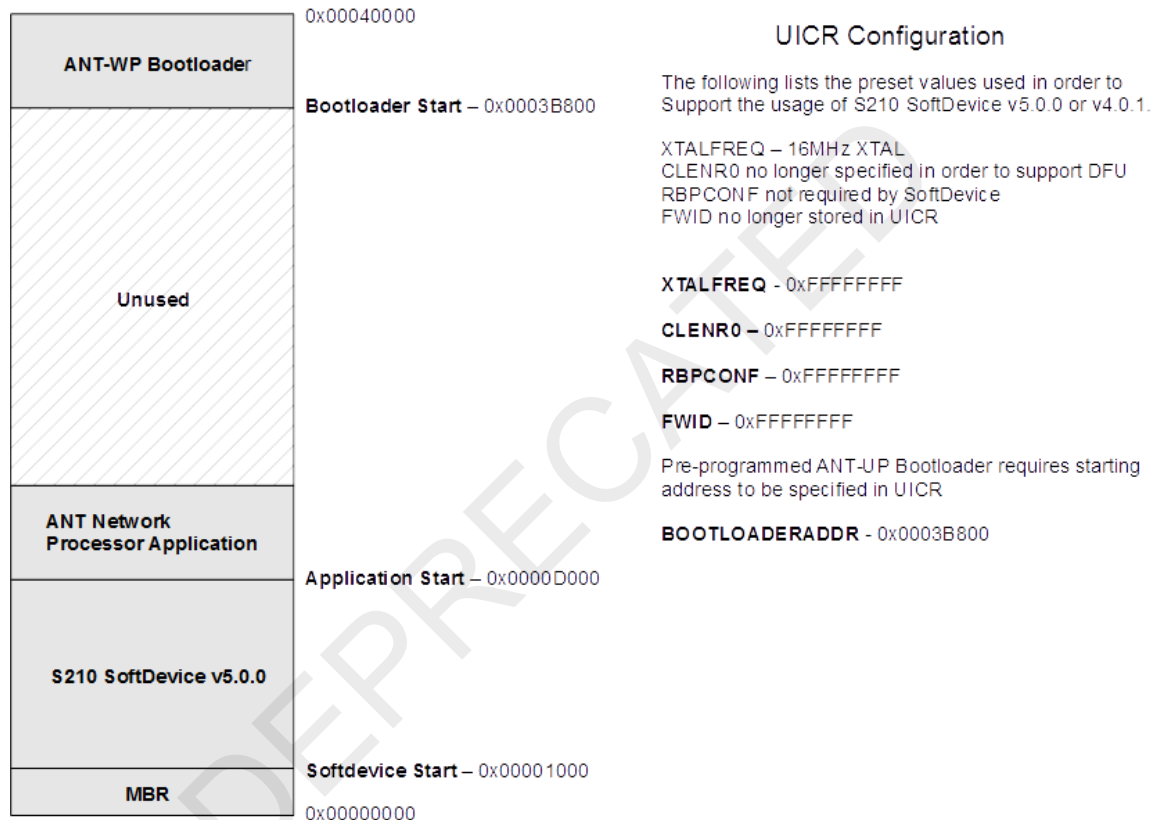


Figure 7: Memory Map of the Preloaded Software

## 2.4 N5 Module Programming

The N5 ANT SoC module series supports two programming methods:

- Standard Serial Wire Debug (SWD) interface
- Over-The-Air (OTA) updates using the preloaded ANT-WP bootloader (Not available for N548 Rev A)

These two programming methods are complementary. While the ANT-WP bootloader offers the convenience of programming wirelessly, it does consume some of the available application space. In case the space for the bootloader must be reclaimed for a large application, programming via SWD interface would be the option.

The three software components (the SoftDevice, the bootloader and the application code) must be version compatible to operate properly. Because each individual component can be reprogrammed, it is not safe to always assume the default factory image on a module by reading the module revision mark and referring to the history of

preloaded images as summarized in Appendix C: N5 Module Pre-Loaded Software Versions. When versions of the software components are unclear, to ensure proper operation after reprogramming, it is recommended that the module undergoes a full erasure (e.g. using the erase-all option in nrfjprog.exe/nRFgo Studio) and all desired software components be explicitly programmed onto the module.

Some reference application code is provided on <https://www.thisisant.com/developer/components/n5/>.

### **2.4.1 Programming via SWD Interface**

The N5 ANT SoC Module series supports the Serial Wire Debug (SWD) interface SWDCLK and SWDIO (refer to Table 3). Programming and debugging of the module only require common available tools, such as the Keil software development environment and the Segger J-Link programmer.

Please refer to “[nRF51422 Evaluation Kit - Developing with the MDK-ARM Microcontroller Development Kit](#)” from Nordic Semiconductor for a specific reference on using the Keil software and J-Link programmer.

It is important to note that the BOOTLOADERADDR field in the UICR is set to the starting bootloader address location by default. If the desired programmed application needs to reclaim the bootloader region and/or if bootloader support is not required, then the BOOTLOADERADDR field in the UICR must be set to 0xFFFFFFFF. The erase-all command via nrfjprog.exe/nRFgo Studio should reset this field. Please refer to Figure 7: Memory Map of the Preloaded Software.

### **2.4.2 Programming Over the Air**

The pre-programmed SoftDevice and ANT-WP bootloader in the N5 ANT SoC Module provides over-the-air firmware update capability. The pre-programmed ANT Network Processor Application provides two methods of entry into the bootloader mode in order to perform the software updates. SoftDevice, bootloader and application code in the module can be changed or updated in this manner.

Please refer to Appendix B: Using the ANT Bootloader for OTA Firmware Update.

### **2.4.3 Initializing the SoftDevice**

The N5 module comes with 50ppm onboard 32 kHz crystal. When initializing the SoftDevice, it is important to set the crystal accuracy to be 50ppm. In the preloaded ANT Network Processor code, this line is used:

```
sd_softdevice_enable(NRF_CLOCK_LFCLKSRC_XTAL_50_PPM, softdevice_assert_callback)
```

### **2.4.4 Configuring the DC/DC Converter**

The N5 module can make use of the DC/DC Converter on supported nRF51422 chip revisions. This can improve power consumption under certain conditions.

```
sd_softdevice_enable(NRF_CLOCK_LFCLKSRC_XTAL_50_PPM, softdevice_assert_callback)
```

## **2.5 Design Considerations**

RF performance is always affected by the environment. Good design makes a product less susceptible. Guidelines provided in this section are for recommendations only. Users should thoroughly test their products in the intended use cases and make necessary modifications and trade-offs.

For design assistance purpose, a STEP model package of all the three module types and an Altium library of the M8 module are provided online.

### **2.5.1 M8 Module Mounting**

Best RF performance is achieved by using 0.032" thickness FR4 under the module antenna and following the guideline on Figure 8.

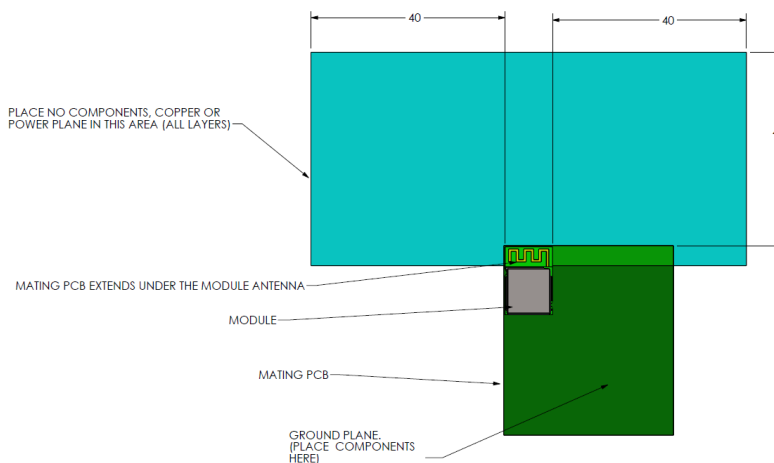


Figure 8: N5 M8 Module Mounting (all dimensions in mm)

### 2.5.2 M4 Module Mounting

Best possible RF performance is achieved when the module is placed such that the module antenna is protruding out from the mating PCB into free space as Figure 9. Place no exposed copper underneath the M4 module. If possible, place continuous ground plane under the module.

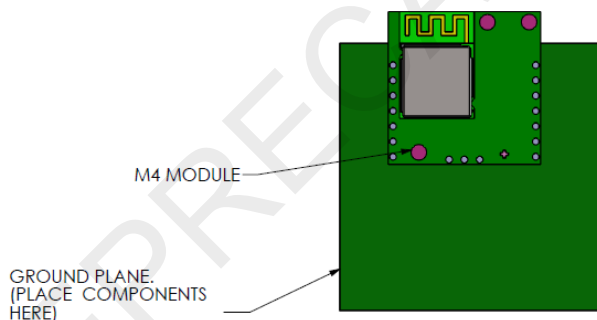


Figure 9: N5 M4 Module Mounting

### 2.5.3 M5 Module Mounting

The mating socket is Molex 52991-0208.

Note: The M5 module is provided for application prototyping and lab use. The M5 module should not be used to evaluate the RF performance of the N5 module family.

## 2.6 Assembly Considerations

### 2.6.1 Moisture Control

The moisture control of the module is rated at level 1 defined by IPC/JEDEC J-STD-020. The modules do not require special storage conditions provided:

- They are maintained at conditions equal to or less than 30 °C/85 % RH, and
- They are solder reflowed at a peak body temperature which does not exceed 260 °C

To ensure good solderability of the PCB pads, it is highly recommended to always have the modules intended for reflow well sealed when in storage.

### 2.6.2 Solder Stencil Design of M8 Module

The following reference stencil design is used to produce N5 M4 and M5 models.

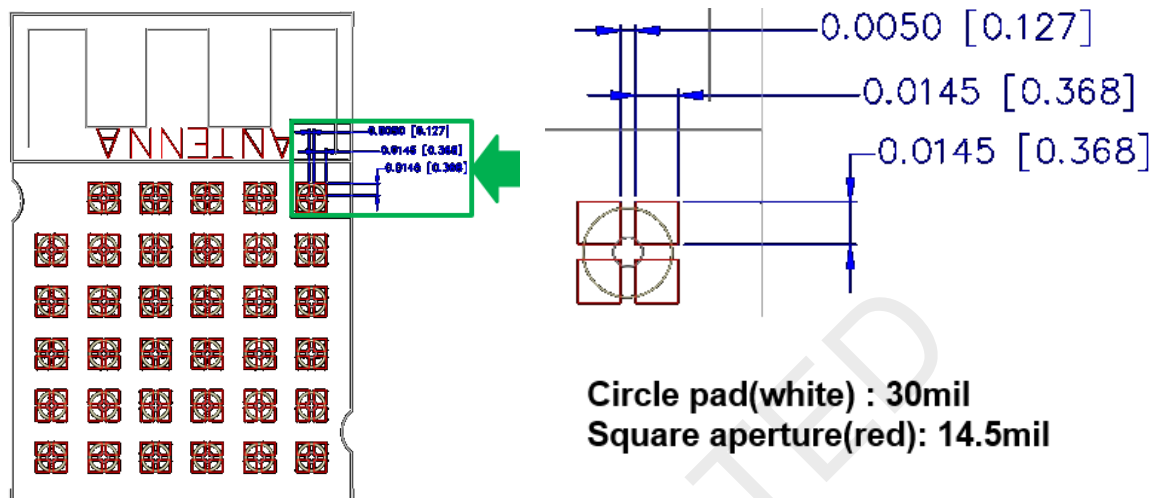


Figure 10: Solder Stencil Reference

### 2.6.3 Cleaning Process

The module is made using no-clean solder paste. No-clean process is recommended.



### 3 Regulatory Approvals and Compliances

The N5 ANT SoC module series, when loaded with ANT and/or BLUETOOTH low energy stack, has received regulatory approvals in the United States (FCC) and Canada (IC), and has been verified to conform to the appropriate regulations in Europe, Great Britain, Australia and New Zealand, and Japan. The module series has been qualified by BLUETOOTH SIG. Such approvals and qualification allow the user to place the module inside a finished product and, in most cases, not require regulatory testing for an intentional radiator, provided no changes or modifications are made to the module circuitry. This does not preclude the possibility that some other form of authorization or testing may be required for the finished product. Changes or modifications could void the user's authority to operate the equipment. The end user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

#### 3.1 United States

The N5 ANT SoC module series has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

The N5 module series complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The N5 module series does not contain any user-serviceable parts. Unauthorized repairs or modifications could result in permanent damage to the equipment, and void your warranty and your authority to operate this device under Part 15 regulations.

The N5 module series is labelled with its own FCC ID, O6R2398 (note: First Character is the letter O, not the # 0.) If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: O6R2398" or "Contains FCC ID: O6R2398". Any similar wording that expresses the same meaning may be used.

#### 3.2 Canada

The N5 ANT SoC module series complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

(Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.)

To comply with Industry Canada regulations, it is required that product containing the N5 module series display a label referring to the enclosed module. This exterior label can use wording similar to the following: "Contains IC: 3797A-2398"

This information shall be affixed in such a manner as not to be removable except by destruction or defacement. The size of the lettering shall be legible without the aid of magnification but is not required to be larger than 8-point font size. If the device is too small to meet this condition, the information can be included in the user manual upon agreement with Industry Canada.

### 3.3 European Economic Area and Great Britain

N5 series modules are declared to be category 2 receivers in conformance with the essential requirements and other relevant provisions of Directive 2014/53/EU and 2011/65/EU, as a low-powered unlicensed transmitter:



IEC 60950-1:2005(2<sup>nd</sup> Edition) +  
A1:2009 + A2:2013

Information technology equipment – Safety – Part 1:  
General requirements

EN 60950-1: 2006 + A11:2009 +  
A1:2010 + A12:2011 + A2:2013

EN 62479:2010

Assessment of the compliance of low power electronic and electrical equipment with the basic restrictions related to human exposure to electromagnetic fields (10 MHz to 300 GHz)

EN 300 328 v2.1.1 2016-11

Wideband transmission systems; Data transmission equipment operating in the 2,4 GHz ISM band and using wide band modulation techniques

EN 300 440 v2.1.1 2017-03

Short Range Devices (SRD); Radio equipment to be used in the 1 GHz to 40 GHz frequency range

EN 301 489-1 v2.1.1 2017-02

EN 301 489-3 v2.1.1 2017-03

EN 301 489-17 v3.1.1 2017-02

ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements; Part 3: Specific conditions for Short-Range Devices (SRD) operating on frequencies between 9 kHz and 246 GHz; Part 17: Specific conditions for Broadband Data Transmission Systems

### 3.4 Australia & New Zealand

The N5 ANT SoC module series has been tested and found to comply with:



- AS/NZS 4268:2012 + A1:2013 Radio equipment and systems – Short range devices – Limits and methods of measurement
- AS/NZS CISPR 22:2009 + A1:2010 Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement

The ACMA supplier code number is N20233

### 3.5 Japan

The N548, N550 and N5150 models have been granted type certificate (mark number R203-JN6049). Standard applied:

Notification No. 88 of MIC 2004, 2.4GHz band wide-band low-power data communication system (item 19 of Article 2 paragraph 1)

### 3.6 BLUETOOTH Qualification

The N5 ANT SoC module series is listed as a Bluetooth End Product on the Bluetooth SIG Qualified Design List [Qualified Design ID 54799; Declaration ID is D022375]. Further use of this design to create subsequent BLUETOOTH implementations can be achieved without further qualification provided that the resulting implementation has no negative material impact on the BLUETOOTH performance or functionality of the design.

## 4 Electrical Specifications

### 4.1 Absolute Maximum Ratings

| PARAMETER                  | TEST CONDITIONS                                                    | Min  | Max            | Unit |
|----------------------------|--------------------------------------------------------------------|------|----------------|------|
| Supply voltage (VCC)       | All supply pins must have the same voltage                         | -0.3 | 3.9            | V    |
| Voltage on any digital pin |                                                                    | -0.3 | VCC+0.3, ≤ 3.9 | V    |
| Storage temperature range  |                                                                    | -40  | 85             | °C   |
| ESD                        | All pads, according to human-body model, JEDEC STD 22, method A114 |      | 4              | kV   |
|                            | According to charged-device model, JEDEC STD 22, method C101       |      | 500            | V    |

Table 4: Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 4.2 Recommended Operating Conditions

| PARAMETER                                           | Min | Max | Unit |
|-----------------------------------------------------|-----|-----|------|
| Operating ambient temperature range, T <sub>A</sub> | -25 | +75 | °C   |
| Operating supply voltage                            | 1.8 | 3.6 | V    |

Table 5: Recommended Operating Conditions

### 4.3 Industrial Temperature Range

The N550 modules are able to operate from -40°C to +85°C when the supply voltage is from 1.9V to 3.6V. For details, please refer to “nRF51422 Specification for Industrial Temperature Range” from Nordic Semiconductor.

### 4.4 Radio Operation Specifications and Antenna Characteristics

| nRF5142 Output Setting (dBm) | Peak Antenna Gain (dBi) | EIRP (dBm) |
|------------------------------|-------------------------|------------|
| 0                            | 0                       | 0          |
| +4                           | 0                       | +4         |

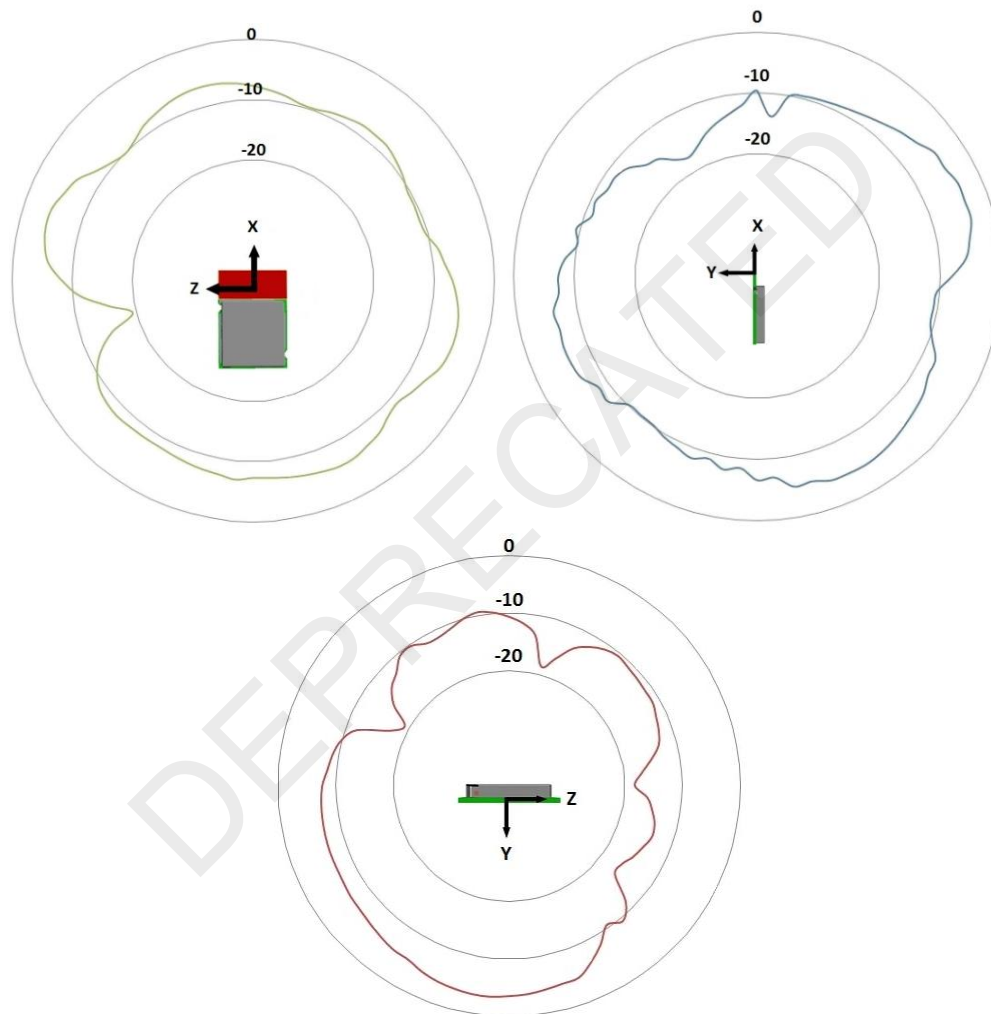
Table 6: N5 Module Antenna Gain

| nRF51422 Output Setting (dBm) | Typical Radio current (mA) * |
|-------------------------------|------------------------------|
| 0                             | 10.5                         |
| +4                            | 16.0                         |

**Table 7: Current Consumption of Radio Operation**

\* Note: For additional information regarding radio current, please refer to the nRF51422 product specification by Nordic Semiconductor.

The following typical radiation pattern is recorded in an anechoic chamber at 2440MHz and 0dBm output following the recommended mounting guideline.



**Figure 11: N5 M4 Module Typical Antenna Gain (dBi)**

To understand and properly use the radiation pattern for your design, please refer to the application note: Interpreting RF Radiation Patterns.

#### 4.5 Electrical Specifications

Please refer to the nRF51422 Product Specification by Nordic Semiconductor.

5 Mechanical Drawings

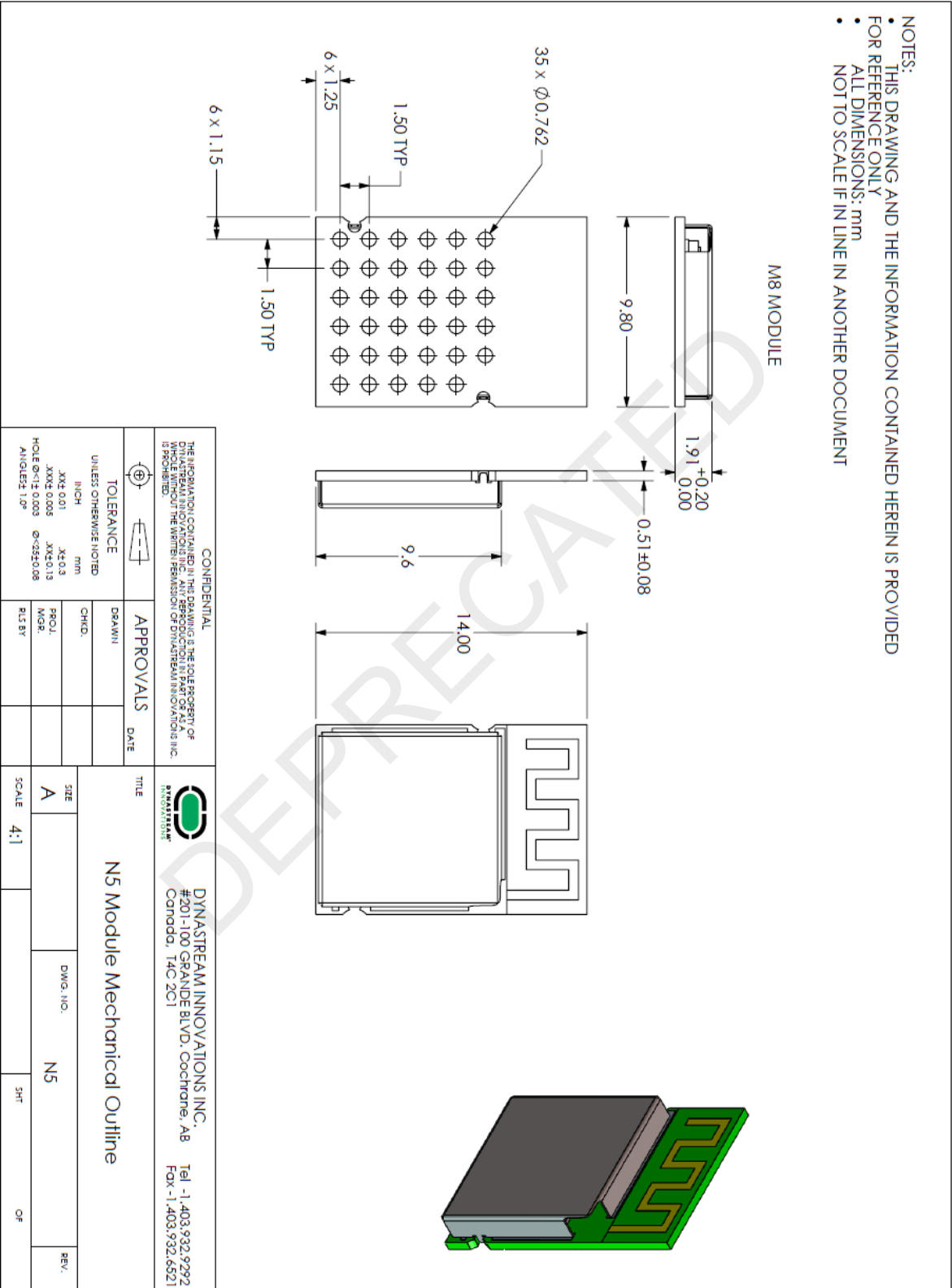


Figure 12: N5 M8 Mechanical Drawing

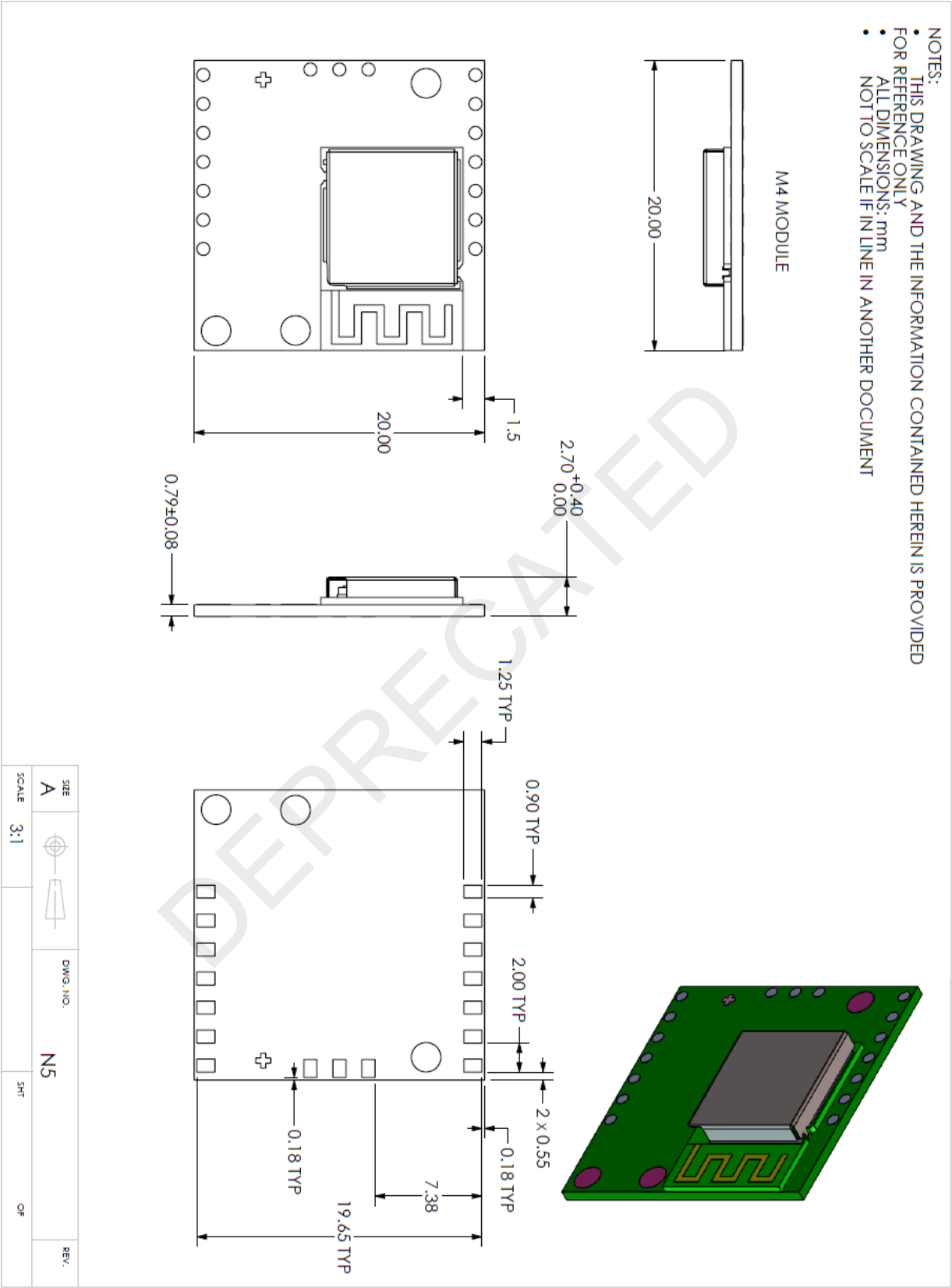


Figure 13: N5 M4 Mechanical Drawing

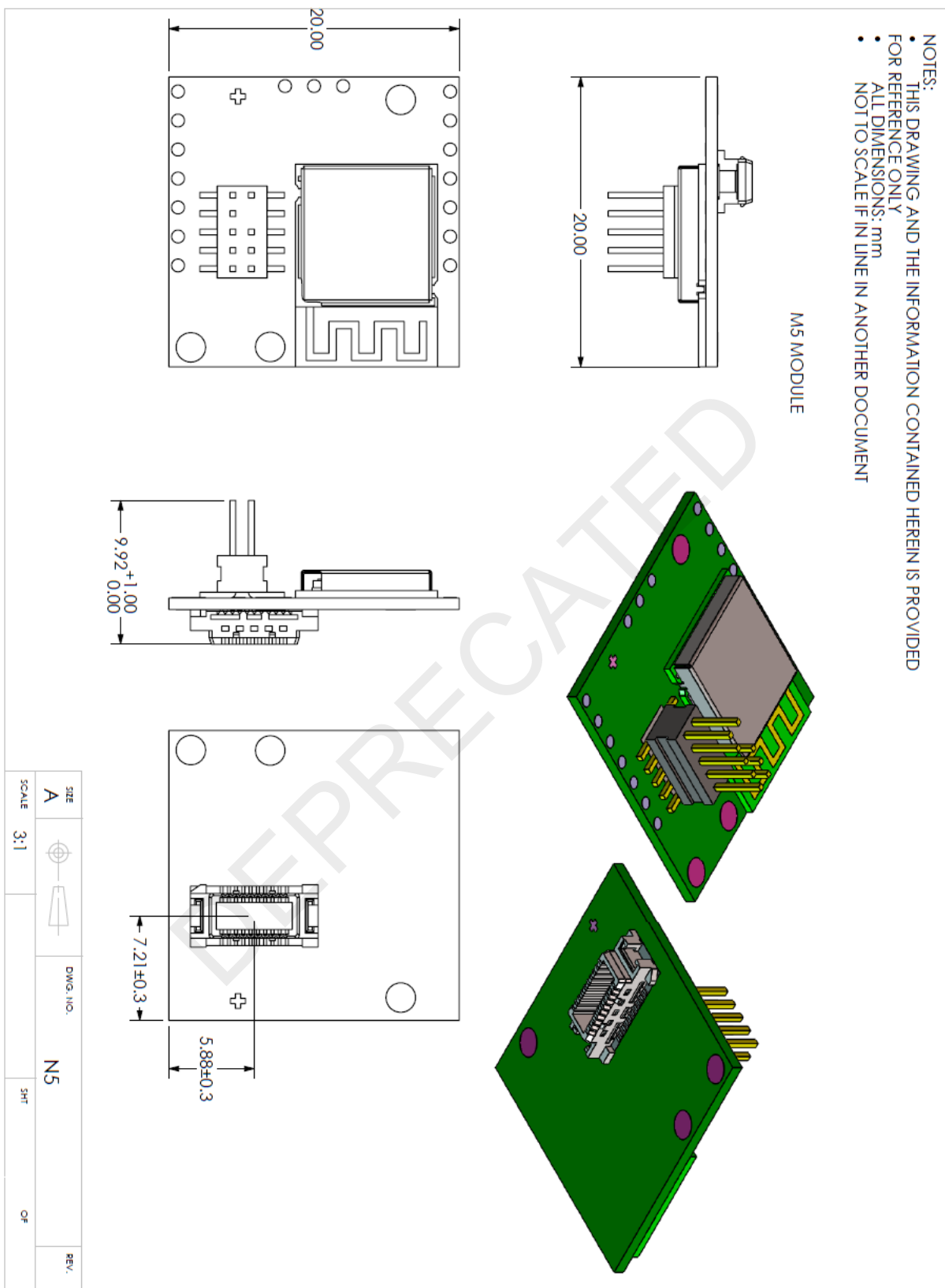


Figure 14: N5 M5 Mechanical Drawing

## 6 Support

The N5 ANT SoC module series uses nRF51422 from Nordic Semiconductor. Users can seek technical support from Nordic Semiconductor, [www.nordicsemi.com](http://www.nordicsemi.com). Users can seek application support from Garmin Canada Inc., [www.thisisant.com](http://www.thisisant.com).

### 6.1 ANT Forum

Users are encouraged to participate in the ANT forum moderated by the application engineering team of Garmin Canada Inc. for any engineering discussions. Joining the ANT forum is free and open at <http://www.thisisant.com/forum>.

### 6.2 Technical References

Documents:

1. nRF51422 Product Specification, Nordic semiconductor
2. nRF51422 Specification for Industrial Temperature Range, Nordic Semiconductor
3. nRF51 Series Compatibility Matrix, Nordic Semiconductor
4. nRF51822 and nRF51422 Product Anomaly Notification (PAN-028), Nordic Semiconductor
5. nRF51 Series Reference Manual, Nordic Semiconductor
6. nRF51422 S210 SoftDevice Specification, Nordic Semiconductor
7. nRF51422 S310 SoftDevice Specification, Nordic Semiconductor
8. nRF51822 S110 SoftDevice Specification, Nordic Semiconductor
9. nRF51822 S120 SoftDevice Specification, Nordic Semiconductor
10. S130 nRF51822 SoftDevice Specification, Nordic Semiconductor
11. nRF51422 Evaluation Kit - Developing with the MDK-ARM Microcontroller Development Kit, Nordic Semiconductor
12. N5 Starter Kit User Manual, Dynastream Innovations
13. ANT Message Protocol and Usage, Dynastream Innovations
14. Interfacing with ANT General Purpose Chipsets and Modules, Dynastream Innovations
15. ANT-FS Technical Specification, Dynastream Innovations
16. Application Note: Interpreting RF Radiation Patterns, Dynastream Innovations
17. Application Note: Over the Air Firmware Updates Using ANT-FS, Dynastream Innovations

Software:

18. S210 nRF51422 SoftDevice, Nordic Semiconductor
19. S310 nRF51422 SoftDevice, Nordic Semiconductor
20. S110 nRF51822 SoftDevice, Nordic Semiconductor
21. S120 nRF51822 SoftDevice, Nordic Semiconductor
22. S130 nRF51822 SoftDevice, Nordic Semiconductor
23. N5 Starter Kit SDK, Dynastream Innovations
24. N5 Starter Kit ANT IO Demo, Dynastream Innovations
25. OTA Updater – a wireless firmware update tool, Dynastream Innovations
26. ANTwareII – a system testing and debugging tool, Dynastream Innovations
27. ObservANT – an ANT debugging tool, Dynastream Innovations

Design models:

28. N5 M8 Altium library, Dynastream Innovations
29. N5 module STEP mode, Dynastream Innovations

The above documents and software are available at [www.thisisant.com](http://www.thisisant.com) and/or [www.nordicsemi.com](http://www.nordicsemi.com). User registration or supplier product code may be required.

### 6.3 ANT Developer's Zone

ANT development software tools, application notes, reference designs and other public resources are found in the ANT Developer's Zone at <http://www.thisisant.com/developer>.

To begin development with the ANT+ interoperability, please become an [ANT+ Adopter or ANT+ Alliance member](#) to obtain the access to the ANT+ Adopter Zone. ANT+ documents and design tools contained in the ANT+



Adopter zone include the ANT+ Device Profiles, ANT-FS specification, ANT software (PC/Mac) libraries with source code, simulator tools (SimulANT+), embedded reference designs with source code, and more.

#### **6.4 ANT and ANT+ Social Media**

ANT is on the following social media sites,

YouTube: <http://www.youtube.com/user/ANTAlliance>

Twitter: <http://twitter.com/ANTPlus>

Facebook: <https://www.facebook.com/thisisant>

LinkedIn: <http://www.linkedin.com/groups?gid=1379137>

DEPRECATED

## Appendix A: Using the ANT Network Processor Configuration

N5 modules are preloaded with a default ANT network processor reference code image in the application code space of the nRF51422. Using this configuration is similar to ANT legacy ICs or modules, as illustrated in the diagram below. This reference code is available upon request.

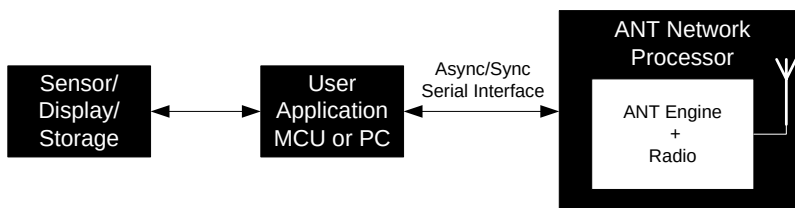


Figure 15: Using ANT Network Processor

With this configuration, the N5 M4/5 model is basically drop-in compatible with ANT11TS33M4/5IB, ANTAP281M4/5IB and ANTC782M4/5IB modules.

For information regarding ANT network processor serial interfaces, please refer to document “Interfacing with ANT General Purpose Chipsets and Modules”.

### 1. Pin Assignments in the ANT Network Processor Configuration

In the pre-loaded ANT network processor configuration, specific functions are assigned to the module pins. The details are summarized below:

| N5xxM8xx<br>LGA Pad | N5xxM4xx<br>Pin | N5xxM5xx<br>Molex<br>Connector | nRF51422<br>Pin Name | ANT Network Processor Pin Assignments |            |           |                                                       |
|---------------------|-----------------|--------------------------------|----------------------|---------------------------------------|------------|-----------|-------------------------------------------------------|
|                     |                 |                                |                      | Pin Name                              | Async Mode | Sync Mode | Function                                              |
| A2-6                | 4               | 19                             | GND                  | GND                                   | GND        | GND       | Power supply ground                                   |
| B1                  | 2               | 10                             | RST<br>/SWDIO        | RST                                   | RST        | RST       | Reset the device                                      |
| B2                  |                 |                                | P018                 | Unused                                | Unused     | Unused    | Not used                                              |
| B3                  |                 |                                | P020                 | Unused                                | Unused     | Unused    | Not used                                              |
| B4                  |                 |                                | P019                 | Unused                                | Unused     | Unused    | Not used                                              |
| B5, B6              | 3               | 1                              | Vcc                  | Vcc                                   | Vcc        | Vcc       | Power supply source                                   |
| C1                  | 5               | 6                              | SWDCLK               | Unused                                | Unused     | Unused    | Not used                                              |
| C2                  |                 |                                | P013                 | Unused                                | Unused     | Unused    | Not used                                              |
| C3                  |                 |                                | P016                 | Unused                                | Unused     | Unused    | Not used                                              |
| C4                  |                 |                                | P022                 | Unused                                | Unused     | Unused    | Not used                                              |
| C5, C6              | 3               | 1                              | Vcc                  | Vcc                                   | Vcc        | Vcc       | Power supply source                                   |
| D1                  | 12              | 3                              | P012                 | RXD0/SIN                              | RXD0       | SIN       | Async -> Receive data signal<br>Sync -> Data input    |
| D2                  | 11              | 4                              | P015                 | TXD0/SOUT                             | TXD0       | SOUT      | Async -> Transmit data signal<br>Sync -> Data output  |
| D3                  |                 |                                | P025                 | Unused                                | Unused     | Unused    | Not used                                              |
| D4                  | 6               | 17                             | P023                 | SUSPEND<br>/ SRDY                     | SUSPEND    | SRDY      | Async -> Suspend control<br>Sync -> Serial port ready |
| D5                  |                 | 16                             | P021                 | Unused                                | Unused     | Unused    | Not used                                              |
| D6                  | 10              | 7                              | P024                 | BR2/SCLK                              | BR2        | SCLK      | Async -> Baud rate selection                          |

| N5xxM8xx<br>LGA Pad | N5xxM4xx<br>Pin | N5xxM5xx<br>Molex<br>Connector | nRF51422<br>Pin Name | ANT Network Processor Pin Assignments |               |                          |                                                                      |
|---------------------|-----------------|--------------------------------|----------------------|---------------------------------------|---------------|--------------------------|----------------------------------------------------------------------|
|                     |                 |                                |                      | Pin Name                              | Async<br>Mode | Sync Mode                | Function                                                             |
|                     |                 |                                |                      |                                       |               |                          | Sync -> Clock output<br>signal                                       |
| E1                  | 14              | 9                              | P009                 | BR3/SPD_SEL                           | BR3           | SPD_SEL                  | Async -> Baud rate<br>selection<br>Sync -> Clock speed<br>Selection  |
| E2                  | 15              | 14                             | P011                 | BOOT                                  | BOOT          | BOOT                     | Bootloader Startup.<br>if not used, tie to ground<br>or unconnected  |
| E3                  | 13              | 5                              | P006                 | BR1                                   | BR1           | Unused                   | Async -> Baud rate<br>selection<br>Sync -> Not used                  |
| E4                  |                 | 20                             | P004                 | Unused                                | Unused        | Unused                   | Not used                                                             |
| E5                  | 9               | 11                             | P000                 | PORTSEL                               | Tie to GND    | Tie to VCC               | Asynchronous or<br>synchronous port select                           |
| E6                  | 8               | 13                             | P030                 | Unused                                | Unused        | Unused                   | Not used                                                             |
| F1                  | 16              | 12                             | P008                 | Unused                                | Unused        | Unused                   | Not used                                                             |
| F2                  | 17              | 2                              | P005                 | RTS/SEN                               | RTS           | SEN                      | Async -> Request to send<br>Sync -> Serial enable<br>signal          |
| F3                  | 1               | 8                              | P003                 | Unused                                | Unused        | Unused                   | Not used                                                             |
| F4                  |                 | 18                             | P001                 | Unused                                | Unused        | Unused                   | Not used                                                             |
| F5                  | 7               | 15                             | P002                 | SLEEP/ $\overline{\text{MRDY}}$       | SLEEP         | $\overline{\text{MRDY}}$ | Async -> Sleep mode<br>enable<br>Sync -> Message ready<br>indication |
| F6                  |                 |                                | P031                 | Unused                                | Unused        | Unused                   | Not used                                                             |

Table 8: Pin Assignments in ANT Network Processor Configuration

Notes:

- Pins marked unused can be tied to GND
- Bit Serial Synchronous mode is not supported in the current version of the ANT Network Processor code

## 2. Asynchronous Serial Mode

The baud rate of the asynchronous communication is controlled by the speed select signals BR1, BR2 and BR3. Please refer to the table below.

| BR3 | BR2 | BR1 | Baud Rate |
|-----|-----|-----|-----------|
| 0   | 0   | 0   | 4800      |
| 1   | 0   | 1   | 9600      |
| 0   | 1   | 0   | 19200     |
| 0   | 0   | 1   | 38400     |
| 1   | 1   | 1   | 57600     |
| 1   | 0   | 0   | 115200    |

Table 9: Asynchronous Serial Mode Baud Rate Select

### Asynchronous Serial Mode Connection Example

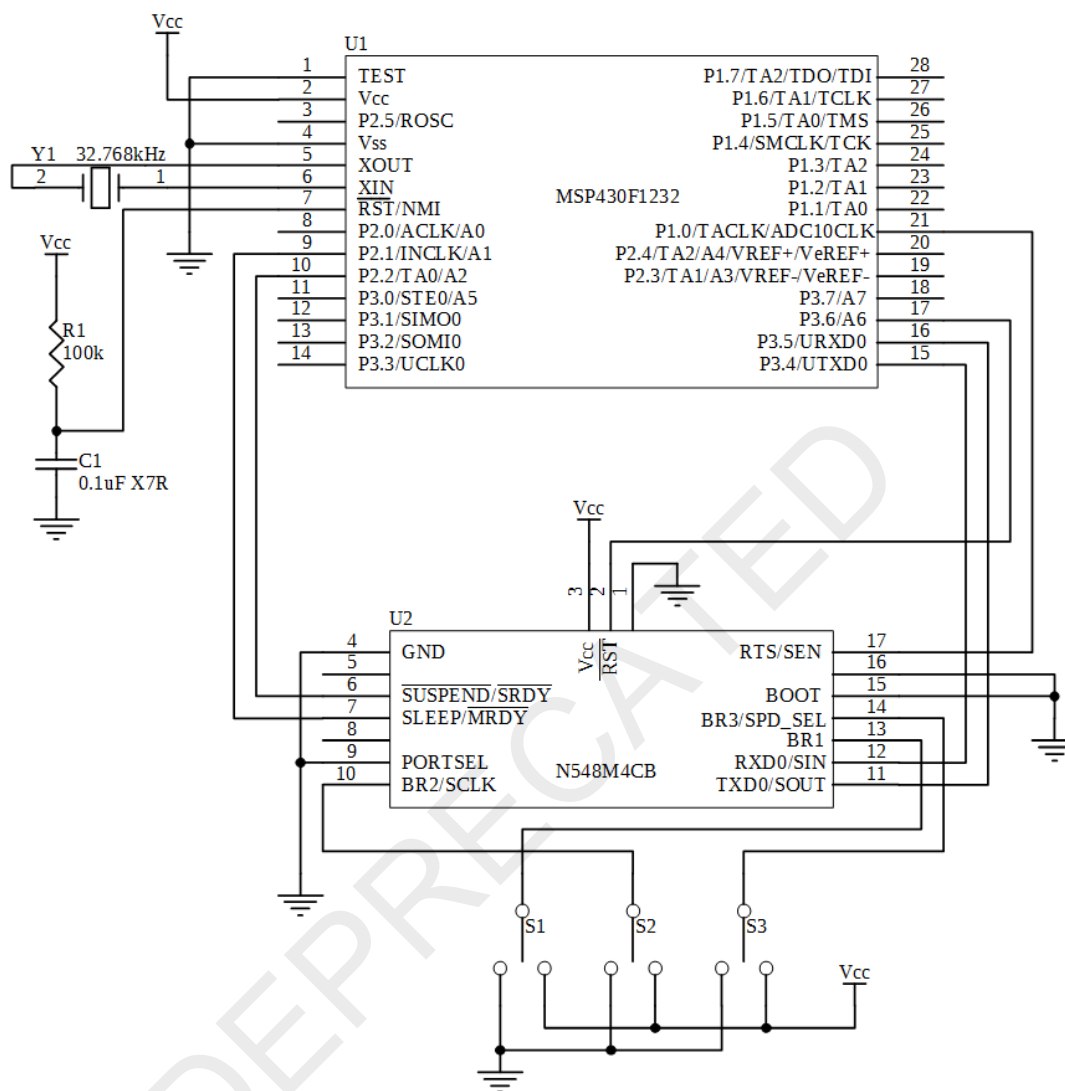


Figure 16: N5 M4 ANT NP Configuration Async Serial Connection

#### Notes:

- Module RXD and TXD connected directly to hardware USART of microcontroller.
- Switches on baud rate selection pins (BR1, BR2 and BR3) are for ease of use only. They can be connected directly to the logic level of interest.
- RTS is hardware controlled on the N5 module and follows the RTS behaviour described in the nRF51 Series Reference Manual. In addition, RTS is toggled by the network processor application during message processing. If HW flow control is not available on MCU, the software implemented flow control must be able to manage serial communication flow control on a per byte level.

### 3. Byte Synchronous Serial Mode

The clock speed of the byte-Sync mode can be set to either 500KHz or 4MHz by setting BR3. Please refer to the table below.

| SPD-SEL | Byte-Sync Speed |
|---------|-----------------|
| 0       | 500KHz          |
| 1       | 4MHz            |

Table 10 Byte-Sync Mode Speed Selection

#### Byte Synchronous Mode Connection Example

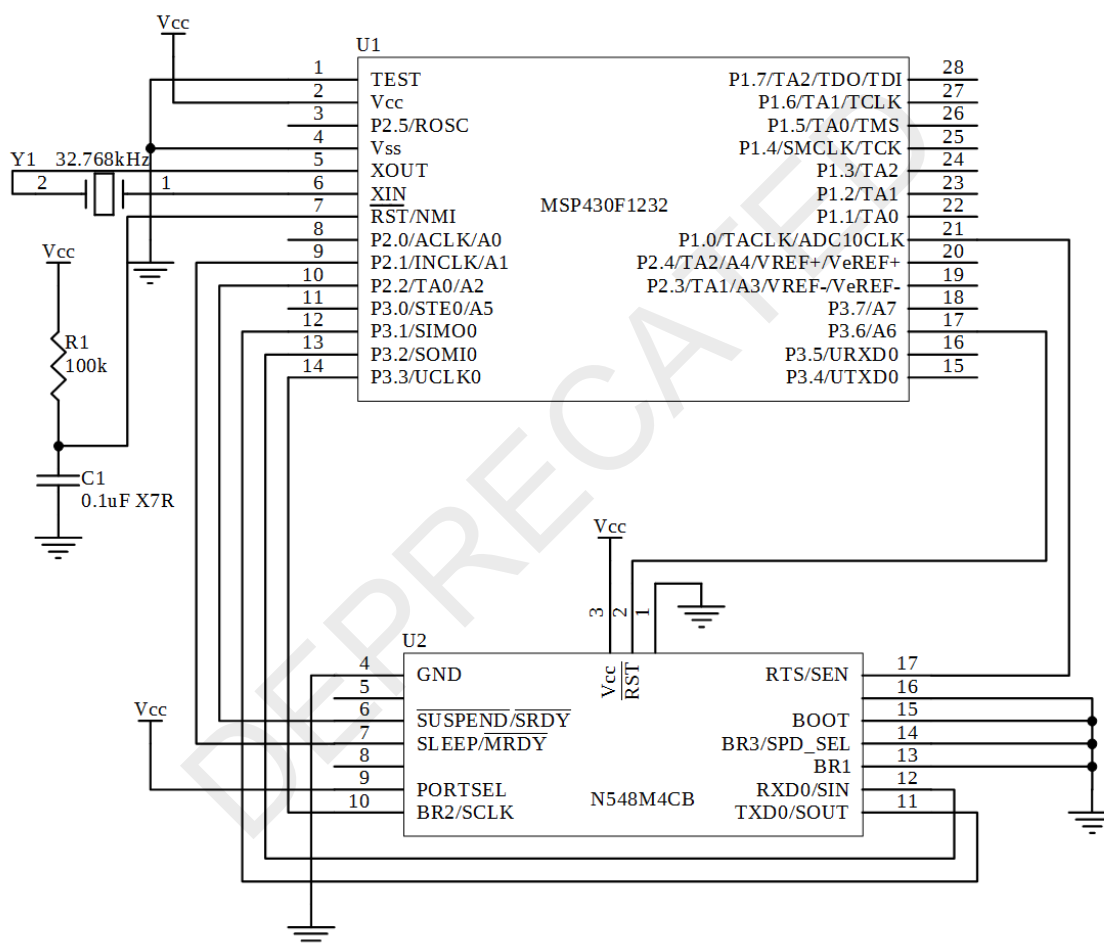


Figure 17: N5 M4 ANT NP Configuration Byte Sync Connection

#### Notes:

- Module SOUT, SIN, and SCLK connected directly to hardware USART of microcontroller.
- SEN needs to be on an interrupt capable I/O pin on the microcontroller. (Interrupt pins located on Port 1&2 on the MSP430F1232)

### 4. ANT-WP Bootloader Activation

The pre-programmed ANT Network Processor Application provides two methods of entry into the ANT-WP bootloader mode. The methods are described in the following sections.

Once the ANT-WP bootloader has been activated, the N5 module will remain in bootloader mode until one of the following conditions are met:

- The existing network processor application is successfully replaced using the ANT-WP bootloader and the new application is activated.
- The existing network processor application is not replaced. The ANT-WP bootloader successfully disconnected from ANT PC OTA updater tool.
- The existing network processor application is not replaced. The ANT-WP bootloader reaches 2 min inactivity timeout.

For more details on the ANT-WP bootloader functionality, please refer to Appendix B: Using the ANT Bootloader for OTA Firmware Update.

### ***Using BOOT Pin***

A dedicated BOOT pin is assigned in the network processor application in order to activate the ANT-WP bootloader code. If BOOT is held high upon power-up or start-up, the operation of the network processor code is bypassed and the ANT-WP bootloader code is started.

The intent of this functionality is to assist in updating/replacing the default images on the N5 modules using the OTA firmware update capability of the ANT-WP bootloader without requiring host microcontroller intervention.

This mode of operation is not intended to be used to upgrade the existing network processor application on the N5 module.

### ***Using Serial Command***

The following serial command message has been defined in the ANT network processor code. A host microcontroller can issue this command to the ANT network processor application to put the N5 module into the ANT-WP bootloader mode.

| Sync | Length | MsgID |      | Payload | Checksum |
|------|--------|-------|------|---------|----------|
|      | 0x02   | 0xE4  | 0x00 | 0x00    |          |

**Table 11: ANT OTA Update Enable Command**

After issuing the command, the following response is generated prior to activation of the ANT-WP bootloader.

| Sync | Length | MsgID |      |      |      | Response | Checksum |
|------|--------|-------|------|------|------|----------|----------|
|      | 0x04   | 0xE0  | 0x00 | 0xE4 | 0x00 | 0x00     |          |

**Table 12: ANT OTA Update Enable Response**

Note: Sync and Chksum values are defined in the document “Interfacing with ANT General Purpose Chipsets and Modules”.

A response of 0x00 indicates successful pending ANT-WP bootloader activation. The N5 module enters the ANT-WP bootloader mode shortly after sending the response. Serial communication to the module is not available when the bootloader is active.

This mode of operation can be used to upgrade the existing ANT network processor application on the N5 module. When exiting the ANT-WP bootloader mode, an ANT startup message will be generated by the network processor application code. Refer to Start-up Message in the document “ANT Message Protocol and Usage”.

## 5. DC/DC Configuration

Note: this feature is not provided on the N548 models.

The pre-programmed ANT Network Processor Application provides a method of configuring the DC/DC converter on the module via Serial Command. This allows modules featuring compatible ICs to use the DC/DC features of the nRF51422. Please refer to the nRF51422 Product Specification v3.1 for details on the DC/DC (Sections 3.4 and 8.5 particularly). DC/DC should only be used on appropriate modules.

The following serial command message has been defined in the ANT network processor code. A host microcontroller can issue this command to the ANT network processor application to configure the DC/DC operation on the N5 module.

| Sync | Length | MsgID |      | Payload                                     | Checksum |
|------|--------|-------|------|---------------------------------------------|----------|
|      | 0x02   | 0xE4  | 0x01 | 0x00 – DC/DC Disable<br>0x01 – DC/DC Enable |          |

**Table 13: ANT DC/DC Configuration Command**

After issuing the command, the following response is generated.

| Sync | Length | MsgID |      |      |      | Response | Checksum |
|------|--------|-------|------|------|------|----------|----------|
|      | 0x04   | 0xE0  | 0x00 | 0xE4 | 0x01 | 0x00     |          |

**Table 14: ANT DC/DC Configuration Response**

Note: Sync and Chksum values are defined in the document “Interfacing with ANT General Purpose Chipsets and Modules”.

A response of 0x00 indicates successful configuration of the DC/DC.

## Appendix B: Using the ANT Bootloader for OTA Firmware Update

The ANT bootloader supports over-the-air firmware update using ANT File Share (ANT-FS) technology. The following features are supported:

- Application updates with or without existing application on the device
- Bootloader updates
- SoftDevice updates, including swaps from S210 to S310 and vice-versa
- Combined SoftDevice and bootloader updates

A primary ANT bootloader demo and reference code is provided in the nRF51 SDK. The N5 module (except for N548 Rev A) is preloaded with the ANT-WP (Wireless Programming) bootloader that is specially made to work with the ANT Network Processor code.

### 1. Operational Memory Layout

The UICR BOOTLOADERADDR is set to the starting address of the bootloader image. The operational memory layout is shown in the figure below:

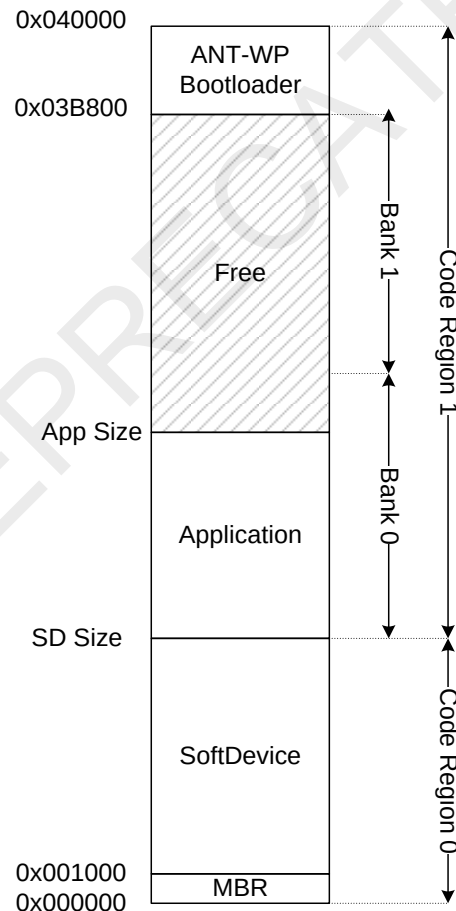


Figure 18: ANT-WP Bootloader Operational Memory Layout

- **ANT-WP Bootloader:** Occupies the reserved flash region between 0x3B800 – 0x40000. Implements an ANT-FS client that uses the ANT SoftDevice stack to handle session based file transfers with an ANT-FS



host over-the-air. Responsible for receiving, processing, storing and activating received images in banked regions Bank0/Bank1.

- **Master Boot Record (MBR):** Occupies region 0x0000 – 0x1000. Manages system startup and interrupt forwarding to the bootloader and the SoftDevice. Used by the ANT-WP bootloader in order to execute the SoftDevice and bootloader image swaps and verification. The MBR is non-updateable and is initially programmed in along with the SoftDevice.
- **SoftDevice:** Occupies flash region starting at address 0x1000, with size depending on the specific SoftDevice (S210/S310) used. Contains ANT protocol stack and SoC interface components used by the ANT-WP bootloader and the ANT Network Processor application code.
- **Application Code/Swap Region (Bank0/Bank1):** The remaining space is divided into two memory banks of equal size, BANK0 (starting after the SoftDevice) and BANK1 (ending before the bootloader). If an application is present in the device, it is placed in the space right after the SoftDevice, and depending on its size, may occupy part or the entirety of BANK0, and none, part or the entirety of BANK1. During image reception, the ANT-WP bootloader uses the banked region(s) as storage space for the incoming image.

The memory region allocation is summarized in the table below:

| Usage                         | Memory ranges (Using S210 V4.0.1 or V5.0.0) | Memory ranges (Using S310 V2.0.0 or V3.0.0) |
|-------------------------------|---------------------------------------------|---------------------------------------------|
| ANT-WP Bootloader             | 0x3B800 – 0x40000                           | 0x3B800 – 0x40000                           |
| Application Code / Swap Space | 0xD000 – 0x3B800                            | 0x1D000 – 0x3B800                           |
| SoftDevice                    | 0x1000 – 0xD000                             | 0x1000 – 0x1D000                            |
| Master Boot Record (MBR)      | 0x0000 – 0x1000                             | 0x0000 – 0x1000                             |

**Table 15: Summary of the ANT-WP Bootloader Operational Memory Layout**

## 2. Entering Bootloader Mode

If there is no existing application on the device, the device will always start in bootloader mode. In the case of an existing application being present, to enter bootloader mode, the application must request bootloader entry by writing to a shared memory block field in the bootloader code region.

Application Programming Interfaces (APIs) used to request bootloader entry are provided in the example N5 ANT Bootloader Demo code mentioned in the document “N5 Module Starter Kit User Manual”. The following files provide the interface.

- ant\_boot\_settings.h
- ant\_boot\_settings\_api.h
- ant\_boot\_settings\_api.c

For more information regarding the shared memory block field between the bootloader code and the application, please refer to the aforementioned “N5 Module Starter Kit User Manual”, under *Passing Information between Application and Bootloader*.

## 3. Bootloader ANT-FS Functionality

Upon entering bootloader state, the ANT-FS-client code is initiated. ANT-FS is a session based transport mechanism designed to handle data file transfers between two ANT enabled devices. A detailed description of ANT-FS is available in the document “ANT-FS Technical Specification”. The specific details of the over-the-air message exchange used for the update process as defined by ANT-FS are outlined in the application note “ANT AN Over the Air Firmware Updates Using ANT-FS”, including the format of files exchanged.

As indicated in the “N5 Module Starter Kit User Manual”, a customized PC implementation of an ANT-FS host used to perform OTA updates (OTA Updater Tool) is provided. This tool automates all of the interactions between host and client to for device information and transfer new images to the module.

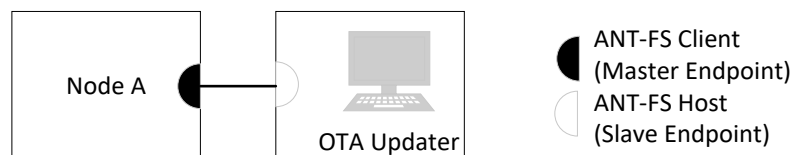


Figure 19: ANT Bootloader Topology

### ANT-FS Configuration

The following tables list the default ANT configurations and ANTFS device identification values used by the preloaded ANT-WP bootloader and supplied OTA Updater tool in order to communicate with each other.

| Parameter         | Value                                                       |
|-------------------|-------------------------------------------------------------|
| Channel Type      | Master                                                      |
| Radio Frequency   | 2450 MHz                                                    |
| Network Key       | ANT-FS Managed Network Key                                  |
| Device Type       | 16                                                          |
| Transmission Type | 5                                                           |
| Device Number     | Least significant 2 bytes of the ANTFS_CLIENT_SERIAL_NUMBER |
| Channel Period    | 8192 (4Hz)                                                  |

Table 16: ANT-WP Bootloader Default ANT Channel Parameters

| Parameter                  | Value                                                               |
|----------------------------|---------------------------------------------------------------------|
| ANTFS_CLIENT_MANUF_ID      | 255. Reserved as development ID.                                    |
| ANTFS_CLIENT_DEV_TYPE      | 1                                                                   |
| ANTFS_CLIENT_SERIAL_NUMBER | Least 4 significant bytes of device identifier in FICR, DEVICEID[0] |
| ANTFS_CLIENT_NAME          | “ANTFS OTA Update”                                                  |

Table 17: ANT-WP Bootloader ANT-FS Device Identification Parameters

ANT-FS authentication method supported by the default ANT-WP bootloader is the PassThru mode. Pairing or passkey authentication methods are not supported in the current version.

## 4. OTA Firmware Update Procedure

Before updating any image component of the N5 module, it is important to review the release notes and test all image components for compatibility.

### Example Usage

The following procedure is a basic example of how to use the provided ANT-WP bootloader code and OTA Updater Tool PC application to perform an OTA firmware update.

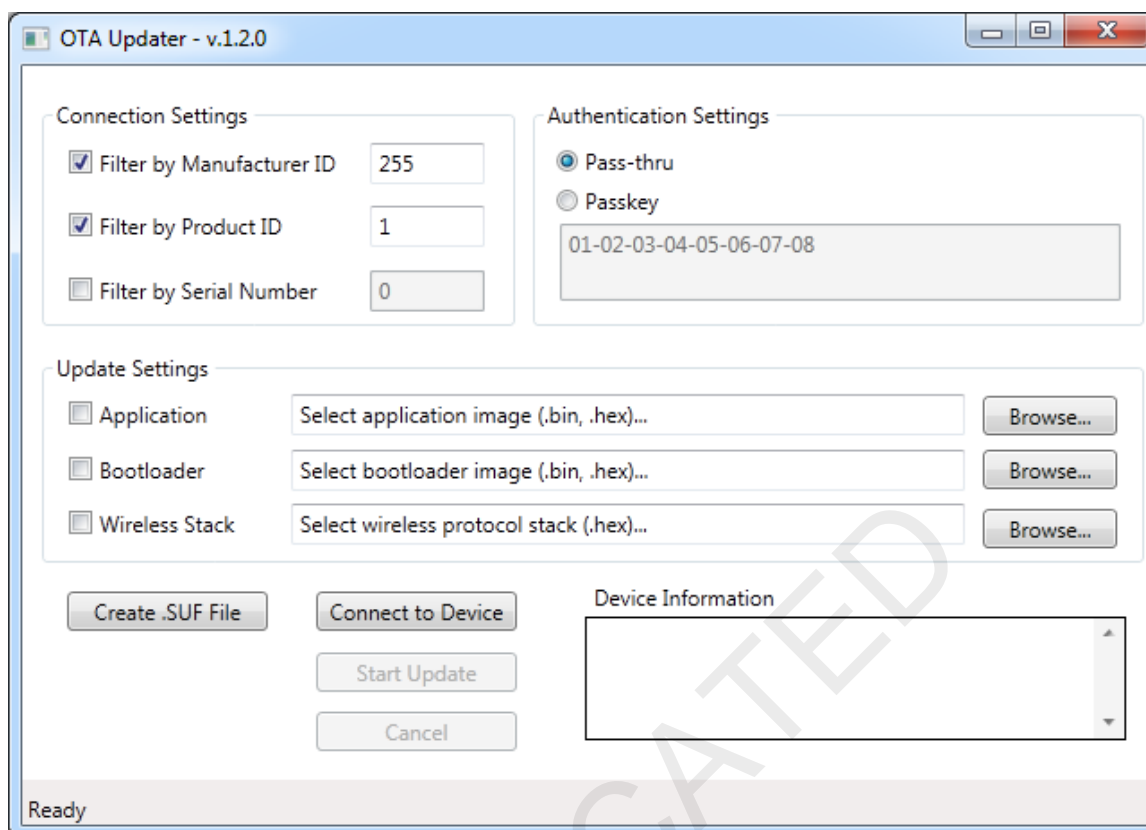


Figure 20: OTA Updater to PC Application

1. Connect an ANT USB stick to the PC
2. Start the OTA Updater application. The status bar at the bottom should indicate "Ready"
3. Configure the Connection Settings. Use the configuration specified in Table 17: ANT-WP Bootloader ANT-FS Device Identification Parameters.
  - a. Specifying the ANTFS\_CLIENT\_SERIAL\_NUMBER (obtained by reading the DEVICE[0] FICR field of the module) will allow the OTA Updater application to connect only to the specified module.
  - b. Specifying 0 (wildcarding) will allow the OTA Updater application to connect to any module in the bootloader state.
4. Configure the Authentication Settings. The ANT-WP bootloader uses pass-thru authentication by default. Passkey authentication is not supported in this version.
5. Browse for the image to update, and make sure the corresponding checkbox is checked. Both binary and hex formats are supported.
6. Initiate the bootloader mode on the target N5 module. Use the bootloader entry methods described in *Entering Bootloader Mode* section or *Bootloader Activation* of Appendix A: Using the ANT Network Processor Configuration.
7. Click on "Connect to Device". Once the bootloader is discovered, the Device Information panel will show *information about the current device, e.g., manufacturer ID, product ID, serial number and versions of the images currently installed on it.*

8. Click on "Start Update". The update process will begin.
9. When the update is complete, the status bar will indicate "Image upload complete. Image will be activated, do not power down device".

### ***Image Activation***

N5 module will remain in the bootloader mode if there is no valid existing application. Preservation of an existing application code may not be guaranteed and can be overwritten by temporary banked data during ANT-FS file transfer. Therefore, it is important to understand the conditions where this can occur.

- Attempting to update the SoftDevice will always invalidate an existing application image
- Attempting to update the bootloader or application, by default, will invalidate an existing application image unless the current application notifies its current usage size using the shared memory block field as described in the "N5 Module Starter Kit User Manual" under *Passing information between Application and Bootloader*. However, if the passed in size value exceeds the size of a single bank region (see Operational Memory Layout), the existing application image cannot be preserved across firmware update.
- If the size of the image update file being transferred during the ANT-FS session exceeds the size of a single bank region, the existing application image will be invalidated.

## Appendix C: N5 Module Pre-Loaded Software Versions

| Module Version | S210 Softv5.0.0Device | ANT-WP Bootloader | ANT Network Processor Code |
|----------------|-----------------------|-------------------|----------------------------|
| N550 and N5150 | V5.0.0 (AXX5.00B00)   | BFD2.00B00        | BAW4.00B00                 |
| N548 rev B     | V4.0.1 (AXX4.00B00)   | BFD1.00B00        | BAW3.00B00                 |
| N548 rev A     | V3.0.0 (AXX3.02B00)   | None              | BAW2.02B00                 |

Table 18: N5 Module Versions and Factory Loaded Software

### 1. Key functional changes in N550 and N5150

- For S210 SoftDevice upgrade details, please refer to S210 v5.0.0 release note in the SoftDevice package.
- For important details on upgrading the SoftDevice via ANT-WP Bootloader from v4.0.1 to v5.0.0, please refer to the S210 v5.0.0 migration document in the SoftDevice package.
- ANT Network processor code BAW4.00B00 provides support for configuring the DC/DC converter.

### 2. Key functional changes in rev B over rev A

- For S210 SoftDevice upgrade details, please refer to S210 v4.0.1 release note in the SoftDevice package.
- The ANT-WP bootloader code, when activated, provides over-the-air firmware update capability using ANT File Share (ANT-FS) technology.
- ANT Network processor code BAW3.00B00 assigned a previously unused Pin to the new BOOT function. The intent of BOOT function is to assist in updating/replacing the default images on the N5 modules using the ANT-WP bootloader without requiring host microcontroller intervention.
- The ANT network process application BAW3.00B00 changes the serial interface behaviour.
  - For synchronous Serial Interface: the SPI rate has been changed from 4MHz to 500kHz when SPD\_SEL (BR3) is low and SPI rate from 500kHz to 4MHz when the pin is high. This change makes it be compatible with AP2/C7 modules.
  - Asynchronous Serial Interface: the RTS now toggles at the end of each message received to indicate message processing