



16K-Bit Microwire Serial EEPROM



FEATURES

- High speed operation: 3 MHz
- Low power CMOS technology
- 1.8 to 5.5 volt operation
- Selectable x8 or x16 memory organization
- Self-timed write cycle with auto-clear
- Hardware and software write protection
- Power-up inadvertant write protection
- Sequential read
- Program enable (PE) pin
- 1,000,000 Program/erase cycles
- 100 year data retention
- Commercial, industrial and automotive temperature ranges
- RoHS-compliant packages

PIN CONFIGURATION

| | PDIP (L) SOIC (V, X) TDFN (ZD4) | | | | SOIC (W) | | |
|----|---------------------------------------|---|-----------------|-----------------|----------|---|-----|
| CS | 1 | 8 | V _{CC} | PE | 1 | 8 | ORG |
| SK | 2 | 7 | PE | V _{CC} | 2 | 7 | GND |
| DI | 3 | 6 | ORG | CS | 3 | 6 | DO |
| DO | 4 | 5 | GND | SK | 4 | 5 | DI |

PIN FUNCTION ⁽¹⁾

| Pin Name | Function |
|-----------------|---------------------|
| CS | Chip Select |
| SK | Clock Input |
| DI | Serial Data Input |
| DO | Serial Data Output |
| V _{CC} | Power Supply |
| GND | Ground |
| ORG | Memory Organization |
| PE | Program Enable |

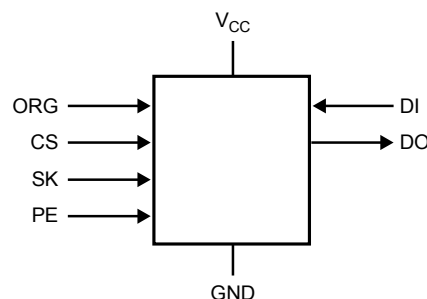
Notes:

- (1) When the ORG pin is connected to V_{CC}, x16 organization is selected. When it is connected to ground, x8 pin is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.

DESCRIPTION

The CAT93C86 is a 16K-bit Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at V_{CC}) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C86 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin DIP, 8-pin SOIC and 8-pad TDFN packages.

FUNCTIONAL SYMBOL



For Ordering Information details, see page 12.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| Parameters | Ratings | Units |
|--|-------------------------------|-------|
| Temperature Under Bias | –55 to +125 | °C |
| Storage Temperature | –65 to 150 | °C |
| Voltage on any Pin with Respect to Ground ⁽²⁾ | –2.0 to +V _{CC} +2.0 | V |
| V _{CC} with Respect to Ground | –2.0 to +7.0 | V |
| Package Power Dissipation Capability (T _A = 25°C) | 1.0 | W |
| Lead Soldering Temperature (10 seconds) | 300 | °C |
| Output Short Circuit Current ⁽³⁾ | 100 | mA |

RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Units |
|------------------------------------|--------------------|-------------------------------|-----------|-------------|
| N _{END} ⁽⁴⁾ | Endurance | MIL-STD-883, Test Method 1033 | 1,000,000 | Cycles/Byte |
| T _{DR} ⁽⁴⁾ | Data Retention | MIL-STD-883, Test Method 1008 | 100 | Years |
| V _{ZAP} ⁽⁴⁾ | ESD Susceptibility | MIL-STD-883, Test Method 3015 | 2000 | V |
| I _{LTH} ⁽⁴⁾⁽⁵⁾ | Latch-Up | JEDEC Standard 17 | 100 | mA |

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8 V to +5.5 V unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|------------------|--|--|-----------------------|-----|-----------------------|-------|
| I _{CC1} | Power Supply Current (Write) | f _{SK} = 1 MHz; V _{CC} = 5.0 V | | | 3 | mA |
| I _{CC2} | Power Supply Current (Read) | f _{SK} = 1 MHz; V _{CC} = 5.0 V | | | 500 | μA |
| I _{SB1} | Power Supply Current (Standby) (x8 Mode) | CS = 0 V ORG = GND | | | 10 | μA |
| I _{SB2} | Power Supply Current (Standby) (x16 Mode) | CS = 0 V ORG = Float or V _{CC} | | 0 | 10 | μA |
| I _{LI} | Input Leakage Current | V _{IN} = 0 V to V _{CC} | | | 1 | μA |
| I _{LO} | Output Leakage Current (Including ORG pin) | V _{OUT} = 0 V to V _{CC} , CS = 0 V | | | 1 | μA |
| V _{IL1} | Input Low Voltage | 4.5 V ≤ V _{CC} < 5.5 V | –0.1 | | 0.8 | V |
| V _{IH1} | Input High Voltage | 4.5 V ≤ V _{CC} < 5.5 V | 2 | | V _{CC} + 1 | V |
| V _{IL2} | Input Low Voltage | 1.8 V ≤ V _{CC} < 4.5 V | 0 | | V _{CC} × 0.2 | V |
| V _{IH2} | Input High Voltage | 1.8 V ≤ V _{CC} < 4.5 V | V _{CC} × 0.7 | | V _{CC} + 1 | V |
| V _{OL1} | Output Low Voltage | 4.5 V ≤ V _{CC} < 5.5 V; I _{OL} = 2.1 mA | | | 0.4 | V |
| V _{OH1} | Output High Voltage | 4.5 V ≤ V _{CC} < 5.5 V; I _{OH} = –400 μA | 2.4 | | | V |
| V _{OL2} | Output Low Voltage | 1.8 V ≤ V _{CC} < 4.5 V; I _{OL} = 1 mA | | | 0.2 | V |
| V _{OH2} | Output High Voltage | 1.8 V ≤ V _{CC} < 4.5 V; I _{OH} = –100 μA | V _{CC} – 0.2 | | | V |

Notes:

- (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) These parameters are tested initially and after a design or process change that affects the parameter.
- (5) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V.

PIN CAPACITANCE ⁽¹⁾

| Symbol | Test | Conditions | Min | Typ | Max | Units |
|------------------|-------------------------------------|------------------------|-----|-----|-----|-------|
| C _{OUT} | Output Capacitance (DO) | V _{OUT} = 0 V | | | 5 | pF |
| C _{IN} | Input Capacitance (CS, SK, DI, ORG) | V _{IN} = 0 V | | | 5 | pF |

POWER-UP TIMING ⁽¹⁾⁽²⁾

| Symbol | Parameter | Max | Units |
|------------------|-----------------------------|-----|-------|
| t _{PUR} | Power-up to Read Operation | 1 | ms |
| t _{PUW} | Power-up to Write Operation | 1 | ms |

A.C. TEST CONDITIONS

| | | |
|---------------------------|--|---------------------------------|
| Input Rise and Fall Times | ≤ 50 ns | |
| Input Pulse Voltages | 0.4 V to 2.4 V | 4.5 V ≤ V _{CC} ≤ 5.5 V |
| Timing Reference Voltages | 0.8 V, 2.0 V | 4.5 V ≤ V _{CC} ≤ 5.5 V |
| Input Pulse Voltages | 0.2 x V _{CC} to 0.7 x V _{CC} | 1.8 V ≤ V _{CC} ≤ 4.5 V |
| Timing Reference Voltages | 0.5 x V _{CC} | 1.8 V ≤ V _{CC} ≤ 4.5 V |

A.C. CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} = 1.8 V - 5.5 V | | V _{CC} = 2.5 V - 5.5 V | | V _{CC} = 4.5 V - 5.5 V | | Units |
|--------------------------------|------------------------------|--|---------------------------------|-----|---------------------------------|------|---------------------------------|------|-------|
| | | | Min | Max | Min | Max | Min | Max | |
| t _{CSS} | CS Setup Time | | 200 | | 100 | | 50 | | ns |
| t _{CSH} | CS Hold Time | | 0 | | 0 | | 0 | | ns |
| t _{DIS} | DI Setup Time | | 200 | | 100 | | 50 | | ns |
| t _{DIH} | DI Hold Time | | 200 | | 100 | | 50 | | ns |
| t _{PD1} | Output Delay to 1 | | | 1 | | 0.5 | | 0.15 | μs |
| t _{PD0} | Output Delay to 0 | C _L = 100 pF ⁽³⁾ | | 1 | | 0.5 | | 0.15 | μs |
| t _{HZ} ⁽¹⁾ | Output Delay to High-Z | | | 400 | | 200 | | 100 | ns |
| t _{EW} | Program/Erase Pulse Width | | | 5 | | 5 | | 5 | ms |
| t _{CSMIN} | Minimum CS Low Time | | 1 | | 0.5 | | 0.15 | | μs |
| t _{SKHI} | Minimum SK High Time | | 1 | | 0.5 | | 0.15 | | μs |
| t _{SKLOW} | Minimum SK Low Time | | 1 | | 0.5 | | 0.15 | | μs |
| t _{SV} | Output Delay to Status Valid | | | 1 | | 0.5 | | 0.1 | μs |
| SK _{MAX} | Maximum Clock Frequency | | DC | 500 | DC | 1000 | DC | 3000 | kHz |

Notes:

- (1) These parameters are tested initially and after a design or process change that affects the parameter.
- (2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
- (3) The input levels and timing reference points are shown in the "AC Test Conditions" table.

INSTRUCTION SET

| Instruction | Start Bit | Opcode | Address | | Data | | Comments |
|-------------|-----------|--------|--------------|--------------|-------|--------|----------------------|
| | | | x8 | x16 | x8 | x16 | |
| READ | 1 | 10 | A10-A0 | A9-A0 | | | Read Address AN– A0 |
| ERASE | 1 | 11 | A10-A0 | A9-A0 | | | Clear Address AN– A0 |
| WRITE | 1 | 01 | A10-A0 | A9-A0 | D7-D0 | D15-D0 | Write Address AN– A0 |
| EWEN | 1 | 00 | 11XXXXXXXXXX | 11XXXXXXXXXX | | | Write Enable |
| EWDS | 1 | 00 | 00XXXXXXXXXX | 00XXXXXXXXXX | | | Write Disable |
| ERAL | 1 | 00 | 10XXXXXXXXXX | 10XXXXXXXXXX | | | Clear All Addresses |
| WRAL | 1 | 00 | 01XXXXXXXXXX | 01XXXXXXXXXX | D7-D0 | D15-D0 | Write All Addresses |

DEVICE OPERATION

The CAT93C86 is a 16,384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C86 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 14-bit instructions control the reading, writing and erase operations of the device. The CAT93C86 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 10-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

Note: The Write, Erase, Write all and Erase all instructions require PE=1. If PE is left floating, 93C86

is in Program Enabled mode. For Write Enable and Write Disable instruction PE = don't care.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C86 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C86 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

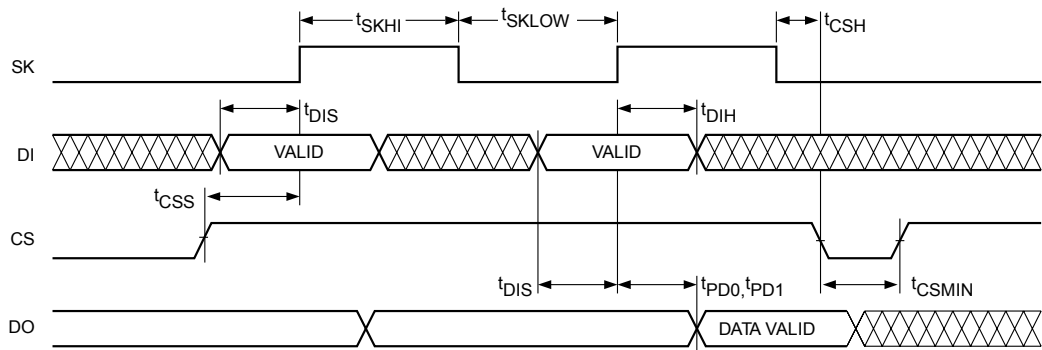


Figure 1. Synchronous Data Timing

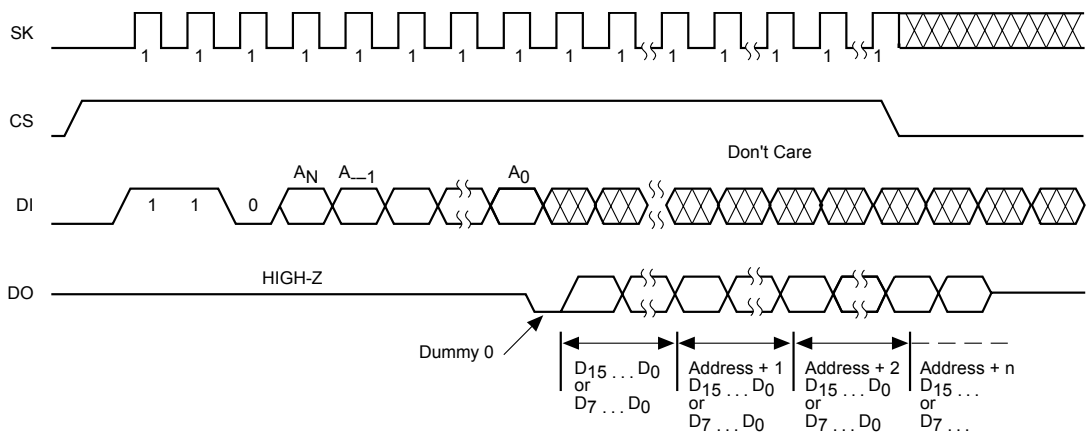


Figure 2. Read Instruction Timing

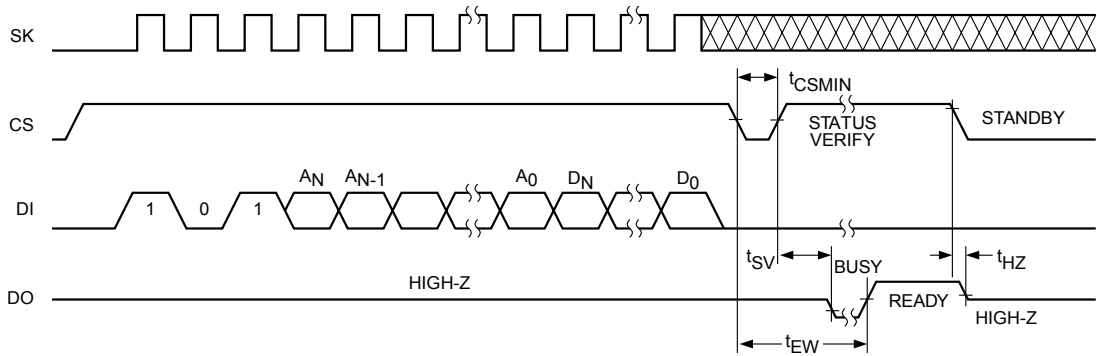


Figure 3. Write Instruction Timing

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C86 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C86 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C86 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C86 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C86 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

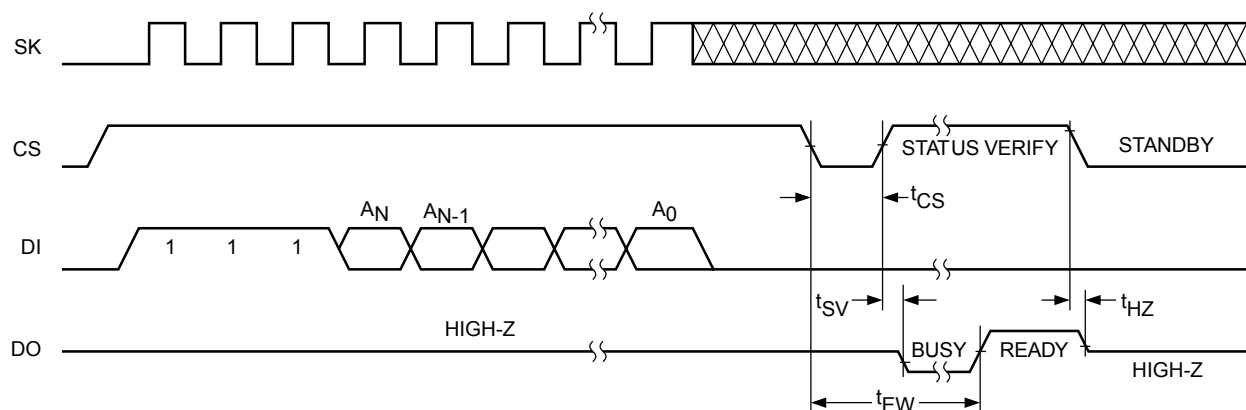
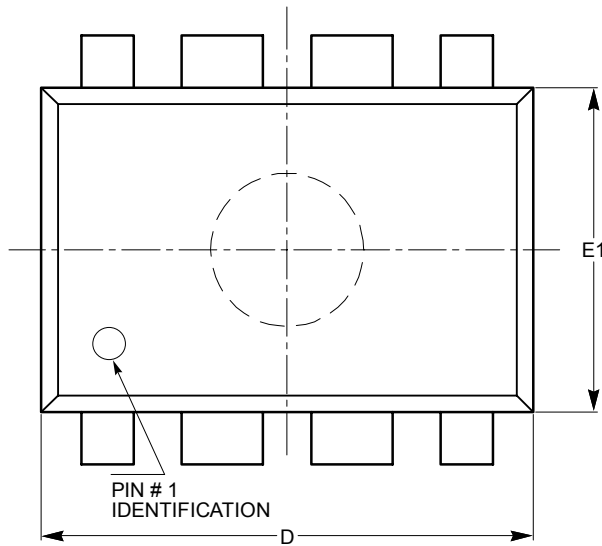


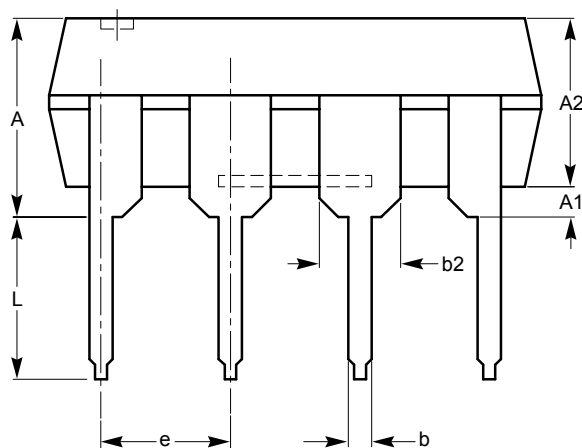
Figure 4. Erase Instruction Timing

PACKAGE OUTLINE DRAWINGS

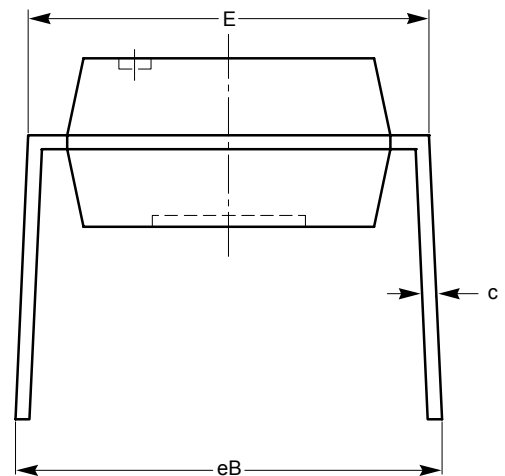
PDIP 8-Lead 300 mils (L) ⁽¹⁾⁽²⁾

TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|-------|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| e | 2.54 BSC | | |
| E1 | 6.10 | 6.35 | 7.11 |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |



SIDE VIEW



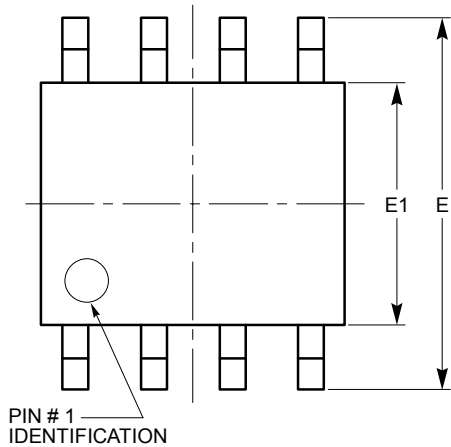
END VIEW

For current Tape and Reel information, download the PDF file from:
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Notes:

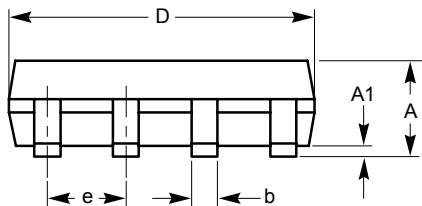
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard MS-001.

SOIC 8-Lead 150 mils (V) ⁽¹⁾⁽²⁾

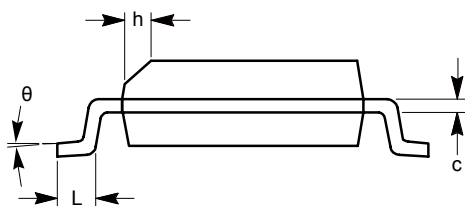


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|-----|------|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0° | | 8° |



SIDE VIEW

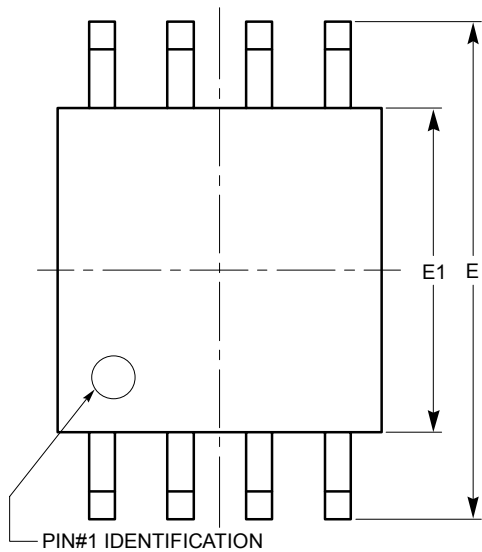


END VIEW

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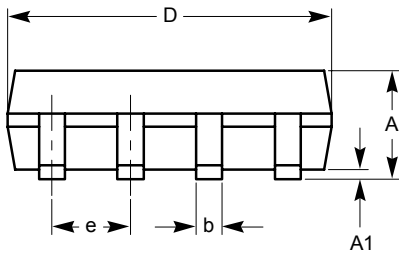
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MS-012.

SOIC 8-Lead EIAJ 208 mils (X) ⁽¹⁾⁽²⁾

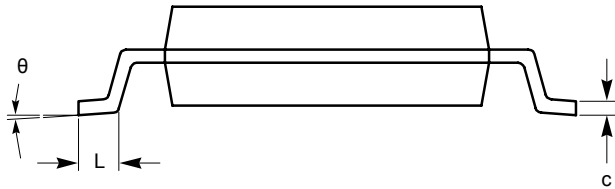


TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|----------|-----|------|
| A | | | 2.03 |
| A1 | 0.05 | | 0.25 |
| b | 0.36 | | 0.48 |
| c | 0.19 | | 0.25 |
| D | 5.13 | | 5.33 |
| E | 7.75 | | 8.26 |
| E1 | 5.13 | | 5.38 |
| e | 1.27 BSC | | |
| L | 0.51 | | 0.76 |
| θ | 0° | | 8° |



SIDE VIEW



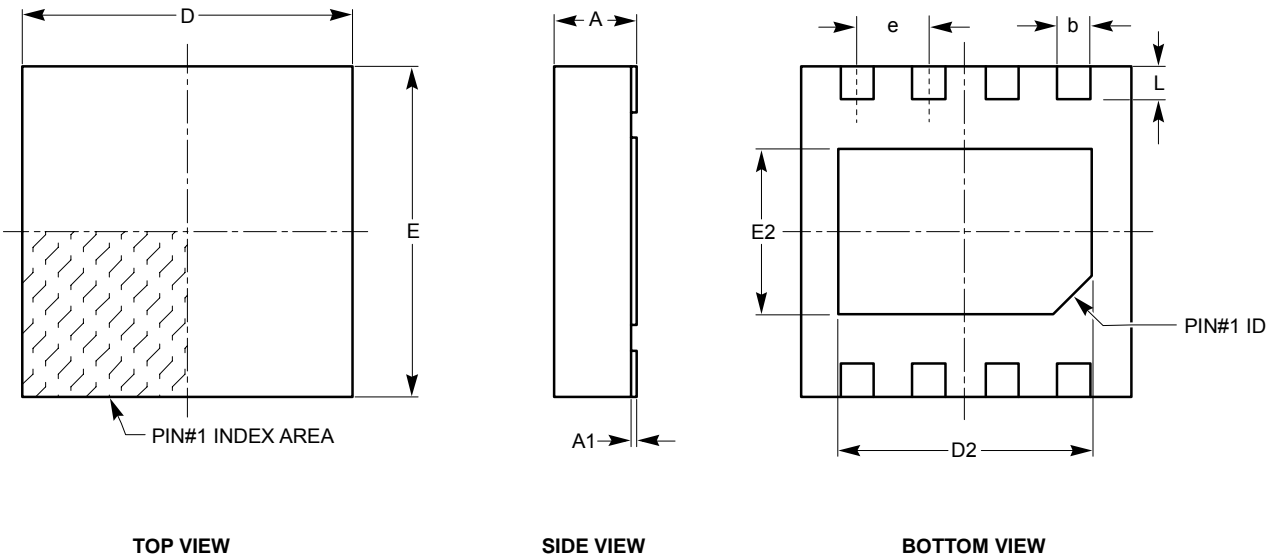
END VIEW

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<http://www.catsemi.com/documents/tapeandreel.pdf>.

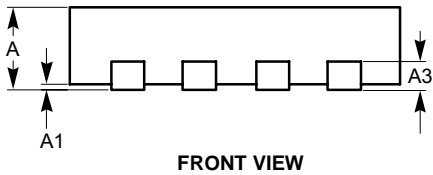
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with EIAJ standard EDR-7320.

TDFN 8-Pad 3 x 3 mm (ZD4) ⁽¹⁾⁽²⁾



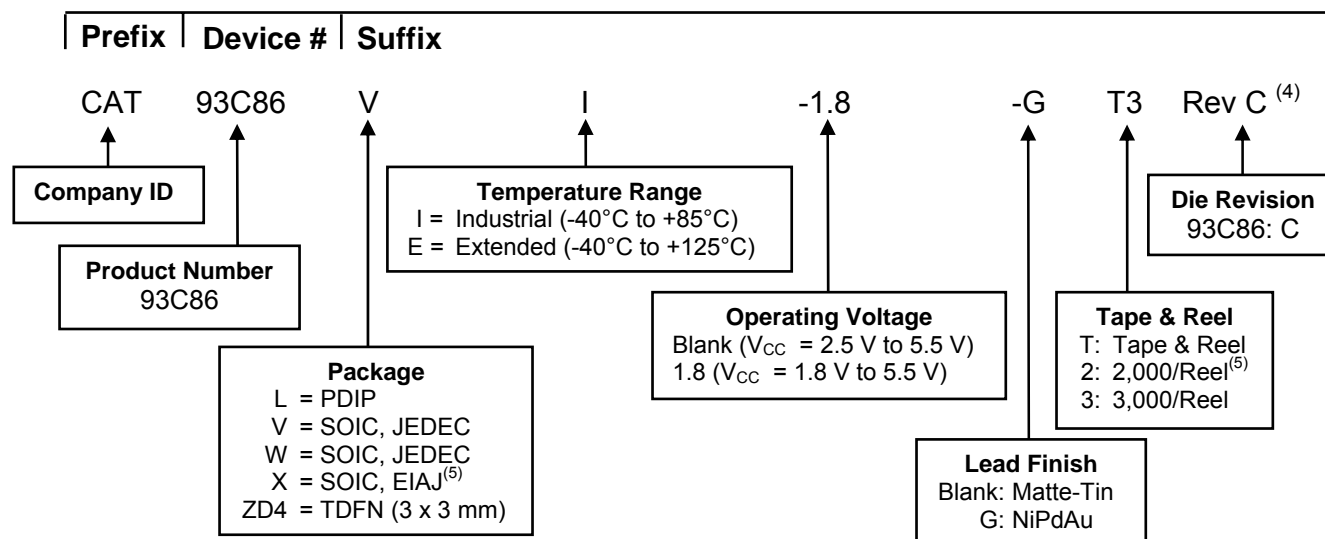
| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.23 | 0.30 | 0.37 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.20 | — | 2.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.40 | — | 1.80 |
| e | 0.65 TYP | | |
| L | 0.20 | 0.30 | 0.40 |



For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-229.

EXAMPLE OF ORDERING INFORMATION



ORDERING INFORMATION

| Orderable Part Numbers | |
|------------------------|------------------|
| CAT93C86LI-G | CAT93C86LE-G |
| CAT93C86VI-GT3 | CAT93C86VE-GT3 |
| CAT93C86WI-GT3 | CAT93C86WE-GT3 |
| CAT93C86XI-T2 | CAT93C86XE-T2 |
| CAT93C86ZD4I-GT3 | CAT93C86ZD4E-GT3 |
| CAT93C86VI1.8GT3* | |

* Part number is not exactly the same as the "Example of Ordering Information" shown above. For part numbers marked with * there are NO hyphens in the orderable part numbers.

For Product Top Mark Codes, click here:
<http://www.catsemi.com/techsupport/producttopmark.asp>


Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a 93C86VI-GT3 (SOIC, Industrial Temperature, 1.8 V to 5.5 V, NiPdAu, Tape & Reel, 3,000/Reel)
- (4) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWE.) For additional information, please contact your ON Semiconductor sales office.
- (5) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2,000/Reel, i.e., CAT93C86XI-T2.
- (6) For additional package and temperature options, please contact your nearest ON Semiconductor sales office.

CAT93C86 (Rev. C)

REVISION HISTORY

| Date | Rev. | Comments |
|-----------|------|--|
| 14-May-04 | L | New Data Sheet Created From CAT93C46/56/57/66/86. Parts CAT93C56, CAT93C56, CAT93C57, CAT93C66, CAT93C76 and CAT93C86 have been separated into single data sheets Add Die Revision ID Letter Update Features Update Description Update Pin Condition Add Functional Diagram Update Pin Function Update D.C. Operating Characteristics Update Pin Capacitance Update Instruction Set Update Device Operation Update Ordering Information |
| 10-Aug-04 | M | Added TDFN Package pin out |
| 03-Sep-04 | N | Minor changes |
| 13-Oct-06 | O | Update Features Update Pin Configuration Update Pin Functions Update D.C. Operating Characteristics (VCC Range) Update A.C. Characteristics (VCC Range) Update Ordering Information |
| 21-May-08 | P | Update Package Outline Drawings Add Top Mark Code Link Update Document Layout |
| 29-Oct-08 | R | Change logo and fine print to ON Semiconductor |
| 13-Jul-09 | S | Update Ordering Information table |

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