# MC74HCT259A

# 8-Bit Addressable Latch 1-of-8 Decoder with LSTTL Inputs

## High−Performance Silicon−Gate CMOS

The MC74HCT259A is identical in pinout to the LS259. The device inputs are compatible with standard CMOS and LSTTL outputs.

The HCT259A has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non−addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one−of−eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode all outputs are LOW and unaffected by the address and data inputs. When operating the HCT259A as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb−Free Devices

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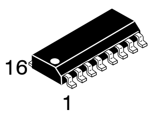
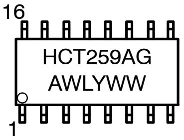
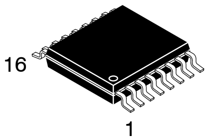
### MARKING DIAGRAMS

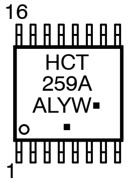


**SOIC−16**
**D SUFFIX**
**CASE 751B**



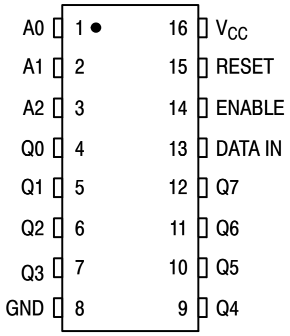


**TSSOP−16**
**DT SUFFIX**
**CASE 948F**



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### MODE SELECTION TABLE

| Enable | Reset | Mode |
|---|---|---|
| L | H | Addressable Latch |
| H | H | Memory |
| L | L | 8−Line Demultiplexer |
| H | L | Reset |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

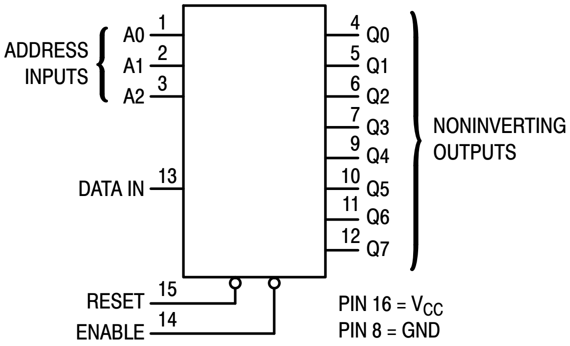


**Figure 1. Logic Diagram**

### LATCH SELECTION TABLE

| Address Inputs | | | Latch Addressed |
|---|---|---|---|
| **C** | **B** | **A** | |
| L | L | L | Q0 |
| L | L | H | Q1 |
| L | H | L | Q2 |
| L | H | H | Q3 |
| H | L | L | Q4 |
| H | L | H | Q5 |
| H | H | L | Q6 |
| H | H | H | Q7 |

### MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | –0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | –0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | –0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, SOIC Package<br>TSSOP Package | 500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | –65 to + 150 | °C |
| $V_{ESD}$ | ESD Withstand Voltage<br>Human Body Model (Note 1)<br>Machine Model (Note 2) | <br>>2000<br>>200 | V |
| $I_{Latchup}$ | Latchup Performance Above $V_{DD}$ and Below GND at 125°C (Note 3) | ±100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA / JESD22–A114–A.
2. Tested to EIA / JESD22–A115–A.
3. Tested to EIA / JESD78.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

### RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | –55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 2) | 0 | 500 | ns |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\lvert I_{out}\rvert \leq 20$ µA | 4.5<br>5.5 | 2.0<br>2.0 | 2.0<br>2.0 | 2.0<br>2.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\lvert I_{out}\rvert \leq 20$ µA | 4.5<br>5.5 | 0.8<br>0.8 | 0.8<br>0.8 | 0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\lvert I_{out}\rvert \leq 20$ µA | 4.5<br>5.5 | 4.4<br>5.4 | 4.4<br>5.4 | 4.4<br>5.4 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\lvert I_{out}\rvert \leq 5.2$ mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\lvert I_{out}\rvert \leq 20$ µA | 4.5<br>5.5 | 0.1<br>0.1 | 0.1<br>0.1 | 0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\lvert I_{out}\rvert \leq 5.2$ mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 µA | 5.5 | 4 | 40 | 160 | µA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Additional Quiescent Supply Current | $V_{in}$ = 2.4V, Any One Input<br>$V_{in}$ = $V_{CC}$ or GND, Other Inputs<br>$I_{out}$ = 0µA | | ≥ –55°C | 25 to 125°C | |
| | | | 5.5 | 2.9 | 2.4 | mA |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 4.5 to 5.5 V, $C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Data to Output (Figures 2 and 7) | 32 | 32 | 42 | ns |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Address Select to Output (Figures 3 and 7) | 32 | 40 | 45 | ns |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Enable to Output (Figures 4 and 7) | 32 | 40 | 45 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Output (Figures 5 and 7) | 22 | 26 | 32 | ns |
| $t_{TLH}$,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 7) | 15 | 19 | 22 | ns |
| $C_{in}$ | Maximum Input Capacitance | 10 | 10 | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package) | 30 | pF |

**TIMING REQUIREMENTS** ($V_{CC}$ = 4.5 to 5.5 V, Input $t_r$ = $t_f$ = 6 ns)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|
| | | –55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{su}$ | Minimum Setup Time, Address or Data to Enable (Figure 6) | 15 | 19 | 22 | ns |
| $t_h$ | Minimum Hold Time, Enable to Address or Data (Figure 6) | 1 | 1 | 1 | ns |
| $t_w$ | Minimum Pulse Width, Reset or Enable (Figure 4 or 5) | 15 | 19 | 22 | ns |

## SWITCHING WAVEFORMS

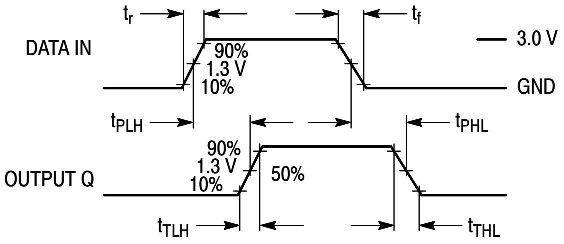


**Figure 2.**

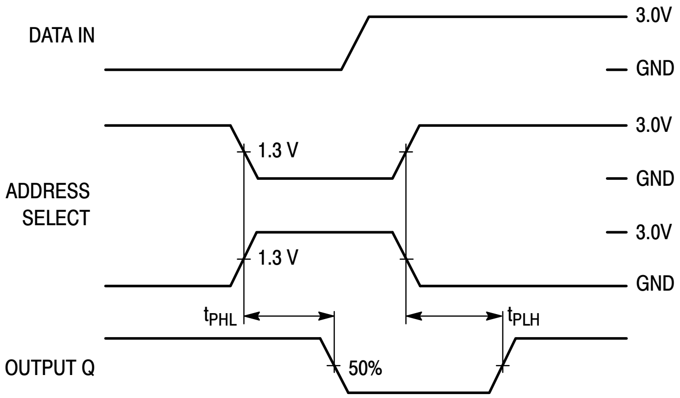


**Figure 3.**

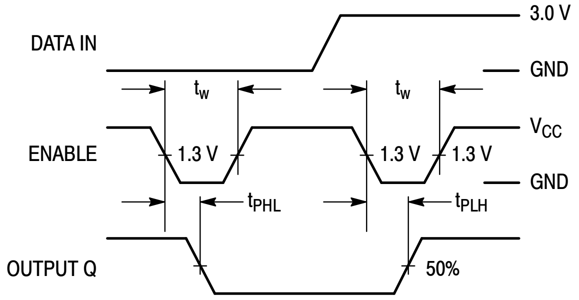


**Figure 4.**

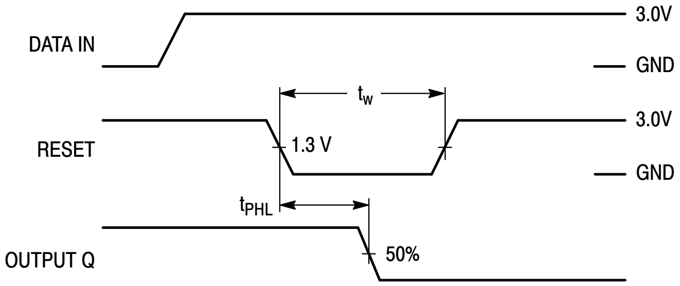


**Figure 5.**

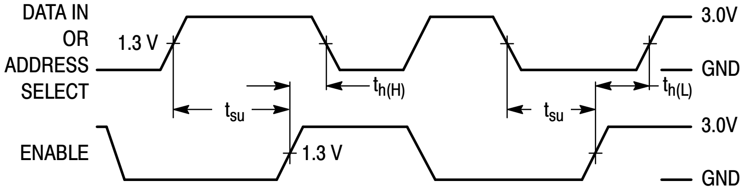
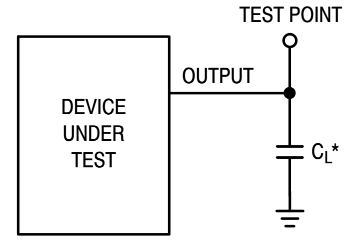


**Figure 6.**



*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

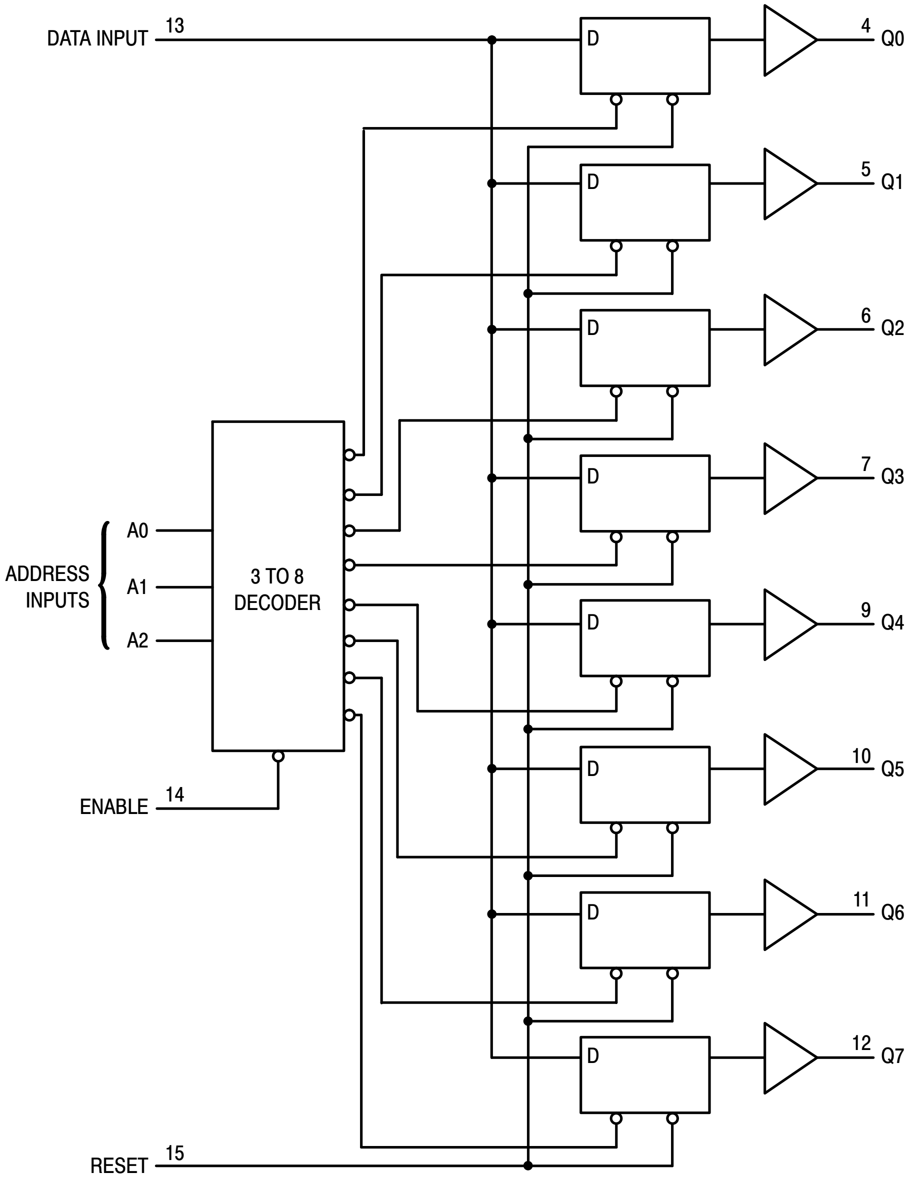


Figure 8. Expanded Logic Diagram

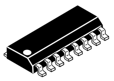
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HCT259ADG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC74HCT259ADR2G | SOIC−16<br>(Pb−Free) | 2500 Tape & Reel |
| MC74HCT259ADTR2G | TSSOP−16* | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb−Free.

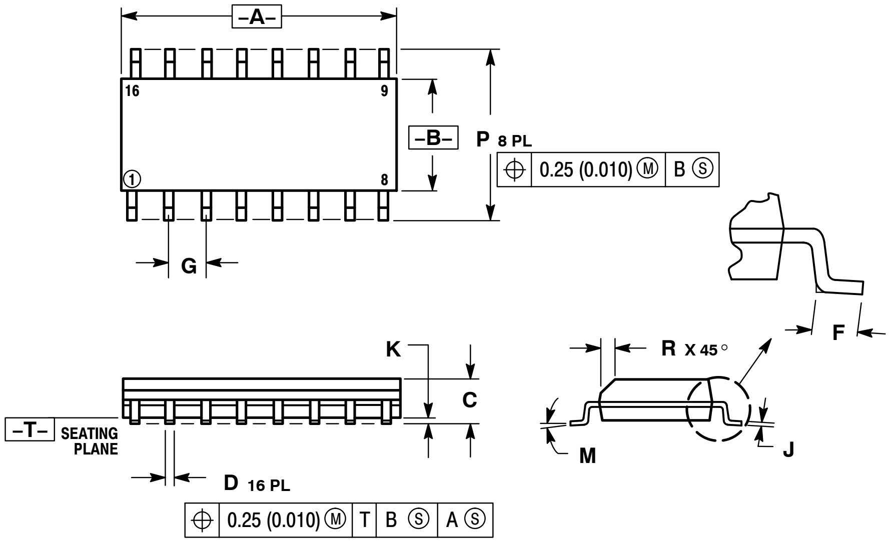
# MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

## SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

| STYLE 1: | |
|---|---|
| PIN 1. | COLLECTOR |
| 2. | BASE |
| 3. | EMITTER |
| 4. | NO CONNECTION |
| 5. | EMITTER |
| 6. | BASE |
| 7. | COLLECTOR |
| 8. | COLLECTOR |
| 9. | BASE |
| 10. | EMITTER |
| 11. | NO CONNECTION |
| 12. | EMITTER |
| 13. | BASE |
| 14. | COLLECTOR |
| 15. | EMITTER |
| 16. | COLLECTOR |

| STYLE 2: | |
|---|---|
| PIN 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

| STYLE 3: | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE, #1 |
| 3. | EMITTER, #1 |
| 4. | COLLECTOR, #1 |
| 5. | COLLECTOR, #2 |
| 6. | BASE, #2 |
| 7. | EMITTER, #2 |
| 8. | COLLECTOR, #2 |
| 9. | COLLECTOR, #3 |
| 10. | BASE, #3 |
| 11. | EMITTER, #3 |
| 12. | COLLECTOR, #3 |
| 13. | COLLECTOR, #4 |
| 14. | BASE, #4 |
| 15. | EMITTER, #4 |
| 16. | COLLECTOR, #4 |

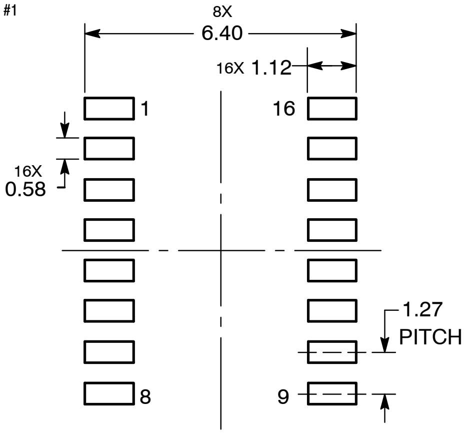
| STYLE 4: | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | COLLECTOR, #1 |
| 3. | COLLECTOR, #2 |
| 4. | COLLECTOR, #2 |
| 5. | COLLECTOR, #3 |
| 6. | COLLECTOR, #3 |
| 7. | COLLECTOR, #4 |
| 8. | COLLECTOR, #4 |
| 9. | BASE, #4 |
| 10. | EMITTER, #4 |
| 11. | BASE, #3 |
| 12. | EMITTER, #3 |
| 13. | BASE, #2 |
| 14. | EMITTER, #2 |
| 15. | BASE, #1 |
| 16. | EMITTER, #1 |

| STYLE 5: | |
|---|---|
| PIN 1. | DRAIN, DYE #1 |
| 2. | DRAIN, #1 |
| 3. | DRAIN, #2 |
| 4. | DRAIN, #2 |
| 5. | DRAIN, #3 |
| 6. | DRAIN, #3 |
| 7. | DRAIN, #4 |
| 8. | DRAIN, #4 |
| 9. | GATE, #4 |
| 10. | SOURCE, #4 |
| 11. | GATE, #3 |
| 12. | SOURCE, #3 |
| 13. | GATE, #2 |
| 14. | SOURCE, #2 |
| 15. | GATE, #1 |
| 16. | SOURCE, #1 |

| STYLE 6: | |
|---|---|
| PIN 1. | CATHODE |
| 2. | CATHODE |
| 3. | CATHODE |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | CATHODE |
| 7. | CATHODE |
| 8. | CATHODE |
| 9. | ANODE |
| 10. | ANODE |
| 11. | ANODE |
| 12. | ANODE |
| 13. | ANODE |
| 14. | ANODE |
| 15. | ANODE |
| 16. | ANODE |

| STYLE 7: | |
|---|---|
| PIN 1. | SOURCE N-CH |
| 2. | COMMON DRAIN (OUTPUT) |
| 3. | COMMON DRAIN (OUTPUT) |
| 4. | GATE P-CH |
| 5. | COMMON DRAIN (OUTPUT) |
| 6. | COMMON DRAIN (OUTPUT) |
| 7. | COMMON DRAIN (OUTPUT) |
| 8. | SOURCE P-CH |
| 9. | SOURCE P-CH |
| 10. | COMMON DRAIN (OUTPUT) |
| 11. | COMMON DRAIN (OUTPUT) |
| 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE N-CH |
| 14. | COMMON DRAIN (OUTPUT) |
| 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE N-CH |

## RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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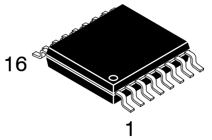
| **DESCRIPTION:** | **SOIC−16** | **PAGE 1 OF 1** |

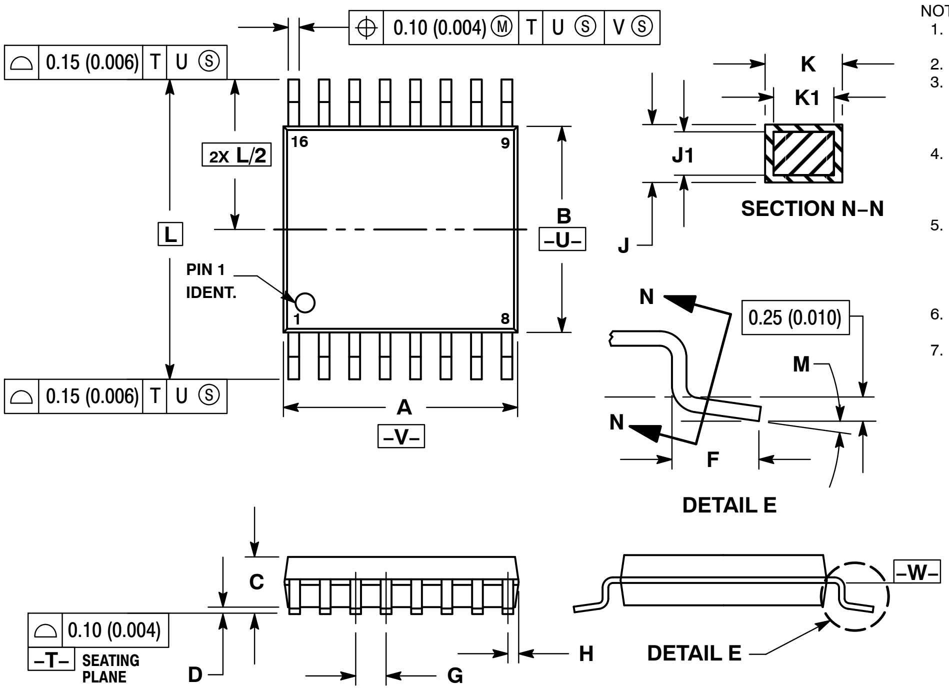
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 2:1

### TSSOP−16 WB
CASE 948F
ISSUE B

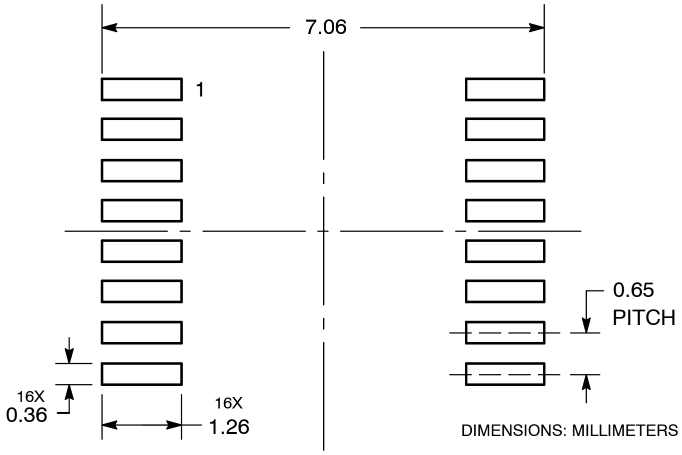
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

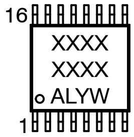
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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