PESD5V0V1BSF

Ultra low profile bidirectional very low capacitance ESD protection diode

9 September 2025 **Product data sheet**

1. General description

Very low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a SOD962 leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Bidirectional ESD protection of one line
- Very low diode capacitance C_d = 3.5 pF
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Ultra small SMD package
- Symmetrical breakdown voltage

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

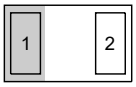
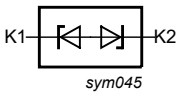
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-5	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[1]	2.5	3.5	4.5	pF

[1] This parameter is guaranteed by design.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 Transparent top view **DSN0603-2 (SOD962)**	
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0V1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 x 0.3 x 0.3 mm body	SOD962

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0V1BSF	V

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	rated peak pulse power	t_p = 8/20 µs	[1] [2]	-	8	W
I_{PPM}	rated peak pulse current		[1] [2]	-	1	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2] [3]	-	15	kV
		IEC 61000-4-2 (air discharge)		-	15	kV
		MIL-STD-883 (human body model)		-	15	kV

[1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.
[2] Measured from pin 1 to pin 2.
[3] Device stressed with ten non-repetitive ESD pulses; see Figure 2.

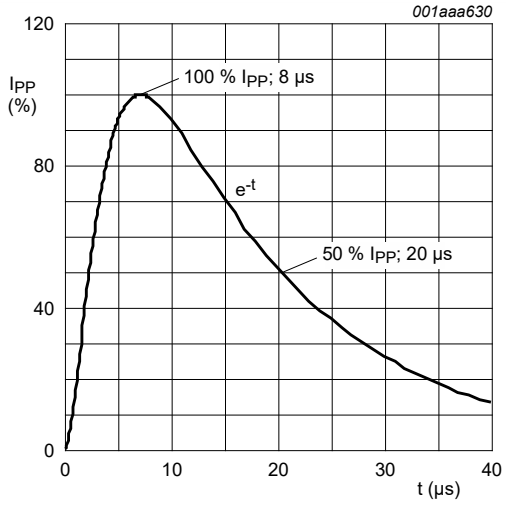


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

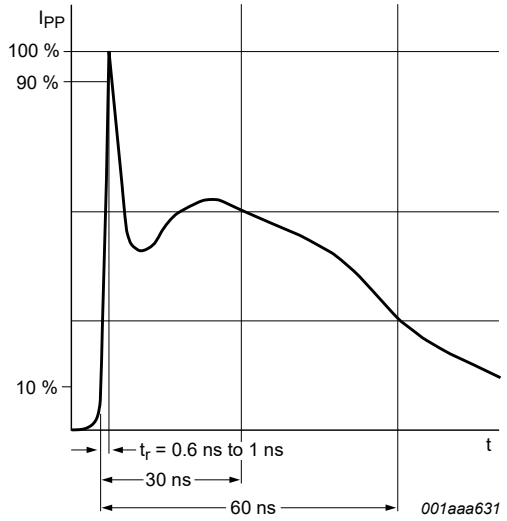


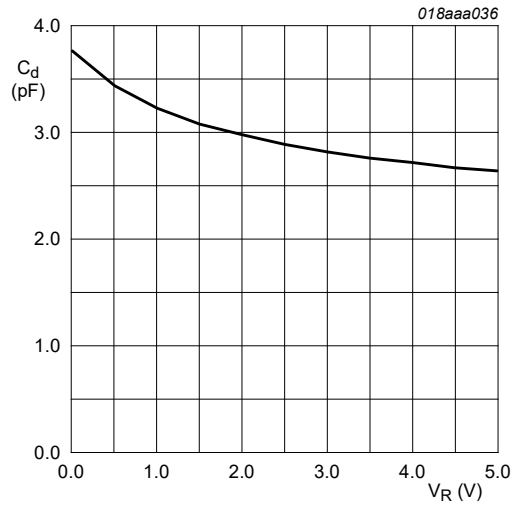
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-5	-	5	V
V_{BR}	breakdown voltage	I_R = 1 mA; T_{amb} = 25 °C	[1]	6	-	10	V
		I_R = -1 mA; T_{amb} = 25 °C	[1]	-10	-	-6	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V; T_{amb} = 25 °C		-	1	100	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C	[2]	2.5	3.5	4.5	pF
		f = 1 MHz; V_R = 2.5 V; T_{amb} = 25 °C	[2]	-	2.7	3.5	pF
		f = 1 MHz; V_R = 5 V; T_{amb} = 25 °C	[2]	-	2.5	3.2	pF
V_{CL}	clamping voltage	I_{PP} = 0.5 A; T_{amb} = 25 °C	[3] [4]	-	-	11.5	V
		I_{PP} = 1 A; T_{amb} = 25 °C	[3] [4]	-	-	12.8	V
L_s	series inductance	T_{amb} = 25 °C	[5]	-	0.05	-	nH
R_{dyn}	dynamic resistance		[6]	-	2.5	-	Ω

[1] Breakdown voltage is always symmetrical within the characterized range, which means no difference in breakdown voltage from pin 1 to pin 2 and vice versa.
[2] This parameter is guaranteed by design.
[3] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.
[4] Measured from pin 1 to pin 2.
[5] Calculated from S-parameter values.
[6] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI/ESD STM5.5.1-2008.



f = 1 MHz; T_{amb} = 25 °C

Fig. 3. Diode capacitance as a function of reverse voltage; typical values

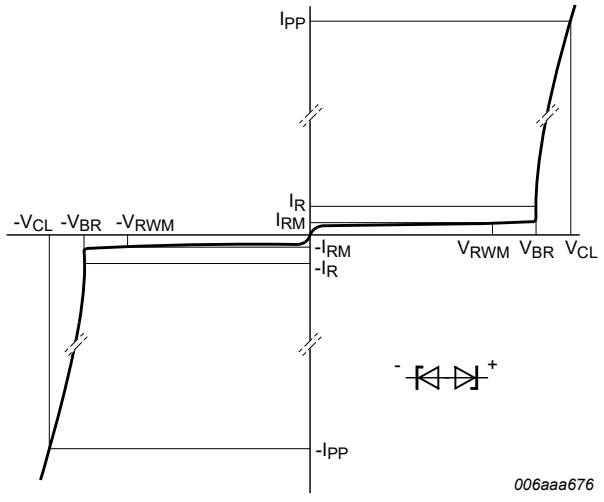


Fig. 4. V-I characteristics for a bidirectional ESD protection diode

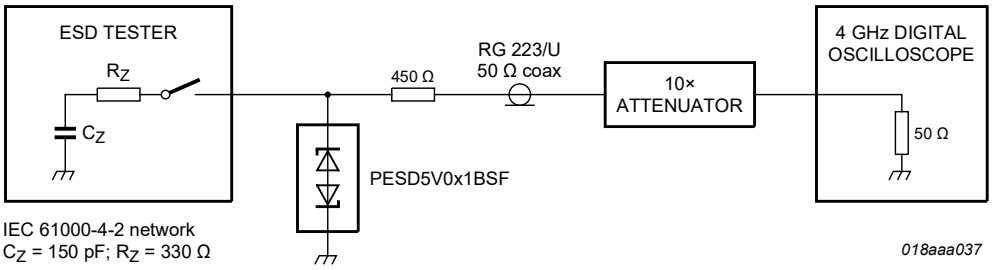
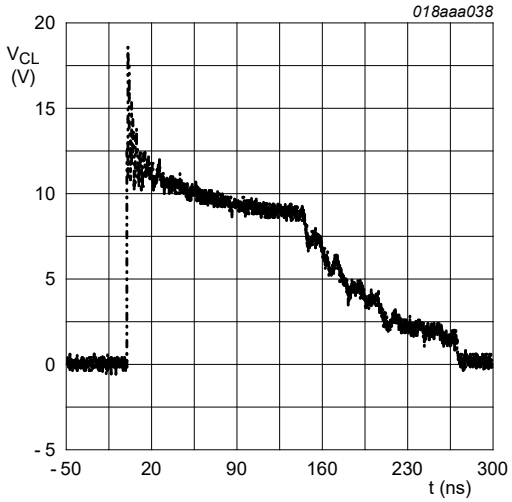
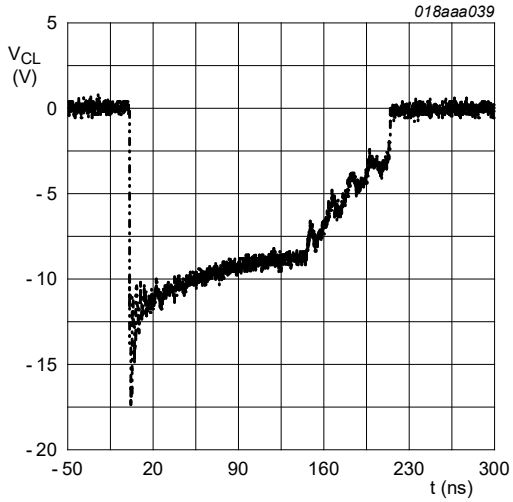


Fig. 5. ESD clamping test setup



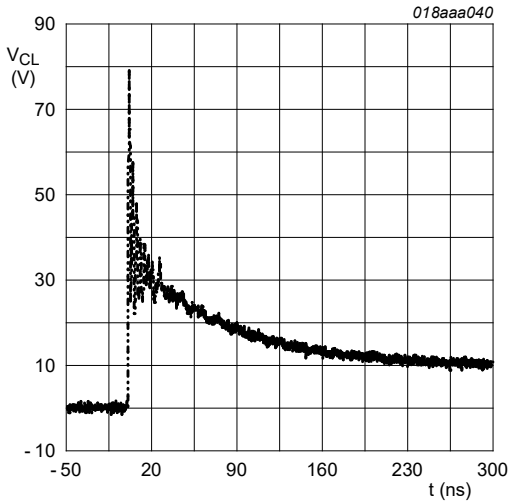
f = 1 MHz; T_{amb} = 25 °C

Fig. 6. Clamped +1 kV ESD pulse waveform (IEC 61000-4-2 network)



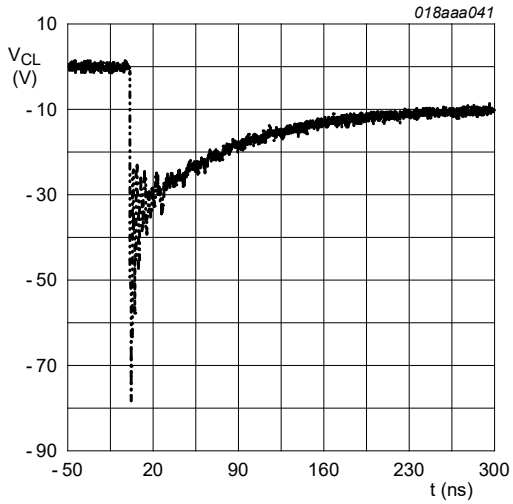
f = 1 MHz; T_{amb} = 25 °C

Fig. 7. Clamped −1 kV ESD pulse waveform (IEC 61000-4-2 network)



f = 1 MHz; T_{amb} = 25 °C

Fig. 8. Clamped +8 kV ESD pulse waveform (IEC 61000-4-2 network)



f = 1 MHz; T_{amb} = 25 °C

Fig. 9. Clamped -8 kV ESD pulse waveform (IEC 61000-4-2 network)

10. Application information

The PESD5V0V1BSF is designed for the protection of one data or signal line from the damage caused by ESD and/or other surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground. It provides protection against surges with up to 8 W per line.

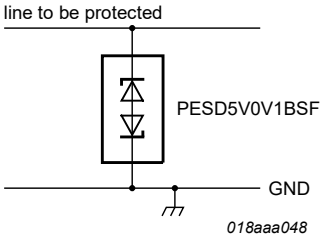


Fig. 10. Application diagram

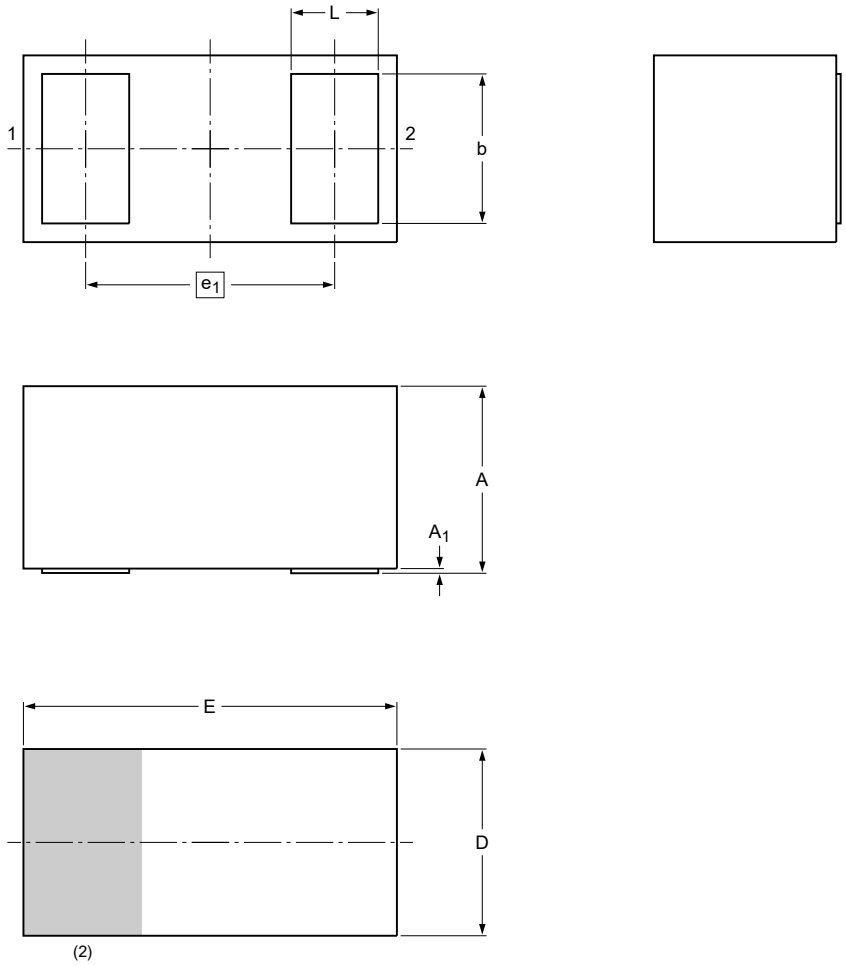
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD and Electrical Fast Transient (EFT). The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible
2. The path length between the device and the protected line should be minimized
3. Avoid running protected conductors in parallel with unprotected conductors
4. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops
5. Minimize the length of the transient return path to ground
6. Avoid using shared transient return paths to a common ground point
7. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm **SOD962**



Dimensions

Unit		A(1)	A1	b	D	E	e1	L
mm	max	0.32	0.0076	0.25	0.325	0.625		0.15
	nom						0.4	
	min	0.28		0.23	0.275	0.575		0.13

Note
1. Dimension A is including coating foil thickness.
2. The marking bar indicates the cathode.

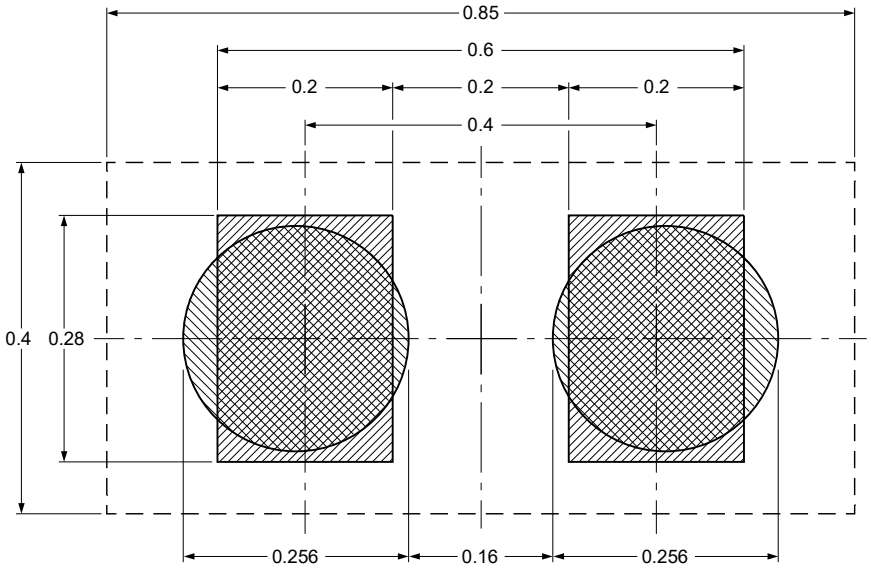
sod962_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD962						~~10-11-03~~ 10-11-11

Fig. 11. Package outline DSN0603-2 (SOD962)

12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962**



recommended stencil thickness: 0.1 mm

occupied area

solder paste

solder lands

Dimensions in mm

Issue date ~~16-01-26~~ 20-09-15

sod962_fr

Fig. 12. Reflow soldering footprint for DSN0603-2 (SOD962)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0V1BSF v.3	20250909	Product data sheet	-	PESD5V0V1BSF v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Chapter "Soldering": Figure updated.			
PESD5V0V1BSF v.2	20110217	Product data sheet	-	PESD5V0V1BSF v.1
PESD5V0V1BSF v.1	20101112	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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