16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74LVC16T245-EP

FEATURES

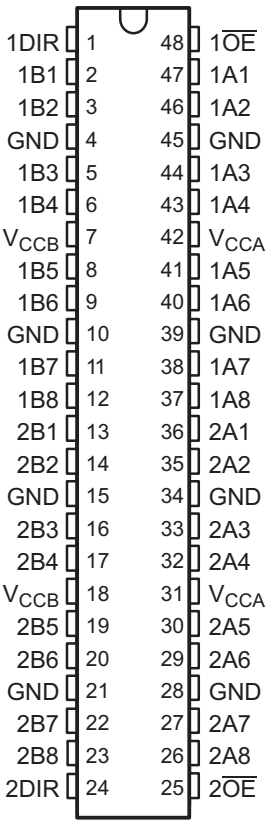
- **Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **Overvoltage-Tolerant Inputs and Outputs Allow Mixed-Voltage-Mode Data Communications**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (-55°C to 125°C) Temperature Ranges** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DGG PACKAGE
(TOP VIEW)



DESCRIPTION

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

DESCRIPTION (CONTINUED)

The SN74LVC16T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74LVC16T245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP-DGG	Reel of 2000	CLVC16T245MDGGREP	LVC16T245M	V62/12667-01XE
		Tube of 40	CLVC16T245MDGGEP		V62/12667-01XE-T

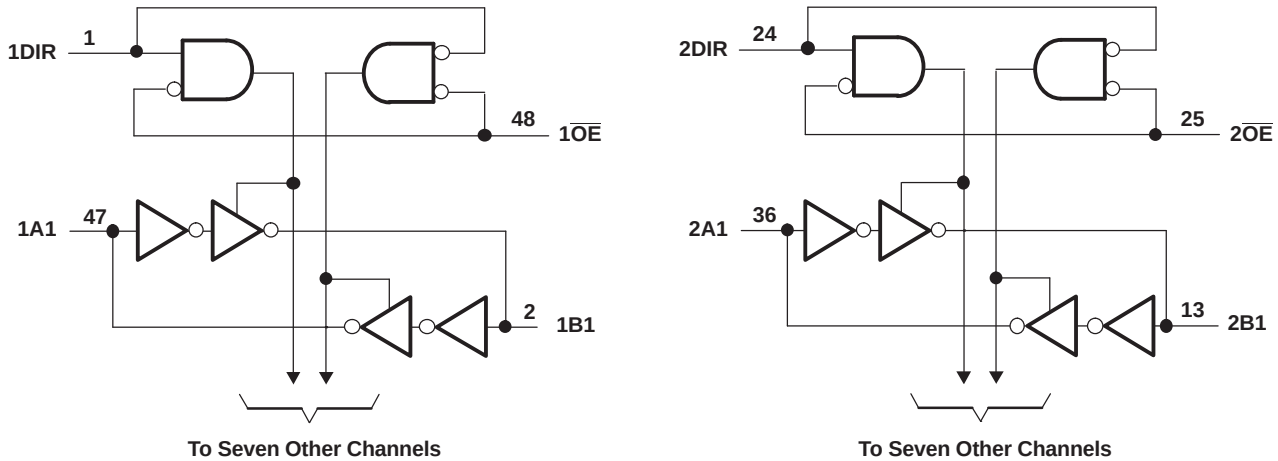
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE(1)
(EACH 8-BIT SECTION)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	6.5	V
		I/O ports (B port)	–0.5	6.5	
		Control inputs	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	6.5	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA}, V_{CCB}, and GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74LVC16T245 DGG 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	59.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	13.9	
θ_{JB}	Junction-to-board thermal resistance(4)	27.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	26.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Recommended Operating Conditions (1)(2)(3)(4)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs (5)	1.65 V to 1.95 V		V_{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs (5)	1.65 V to 1.95 V			V_{CCI} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA}) (6)	1.65 V to 1.95 V		V_{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA}) (6)	1.65 V to 1.95 V			V_{CCA} × 0.35	V
			2.3 V to 2.7 V			0.7	
			3 V to 3.6 V			0.8	
			4.5 V to 5.5 V			V_{CCA} × 0.3	
V_I	Input voltage	Control inputs			0	5.5	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-State			0	5.5	
I_{OH}	High-level output current			1.65 V to 1.95 V		–4	mA
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–24	
				4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current			1.65 V to 1.95 V		4	mA
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		24	
				4.5 V to 5.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V			20	ns/V
			2.3 V to 2.7 V			20	
			3 V to 3.6 V			10	
			4.5 V to 5.5 V			5	
T_A	Operating free-air temperature				–55	125	°C

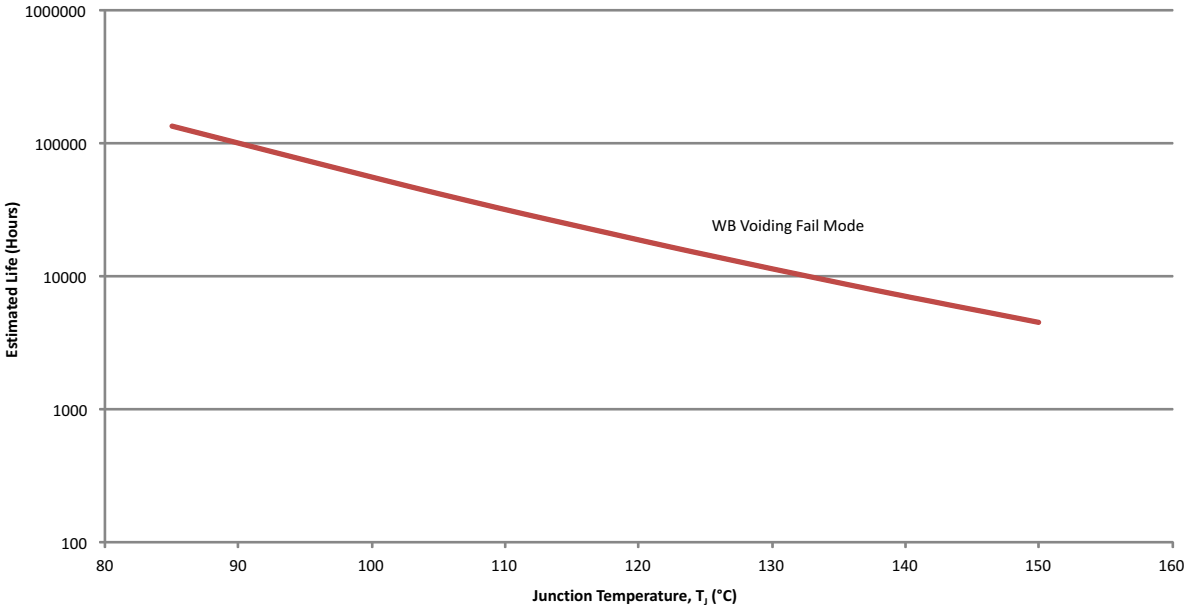
(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) All unused data inputs of the device must be held at V_{CCA} or GND to ensure proper device operation.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics (1)(2)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA, $V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V	V_{CCO} – 0.1			V
		I_{OH} = –4 mA, $V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OH} = –8 mA, $V_I = V_{IH}$	2.3 V	2.3 V	1.9			
		I_{OH} = –24 mA, $V_I = V_{IH}$	3 V	3 V	2.35			
		I_{OH} = –32 mA, $V_I = V_{IH}$	4.5 V	4.5 V	3.75			
V_{OL}		I_{OL} = 100 µA, $V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V			0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OL} = 8 mA, $V_I = V_{IL}$	2.3 V	2.3 V			0.3	
		I_{OL} = 24 mA, $V_I = V_{IL}$	3 V	3 V			0.65	
		I_{OL} = 32 mA, $V_I = V_{IL}$	4.5 V	4.5 V			0.65	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±2	µA
I_{off}	A or B port	V_I or V_O = 0 to 5.5 V	0 V	0 to 5.5 V			±10	µA
			0 to 5.5 V	0 V			±10	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±10	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			20	µA
			5 V	0 V			20	
			0 V	5 V			–2.5	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			20	µA
			5 V	0 V			–2.5	
			0 V	5 V			20	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V			30	µA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6 V, DIR at V_{CCA}, B port = open	3 V to 5.5 V	3 V to 5.5 V			50	µA
	DIR	DIR at V_{CCA} – 0.6 V, B port = open, A port at V_{CCA} or GND					50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V			50	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	3.3 V	3.3 V		4		pF
C_{io}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

Figure 1. SN74LVC16T245-EP Operating Life Derating Chart

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t_{PLH} / t_{PHL}	B	A	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.6	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.8	32	1.6	16	1.2	12.6	0.9	10.8	ns

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B		25.9		13.2		11.4		11.1	ns
t_{PLH} / t_{PHL}	B	A		27.8		27.8		27.4		27.4	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A		33.6		33.4		33.3		33.2	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B		36.2		17.1		16		14.3	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A		28		27.8		27.7		27.7	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B		36		22		16.6		14.8	ns

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B	1.6	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t_{PLH} / t_{PHL}	B	A	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B	1.7	28.2	1.6	12.9	1.2	9.4	1	6.9	ns

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} / t_{PHL}	A	B		25.4		13		10.2		8.8	ns
t_{PLH} / t_{PHL}	B	A		13.3		13.1		12.9		12.8	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	A		13		13		13		13	ns
t_{PHZ} / t_{PLZ}	$\overline{OE}$	B		33.6		14		14.3		10.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	A		14.9		14.9		14.9		14.9	ns
t_{PZH} / t_{PZL}	$\overline{OE}$	B		32.2		16.9		13.4		10.9	ns

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.5	21.2	1.1	8.8	0.8	6.1	0.5	4.4	ns
t_{PHL}											
t_{PLH}	B	A	0.9	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	1.6	8.2	1.6	8.2	1.6	6.2	1.6	8.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.8	7.8	0.8	7.8	0.8	7.8	0.8	7.8	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.6	27.7	1.4	12.4	1.1	8.5	0.9	8.4	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.2		12.8		10.2		8.4	ns
t_{PHL}											
t_{PLH}	B	A		11.2		10.2		10.1		10	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		12.2		12.2		12.2		12.2	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		33		14.3		12.8		10.3	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		11.8		12.1		12.1		12.1	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		31.7		16.4		12.9		10.4	ns
t_{PZL}											

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.6	21.4	1	8.8	0.7	6	0.4	4.2	ns
t_{PHL}											
t_{PLH}	B	A	0.7	6.8	0.4	4.8	0.3	4.5	0.3	4.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A	0.3	5.4	0.3	5.4	0.3	5.4	0.3	6.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A	0.7	5.5	0.7	5.5	0.7	5.5	0.7	5.5	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B	1.6	27.6	1.3	11.4	1	8.1	0.9	6	ns
t_{PZL}											

Switching Characteristics

T_A = −55°C to 125°C, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B		25.4		14.3		10		8.2	ns
t_{PHL}											
t_{PLH}	B	A		11		8.8		8.5		8.3	ns
t_{PHL}											
t_{PHZ}	$\overline{OE}$	A		9.4		9.4		9.4		9.4	ns
t_{PLZ}											
t_{PHZ}	$\overline{OE}$	B		32.7		13.7		12		9.7	ns
t_{PLZ}											
t_{PZH}	$\overline{OE}$	A		10.4		10.4		10.4		10.4	ns
t_{PZL}											
t_{PZH}	$\overline{OE}$	B		31.6		19.3		12.6		10	ns
t_{PZL}											

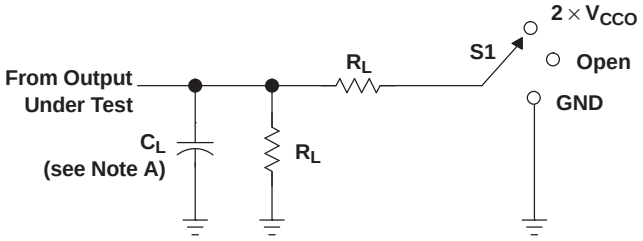
Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	V_{CCA} = V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	2	2	2	3	pF
	B-port input, A-port output		18	19	19	22	
C_{pdB} (1)	A-port input, B-port output		18	19	20	22	
	B-port input, A-port output		2	2	2	2	

(1) Power dissipation capacitance per transceiver

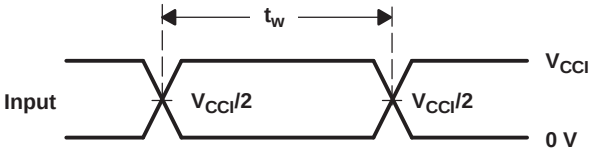
PARAMETER MEASUREMENT INFORMATION



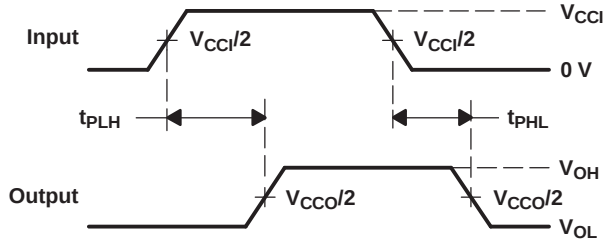
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

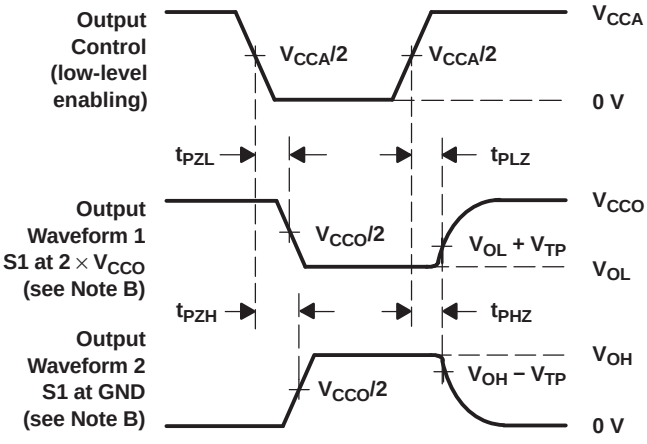
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC16T245MDGGEP	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
CLVC16T245MDGGREP	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
V62/12667-01XE	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
V62/12667-01XE-T	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC16T245-EP :

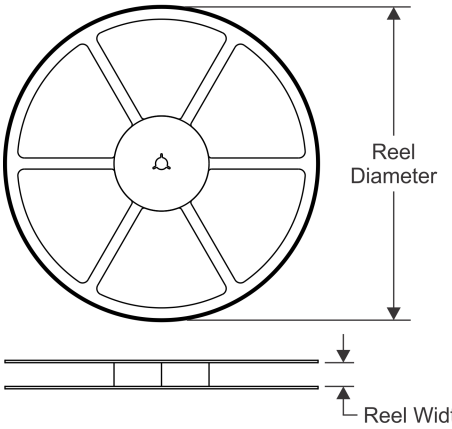
- Catalog: SN74LVC16T245

NOTE: Qualified Version Definitions:

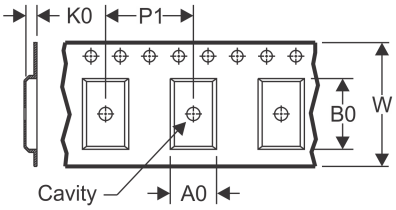
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

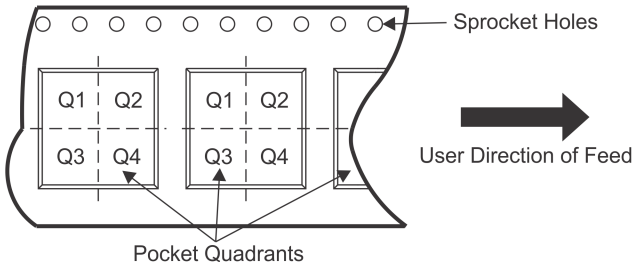


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

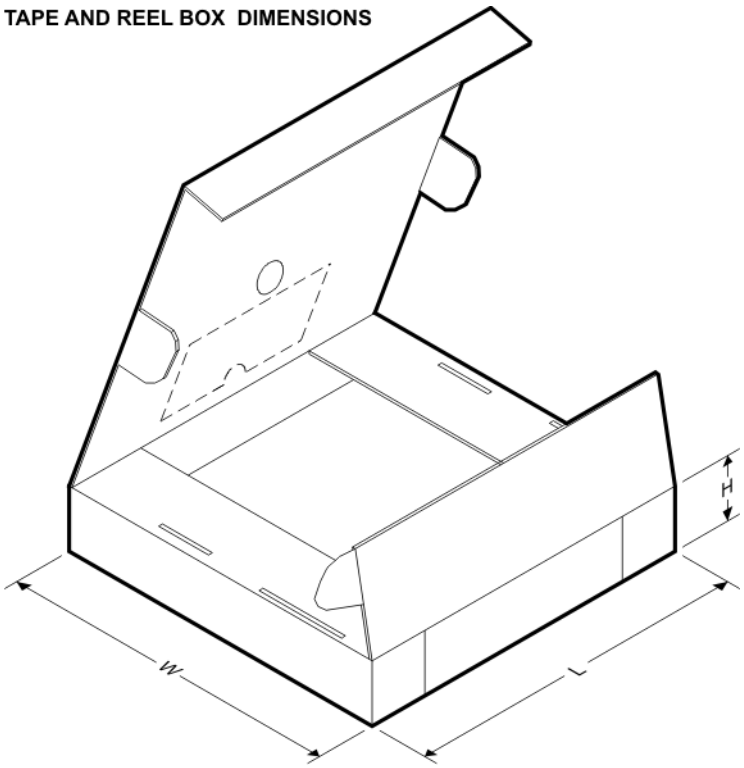
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

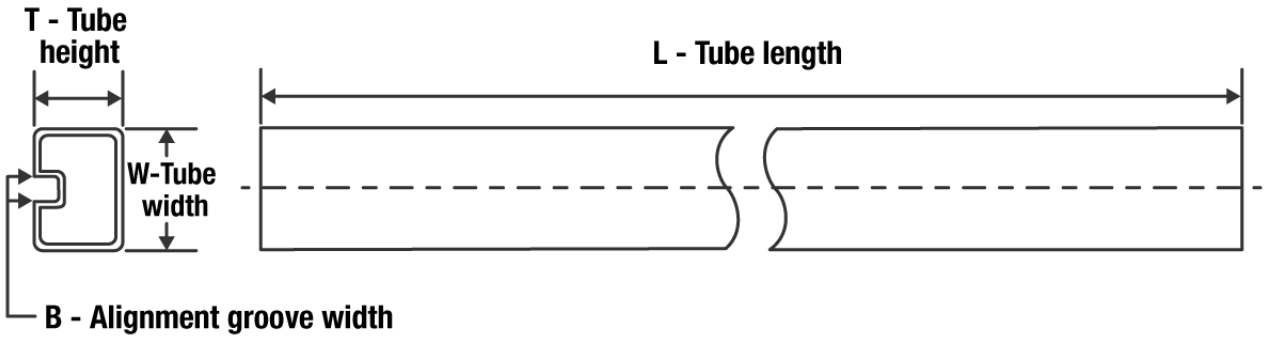
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

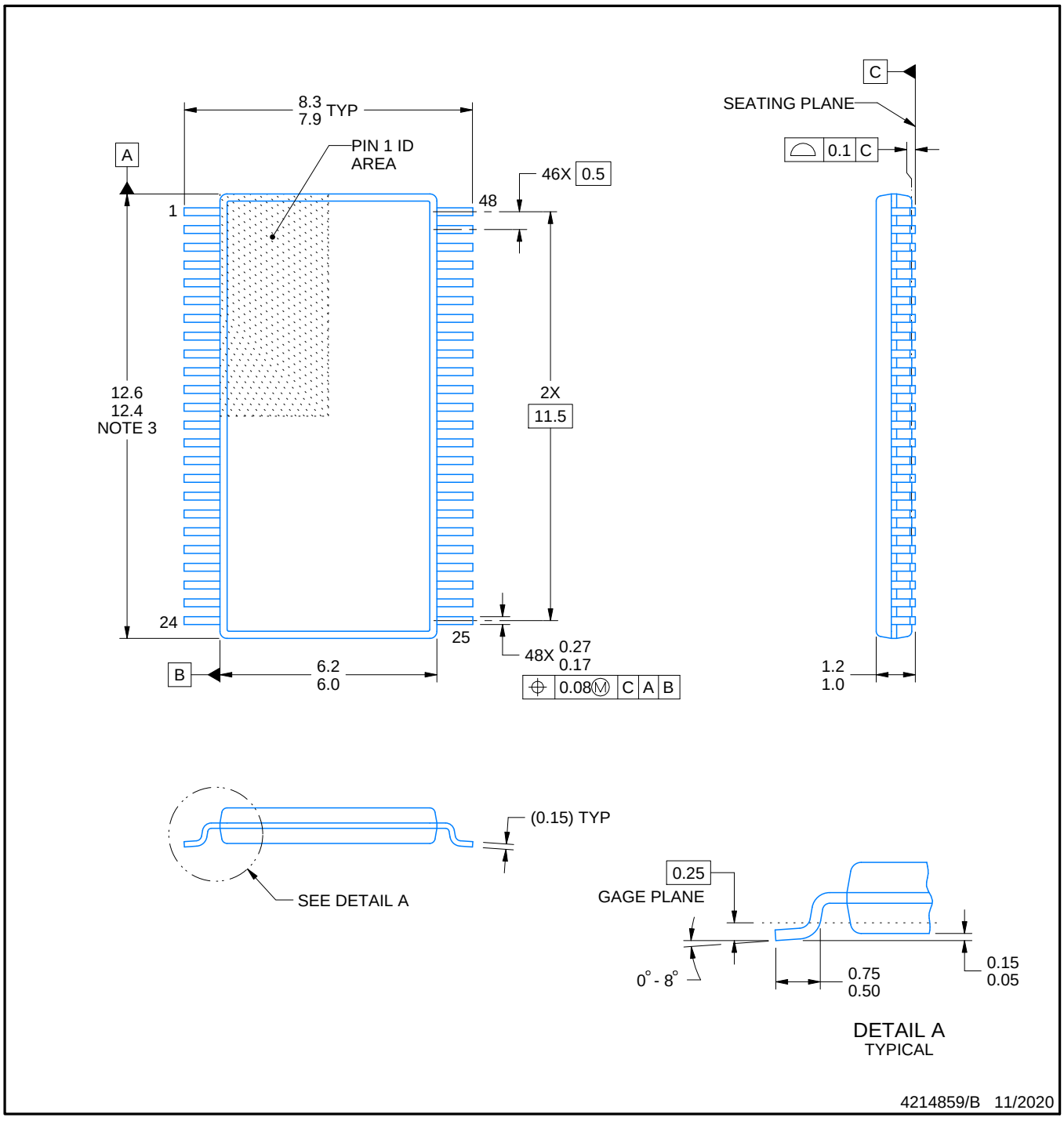
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CLVC16T245MDGGEP	DGG	TSSOP	48	40	530	11.89	3600	4.9
V62/12667-01XE-T	DGG	TSSOP	48	40	530	11.89	3600	4.9

PACKAGE OUTLINE

DGG0048A

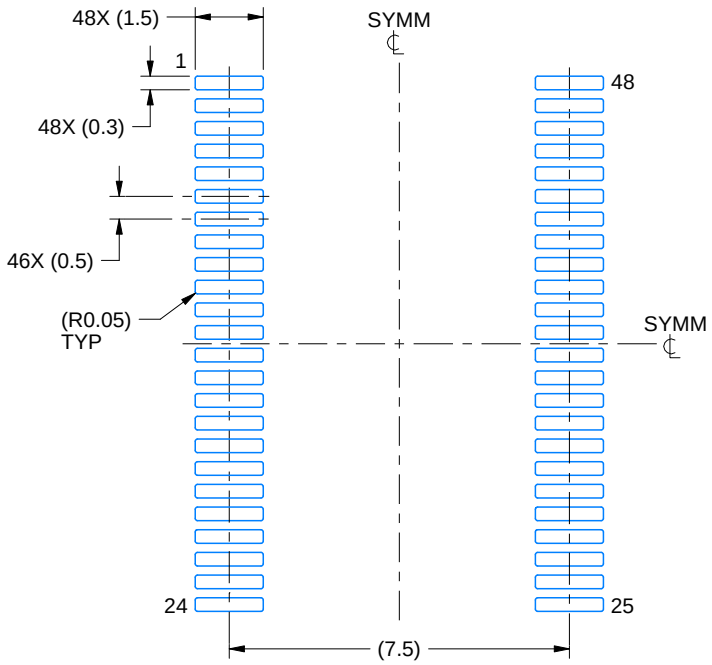
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

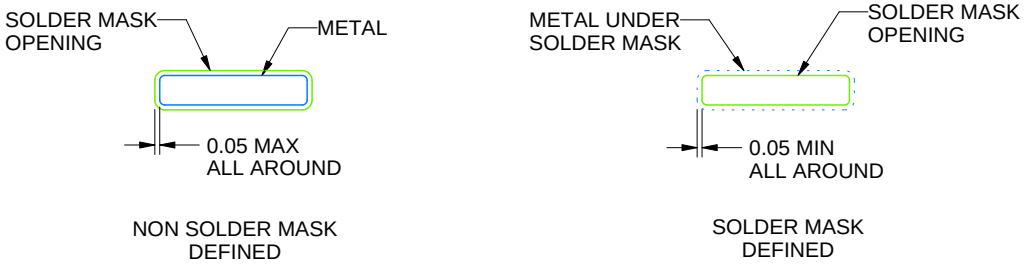


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

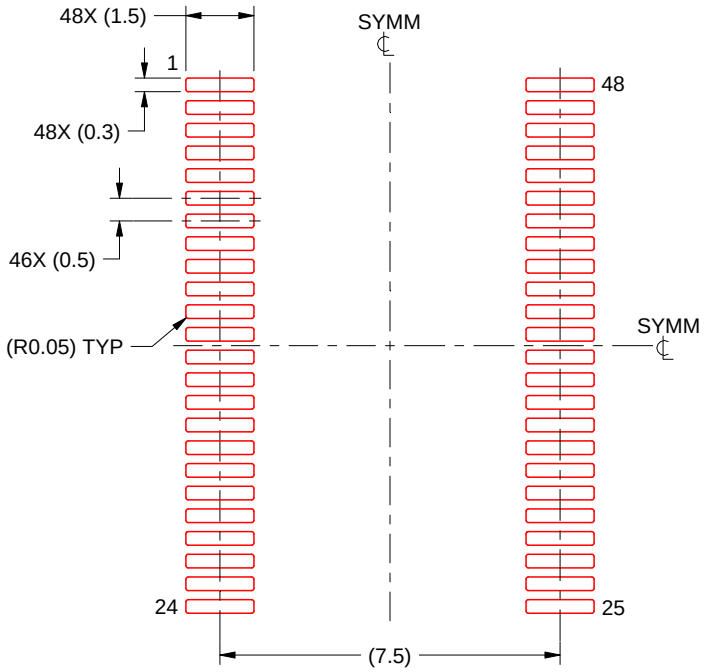


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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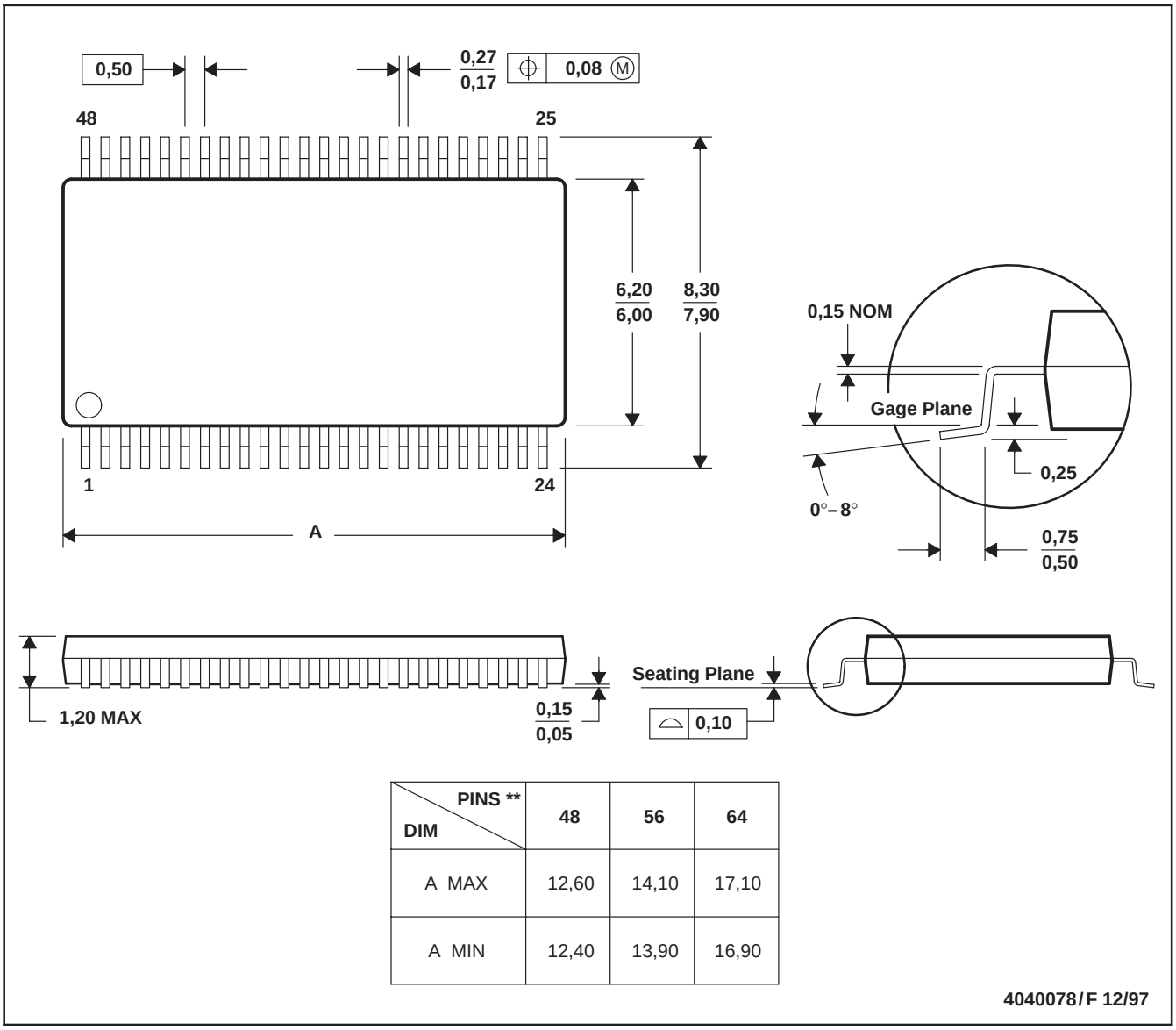
DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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