

# LC450029PKB

## 1/4 and 1/3-Duty General-Purpose LCD Driver



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

### Overview

The LC450029PKB is 1/4 duty and 1/3 duty general-purpose microcontroller-controlled LCD drivers that can be used in applications such as frequency display in products with electronic tuning. In addition to being capable to drive up to 208 segments directly. The internal oscillation circuit helps to reduce the number of external resistors and capacitors required. The chip shape is slim for COG (Chip-On-Glass) implementation. The operating temperature range is from  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$

### Application

- Car or general consumer electronic LCD display equipment.

### Features

- Selectable 1/4-duty or 1/3-duty drive by the serial control data
  - When 1/4-duty: Capable of driving up to 208 segments
  - When 1/3-duty: Capable of driving up to 159 segments
- 1/3-bias only
- Serial data input supports CCB\* format communication with the system controller. (For 5 V operation only)
- The power-saving mode is selectable by the serial control data, and supports low power consumption.
- Adjustable the frame frequency of the common and segment output waveforms by the serial control data
- Selectable the internal oscillator operating or external clock operating mode by the serial control data
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- The  $\overline{\text{INH}}$  pad allows all LCD segments to be forced to the off state.
- With a built-in oscillator circuit  
(External resistors and capacitors are unnecessary.)
- The stability of the LCD bias voltage is high by a built-in LCD bias generator with voltage-follower buffers.
- Shipping form: Chip with Au bumps in tray.
- Allowable operating voltage ( $V_{\text{DD}}$ ,  $V_{\text{DDI}}$ ) :  $+4.5\text{ V}$  to  $+6.0\text{ V}$
- Allowable wide operating temperature ranges :  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$

\* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

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## Specifications

**Absolute Maximum Ratings** at  $T_a = 25^{\circ}\text{C}$ ,  $V_{SS} = 0\text{ V}$

| Parameter              | Symbol                         | Conditions                   | Ratings               | Unit               |
|------------------------|--------------------------------|------------------------------|-----------------------|--------------------|
| Maximum supply voltage | $V_{DD}$ max,<br>$V_{DDI}$ max | $V_{DD}=V_{DDI}$             | -0.3 to +6.5          | V                  |
| Input voltage          | $V_{IN1}$                      | CE, CL, DI, $\overline{INH}$ | -0.3 to +6.5          | V                  |
|                        | $V_{IN2}$                      | OSCI                         | -0.3 to $V_{DDI}+0.3$ |                    |
| Output voltage         | $V_{OUT}$                      | S1 to S53, COM1 to COM4      | -0.3 to $V_{DD}+0.3$  | V                  |
| Output current         | $I_{OUT1}$                     | S1 to S53                    | 300                   | $\mu\text{A}$      |
|                        | $I_{OUT2}$                     | COM1 to COM4                 | 3                     | mA                 |
| Operating temperature  | $T_{opr}$                      |                              | -40 to +105           | $^{\circ}\text{C}$ |
| Storage temperature    | $T_{stg}$                      |                              | -55 to +125           | $^{\circ}\text{C}$ |

(Note) Power supply pads ( $V_{DD}$ ,  $V_{DDI}$ ) should connect all pads to the same power supply.

(See sample applications circuits)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Allowable Operating Ranges** at  $T_a = -40$  to  $+105^{\circ}\text{C}$ ,  $V_{SS} = 0\text{ V}$

| Parameter                          | Symbol                  | Conditions                                        | Ratings     |     |              | Unit          |
|------------------------------------|-------------------------|---------------------------------------------------|-------------|-----|--------------|---------------|
|                                    |                         |                                                   | min         | typ | max          |               |
| Supply voltage                     | $V_{DD}$ ,<br>$V_{DDI}$ | $V_{DD}=V_{DDI}$                                  | 4.5         |     | 6.0          | V             |
| Input high-level voltage           | $V_{IH1}$               | CE, CL, DI, $\overline{INH}$                      | $0.8V_{DD}$ |     | 6.0          | V             |
|                                    | $V_{IH2}$               | OSCI: External clock operating mode               | $0.8V_{DD}$ |     | $V_{DDI}$    |               |
| Input low-level voltage            | $V_{IL1}$               | CE, CL, DI, $\overline{INH}$                      | 0           |     | $0.2V_{DDI}$ | V             |
|                                    | $V_{IL2}$               | OSCI: External clock operating mode               | 0           |     | $0.2V_{DDI}$ |               |
| External clock operating frequency | $f_{CK}$                | OSCI: External clock operating mode<br>[Figure 4] | 10          | 300 | 600          | kHz           |
| External clock duty cycle          | $D_{CK}$                | OSCI: External clock operating mode<br>[Figure 4] | 30          | 50  | 70           | %             |
| Data setup time                    | $t_{ds}$                | CL, DI [Figure 2] [Figure 3]                      | 160         |     |              | ns            |
| Data hold time                     | $t_{dh}$                | CL, DI [Figure 2] [Figure 3]                      | 160         |     |              | ns            |
| CE wait time                       | $t_{cp}$                | CE, CL [Figure 2] [Figure 3]                      | 160         |     |              | ns            |
| CE setup time                      | $t_{cs}$                | CE, CL [Figure 2] [Figure 3]                      | 160         |     |              | ns            |
| CE hold time                       | $t_{ch}$                | CE, CL [Figure 2] [Figure 3]                      | 160         |     |              | ns            |
| High-level clock pulse width       | $t_{\phi H}$            | CL [Figure 2] [Figure 3]                          | 160         |     |              | ns            |
| Low-level clock pulse width        | $t_{\phi L}$            | CL [Figure 2] [Figure 3]                          | 160         |     |              | ns            |
| Rise time                          | $t_r$                   | CE, CL, DI [Figure 2] [Figure 3]                  |             | 160 |              | ns            |
| Fall time                          | $t_f$                   | CE, CL, DI [Figure 2] [Figure 3]                  |             | 160 |              | ns            |
| $\overline{INH}$ switching time    | $t_c$                   | $\overline{INH}$ , CE [Figure 5] [Figure 6]       | 10          |     |              | $\mu\text{s}$ |

(Note) Power supply pads ( $V_{DD}$ ,  $V_{DDI}$ ) should connect all pads to the same power supply.

(See sample applications circuits)

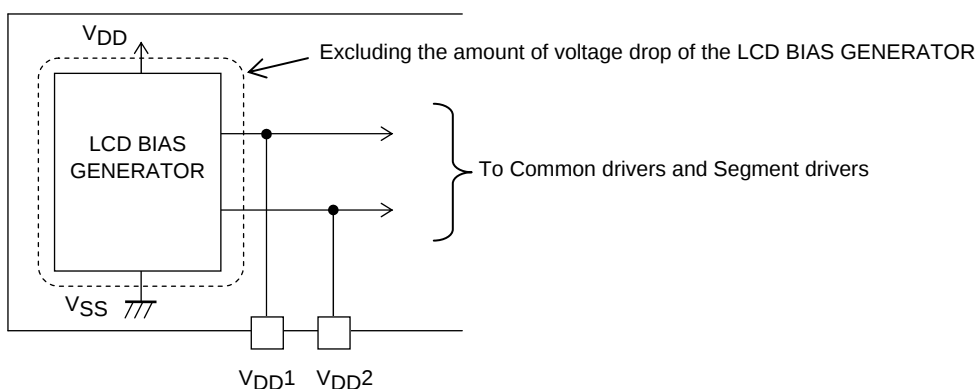
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## Electrical Characteristics for the Allowable Operating Ranges

| Parameter                                                            | Symbol            | Pin                                 | Conditions                                                                                                                             | Ratings                    |                     |                            | Unit          |
|----------------------------------------------------------------------|-------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|----------------------------|---------------------|----------------------------|---------------|
|                                                                      |                   |                                     |                                                                                                                                        | min                        | typ                 | max                        |               |
| Hysteresis                                                           | V <sub>H1</sub>   | CE, CL, DI, $\overline{\text{INH}}$ |                                                                                                                                        |                            | 0.1V <sub>DDI</sub> |                            | V             |
|                                                                      | V <sub>H2</sub>   | OSCI                                | External clock operating mode                                                                                                          |                            | 0.1V <sub>DDI</sub> |                            |               |
| Input high-level current                                             | I <sub>IH1</sub>  | CE, CL, DI, $\overline{\text{INH}}$ | V <sub>I</sub> = 6.0 V                                                                                                                 |                            |                     | 5.0                        | $\mu\text{A}$ |
|                                                                      | I <sub>IH2</sub>  | OSCI                                | V <sub>I</sub> = V <sub>DDI</sub> , External clock operating mode                                                                      |                            |                     | 5.0                        |               |
| Input low-level current                                              | I <sub>IL1</sub>  | CE, CL, DI, $\overline{\text{INH}}$ | V <sub>I</sub> = 0 V                                                                                                                   | -5.0                       |                     |                            | $\mu\text{A}$ |
|                                                                      | I <sub>IL2</sub>  | OSCI                                | V <sub>I</sub> = 0 V, External clock operating mode                                                                                    | -5.0                       |                     |                            |               |
| Output high-level voltage                                            | V <sub>OH1</sub>  | S1 to S53                           | I <sub>O</sub> = -20 $\mu\text{A}$                                                                                                     | V <sub>DD</sub><br>-0.9    |                     |                            | V             |
|                                                                      | V <sub>OH2</sub>  | COM1 to COM4                        | I <sub>O</sub> = -100 $\mu\text{A}$                                                                                                    | V <sub>DD</sub><br>-0.9    |                     |                            |               |
| Output low-level voltage                                             | V <sub>OL1</sub>  | S1 to S53                           | I <sub>O</sub> = 20 $\mu\text{A}$                                                                                                      |                            |                     | 0.9                        | V             |
|                                                                      | V <sub>OL2</sub>  | COM1 to COM4                        | I <sub>O</sub> = 100 $\mu\text{A}$                                                                                                     |                            |                     | 0.9                        |               |
| Output middle-level voltage *1                                       | V <sub>MID1</sub> | S1 to S53                           | I <sub>O</sub> = $\pm 20 \mu\text{A}$                                                                                                  | 2/3V <sub>DD</sub><br>-0.9 |                     | 2/3V <sub>DD</sub><br>+0.9 | V             |
|                                                                      | V <sub>MID2</sub> | S1 to S53                           | I <sub>O</sub> = $\pm 20 \mu\text{A}$                                                                                                  | 1/3V <sub>DD</sub><br>-0.9 |                     | 1/3V <sub>DD</sub><br>+0.9 |               |
|                                                                      | V <sub>MID3</sub> | COM1 to COM4                        | I <sub>O</sub> = $\pm 100 \mu\text{A}$                                                                                                 | 2/3V <sub>DD</sub><br>-0.9 |                     | 2/3V <sub>DD</sub><br>+0.9 |               |
|                                                                      | V <sub>MID4</sub> | COM1 to COM4                        | I <sub>O</sub> = $\pm 100 \mu\text{A}$                                                                                                 | 1/3V <sub>DD</sub><br>-0.9 |                     | 1/3V <sub>DD</sub><br>+0.9 |               |
| Oscillator frequency                                                 | f <sub>osc</sub>  | Internal oscillator circuit         | Internal oscillator operating mode                                                                                                     | 210                        | 300                 | 390                        | kHz           |
| Current drain (Total value of V <sub>DD</sub> and V <sub>DDI</sub> ) | I <sub>DD1</sub>  | V <sub>DD</sub> , V <sub>DDI</sub>  | <Power-saving mode><br>V <sub>DD</sub> = V <sub>DDI</sub> = 6.0 V                                                                      |                            | 40                  | 100                        | $\mu\text{A}$ |
|                                                                      | I <sub>DD2</sub>  | V <sub>DD</sub> , V <sub>DDI</sub>  | <Internal oscillator operating mode><br>V <sub>DD</sub> = V <sub>DDI</sub> = 6.0 V<br>Driver outputs are open.                         |                            | 200                 | 400                        |               |
|                                                                      | I <sub>DD3</sub>  | V <sub>DD</sub> , V <sub>DDI</sub>  | <External clock operating mode><br>V <sub>DD</sub> = V <sub>DDI</sub> = 6.0 V<br>f <sub>CK</sub> = 300 kHz<br>Driver outputs are open. |                            | 170                 | 340                        |               |

\*1: Excluding the amount of voltage drop of the LCD BIAS GENERATOR which generates V<sub>DD1</sub> and V<sub>DD2</sub>.  
(See Figure 1.)

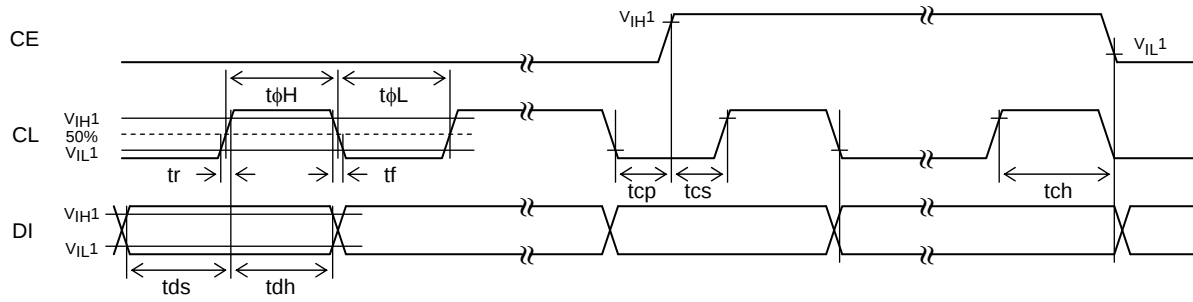


[Figure 1]

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

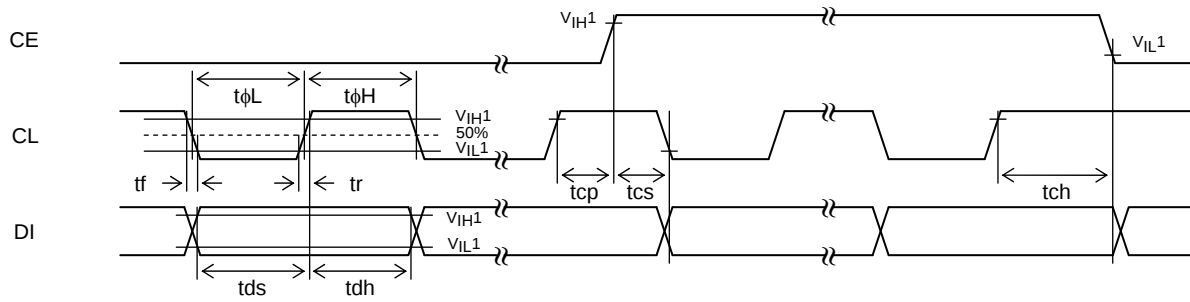
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(1) When CL is stopped at the low level



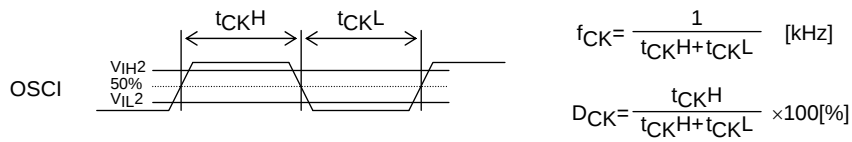
[Figure 2]

(2) When CL is stopped at the high level



[Figure 3]

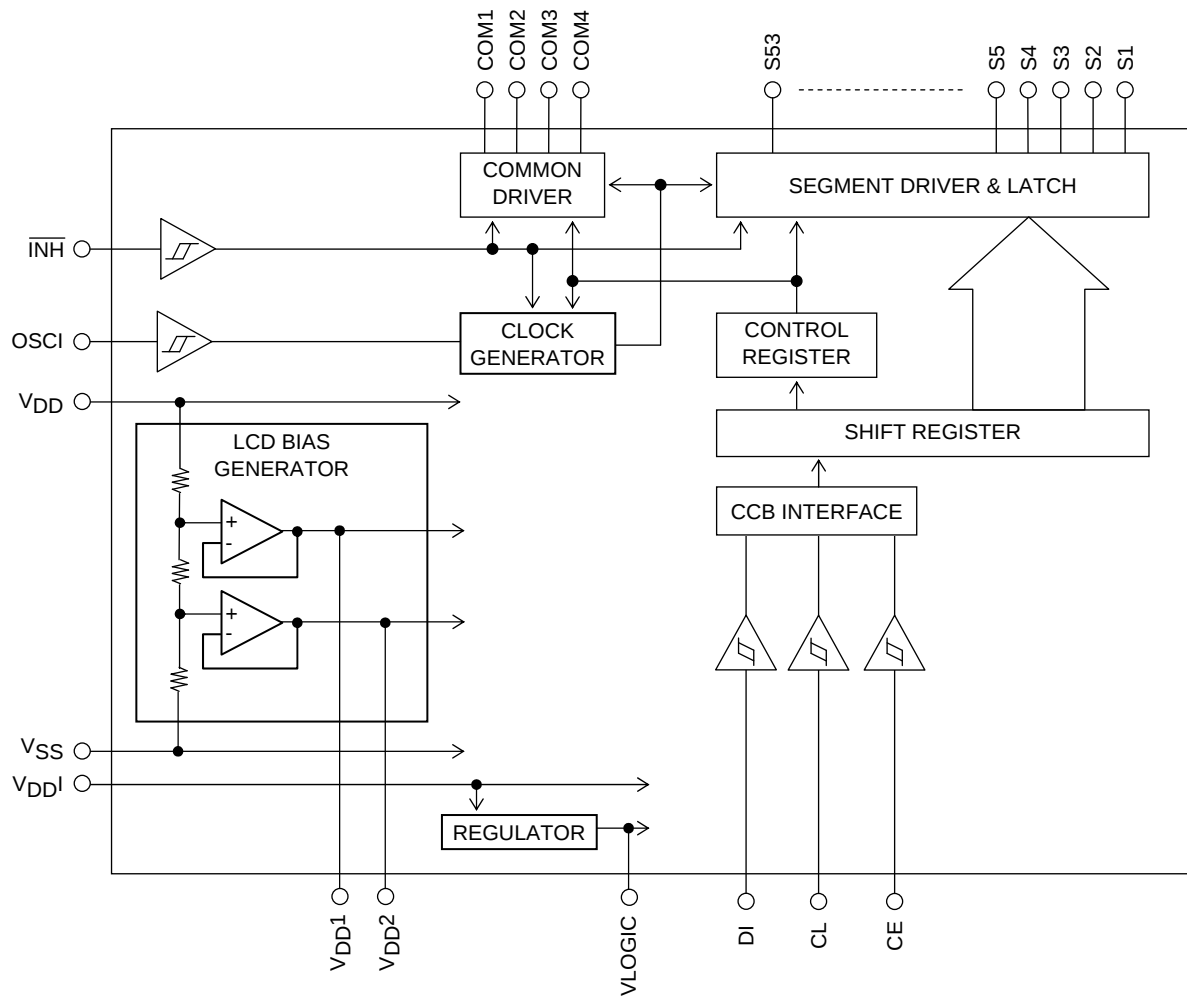
(3) OSCI pad clock timing in external clock operating mode



[Figure 4]

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## Block Diagram



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## Pad Functions

| Symbol           | Pad No.        | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Active                                                                                          | I/O         | Handling when unused |
|------------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|-------------|----------------------|
| COM1 to COM4     | 2 to 5         | Common driver outputs.<br>The frame frequency is $f_0$ [Hz].<br>COM4 pad outputs the $V_{SS}$ level in 1/3-duty.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | -                                                                                               | O           | OPEN                 |
| S1 to S53        | 6 to 58        | Segment outputs for displaying the display data transferred by serial data input.<br>S51 pad outputs the $V_{SS}$ level in 1/4-duty.<br>S52 pad and S53 pad output the $V_{SS}$ level at the control data DN="0".<br>S53 pad outputs the $V_{SS}$ level at external clock operating mode.                                                                                                                                                                                                                                                                                                                                                                                                             | -                                                                                               | O           | OPEN                 |
| $\overline{INH}$ | 61             | Display off control input<br>• $\overline{INH}$ = low ( $V_{SS}$ ) ...Display forced off ( $V_{SS}$ level Output)<br>S1 to S53 = low ( $V_{SS}$ )<br>COM1 to COM4 = low ( $V_{SS}$ )<br>The internal oscillator stops.<br>Stops inputting external clock.<br>Serial data transfer can be used.<br>• $\overline{INH}$ = high ( $V_{DD}$ )...Display on<br>Enables the internal oscillator circuit.<br>(Internal oscillator operating mode)<br>Enables external clock input.<br>(External clock operating mode)<br>While display on, LCD outputs force off ( $V_{SS}$ level output) by the control data BU="1".<br>While display on, LCD outputs off (off waveforms output) by the control data SC="1". | L                                                                                               | I           | GND ( $V_{SS}$ )     |
| CE<br>DI<br>CL   | 62<br>63<br>64 | Serial data transfer inputs. Must be connected to the controller.<br>CE: Chip enable<br>DI: Transfer data<br>CL: Synchronization clock                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | H<br>-<br> | I<br>I<br>I | GND ( $V_{SS}$ )     |
| VLOGIC           | 65             | Used to monitor pad for the power supply voltage of the logic circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -                                                                                               | O           | OPEN                 |
| $V_{DDI}$        | 66 to 71       | Power supply pad. A power voltage of 4.5 to 6.0V must be applied to these pads.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -                                                                                               | -           | -                    |
| OSCI             | 72             | This pad can also be used as the external clock input pad when the external clock operating mode is selected by control data.<br>This pad must be connected to GND at internal oscillator operating mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | -                                                                                               | I           | GND ( $V_{SS}$ )     |
| $V_{SS}$         | 73 to 90       | Ground pad. Must be connected to ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | -                                                                                               | -           | -                    |
| $V_{DD2}$        | 91             | Used to monitor pad for the LCD drive bias voltage (1/3 $V_{DD}$ ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | -                                                                                               | O           | OPEN                 |
| $V_{DD1}$        | 92             | Used to monitor pad for the LCD drive bias voltage (2/3 $V_{DD}$ ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | -                                                                                               | O           | OPEN                 |
| $V_{DD}$         | 93 to 105      | Power supply pad. A power voltage of 4.5 to 6.0V must be applied to these pads.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -                                                                                               | -           | -                    |
| DUMMY            | 1, 59, 60, 106 | Dummy pad. Must not be used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | -                                                                                               | OPEN        | OPEN                 |

(Note)

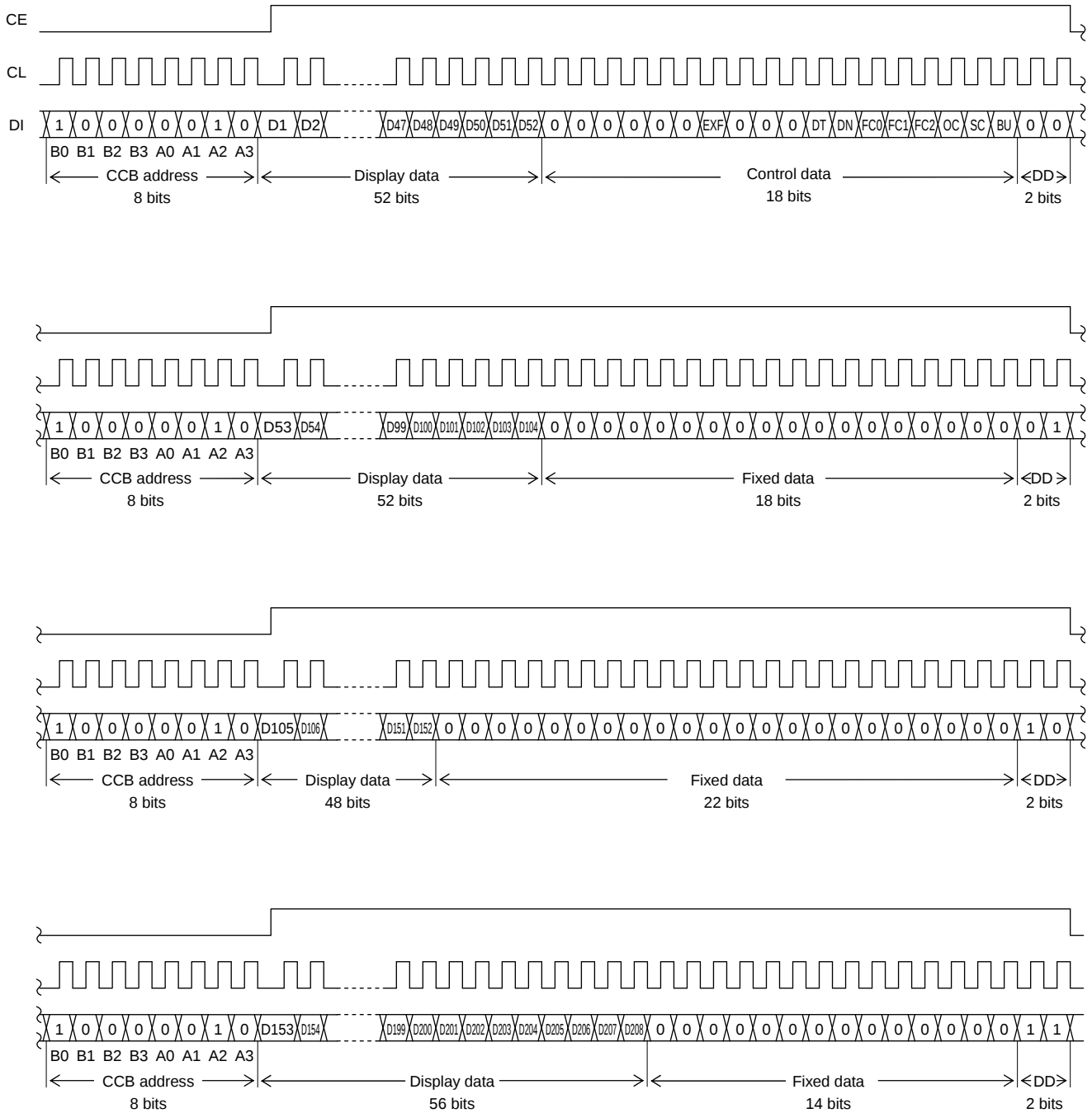
- Power supply pads ( $V_{DD}$ ,  $V_{DDI}$ ) should connect all pads to the same power supply.  
(See sample applications circuits)
- GND pad ( $V_{SS}$ ) should connect all pads to the GND.
- When logic input pads ( $\overline{INH}$ , CE, DI, CL, OSCI) are not used, must be fixed to GND ( $V_{SS}$ ).
- Must not use monitor pads ( $V_{LOGIC}$ ,  $V_{DD1}$ ,  $V_{DD2}$ ) in an external circuit.
- Must not connect dummy pad (DUMMY) mutually. Moreover, never use it in an external circuit.

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## Serial Data Input

### 1. 1/4 duty

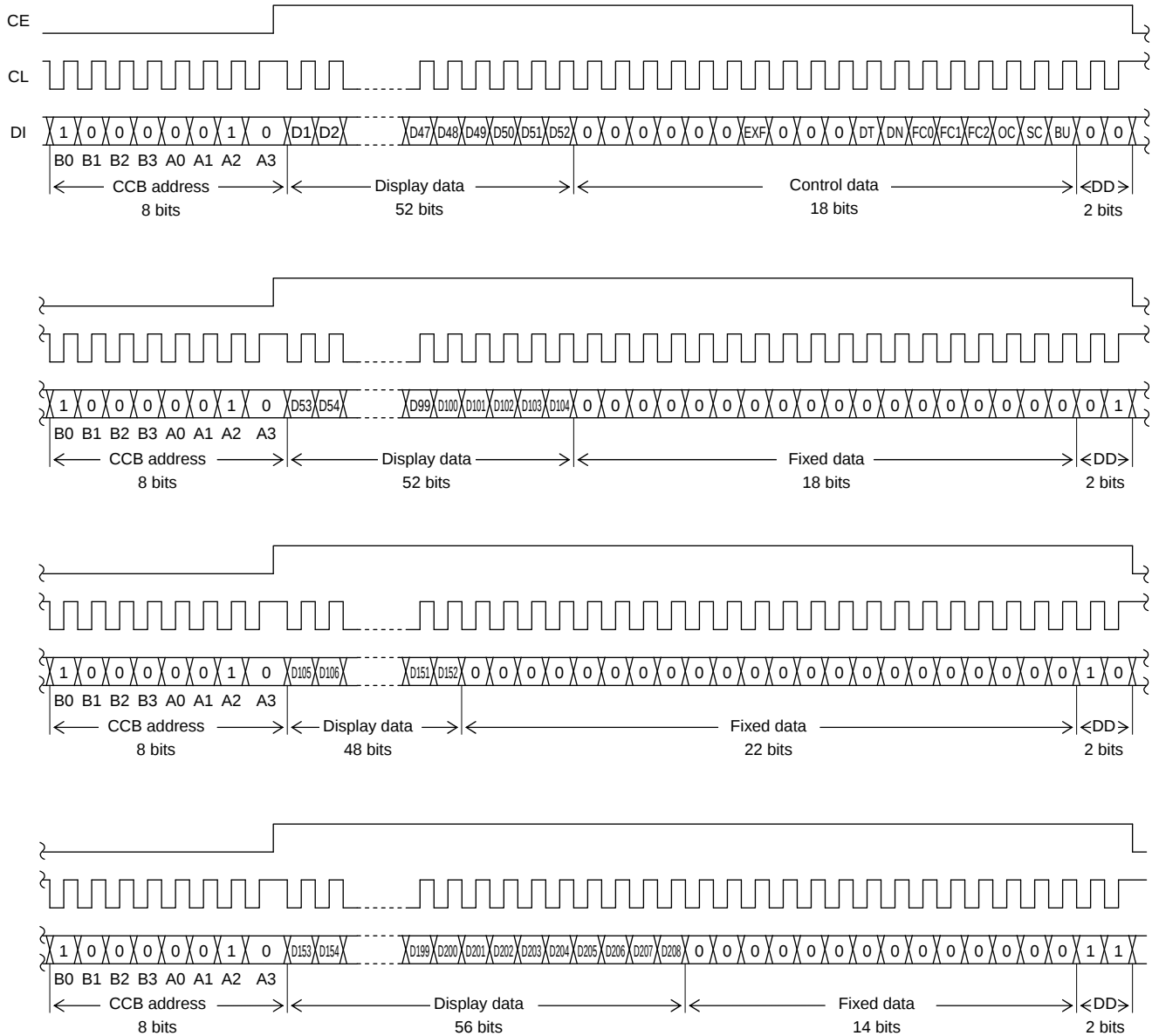
(1) When CL is stopped at the low level



Note: DD is the direction data.

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(2) When CL is stopped at the high level



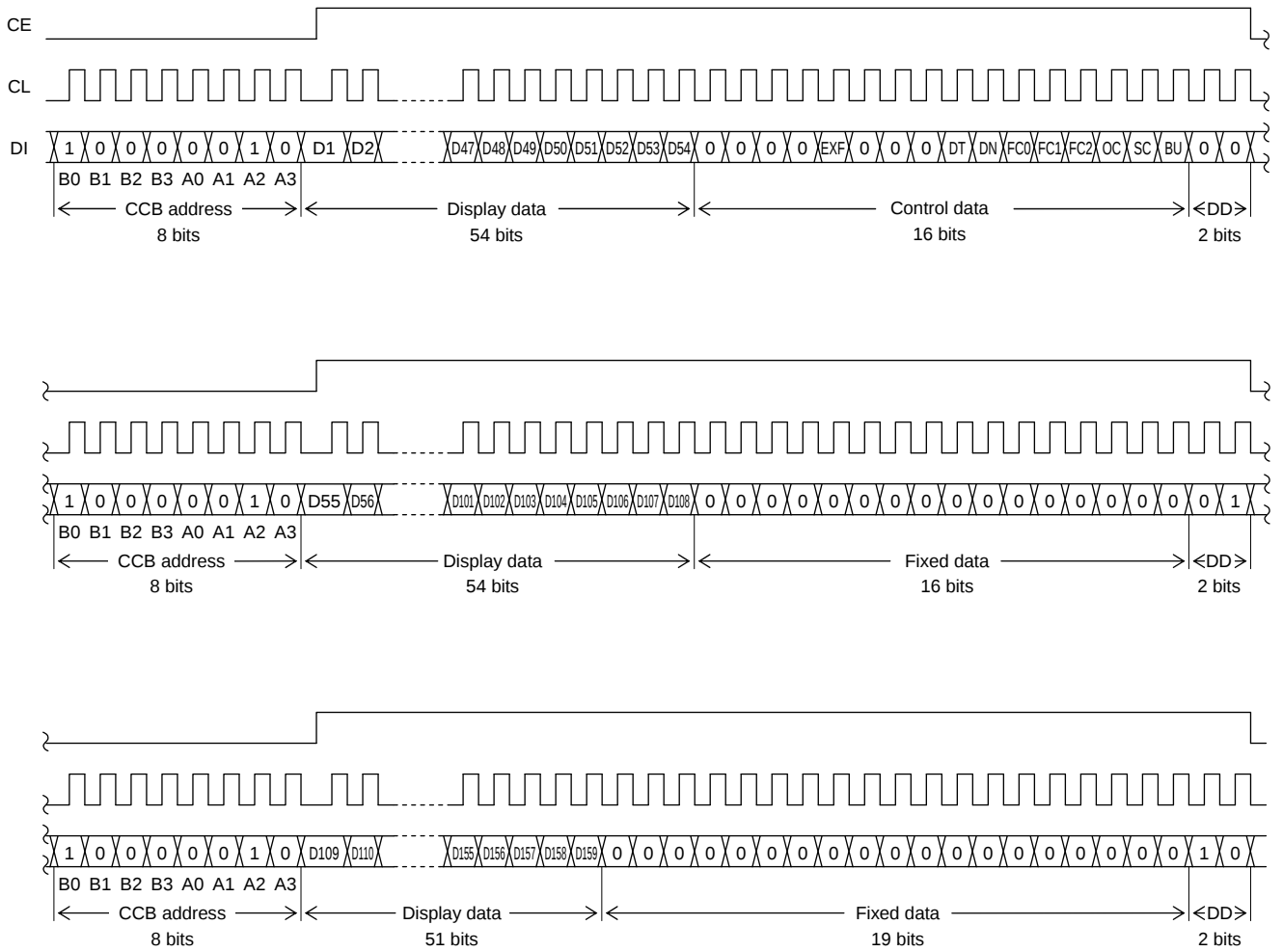
Note: DD is the direction data.

- CCB address ..... “41H”
- D1 to D208 ..... Display data
- EXF ..... Ratio of dividing frequency in external clock operating mode setting control data
- DT ..... 1/4-duty drive or 1/3-duty drive switching control data
- DN ..... The number of the maximum display segments setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off (off waveform output) control data
- BU ..... Normal mode/power-saving mode control data

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## 2. 1/3 duty

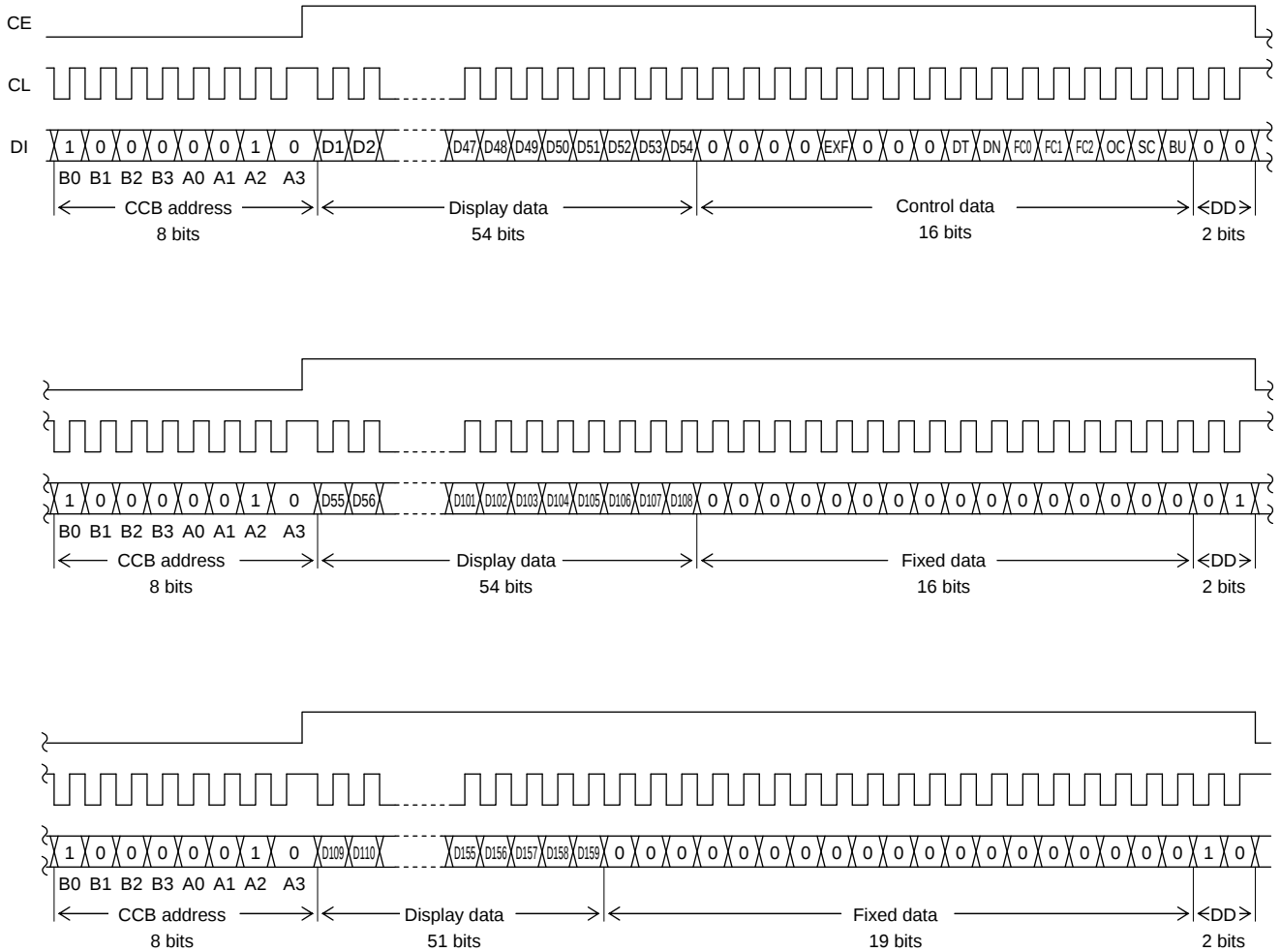
### (1) When CL is stopped at the low level



Note: DD is the direction data.

## LC450029PKB

(2) When CL is stopped at the high level



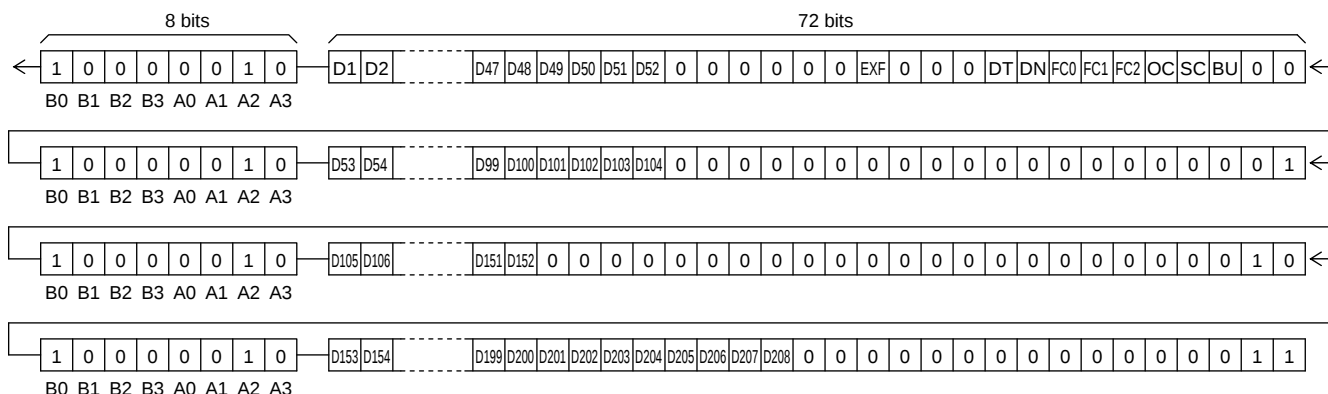
Note: DD is the direction data.

- CCB address ..... “41H”
- D1 to D208 ..... Display data
- EXF ..... Ratio of dividing frequency in external clock operating mode setting control data
- DT ..... 1/4-duty drive or 1/3-duty drive switching control data
- DN ..... The number of the maximum display segments setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off (off waveform output) control data
- BU ..... Normal mode/power-saving mode control data

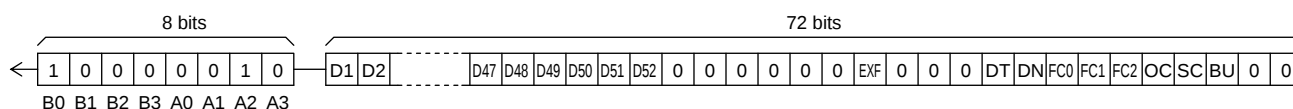
## Serial Data Transfer Example

### 1. 1/4 duty

- When 153 or more segments are used  
All 320 bits (include CCB address) of serial data must be sent.

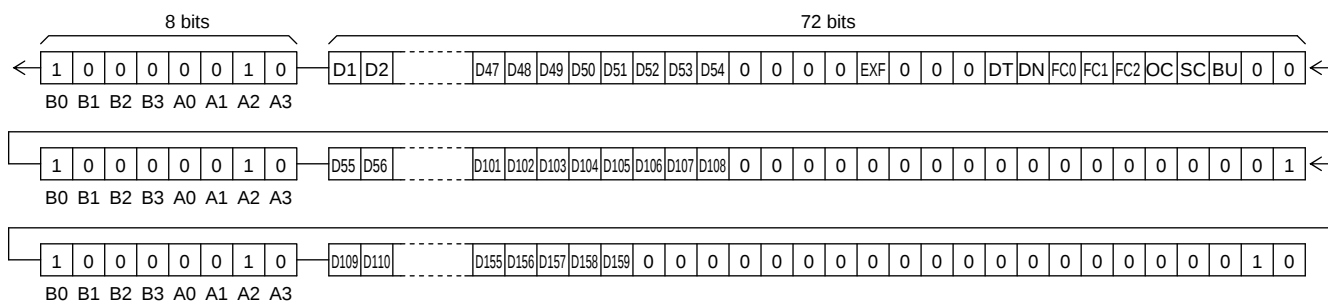


- When fewer than 153 segments are used  
One of 80, 160 and 240 bits of serial data must be sent, depending on the number of segments to be used.  
However, the serial data shown below (the D1 to D52 display data, the control data and DD="00") must always be sent.

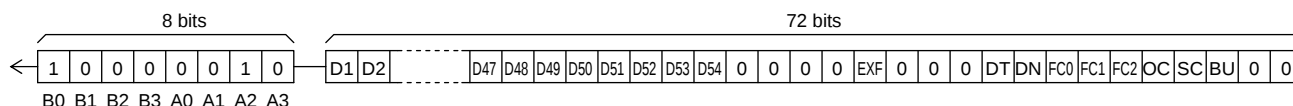


### 2. 1/3 duty

- When 109 or more segments are used  
All 240 bits (include CCB address) of serial data must be sent.



- When fewer than 109 segments are used  
Either 80 or 160 bits of serial data must be sent, depending on the number of segments to be used.  
However, the serial data shown below (the D1 to D54 display data, the control data and DD="00") must always be sent.



## Control Data Functions

### (1) EXF ... Ratio of dividing frequency in external clock operating mode setting control data

This control data sets the ratio of dividing frequency of the external clock which input into the OSCI pad, when the external clock operating mode (OC="1") is set. However, this data is effective only when external clock operating mode (OC= "1") is set. The frame frequency is adjustable by setting EXF, FC0 to FC2 and OC.

| EXF | Ratio of dividing frequency in external clock operating mode |
|-----|--------------------------------------------------------------|
| 0   | $f_{CK} / 8$                                                 |
| 1   | $f_{CK}$                                                     |

### (2) DT ...1/4-duty drive or 1/3-duty drive switching control data

This control data bit selects either 1/4-duty drive or 1/3-duty drive.

| DT | Drive scheme   | S51 pad's state               |
|----|----------------|-------------------------------|
| 0  | 1/4-duty drive | Low ( $V_{SS}$ ) level output |
| 1  | 1/3-duty drive | S51 (segment output)          |

### (3) DN ...The number of the maximum display segments setting control data

This control data bit sets the number of the maximum display segments.

| DN | The number of the maximum display segments |                    | Pad's state          |                      |
|----|--------------------------------------------|--------------------|----------------------|----------------------|
|    | 1/4 duty                                   | 1/3 duty           | S52                  | S53                  |
| 0  | Up to 200 segments                         | Up to 153 segments | "L" ( $V_{SS}$ )     | "L" ( $V_{SS}$ )     |
| 1  | Up to 208 segments                         | Up to 159 segments | S52 (segment output) | S53 (segment output) |

(Note) S53 pad outputs  $V_{SS}$  level in external clock operating mode.

### (4) FC0 to FC2 ...Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms. The frame frequency is adjustable by setting EXF, FC0 to FC2 and OC.

| Control data |     |     | Frame frequency $f_o$ [Hz]                                                                 |                                                                                                       |                                                                                                      |
|--------------|-----|-----|--------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| FC0          | FC1 | FC2 | Internal oscillator operating mode<br>(The control data OC="0",<br>$f_{osc}=300$ [kHz]typ) | External clock operating mode<br>(The control data<br>OC="1", EXF="0")<br>Case is $f_{CK}=300$ [kHz]. | External clock operating mode<br>(The control data<br>OC="1", EXF="1")<br>Case is $f_{CK}=38$ [kHz]. |
| 0            | 0   | 0   | $f_{osc}/6144 = 48.8$ [Hz]typ                                                              | $f_{CK}/6144 = 48.8$ [Hz]                                                                             | $f_{CK}/768 = 49.5$ [Hz]                                                                             |
| 0            | 0   | 1   | $f_{osc}/4608 = 65.1$ [Hz]typ                                                              | $f_{CK}/4608 = 65.1$ [Hz]                                                                             | $f_{CK}/576 = 66.0$ [Hz]                                                                             |
| 0            | 1   | 0   | $f_{osc}/3072 = 97.7$ [Hz]typ                                                              | $f_{CK}/3072 = 97.7$ [Hz]                                                                             | $f_{CK}/384 = 99.0$ [Hz]                                                                             |
| 0            | 1   | 1   | $f_{osc}/2304 = 130.2$ [Hz]typ                                                             | $f_{CK}/2304 = 130.2$ [Hz]                                                                            | $f_{CK}/288 = 131.9$ [Hz]                                                                            |
| 1            | 0   | 0   | $f_{osc}/1536 = 195.3$ [Hz]typ                                                             | $f_{CK}/1536 = 195.3$ [Hz]                                                                            | $f_{CK}/192 = 197.9$ [Hz]                                                                            |
| 1            | 0   | 1   | $f_{osc}/1152 = 260.4$ [Hz]typ                                                             | $f_{CK}/1152 = 260.4$ [Hz]                                                                            | $f_{CK}/144 = 263.9$ [Hz]                                                                            |
| 1            | 1   | 0   | $f_{osc}/768 = 390.6$ [Hz]typ                                                              | $f_{CK}/768 = 390.6$ [Hz]                                                                             | $f_{CK}/96 = 395.8$ [Hz]                                                                             |
| 1            | 1   | 1   | $f_{osc}/3072 = 97.7$ [Hz]typ                                                              | $f_{CK}/3072 = 97.7$ [Hz]                                                                             | $f_{CK}/384 = 99.0$ [Hz]                                                                             |

### (5) OC ...Internal oscillator operating mode/external clock operating mode switching control data

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

| OC | Fundamental clock operating mode   | S53 pad's state               |
|----|------------------------------------|-------------------------------|
| 0  | Internal oscillator operating mode | S53 (segment output)          |
| 1  | External clock operating mode      | Low ( $V_{SS}$ ) level output |

### (6) SC ... Segment on/off (off waveform output) control data

This control data bit controls the on/off (off waveform output) state of all the segments.

| SC | Display state                                 |
|----|-----------------------------------------------|
| 0  | On                                            |
| 1  | Off of all the segments (off waveform output) |

### (7) BU ... Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

| BU | Mode                                                                                                                                                                                                                                                                                                                                    |
|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0  | Normal mode                                                                                                                                                                                                                                                                                                                             |
| 1  | Power-saving mode<br>All of the common and segment output pads output the $V_{SS}$ level.<br>In this mode, the internal oscillator circuit stops oscillation if the IC is in the internal oscillator operating mode (OC=0), and the IC stops receiving external clock signals if the IC is in the external clock operating mode (OC=1). |

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## Display Data and Output Pad Correspondence (1/4 Duty)

| Output pad | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|
| S1         | D1   | D2   | D3   | D4   |
| S2         | D5   | D6   | D7   | D8   |
| S3         | D9   | D10  | D11  | D12  |
| S4         | D13  | D14  | D15  | D16  |
| S5         | D17  | D18  | D19  | D20  |
| S6         | D21  | D22  | D23  | D24  |
| S7         | D25  | D26  | D27  | D28  |
| S8         | D29  | D30  | D31  | D32  |
| S9         | D33  | D34  | D35  | D36  |
| S10        | D37  | D38  | D39  | D40  |
| S11        | D41  | D42  | D43  | D44  |
| S12        | D45  | D46  | D47  | D48  |
| S13        | D49  | D50  | D51  | D52  |
| S14        | D53  | D54  | D55  | D56  |
| S15        | D57  | D58  | D59  | D60  |
| S16        | D61  | D62  | D63  | D64  |
| S17        | D65  | D66  | D67  | D68  |
| S18        | D69  | D70  | D71  | D72  |
| S19        | D73  | D74  | D75  | D76  |
| S20        | D77  | D78  | D79  | D80  |
| S21        | D81  | D82  | D83  | D84  |
| S22        | D85  | D86  | D87  | D88  |
| S23        | D89  | D90  | D91  | D92  |
| S24        | D93  | D94  | D95  | D96  |
| S25        | D97  | D98  | D99  | D100 |
| S26        | D101 | D102 | D103 | D104 |
| S27        | D105 | D106 | D107 | D108 |

| Output pad | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|
| S28        | D109 | D110 | D111 | D112 |
| S29        | D113 | D114 | D115 | D116 |
| S30        | D117 | D118 | D119 | D120 |
| S31        | D121 | D122 | D123 | D124 |
| S32        | D125 | D126 | D127 | D128 |
| S33        | D129 | D130 | D131 | D132 |
| S34        | D133 | D134 | D135 | D136 |
| S35        | D137 | D138 | D139 | D140 |
| S36        | D141 | D142 | D143 | D144 |
| S37        | D145 | D146 | D147 | D148 |
| S38        | D149 | D150 | D151 | D152 |
| S39        | D153 | D154 | D155 | D156 |
| S40        | D157 | D158 | D159 | D160 |
| S41        | D161 | D162 | D163 | D164 |
| S42        | D165 | D166 | D167 | D168 |
| S43        | D169 | D170 | D171 | D172 |
| S44        | D173 | D174 | D175 | D176 |
| S45        | D177 | D178 | D179 | D180 |
| S46        | D181 | D182 | D183 | D184 |
| S47        | D185 | D186 | D187 | D188 |
| S48        | D189 | D190 | D191 | D192 |
| S49        | D193 | D194 | D195 | D196 |
| S50        | D197 | D198 | D199 | D200 |
| S51        | -    | -    | -    | -    |
| S52        | D201 | D202 | D203 | D204 |
| S53        | D205 | D206 | D207 | D208 |

(Note) In external clock operating mode, S53 pad outputs V<sub>SS</sub> level. When DN is “0”, S52 pad and S53 pad output V<sub>SS</sub> level. When duty is 1/4, S51 pad outputs V<sub>SS</sub> level.

For example, the table below lists the output states for the S21 output pad.

| Display data |     |     |     | Output pad (S21) state                                                |
|--------------|-----|-----|-----|-----------------------------------------------------------------------|
| D81          | D82 | D83 | D84 |                                                                       |
| 0            | 0   | 0   | 0   | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off. |
| 0            | 0   | 0   | 1   | The LCD segment corresponding to COM4 is on.                          |
| 0            | 0   | 1   | 0   | The LCD segment corresponding to COM3 is on.                          |
| 0            | 0   | 1   | 1   | The LCD segments corresponding to COM3 and COM4 are on.               |
| 0            | 1   | 0   | 0   | The LCD segment corresponding to COM2 is on.                          |
| 0            | 1   | 0   | 1   | The LCD segments corresponding to COM2 and COM4 are on.               |
| 0            | 1   | 1   | 0   | The LCD segments corresponding to COM2 and COM3 are on.               |
| 0            | 1   | 1   | 1   | The LCD segments corresponding to COM2, COM3, and COM4 are on.        |
| 1            | 0   | 0   | 0   | The LCD segment corresponding to COM1 is on.                          |
| 1            | 0   | 0   | 1   | The LCD segments corresponding to COM1 and COM4 are on.               |
| 1            | 0   | 1   | 0   | The LCD segments corresponding to COM1 and COM3 are on.               |
| 1            | 0   | 1   | 1   | The LCD segments corresponding to COM1, COM3, and COM4 are on.        |
| 1            | 1   | 0   | 0   | The LCD segments corresponding to COM1 and COM2 are on.               |
| 1            | 1   | 0   | 1   | The LCD segments corresponding to COM1, COM2, and COM4 are on.        |
| 1            | 1   | 1   | 0   | The LCD segments corresponding to COM1, COM2, and COM3 are on.        |
| 1            | 1   | 1   | 1   | The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.  |

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## Display Data and Output Pad Correspondence (1/3 Duty)

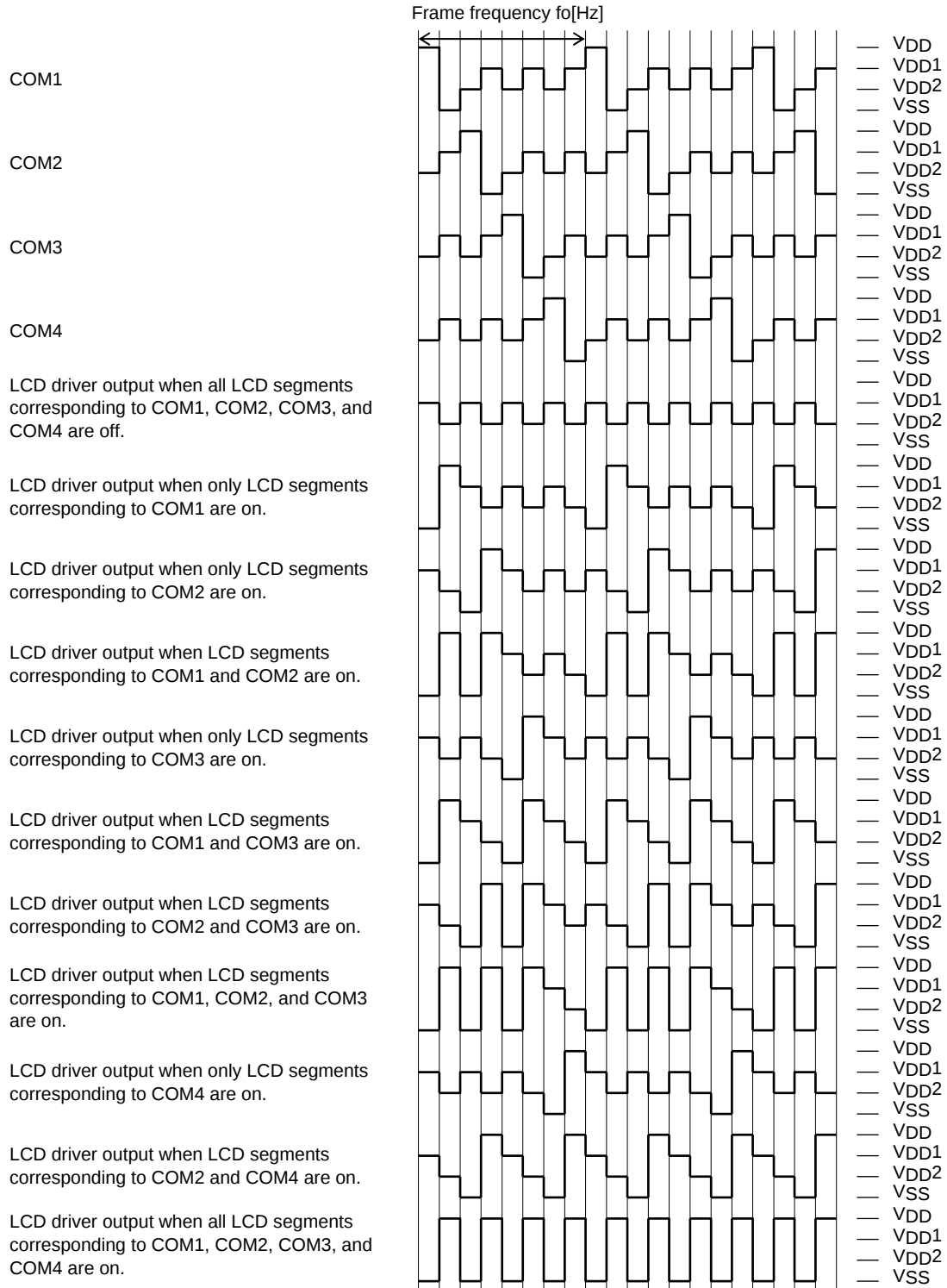
| Output pad | COM1 | COM2 | COM3 | Output pad | COM1 | COM2 | COM3 |
|------------|------|------|------|------------|------|------|------|
| S1         | D1   | D2   | D3   | S28        | D82  | D83  | D84  |
| S2         | D4   | D5   | D6   | S29        | D85  | D86  | D87  |
| S3         | D7   | D8   | D9   | S30        | D88  | D89  | D90  |
| S4         | D10  | D11  | D12  | S31        | D91  | D92  | D93  |
| S5         | D13  | D14  | D15  | S32        | D94  | D95  | D96  |
| S6         | D16  | D17  | D18  | S33        | D97  | D98  | D99  |
| S7         | D19  | D20  | D21  | S34        | D100 | D101 | D102 |
| S8         | D22  | D23  | D24  | S35        | D103 | D104 | D105 |
| S9         | D25  | D26  | D27  | S36        | D106 | D107 | D108 |
| S10        | D28  | D29  | D30  | S37        | D109 | D110 | D111 |
| S11        | D31  | D32  | D33  | S38        | D112 | D113 | D114 |
| S12        | D34  | D35  | D36  | S39        | D115 | D116 | D117 |
| S13        | D37  | D38  | D39  | S40        | D118 | D119 | D120 |
| S14        | D40  | D41  | D42  | S41        | D121 | D122 | D123 |
| S15        | D43  | D44  | D45  | S42        | D124 | D125 | D126 |
| S16        | D46  | D47  | D48  | S43        | D127 | D128 | D129 |
| S17        | D49  | D50  | D51  | S44        | D130 | D131 | D132 |
| S18        | D52  | D53  | D54  | S45        | D133 | D134 | D135 |
| S19        | D55  | D56  | D57  | S46        | D136 | D137 | D138 |
| S20        | D58  | D59  | D60  | S47        | D139 | D140 | D141 |
| S21        | D61  | D62  | D63  | S48        | D142 | D143 | D144 |
| S22        | D64  | D65  | D66  | S49        | D145 | D146 | D147 |
| S23        | D67  | D68  | D69  | S50        | D148 | D149 | D150 |
| S24        | D70  | D71  | D72  | S51        | D151 | D152 | D153 |
| S25        | D73  | D74  | D75  | S52        | D154 | D155 | D156 |
| S26        | D76  | D77  | D78  | S53        | D157 | D158 | D159 |
| S27        | D79  | D80  | D81  |            |      |      |      |

(Note) In external clock operating mode, S53 pad outputs V<sub>SS</sub> level. When DN is “0”, S52 pad and S53 pad output V<sub>SS</sub> level.

For example, the table below lists the output states for the S21 output pad.

| Display data |     |     | Output pad (S21) state                                          |
|--------------|-----|-----|-----------------------------------------------------------------|
| D61          | D62 | D63 |                                                                 |
| 0            | 0   | 0   | The LCD segments corresponding to COM1, COM2, and COM3 are off. |
| 0            | 0   | 1   | The LCD segment corresponding to COM3 is on.                    |
| 0            | 1   | 0   | The LCD segment corresponding to COM2 is on.                    |
| 0            | 1   | 1   | The LCD segments corresponding to COM2 and COM3 are on.         |
| 1            | 0   | 0   | The LCD segment corresponding to COM1 is on.                    |
| 1            | 0   | 1   | The LCD segments corresponding to COM1 and COM3 are on.         |
| 1            | 1   | 0   | The LCD segments corresponding to COM1 and COM2 are on.         |
| 1            | 1   | 1   | The LCD segments corresponding to COM1, COM2, and COM3 are on.  |

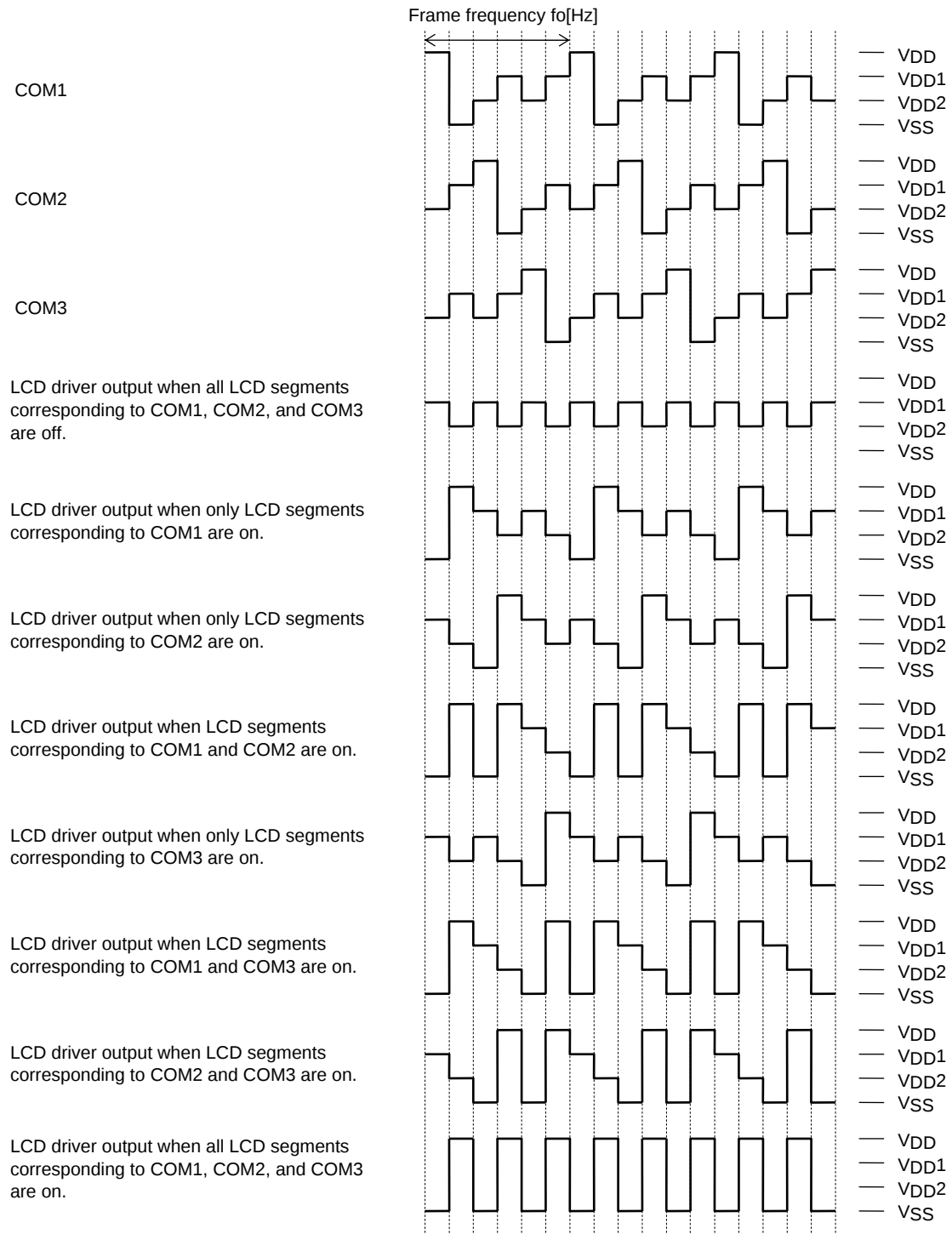
Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)



(Note) The frame frequency  $f_o$ [Hz] is adjustable by setting control data (EXF, FC0 to FC2 and OC).  
(See "Control Data Functions" for details)

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## Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)

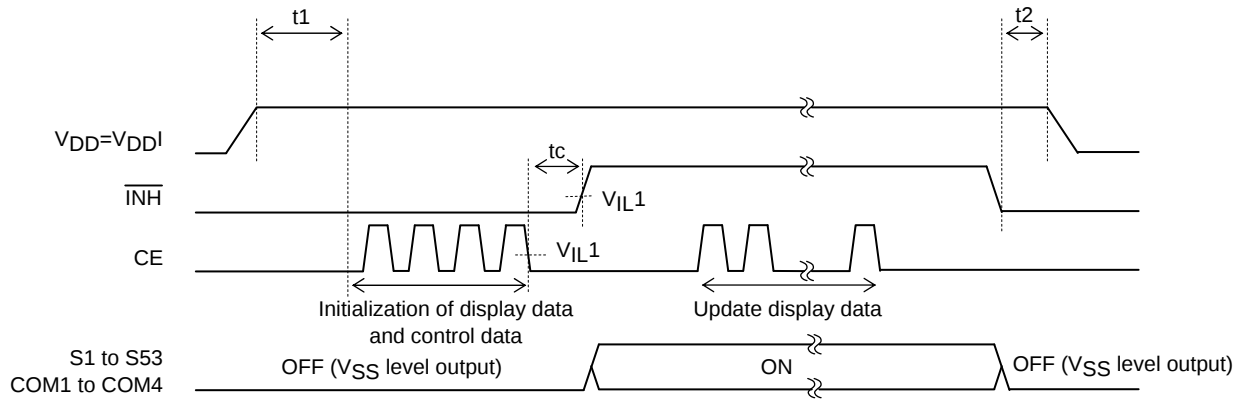


(Note) The frame frequency  $f_o$ [Hz] is adjustable by setting control data (EXF, FC0 to FC2 and OC).  
(See "Control Data Functions" for details)

## Display Control and the $\overline{\text{INH}}$ Pad

Since the LSI internal data (1/4 duty : the display data D1 to D208 and the control data, 1/3 duty : the display data D1 to D159 and the control data) is undefined when power is first applied. Applications should set the  $\overline{\text{INH}}$  pad low at the same time as power is applied to turn off the display (This sets the S1 to S53 and COM1 to COM4 pads the  $V_{SS}$  level.) and during this period send serial data from the controller. The controller should then set the  $\overline{\text{INH}}$  pad high after the data transfer has completed. This procedure prevents meaningless display at power on.  $V_{DD}$  and  $V_{DDI}$  are connected with the same power supply. The timing of turn on and turn off for  $V_{DD}$  and  $V_{DDI}$  should be same time. (See from Figure 5 to Figure 8)

### • 1/4 duty



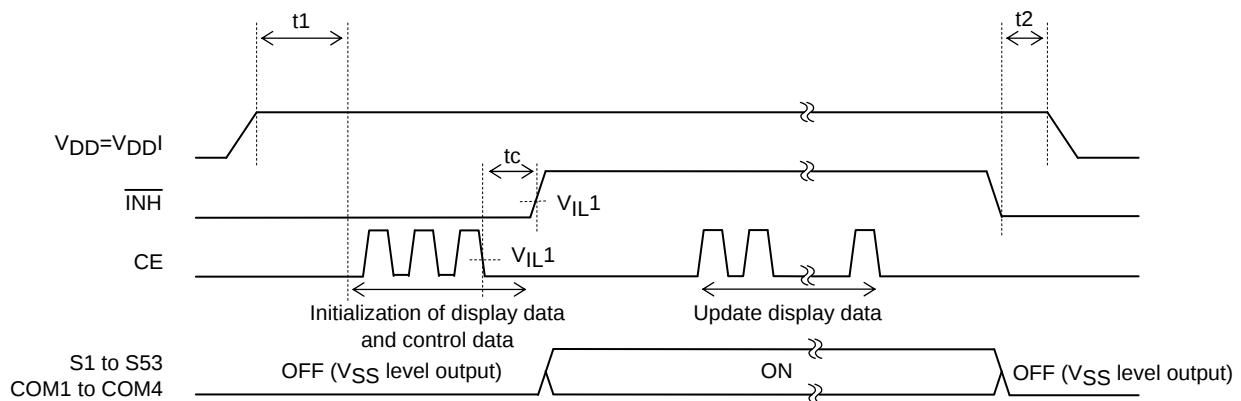
(Note) The wait time ( $t_1$ ) which power supply turn on should be 1ms or more.

The discharge time ( $t_2$ ) of LCD panel's electric charge should be decided the optimum value according to the characteristic of the LCD panel.

The switching time ( $t_c$ ) of  $\overline{\text{INH}}$  should be 10 $\mu$ s or more.

[Figure 5]

### • 1/3 duty



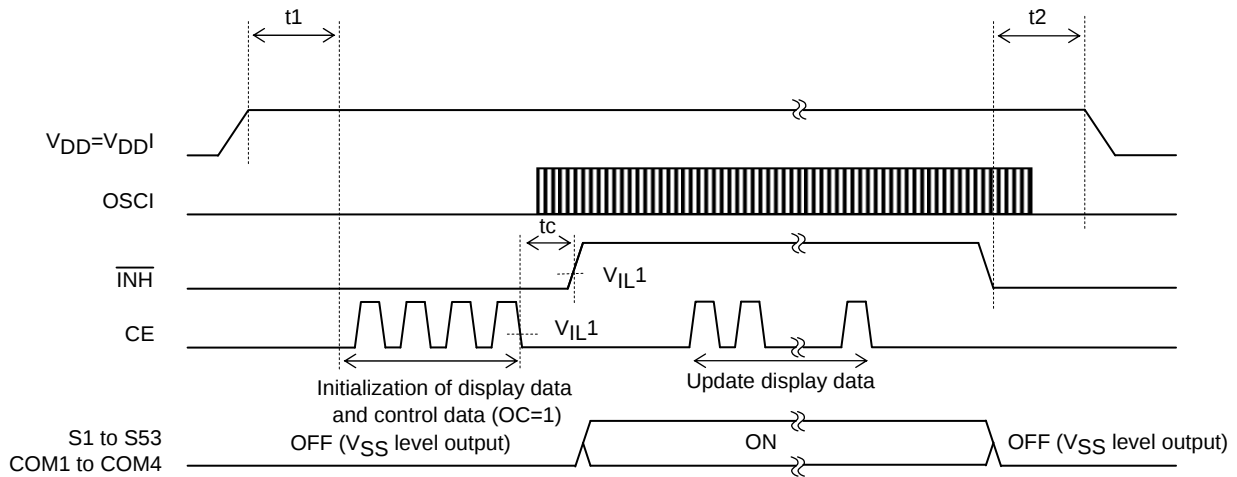
(Note) The wait time ( $t_1$ ) which power supply turn on should be 1ms or more.

The discharge time ( $t_2$ ) of LCD panel's electric charge should be decided the optimum value according to the characteristic of the LCD panel.

The switching time ( $t_c$ ) of  $\overline{\text{INH}}$  should be 10 $\mu$ s or more.

[Figure 6]

• In external clock operating mode



(Note) The wait time (t<sub>1</sub>) which power supply turn on should be 1ms or more.

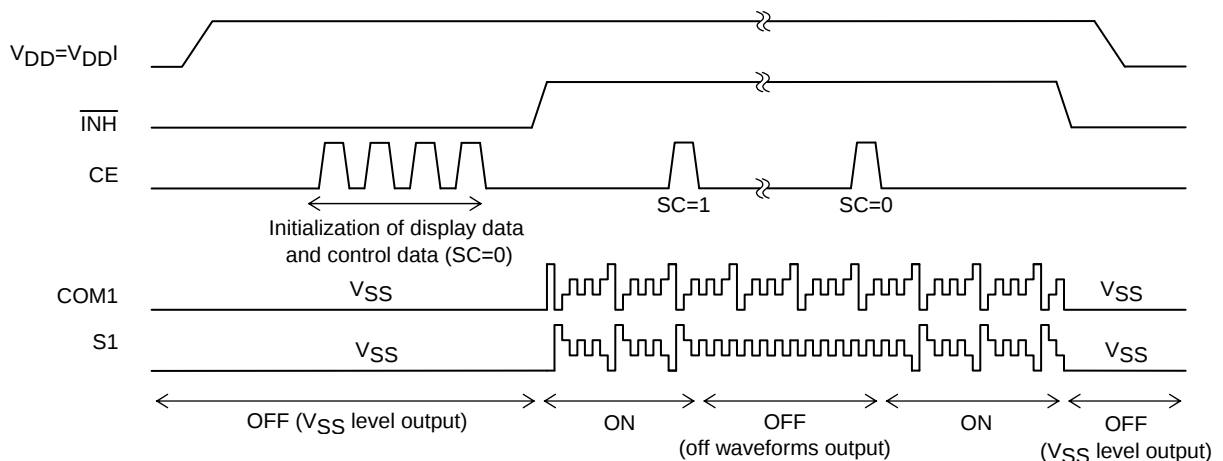
The discharge time (t<sub>2</sub>) of LCD panel's electric charge should be decided the optimum value according to the characteristic of the LCD panel.

The switching time (t<sub>c</sub>) of INH should be 10μs or more.

OSCI pad should be input an external clock at INH is high level.

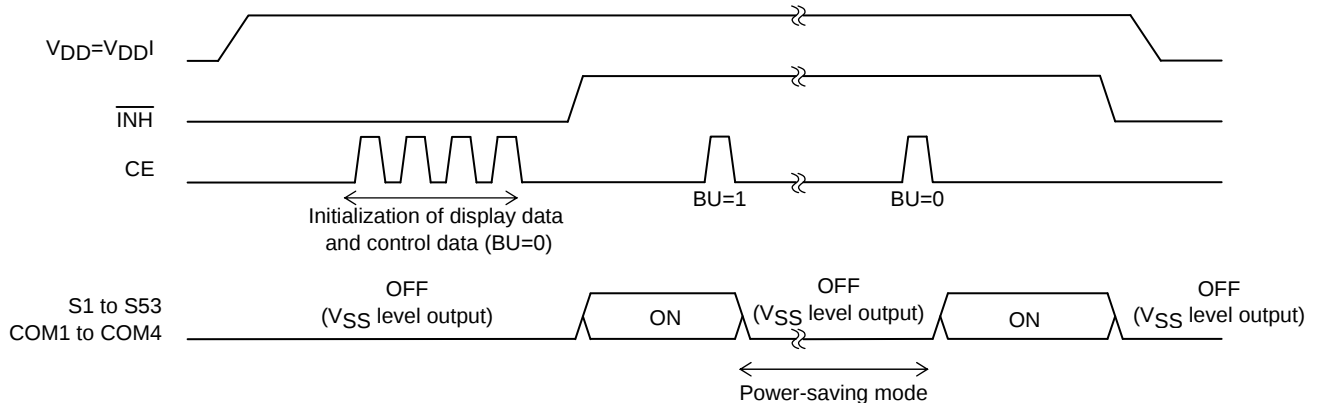
[Figure 7]

• All segments off (off waveforms output)



[Figure 8]

• Power-saving mode



[Figure 9]

## LC450029PKB

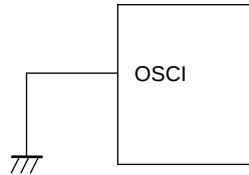
### Notes on Controller Transfer of Display Data

When using the LC450029PKB in 1/4 duty, applications transfer the display data (D1 to D208) in four operations, and in 1/3 duty, they transfer the display data (D1 to D159) in three operations. In either case, applications should transfer all of the display data within 30ms to maintain the quality of displayed image.

About peripheral circuit of the input pad

#### (1) Processing of unused OSCI pad

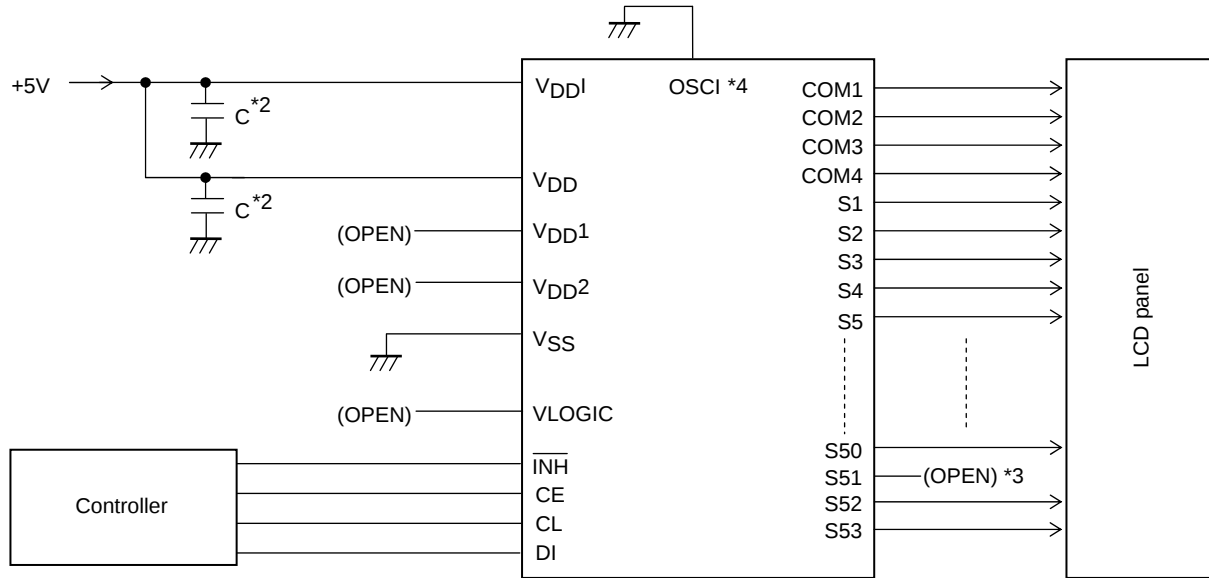
When OSCI pad is not to be used, select the internal oscillator operating mode (control data OC="0"), and OSCI pad is connected to GND.



## LC450029PKB

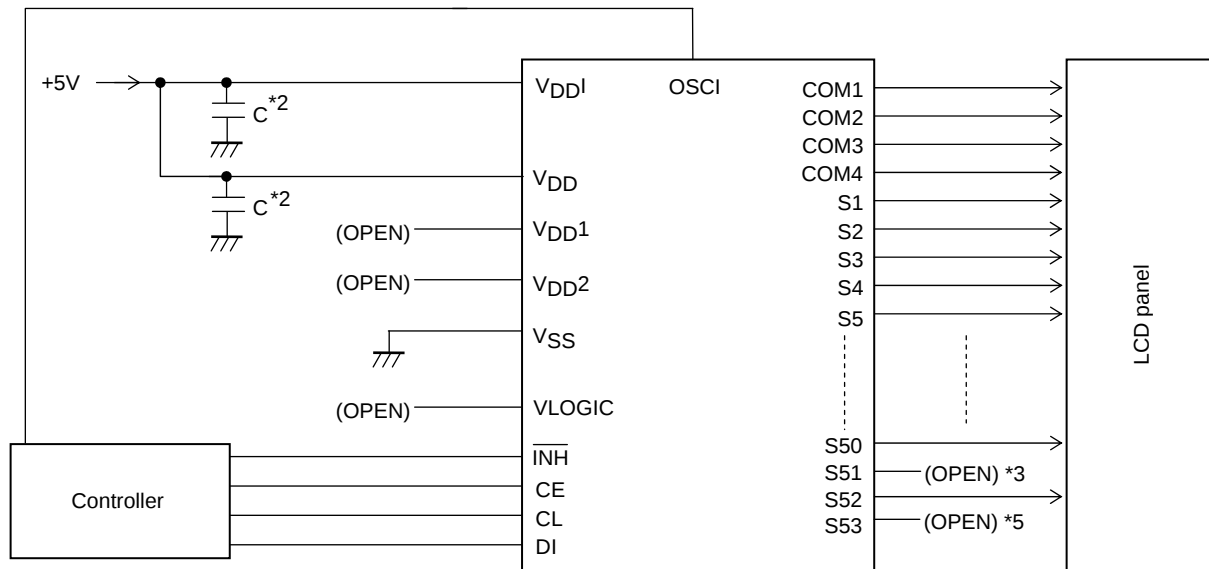
### Sample Applications Circuit 1

1/4 duty, Display data (D1 to D208), Internal oscillator operating mode



### Sample Applications Circuit 2

1/4 duty, Display data (D1 to D204), External clock operating mode



\*2 Connect capacitors between a power supply line and GND for noise removal and power supply stabilization.

Determine the value of a capacitor, after an actual circuit board estimates.

\*3 In 1/4 duty, S51 pad outputs VSS level.

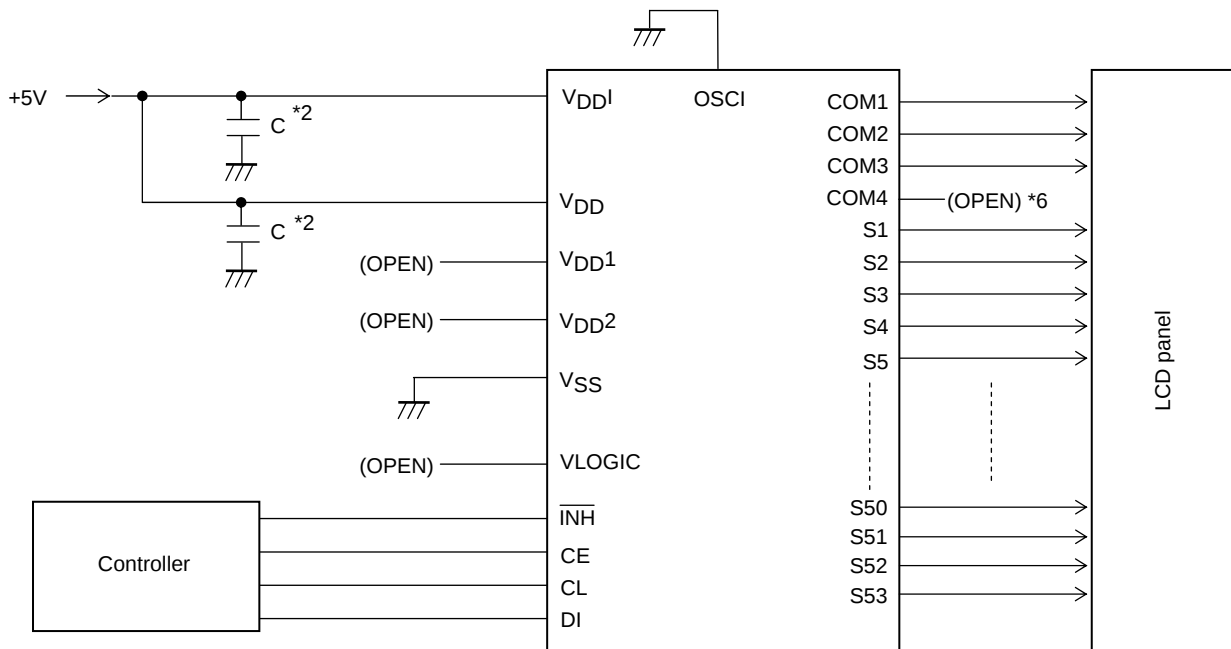
\*4 When OSCI pad is not to be used, select the internal oscillator operating mode (control data OC="0"), and OSCI pad is connected to GND.

\*5 In external clock operating mode, S53 pad outputs VSS level.

## LC450029PKB

### Sample Applications Circuit 3

1/3 duty, Display data (D1 to D159), Internal oscillator operating mode



\*2 Connect capacitors between a power supply line and GND for noise removal and power supply stabilization.

Determine the value of a capacitor, after an actual circuit board estimates.

\*6 In 1/3 duty, COM4 pad outputs V<sub>SS</sub> level.

## The Notes on Use

Important things for stability operation of IC are shown as follows. The contents indicated below do not guarantee IC operation and the characteristic. Moreover, the example of an application circuit written in these specifications is for explaining internal operation and usage. Therefore, please perform the design in consideration of the specification of operation and terms and conditions in the actual LCD panel.

(1) The design of power supply

All power supply pads are connected to the power supply, and do not set open.

(2) ITO (Indium Tin Oxide) wiring

By designing the wire of power supply ( $V_{DD}$ ,  $V_{DDI}$ ,  $V_{SS}$ ) wide and short, make the parasitic resistance of ITO wiring into the minimum.

(3) Signal wiring and connection

The DUMMY pad does not connect to anywhere, and sets open.

(4) Processing of unused input pad

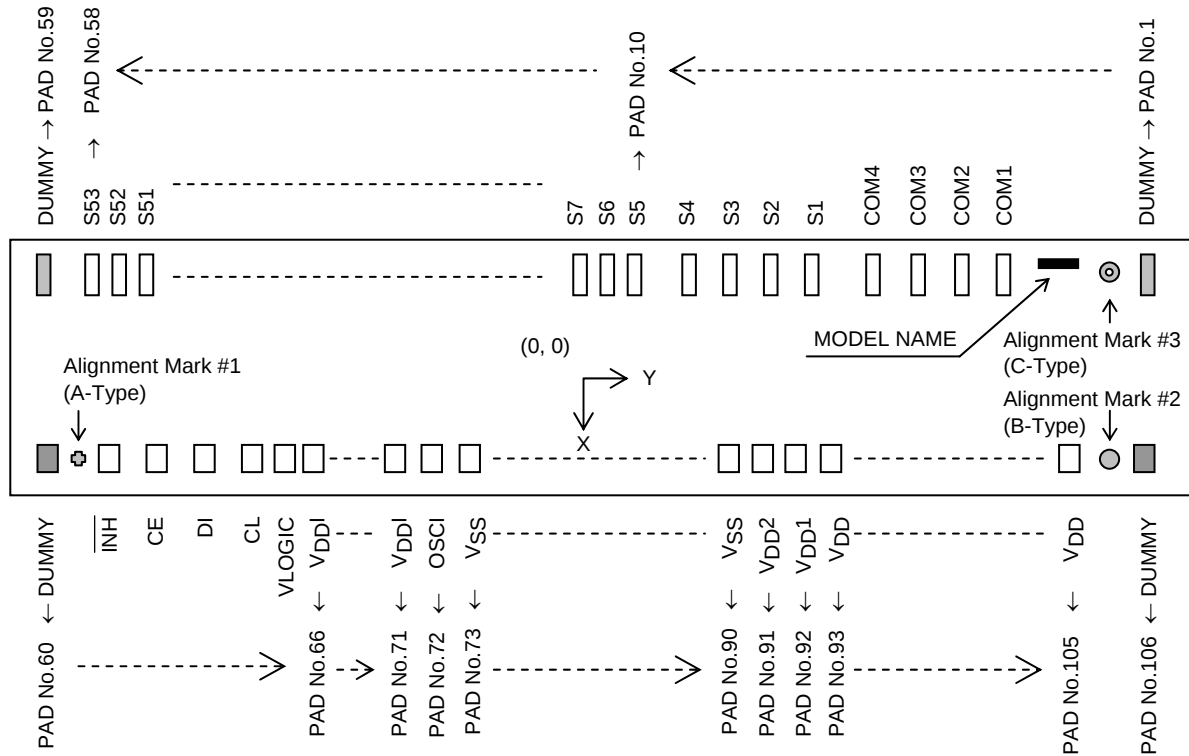
For CMOS process, if an input pad is in open state, operation of IC may become unstable, or unnecessary power supply current may flow through it. Please be sure to connect the empty pad of a logic input to  $V_{SS}$ .

(5) The measure against shading

The optical irradiation to IC causes the mis-operation of IC. When IC is implemented, take the measures against shading about the surface, back and side of IC.

# LC450029PKB

## • PAD Locations (Bump Side View)



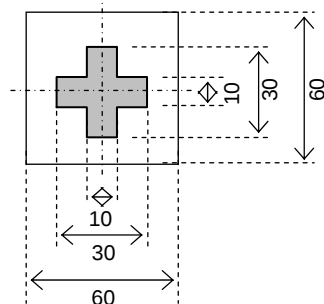
- Chip dimensions (X, Y, S are based on the dicing center.)  
X=1.00mm Y=4.08mm S=4.08mm<sup>2</sup> Wafer thickness=400μm (typ)

## • Au Bump dimensions (typ)

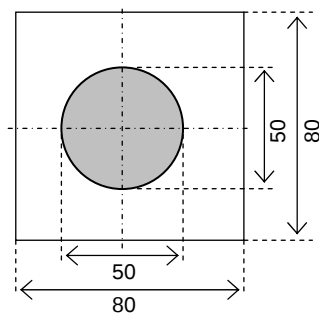
| Item                | PAD No.                                 | Size   |        |                      |
|---------------------|-----------------------------------------|--------|--------|----------------------|
|                     |                                         | X [μm] | Y [μm] | S [μm <sup>2</sup> ] |
| Bump Size           | 1 to 59                                 | 108    | 27     | 2916                 |
|                     | 60 to 106                               | 68     | 42     | 2856                 |
| Min. Bump Pitch     | 10 to 58                                | 50     |        | -                    |
|                     | 1 to 9, 59 to 106                       | -      |        | -                    |
| Min. Bump Clearance | 10 to 58, 66 to 71, 73 to 90, 93 to 105 | 23     |        | -                    |
|                     | 1 to 9, 59 to 65, 72, 91 to 92, 106     | -      |        | -                    |
| Bump Height         | All pads                                | 17     |        | -                    |

## • Alignment marks

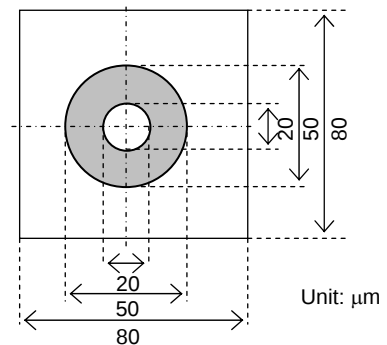
### (1) A-Type



### (2) B-Type



### (3) C-Type



Unit: μm

## LC450029PKB

- Center coordinates of PADs

(All x/y coordinates represent the position of the center of each PAD)

| PAD No. | PAD Name | X [μm] | Y [μm] |
|---------|----------|--------|--------|
| 1       | DUMMY    | -380   | 1950   |
| 2       | COM1     | -380   | 1369   |
| 3       | COM2     | -380   | 1276   |
| 4       | COM3     | -380   | 1183   |
| 5       | COM4     | -380   | 1090   |
| 6       | S1       | -380   | 932    |
| 7       | S2       | -380   | 856    |
| 8       | S3       | -380   | 780    |
| 9       | S4       | -380   | 704    |
| 10      | S5       | -380   | 607    |
| 11      | S6       | -380   | 557    |
| 12      | S7       | -380   | 507    |
| 13      | S8       | -380   | 457    |
| 14      | S9       | -380   | 407    |
| 15      | S10      | -380   | 357    |
| 16      | S11      | -380   | 307    |
| 17      | S12      | -380   | 257    |
| 18      | S13      | -380   | 207    |
| 19      | S14      | -380   | 157    |
| 20      | S15      | -380   | 107    |
| 21      | S16      | -380   | 57     |
| 22      | S17      | -380   | 7      |
| 23      | S18      | -380   | -43    |
| 24      | S19      | -380   | -93    |
| 25      | S20      | -380   | -143   |
| 26      | S21      | -380   | -193   |
| 27      | S22      | -380   | -243   |
| 28      | S23      | -380   | -293   |
| 29      | S24      | -380   | -343   |
| 30      | S25      | -380   | -393   |
| 31      | S26      | -380   | -443   |
| 32      | S27      | -380   | -493   |
| 33      | S28      | -380   | -543   |
| 34      | S29      | -380   | -593   |
| 35      | S30      | -380   | -643   |
| 36      | S31      | -380   | -693   |
| 37      | S32      | -380   | -743   |
| 38      | S33      | -380   | -793   |
| 39      | S34      | -380   | -843   |
| 40      | S35      | -380   | -893   |

| PAD No. | PAD Name         | X [μm] | Y [μm] |
|---------|------------------|--------|--------|
| 41      | S36              | -380   | -943   |
| 42      | S37              | -380   | -993   |
| 43      | S38              | -380   | -1043  |
| 44      | S39              | -380   | -1093  |
| 45      | S40              | -380   | -1143  |
| 46      | S41              | -380   | -1193  |
| 47      | S42              | -380   | -1243  |
| 48      | S43              | -380   | -1293  |
| 49      | S44              | -380   | -1343  |
| 50      | S45              | -380   | -1393  |
| 51      | S46              | -380   | -1443  |
| 52      | S47              | -380   | -1493  |
| 53      | S48              | -380   | -1543  |
| 54      | S49              | -380   | -1593  |
| 55      | S50              | -380   | -1643  |
| 56      | S51              | -380   | -1693  |
| 57      | S52              | -380   | -1743  |
| 58      | S53              | -380   | -1793  |
| 59      | DUMMY            | -380   | -1950  |
| 60      | DUMMY            | 400    | -1943  |
| 61      | INH              | 400    | -1665  |
| 62      | CE               | 400    | -1525  |
| 63      | DI               | 400    | -1385  |
| 64      | CL               | 400    | -1245  |
| 65      | VLOGIC           | 400    | -1161  |
| 66      | V <sub>DDI</sub> | 400    | -1071  |
| 67      | V <sub>DDI</sub> | 400    | -1006  |
| 68      | V <sub>DDI</sub> | 400    | -941   |
| 69      | V <sub>DDI</sub> | 400    | -876   |
| 70      | V <sub>DDI</sub> | 400    | -811   |
| 71      | V <sub>DDI</sub> | 400    | -746   |
| 72      | OSCI             | 400    | -650   |
| 73      | V <sub>SS</sub>  | 400    | -510   |
| 74      | V <sub>SS</sub>  | 400    | -445   |
| 75      | V <sub>SS</sub>  | 400    | -380   |
| 76      | V <sub>SS</sub>  | 400    | -315   |
| 77      | V <sub>SS</sub>  | 400    | -250   |
| 78      | V <sub>SS</sub>  | 400    | -185   |
| 79      | V <sub>SS</sub>  | 400    | -120   |
| 80      | V <sub>SS</sub>  | 400    | -55    |

| PAD No. | PAD Name         | X [μm] | Y [μm] |
|---------|------------------|--------|--------|
| 81      | V <sub>SS</sub>  | 400    | 10     |
| 82      | V <sub>SS</sub>  | 400    | 75     |
| 83      | V <sub>SS</sub>  | 400    | 140    |
| 84      | V <sub>SS</sub>  | 400    | 205    |
| 85      | V <sub>SS</sub>  | 400    | 270    |
| 86      | V <sub>SS</sub>  | 400    | 335    |
| 87      | V <sub>SS</sub>  | 400    | 400    |
| 88      | V <sub>SS</sub>  | 400    | 465    |
| 89      | V <sub>SS</sub>  | 400    | 530    |
| 90      | V <sub>SS</sub>  | 400    | 595    |
| 91      | V <sub>DD2</sub> | 400    | 668    |
| 92      | V <sub>DD1</sub> | 400    | 739    |
| 93      | V <sub>DD</sub>  | 400    | 811    |
| 94      | V <sub>DD</sub>  | 400    | 876    |
| 95      | V <sub>DD</sub>  | 400    | 941    |
| 96      | V <sub>DD</sub>  | 400    | 1006   |
| 97      | V <sub>DD</sub>  | 400    | 1071   |
| 98      | V <sub>DD</sub>  | 400    | 1136   |
| 99      | V <sub>DD</sub>  | 400    | 1201   |
| 100     | V <sub>DD</sub>  | 400    | 1266   |
| 101     | V <sub>DD</sub>  | 400    | 1331   |
| 102     | V <sub>DD</sub>  | 400    | 1396   |
| 103     | V <sub>DD</sub>  | 400    | 1461   |
| 104     | V <sub>DD</sub>  | 400    | 1526   |
| 105     | V <sub>DD</sub>  | 400    | 1591   |
| 106     | DUMMY            | 400    | 1943   |

- Center coordinates of alignment marks

(All x/y coordinates represent the position of the center of each alignment mark)

| Alignment mark | TYPE | X [μm] | Y [μm] |
|----------------|------|--------|--------|
| 1              | A    | 400    | -1800  |
| 2              | B    | 400    | 1790   |
| 3              | C    | -380   | 1800   |

## LC450029PKB

### ORDERING INFORMATION

| Device         | Package            | Shipping (Qty / Packing) |
|----------------|--------------------|--------------------------|
| LC450029PKB-XT | Wafer<br>(Pb-Free) | 1 / Waffle Pack          |

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