Input/Output Rail-to-Rail Low Supply Current CMOS Operational Amplifier for Automotive

BU7244YFV-C

General Description

BU7244YFV-C is an input/output rail-to-rail CMOS operational amplifier that operates on a wide temperature range and low supply current. It is suitable for a sensor amplifier and battery-powered equipment which require low input bias current.

Features

- AEC-Q100 Qualified(Note 1)
- Input/Output Rail-to-Rail
- Low Operating Supply Voltage
- Low Supply Current
- Low Input Bias Current
- Wide Operating Temperature Range

(Note 1) Grade 1

Applications

- Sensor Amplifiers
- Battery-powered Equipment
- Automotive Electronics

Key Specifications

- Operating Supply Voltage Range
  - Single Supply: 1.8 V to 5.5 V
  - Dual Supply: ±0.90 V to ±2.75 V
- Operating Temperature Range: -40 °C to +125 °C
- Supply Current: 360 µA (Typ)
- Input Offset Current: 1 pA (Typ)
- Input Bias Current: 1 pA (Typ)

Special Characteristic

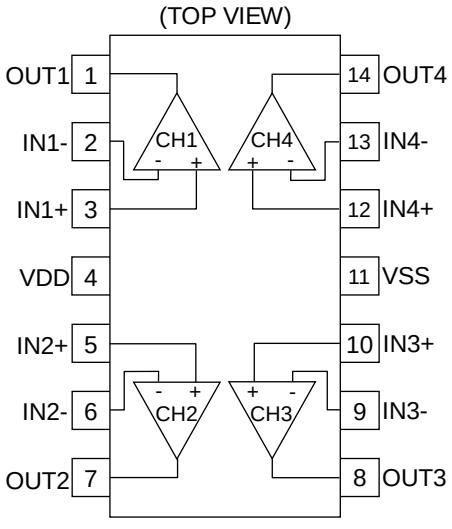
- Input Offset Voltage
  - -40 °C to +125 °C: 12 mV (Max)

Package

Package	W(Typ) x D(Typ) x H(Max)
SSOP-B14	5.00 mm x 6.40 mm x 1.35 mm



Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	OUT1	Output 1
2	IN1-	Inverting input 1
3	IN1+	Non-inverting input 1
4	VDD	Positive power supply
5	IN2+	Non-inverting input 2
6	IN2-	Inverting input 2
7	OUT2	Output 2
8	OUT3	Output 3
9	IN3-	Inverting input 3
10	IN3+	Non-inverting input 3
11	VSS	Negative power supply/Ground
12	IN4+	Non-inverting input 4
13	IN4-	Inverting input 4
14	OUT4	Output 4

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Block Diagram

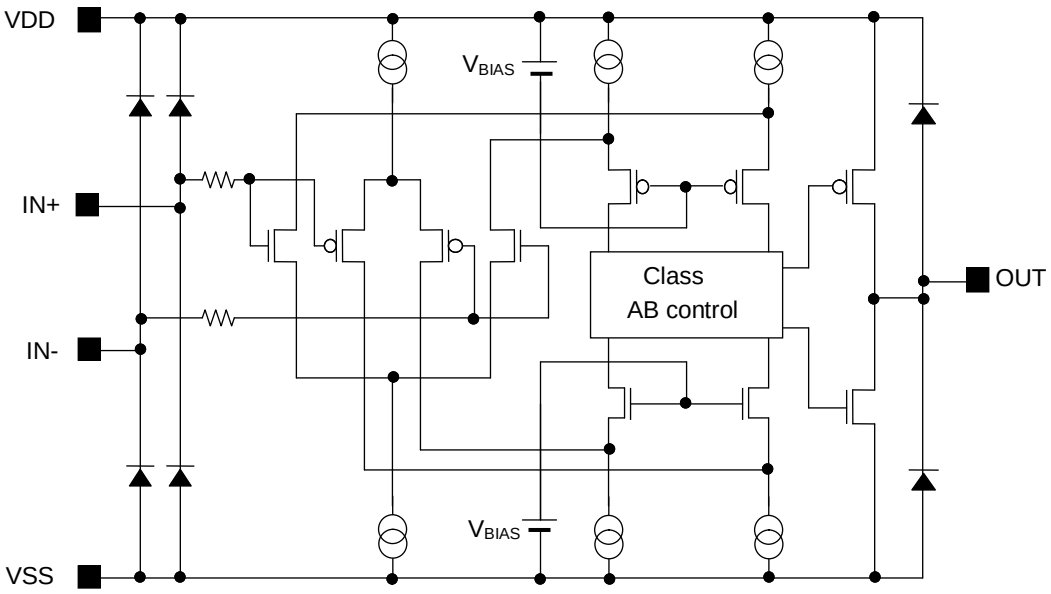


Figure 1. Block Diagram

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}-V_{SS}	7	V
Power Dissipation	Pd	0.87*(Note 2,3)*	W
Differential Input Voltage*(Note 4)*	V_{ID}	V_{DD} - V_{SS}	V
Common-mode Input Voltage Range	V_{ICM}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Input Current	I_I	±10	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 2) To use at temperature above Ta=25 °C reduce 7.0 mW/°C.

(Note 3) Mounted on an FR4 glass epoxy PCB 70 mm×70 mm×1.6 mm (Copper foil area less than 3 %).

(Note 4) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to more than VSS.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	Vopr	1.8 ±0.90	3.0 ±1.5	5.5 ±2.75	V
Operating Temperature	Topr	-40	+25	+125	°C

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Electrical Characteristics (Unless otherwise specified V_{DD}=3 V, V_{SS}=0 V, Ta=25 °C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage*(Note 5,6)*	V_{IO}	25 °C	-	1	10	mV	V_{DD}=1.8 V to 5.5 V
		Full range	-	-	12		
Input Offset Current*(Note 5)*	I_{IO}	25 °C	-	1	-	pA	-
Input Bias Current*(Note 5,6)*	I_B	25 °C	-	1	300	pA	-
		Full range	-	-	6000	pA	-
Supply Current*(Note 6)*	I_{DD}	25 °C	-	360	750	µA	R_L=∞, A_V=0 dB, V_{IN+}=1.5 V
		Full range	-	-	1200		
Maximum Output Voltage (High)*(Note 6)*	V_{OH}	25 °C	V_{DD}-0.05	-	-	V	R_L=10 kΩ
		Full range	V_{DD}-0.10	-	-		
Maximum Output Voltage (Low)*(Note 6)*	V_{OL}	25 °C	-	-	V_{SS}+0.05	V	R_L=10 kΩ
		Full range	-	-	V_{SS}+0.10		
Large Signal Voltage Gain*(Note 6)*	A_V	25 °C	70	100	-	dB	R_L=10 kΩ
		Full range	65	-	-		
Common-mode Input Voltage Range	V_{ICM}	25 °C	0	-	3	V	-
Common-mode Rejection Ratio	CMRR	25 °C	45	70	-	dB	-
Power Supply Rejection Ratio	PSRR	25 °C	60	80	-	dB	-
Output Source Current*(Note 6,7)*	I_{SOURCE}	25 °C	4	10	-	mA	V_{OUT}=V_{DD}-0.4 V
		Full range	2	-	-		
Output Sink Current*(Note 6,7)*	I_{SINK}	25 °C	5	15	-	mA	V_{OUT}=V_{SS}+0.4 V
		Full range	3	-	-		
Slew Rate	SR	25 °C	-	0.4	-	V/µs	C_L=25 pF
Gain Bandwidth Product	GBW	25 °C	-	1	-	MHz	C_L=25 pF, A_V=40 dB
Phase Margin	θ	25 °C	-	50	-	deg	C_L=25 pF, A_V=40 dB
Total Harmonic Distortion + Noise	THD+N	25 °C	-	0.05	-	%	V_{OUT}=0.8 V_{P-P}, f=1 kHz
Channel Separation	CS	25 °C	-	100	-	dB	A_V=40 dB, V_{OUT}=1 Vrms

(Note 5) Absolute value
(Note 6) Full range: Ta=-40 °C to +125 °C
(Note 7) Consider the power dissipation of the IC under high temperature environment when selecting the output current value.
When the output pins are short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

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Description of Terms in Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols generally used are also shown. Note that item names and symbols, and their meanings may differ from those on another manufacturer's or general documents.

1. Absolute Maximum Ratings

Absolute maximum rating items indicates the condition which must not be exceeded even if it is instantaneous. Applying of a voltage exceeding the absolute maximum ratings or use outside the temperature range which is provided in the absolute maximum ratings cause characteristic deterioration or destruction of the IC.

1.1 Supply Voltage (V_{DD}/V_{SS})
This indicates the maximum voltage that can be applied between the positive power supply pin and the negative power supply pin without deteriorating the characteristics of internal circuit or without destroying it.

1.2 Differential Input Voltage (V_{ID})
This indicates the maximum voltage that can be applied between the non-inverting input pin and the inverting input pin without deteriorating the characteristics of the IC or without destroying it.

1.3 Common-mode Input Voltage Range (V_{ICM})
This indicates the maximum voltage that can be applied to the non-inverting input pin and inverting input pin without deteriorating the characteristics of the IC or without destroying it. Common-mode Input Voltage Range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the Common-mode Input Voltage Range characteristics.

1.4 Power Dissipation (Pd)
This indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25 °C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical Characteristics

2.1 Input Offset Voltage (V_{IO})
This indicates the voltage difference between non-inverting and inverting pins. It can be translated as the input voltage difference required for setting the output voltage at 0 V.

2.2 Input Offset Current (I_{IO})
This indicates the difference of input bias current between the non-inverting and inverting pins.

2.3 Input Bias Current (I_B)
This indicates the current that flows into or out from the input pin. It is defined by the average of input bias currents at the non-inverting and inverting pins.

2.4 Supply Current (I_{DD})
This indicates the current of the IC itself flowing under the specified conditions and under no-load or steady-state conditions.

2.5 Maximum Output Voltage (High) / Maximum Output Voltage (Low) (V_{OH}/V_{OL})
This indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

2.6 Large Signal Voltage Gain (A_V)
This indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting pin and inverting pin. It is normally the amplifying rate (gain) with reference to DC voltage.
A_V = (Output voltage) / (Differential input voltage)

2.7 Common-mode Input Voltage Range (V_{ICM})
This indicates the input voltage range where IC normally operates.

2.8 Common-mode Rejection Ratio (CMRR)
This indicates the ratio of fluctuation of input offset voltage when Common-mode Input Voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

2.9 Power Supply Rejection Ratio (PSRR)
This indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

2.10 Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

2.11 Slew Rate (SR)
This is a parameter representing the operational speed of the operational amplifier. This indicates the rate at which the output voltage can change in the specified unit time.

2.12 Gain Band Width (GBW)
This indicates the product of an arbitrary frequency and its gain in the range of the gain slope of 6 dB/octave.

2.13 Phase Margin (θ)
This indicates the margin of phase from the phase delay of 180 degree at the frequency at which the gain of the operational amplifier is 1.

2.14 Total Harmonic Distortion+Noise (THD+N)
This indicates the content ratio of harmonic and noise components relative to the output signal.

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Typical Performance Curves

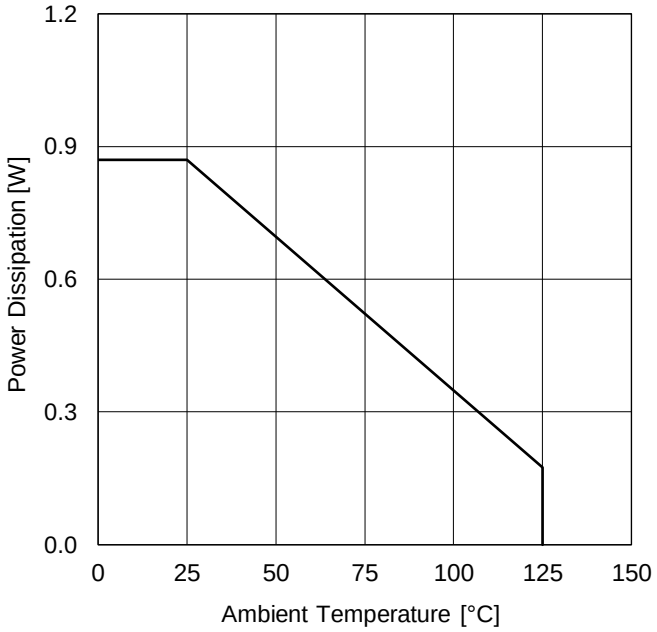


Figure 2. Power Dissipation vs Ambient Temperature (Derating Curve)

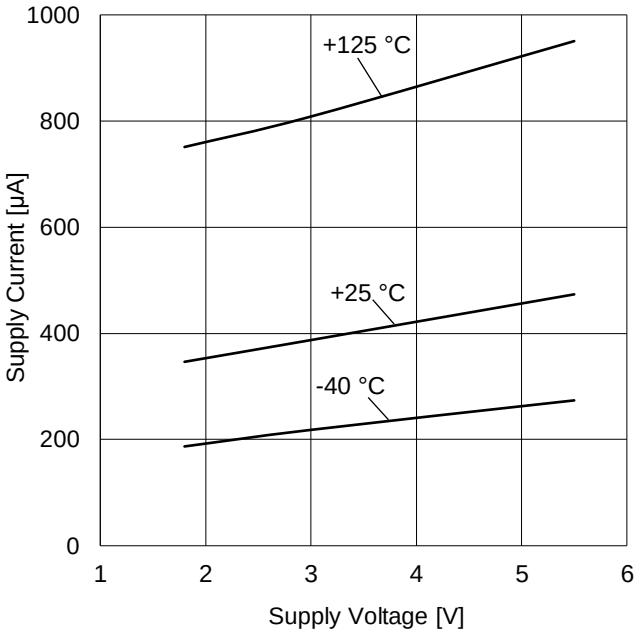


Figure 3. Supply Current vs Supply Voltage

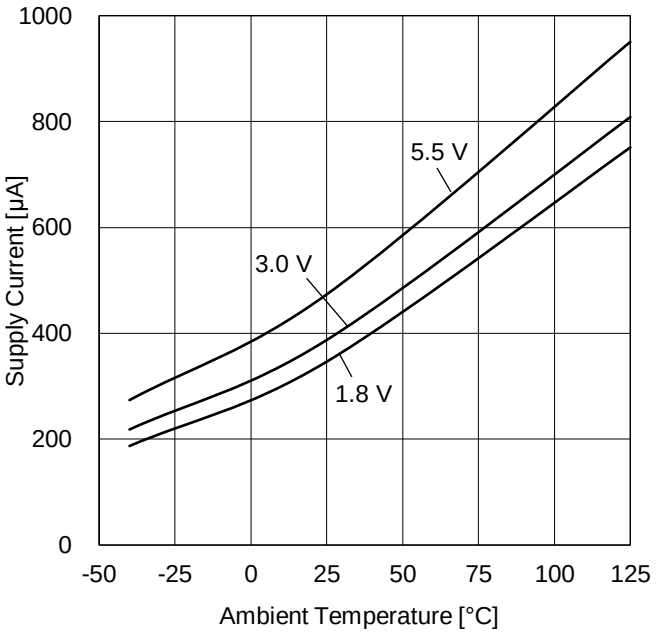


Figure 4. Supply Current vs Ambient Temperature

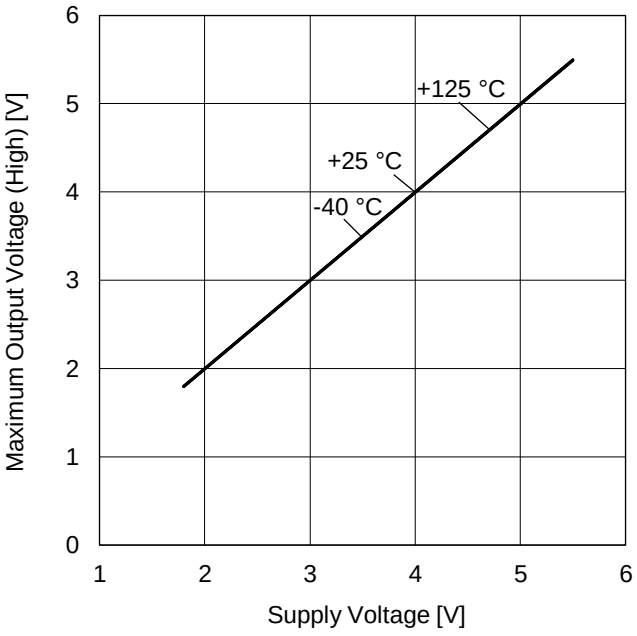


Figure 5. Maximum Output Voltage (High) vs Supply Voltage (R_L=10 kΩ)

(Note) The above characteristics are measurements of typical sample, they are not guaranteed.

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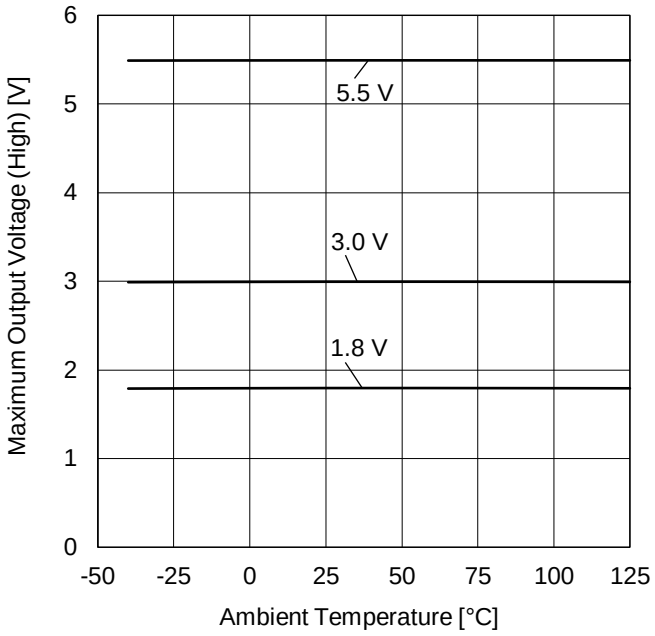


Figure 6. Maximum Output Voltage (High) vs Ambient Temperature (R_L=10 kΩ)

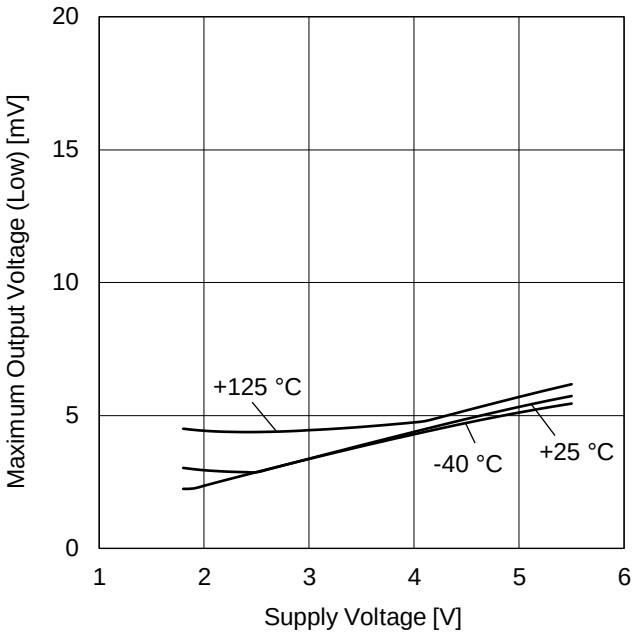


Figure 7. Maximum Output Voltage (Low) vs Supply Voltage (R_L=10 kΩ)

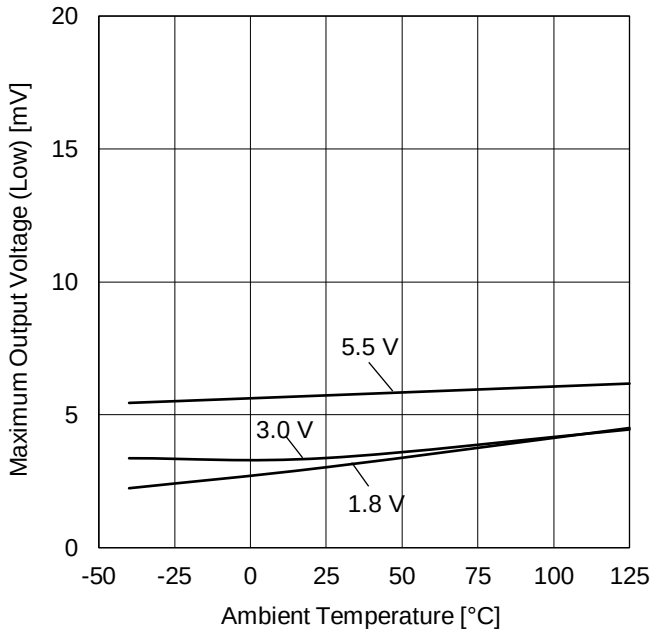


Figure 8. Maximum Output Voltage (Low) vs Ambient Temperature (R_L=10 kΩ)

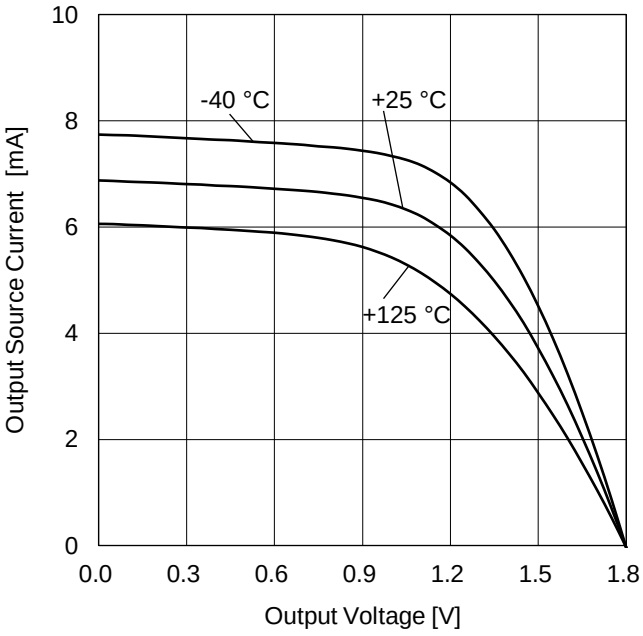


Figure 9. Output Source Current vs Output Voltage (V_{DD}=1.8 V)

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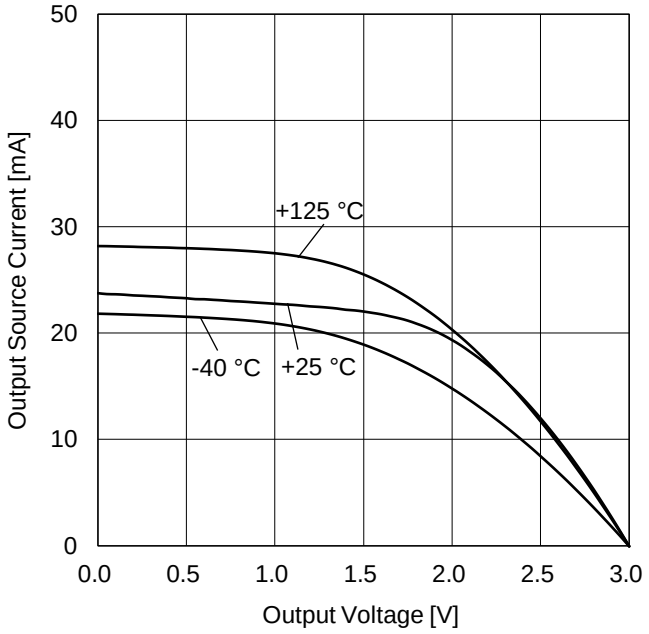


Figure 10. Output Source Current vs Output Voltage (V_{DD}=3.0 V)

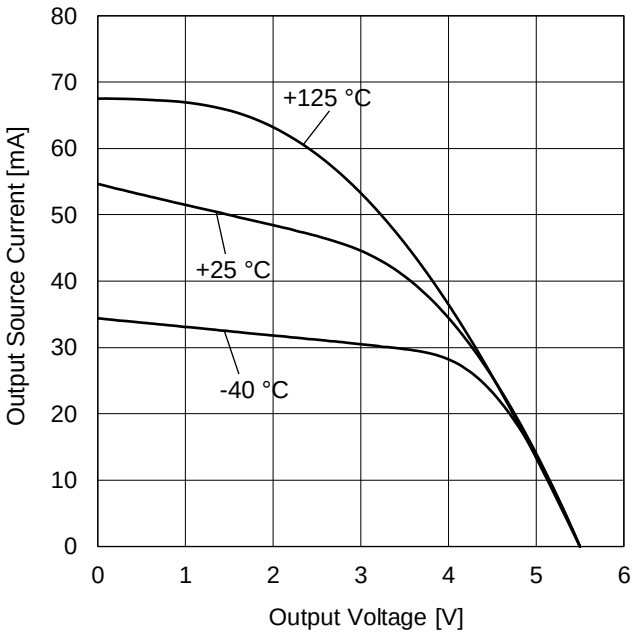


Figure 11. Output Source Current vs Output Voltage (V_{DD}=5.5 V)

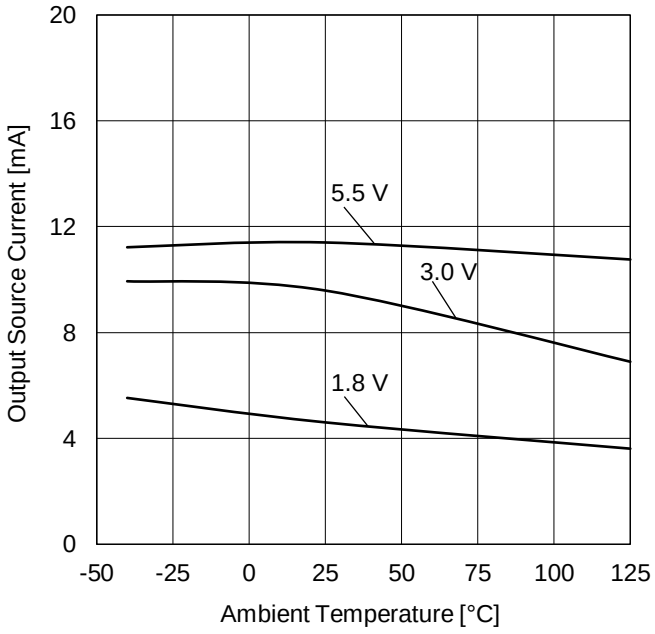


Figure 12. Output Source Current vs Ambient Temperature (V_{OUT}=V_{DD}-0.4 V)

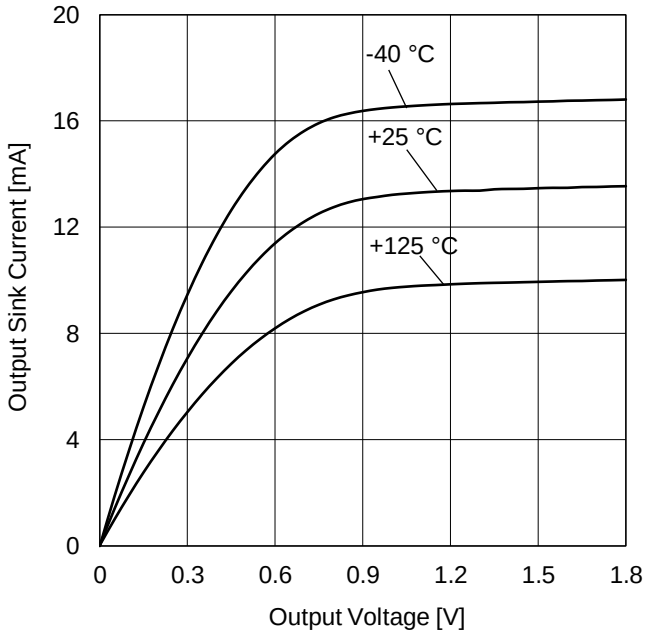


Figure 13. Output Sink Current vs Output Voltage (V_{DD}=1.8 V)

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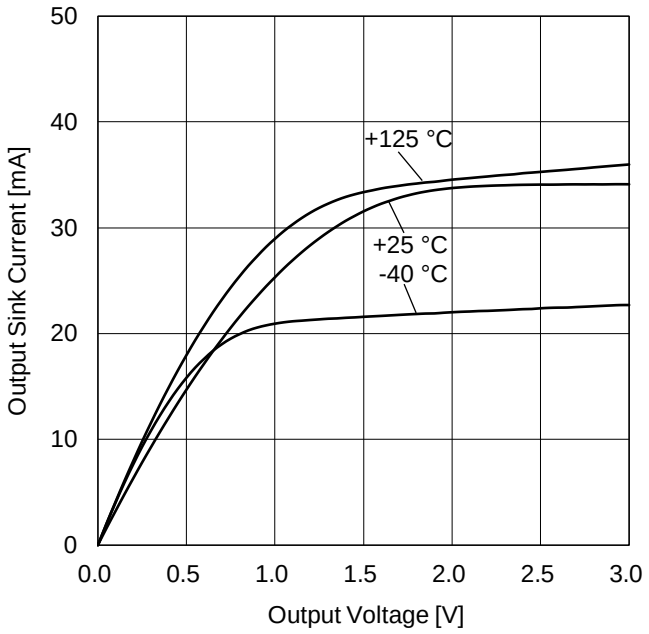


Figure 14. Output Sink Current vs Output Voltage (V_{DD}=3.0 V)

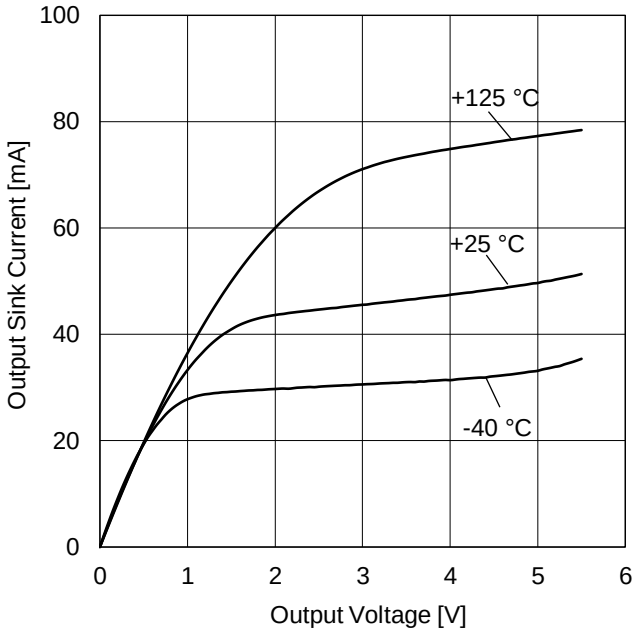


Figure 15. Output Sink Current vs Output Voltage (V_{DD}=5.5 V)

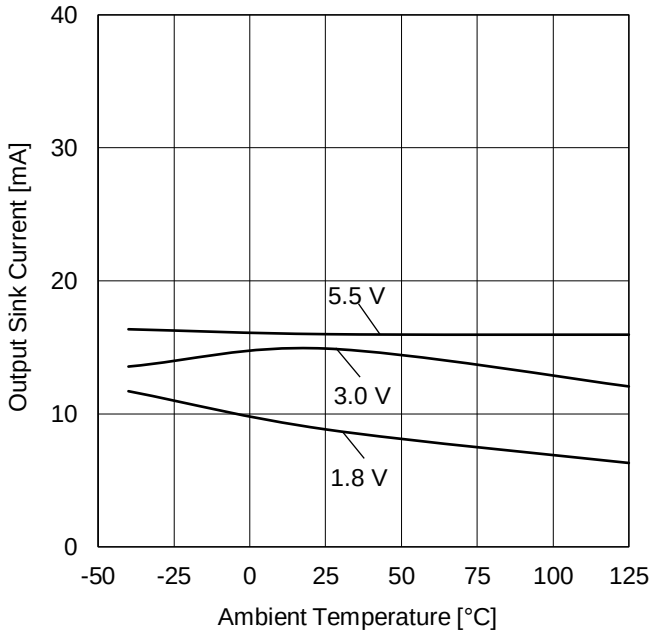


Figure 16. Output Sink Current vs Ambient Temperature (V_{OUT}=V_{SS}+0.4 V)

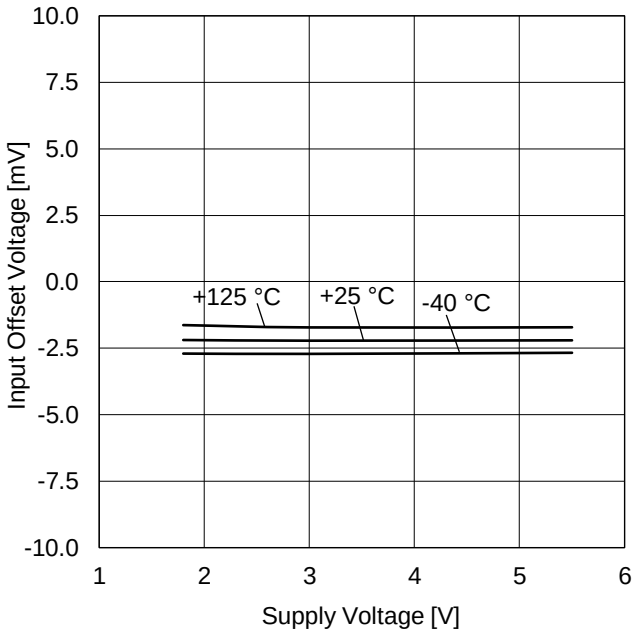


Figure 17. Input Offset Voltage vs Supply Voltage (V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

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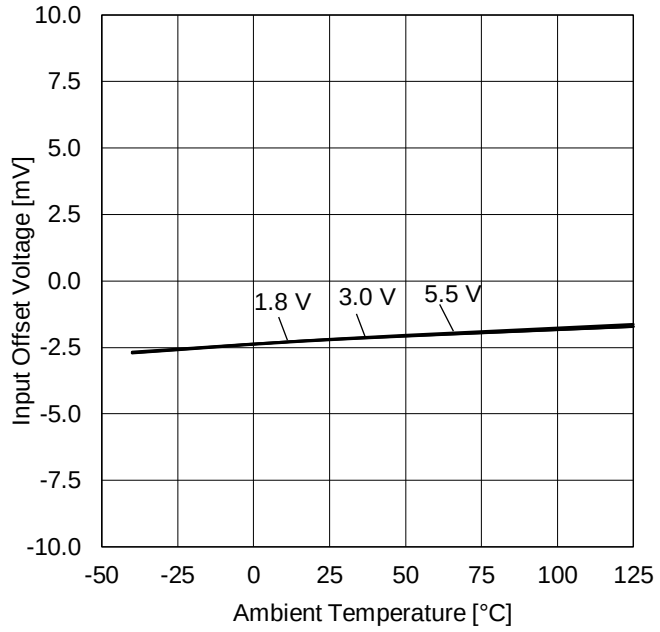


Figure 18. Input Offset Voltage vs Ambient Temperature (V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

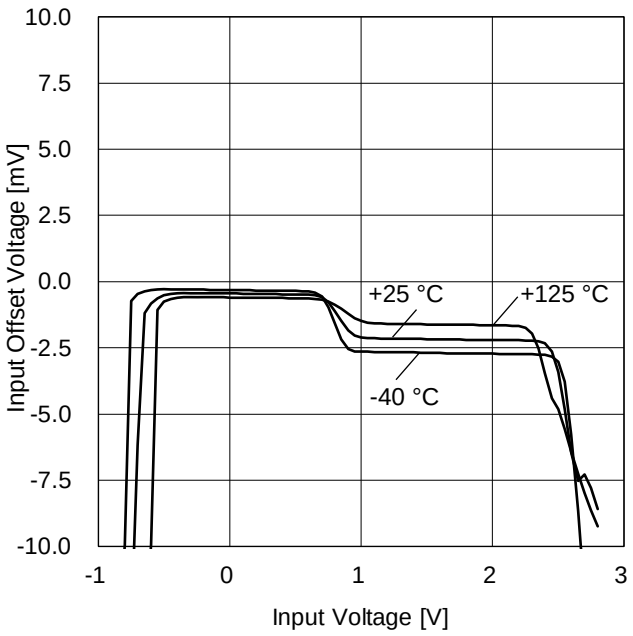


Figure 19. Input Offset Voltage vs Input Voltage (V_{DD}=1.8 V)

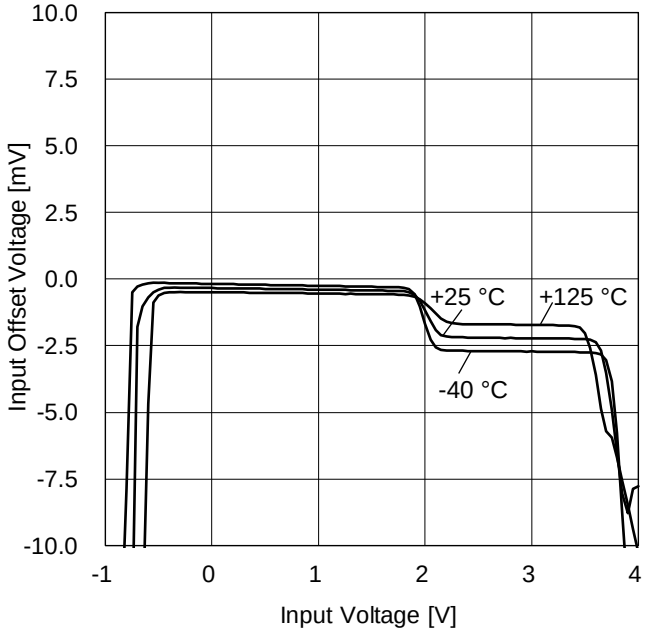


Figure 20. Input Offset Voltage vs Input Voltage (V_{DD}=3.0 V)

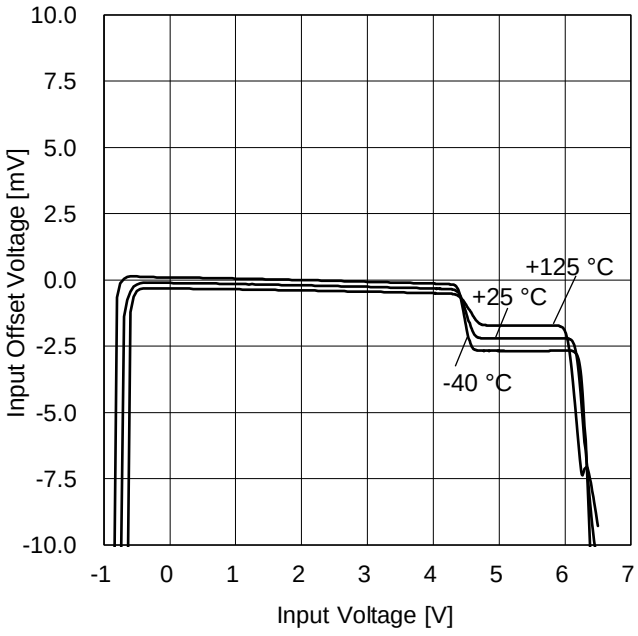


Figure 21. Input Offset Voltage vs Input Voltage (V_{DD}=5.5 V)

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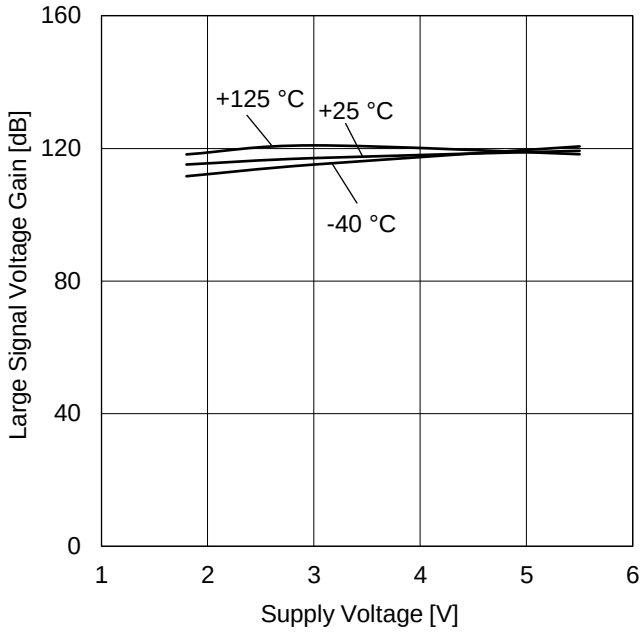


Figure 22. Large Signal Voltage Gain vs Supply Voltage

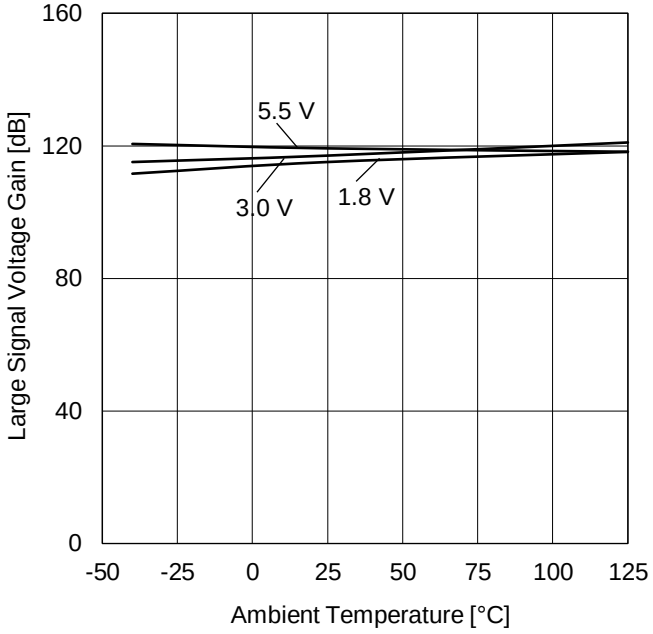


Figure 23. Large Signal Voltage Gain vs Ambient Temperature

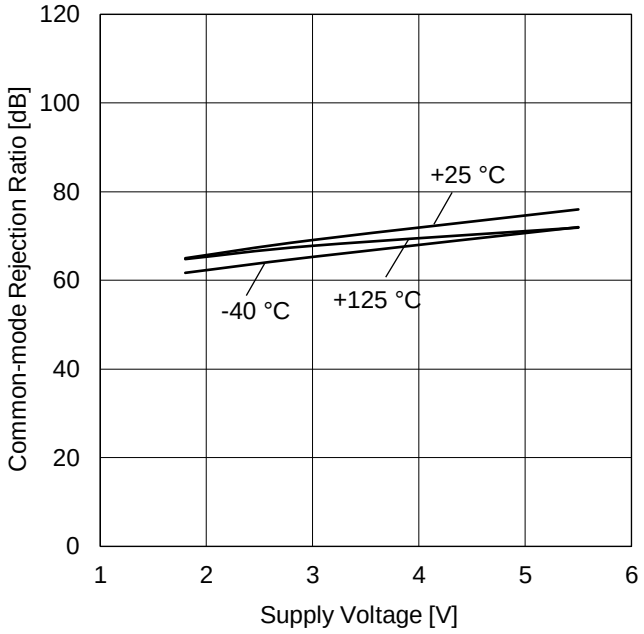


Figure 24. Common-mode Rejection Ratio vs Supply Voltage

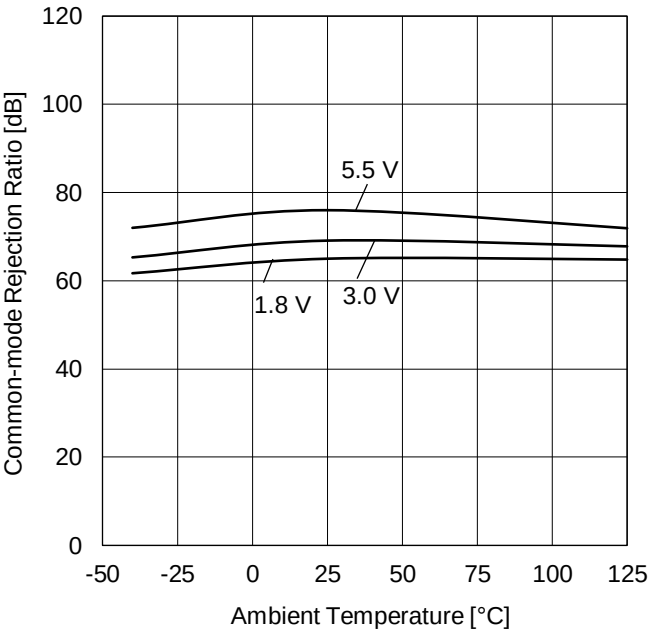


Figure 25. Common-mode Rejection Ratio vs Ambient Temperature

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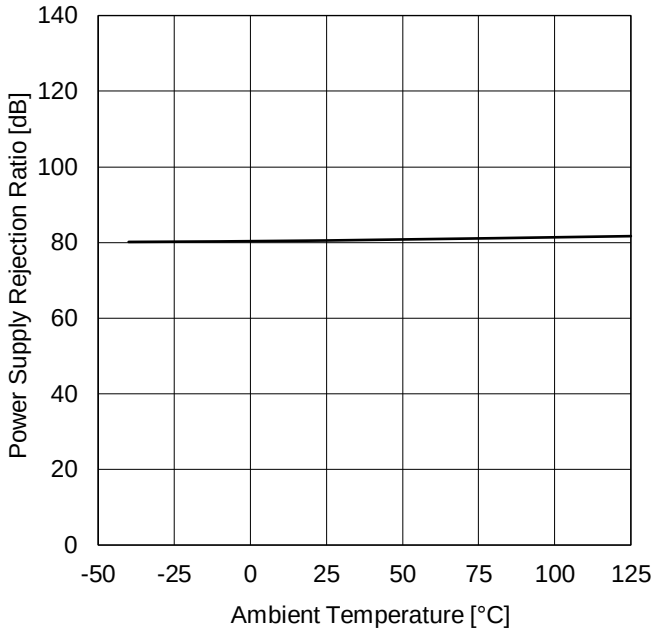


Figure 26. Power Supply Rejection Ratio vs Ambient Temperature

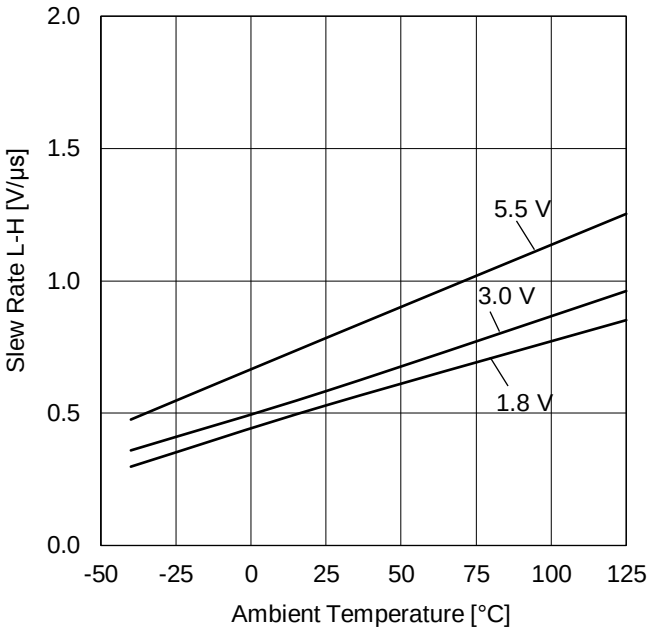


Figure 27. Slew Rate(L-H) vs Ambient Temperature

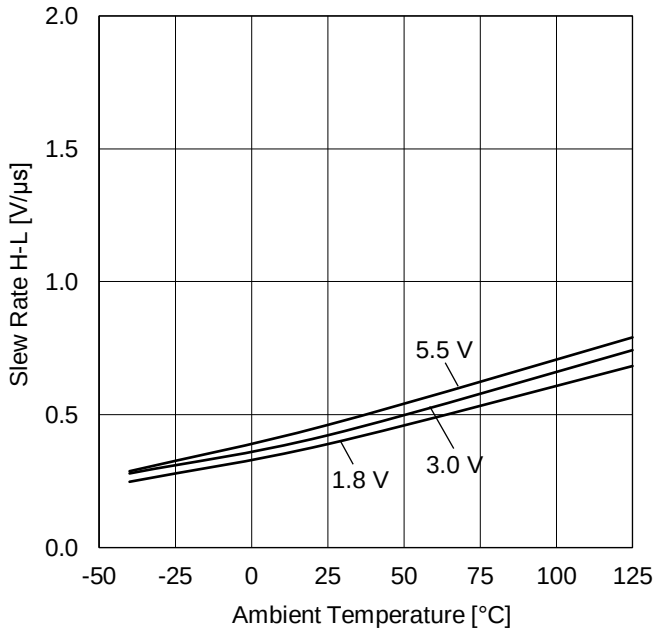


Figure 28. Slew Rate(H-L) vs Ambient Temperature

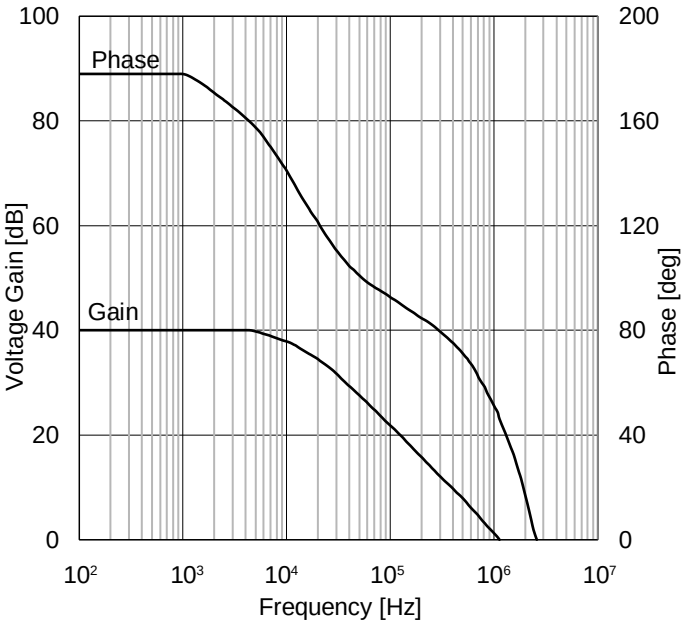


Figure 29. Voltage Gain/Phase vs Frequency (V_{DD}=3.0 V)

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Application Information

NULL method condition for Test Circuit 1

V_{DD}, V_{SS}, E_K, V_{ICM}, V_{RL}, Unit: V

Parameter	V_F	SW1	SW2	SW3	V_{DD}	V_{SS}	E_K	V_{ICM}	V_{RL}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	3	0	-1.5	3	-	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3	0	-0.5	1.5	1.5	2
	V_{F3}						-2.5			
Common-mode Rejection Ratio (Common-mode Input Voltage Range)	V_{F4}	ON	ON	OFF	3	0	-1.5	0	-	3
	V_{F5}							3		
Power Supply Rejection Ratio	V_{F6}	ON	ON	OFF	1.8	0	-0.90	0	-	4
	V_{F7}				5.5		-2.75			

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \quad [V]$$

2. Large Signal Voltage Gain (A_V)

$$Av = 20\mathrm{Log} \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \quad [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20\mathrm{Log} \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4} - V_{F5}|} \quad [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20\mathrm{Log} \frac{\Delta V_{DD} \times (1+ R_F/R_S)}{|V_{F6} - V_{F7}|} \quad [dB]$$

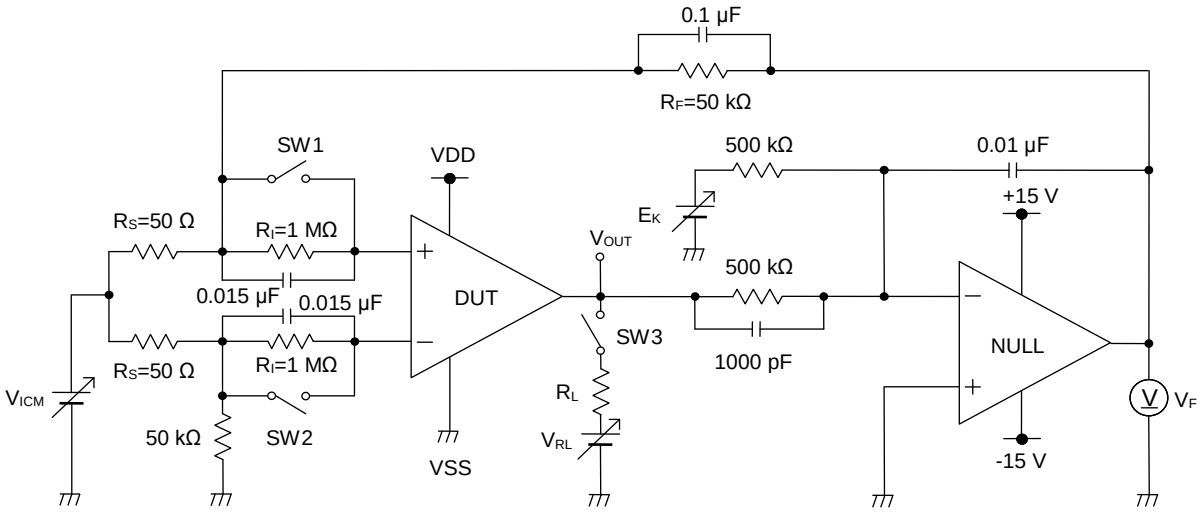


Figure 30. Test Circuit 1

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Application Information - continued

Switch Condition for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (High/Low)	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Gain Bandwidth Product	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

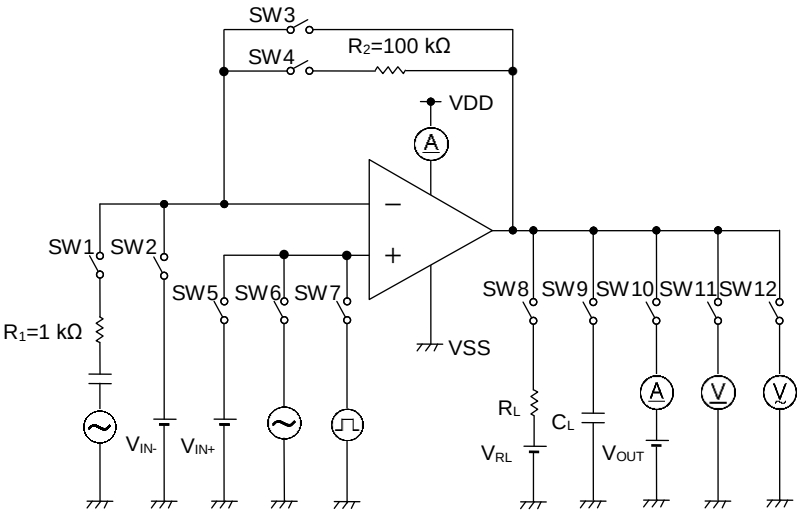


Figure 31. Test Circuit 2

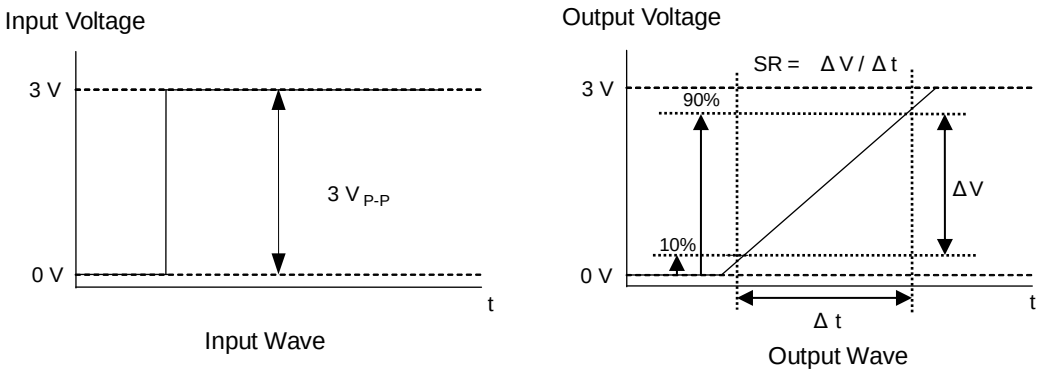


Figure 32. Slew Rate

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Application Information – continued

1. Unused Circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 33, set the non-inverting input pin to a potential within the Common-mode Input Voltage Range (V_{ICM}).

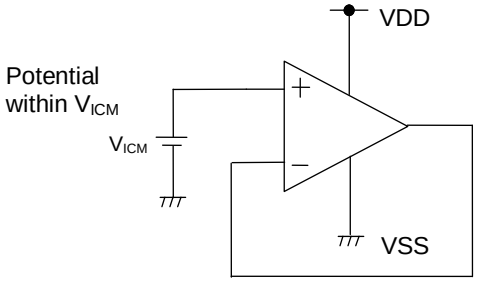


Figure 33. Example of Application Circuit for Unused Op-amp

2. Input Voltage

Applying V_{SS}-0.3V to V_{DD}+0.3V to the input pin is possible without causing deterioration of the electrical characteristics or destruction. However, this does not ensure normal circuit operation. Note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3. Power Supply (Single/Dual)

The operational amplifier operates when the voltage supplied is between the VDD and VSS pin. Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

4. Latch-up

Do not set the voltage of the input/output pin to V_{DD} or more and V_{SS} or less because there is a possibility of latch-up state peculiar to the CMOS device. Also, be careful that the abnormal noise and etc. are not added to the IC.

5. Decoupling Capacitor

Insert the decoupling capacitance between VDD and VSS, for stable operation of operational amplifier.
If a decoupling capacitor is not inserted, malfunction may occur due to power supply noise.

6. Start-up the Supply Voltage

This IC has ESD protection diode between input pin and the VDD and VSS pin. When apply the voltage to input pin before start-up the supply voltage, then a current flows in VDD or VSS pin through this diode. The current is depending on applied voltage. This phenomena causes breakdown the IC or malfunction. Therefore, give a special consideration to input pin protection and start-up order of supply voltage.
Also, after turning on the power supply, this IC outputs High level voltage regardless of the state of input up to around 1 V of the start-up voltage of the circuit. Pay attention to the sequence of turning on the power supply and the etc., because there is a possibility of the set malfunction.

7. Output Capacitor

When the VDD pin is shorted to the VSS(GND) potential with the electric charge accumulated in the external capacitor connected to the output pin, the accumulated electric charge passes through the parasitic element or protective element inside the circuit and is discharged to the VDD pin, the elements inside the circuit may be damaged.(Thermal destruction)
If use this IC as an application circuit which does not cause the oscillation phenomenon due to output capacitive load (e.g., a voltage comparator not constituting a negative feedback circuit), the capacitor connected to the output pin should be 0.1 µF or less in order to prevent the damage of IC due to accumulated charge of it.

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Application Information – continued

8. Oscillation by Output Capacitor

When designing an application circuit which constitutes a negative feedback circuit using this IC, check sufficiently about oscillation by capacitive load.
When the amplifier is used with a full feedback loop, a capacitive load must be up to 100 pF because there is a risk of oscillation.
The following figures show the frequency characteristics for each load capacitance.

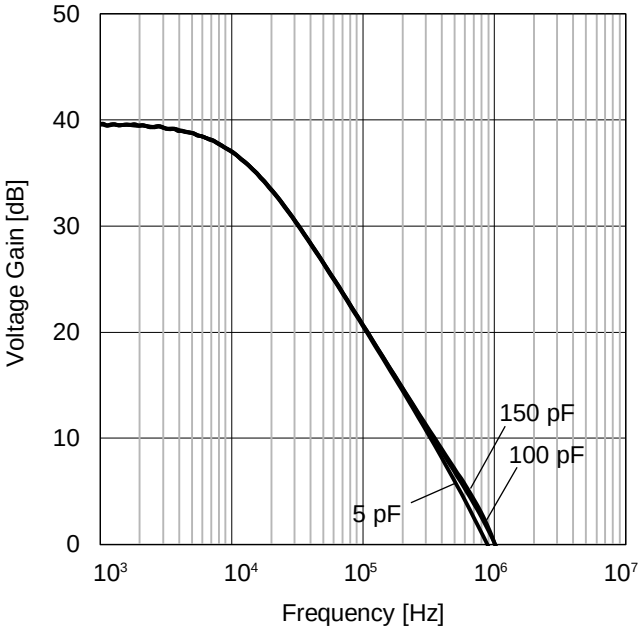


Figure 34. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=40 dB)

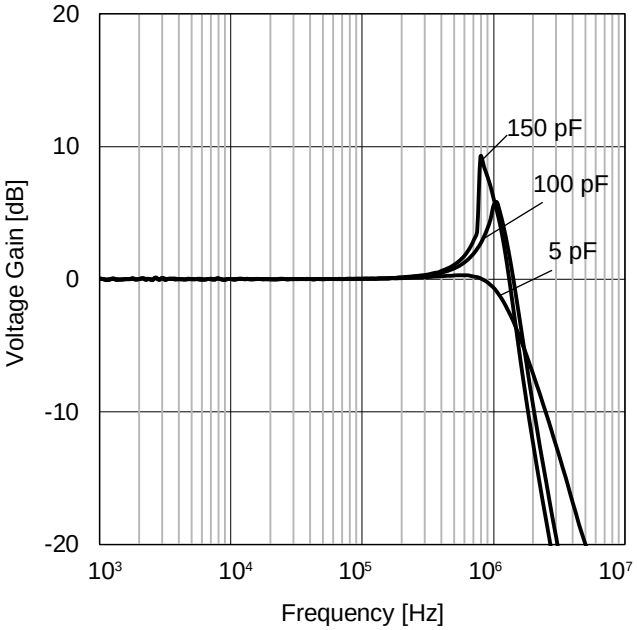


Figure 35. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB)

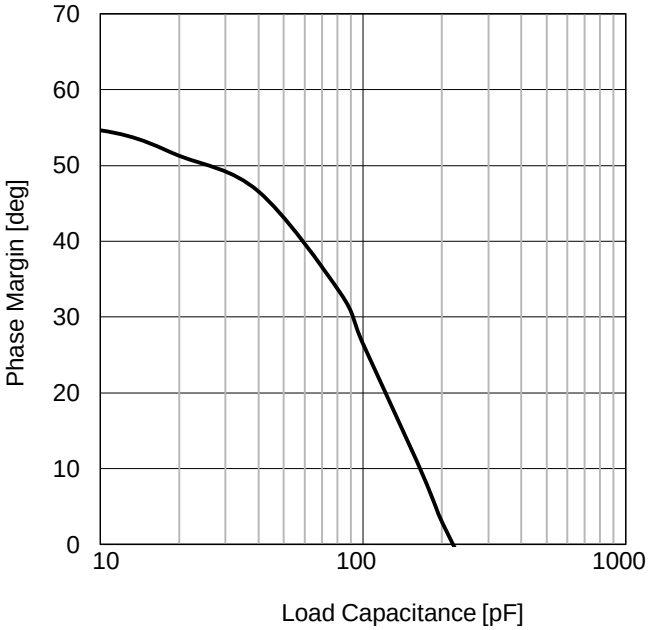


Figure 36. Phase Margin vs Load Capacitance
(V_{DD}=3.0 V, G_V=40 dB)

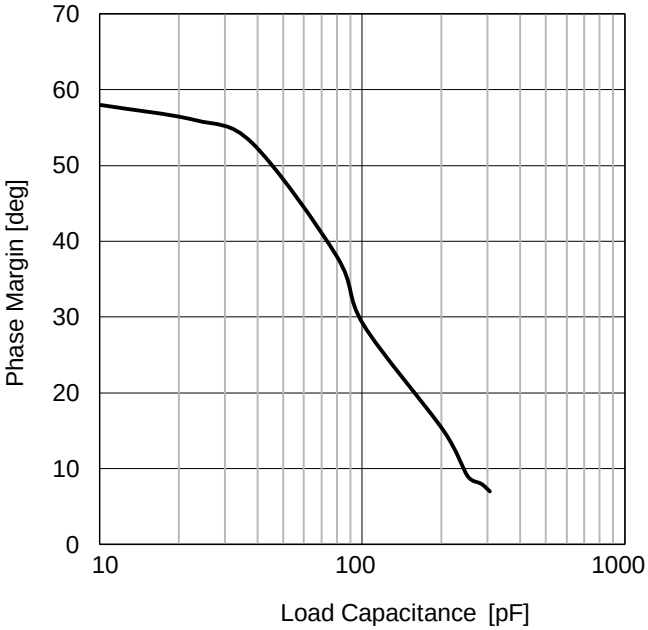


Figure 37. Phase Margin vs Load Capacitance
(V_{DD}=3.0 V, G_V=0 dB)

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8. Oscillation by Output Capacitor – continued

The following figure shows an improved circuit example of the frequency characteristics due to the output capacitor.

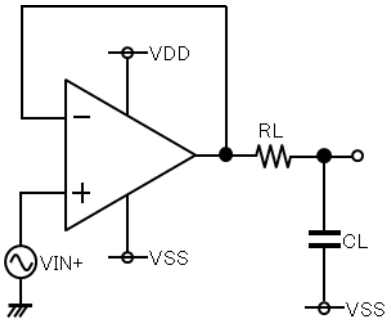


Figure 38. Improvement Circuit Example 1

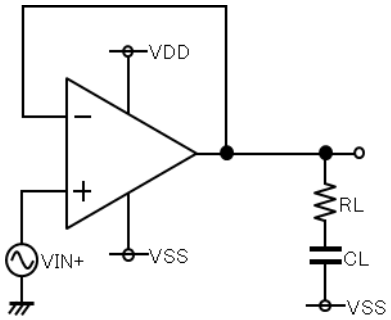


Figure 39. Improvement Circuit Example 2

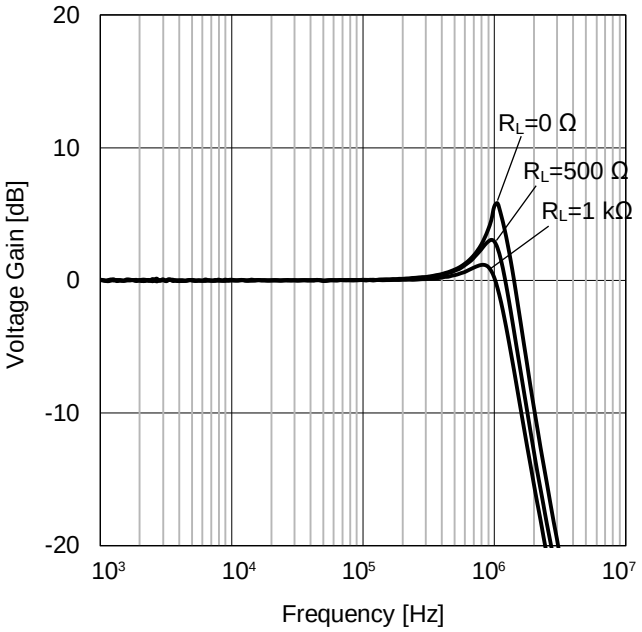


Figure 40. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB, C_L=100 pF, Circuit: Figure38)

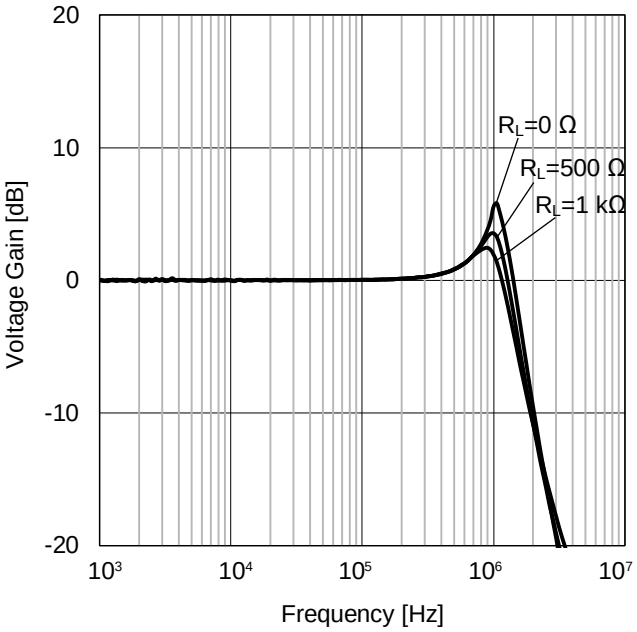


Figure 41. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB, C_L=100 pF, Circuit: Figure39)

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Examples of Circuit

○Voltage Follower

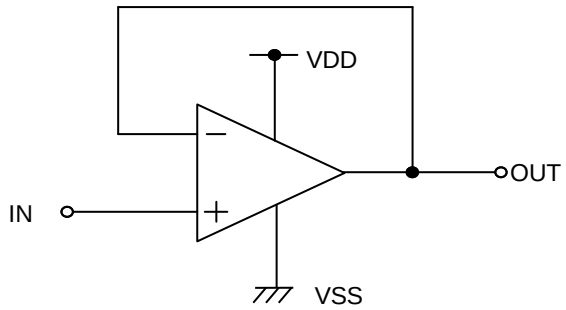


Figure 42. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$V_{OUT}=V_{IN}$

○Inverting Amplifier

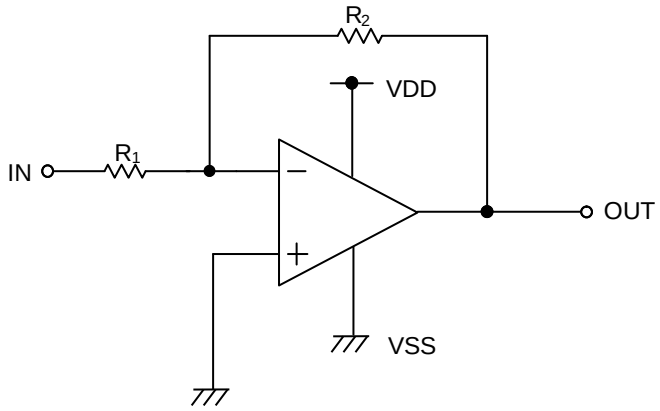


Figure 43. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain and depends on the ratio of R_1 and R_2. The out-of-phase output voltage is shown in the next expression

$V_{OUT}=-(R_2/R_1)V_{IN}$

This circuit has input impedance equal to R_1.

○Non-inverting Amplifier

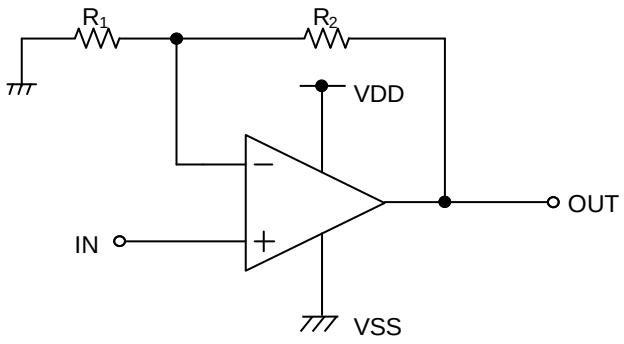


Figure 44. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_1 and R_2. The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$V_{OUT}=(1 + R_2/R_1)V_{IN}$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

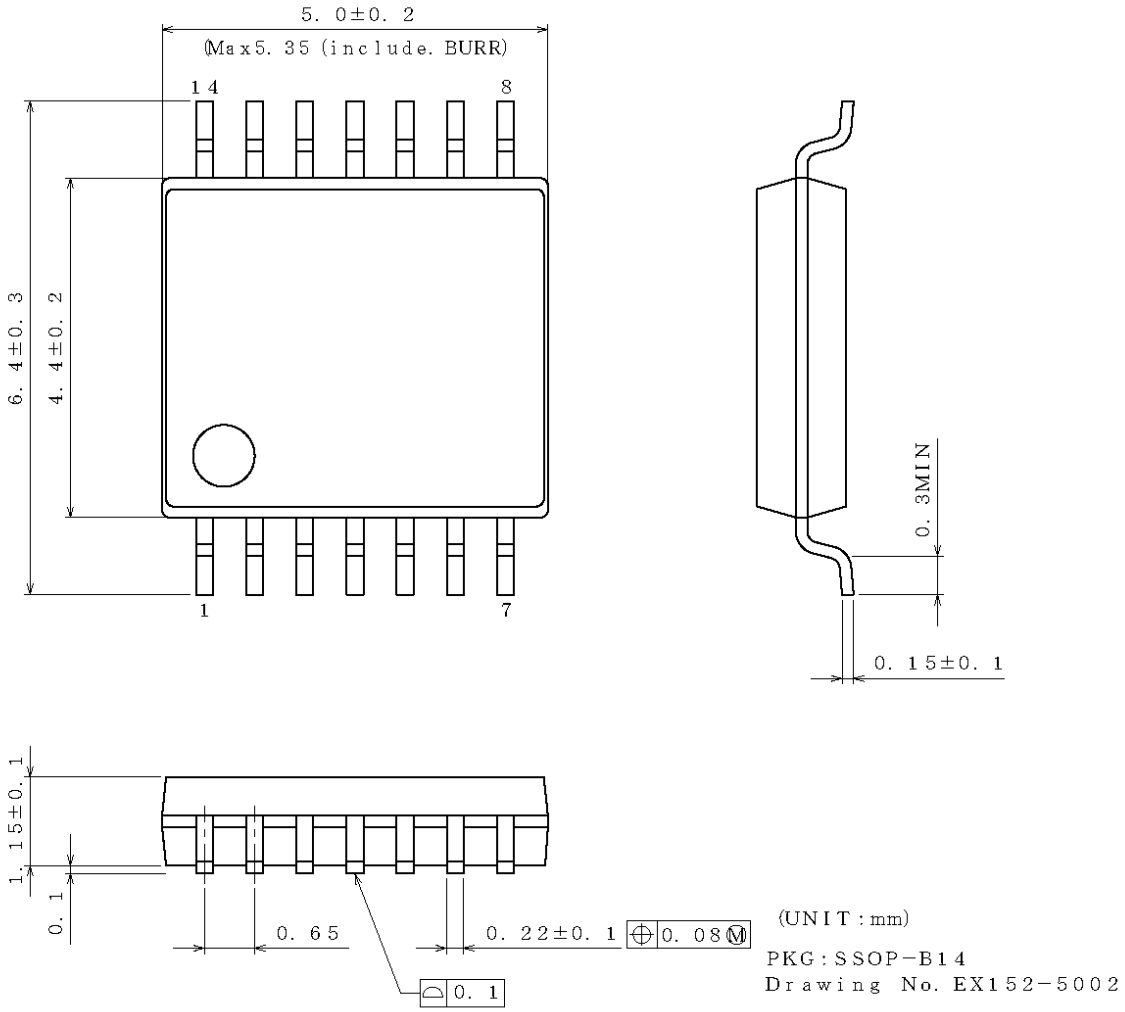
11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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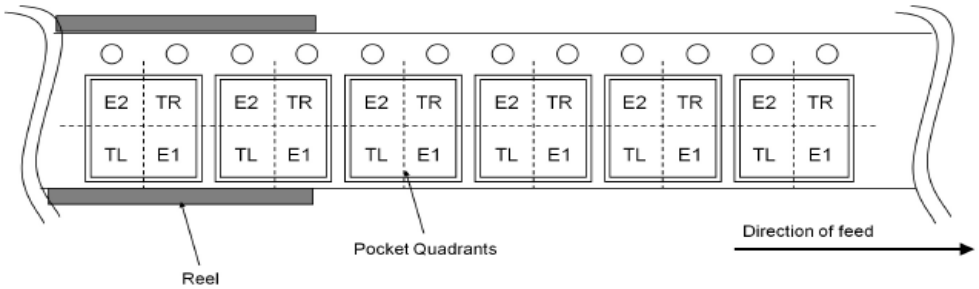
Physical Dimension and Packing Information

Package Name	SSOP-B14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Ordering Information

B U 7 2 4 4 Y F V	-	C E 2

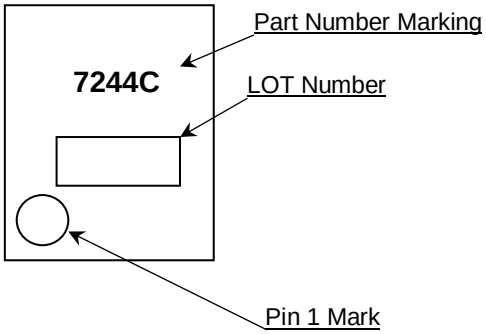
Part Number
BU7244YFV

Package
FV:SSOP-B14

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed Tape and Reel

Marking Diagram

SSOP-B14(TOP VIEW)



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Revision History

Date	Revision	Changes
27.Dec.2017	001	New Release
06.Aug.2019	002	Fix Pin Configuration.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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