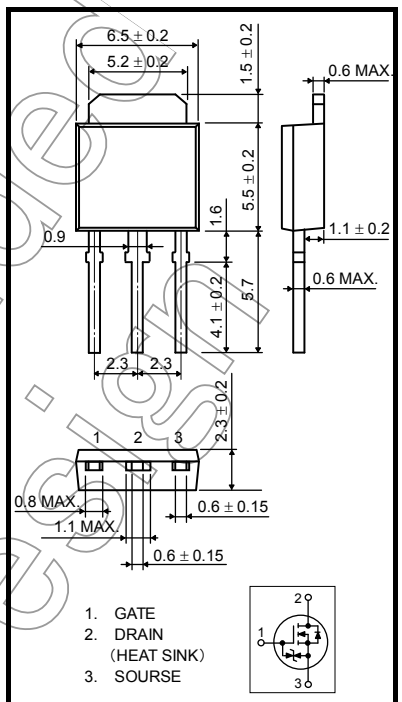
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (π−MOS V)

2SK4020

Chopper Regulators, DC-DC Converters and Motor Drive Applications

- 4-V gate drive
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 0.56 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 4.5 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 200 V)
- Enhancement mode: V_{th} = 1.5 to 3.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-7J2B

Weight: 0.36 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	200	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	200	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	5	A
	Pulse (Note 1)	I_{DP}	20	A
Drain power dissipation (Tc = 25°C)		P_D	20	W
Single-pulse avalanche energy (Note 2)		E_{AS}	65	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 3)		E_{AR}	2	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	6.25	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	125	°C / W

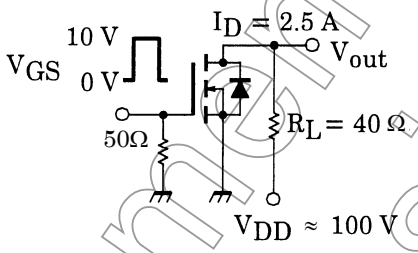
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 4.2 mH, R_G = 25 Ω, I_{AR} = 5 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

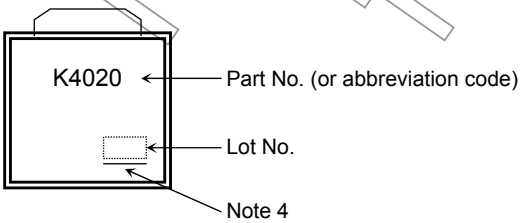
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	200	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	V
Drain−source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 2.5 A	—	0.56	0.8	Ω
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2.5 A	2.0	4.5	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	440	—	pF
Reverse transfer capacitance		C_{rss}		—	35	—	
Output capacitance		C_{oss}		—	120	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	20	—	
	Fall time	t_f		—	15	—	
	Turn-off time	t_{off}		—	60	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ 100 V, V_{GS} = 10 V, I_D = 5 A	—	10	—	nC
Gate−source charge		Q_{gs}		—	6	—	
Gate−drain (“Miller”) Charge		Q_{gd}		—	4	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 5 A, V_{GS} = 0 V	—	—	−2.0	V
Reverse recovery time	t_{rr}	I_{DR} = 5 A, V_{GS} = 0 V, dI_{DR} / dt = 100 A / μs	—	150	—	ns
Reverse recovery charge	Q_{rr}		—	0.45	—	μC

Marking

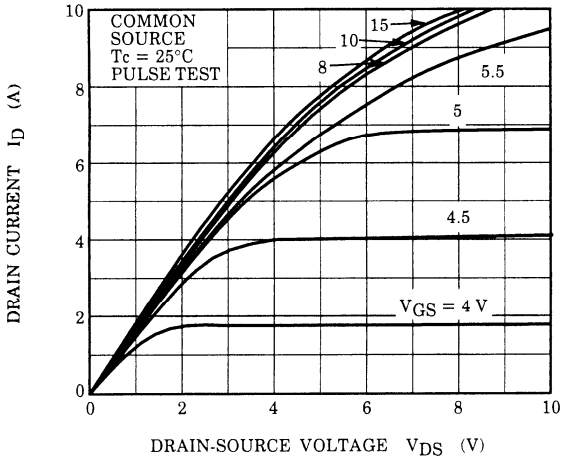


Note 4: A line under a Lot No. identifies the indication of product Labels.

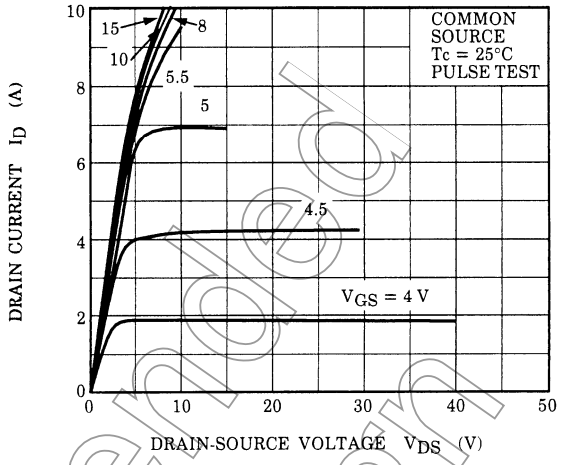
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

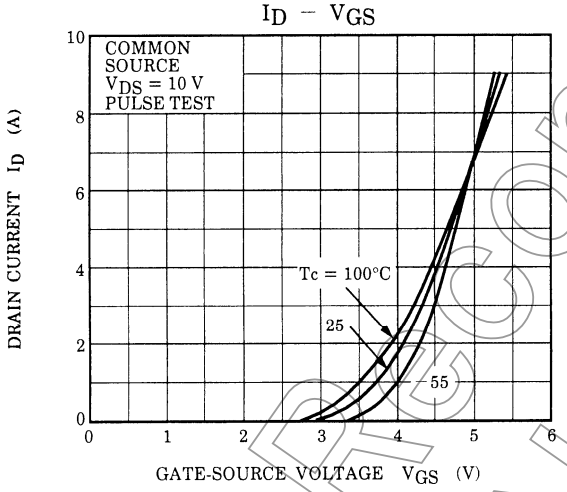
$I_D - V_{DS}$



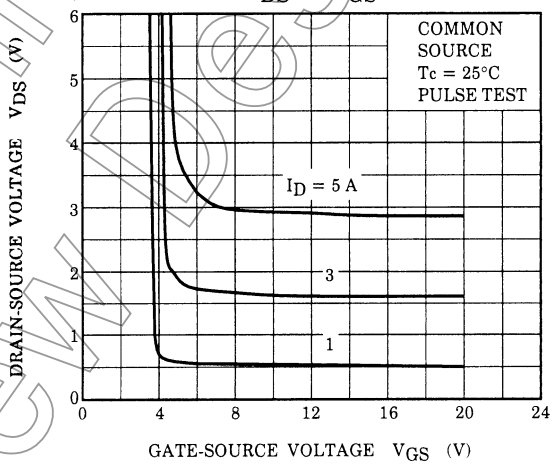
$I_D - V_{DS}$



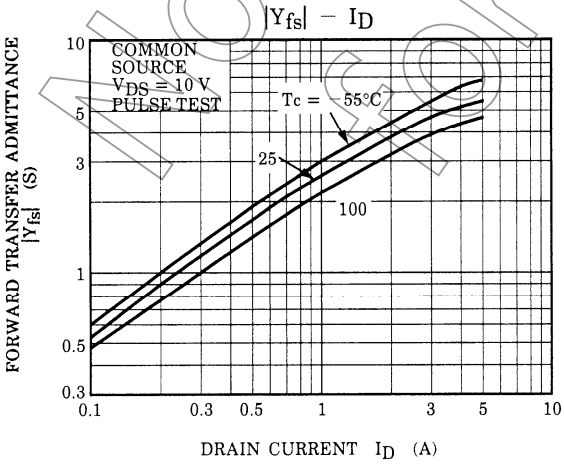
$I_D - V_{GS}$



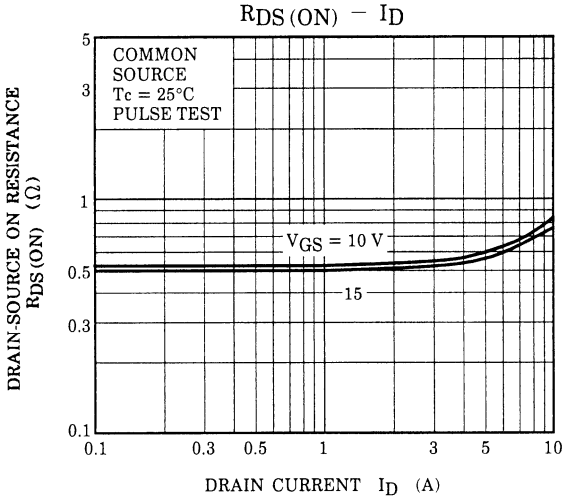
$V_{DS} - V_{GS}$



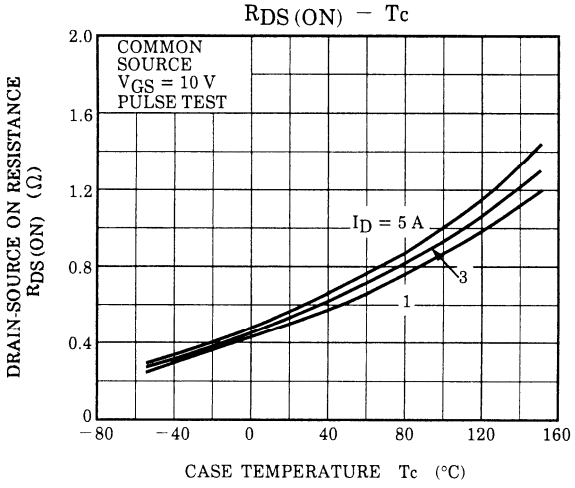
$|Y_{fs}| - I_D$



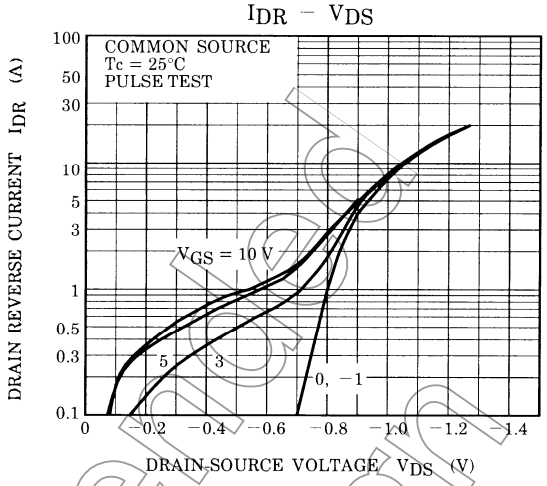
$R_{DS\,(ON)} - I_D$



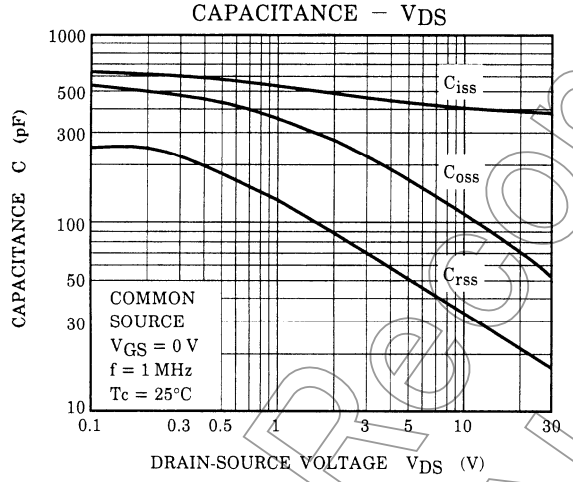
$R_{DS\,(ON)}$ – Tc



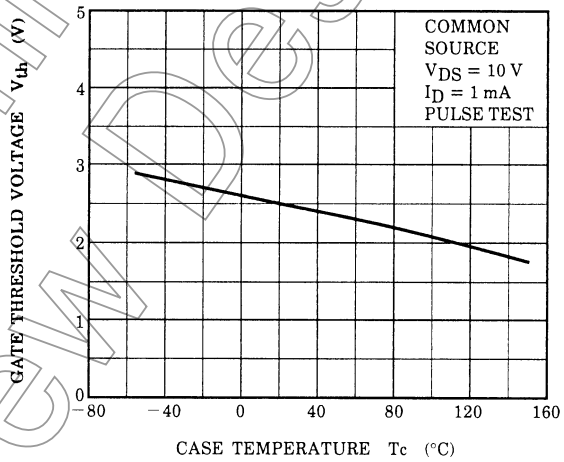
I_{DR} – V_{DS}



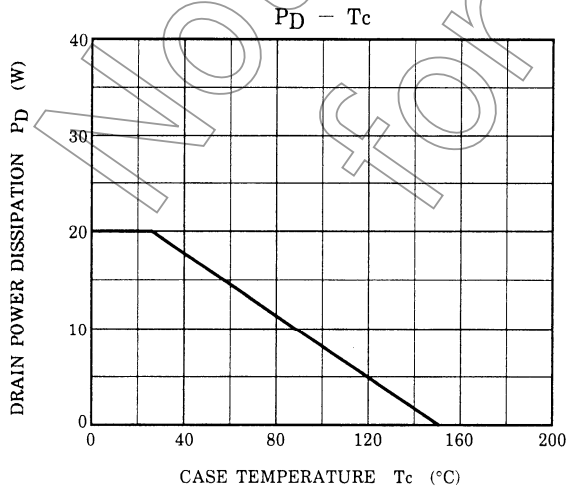
CAPACITANCE – V_{DS}



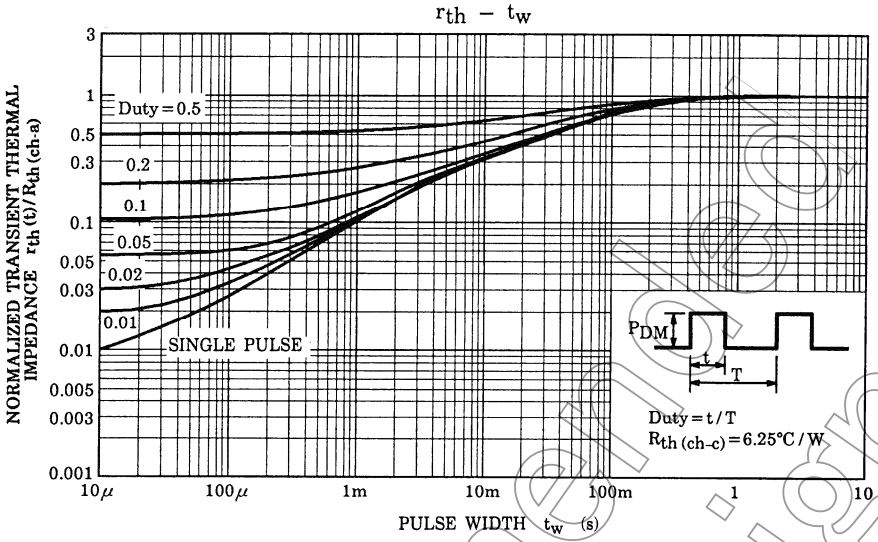
V_{th} – Tc



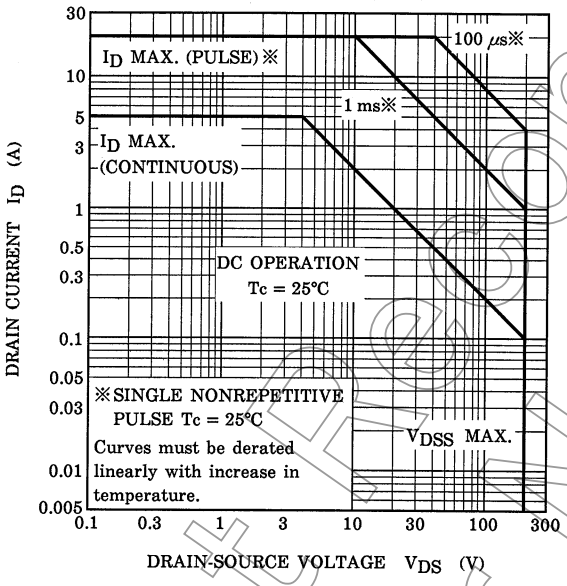
P_D – Tc



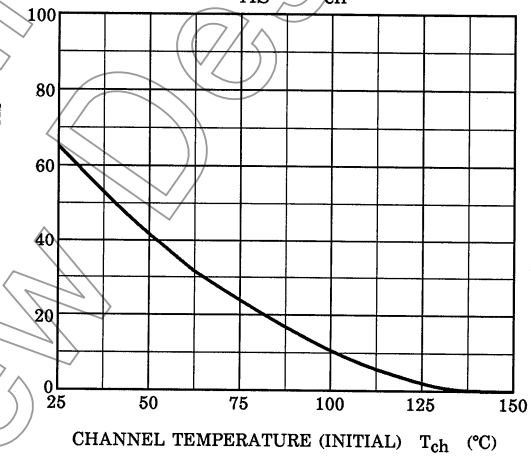
r_{th} – t_w

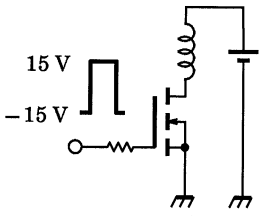


SAFE OPERATING AREA

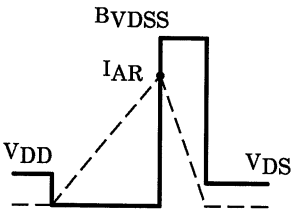


EAS – T_{ch}





TEST CIRCUIT



WAVE FORM

R_G = 25 Ω
V_{DD} = 25 V, L = 4.2 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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