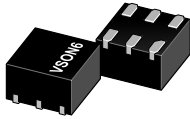


Programmable magnetic switch



Features

- Standalone switch functionality (no external MCU required) with ultra-low power consumption down to 48 nA
- Threshold selection 3-state hardware pin
- Threshold selection data bit(s) in an I²C accessible register
- Sample rate selection 3-state hardware pin
- Sample rate selection data bit(s) in an I²C accessible register
- Mode selection hardware pin to select between standalone or I²C serial interface
- Mode selection data bit(s) in an I²C accessible register
- Two outputs indicate the state of the switch:
 - Binary state hardware pin
 - Binary state data bit(s) in an I²C accessible register

Applications

- **Electronic system wake-up:** To automatically wake an electronic device when its magnet-equipped package is opened.
- **Laptop lid open / closed:** To trigger an action when a magnet-equipped lid of a laptop is opened or closed.
- **Door or window open / closed:** To trigger an action when a window or door opens or closes, or to check whether it is currently open or closed.

Description

The NMH1000 is a hall effect magnetic field switch. The switch is most sensitive to a vertical field passing through the top-to-bottom surfaces, orthogonal to the plane of the application printed circuit board. The switch operates at low voltage, low current, low output data rate, and is a small physical size.

1 Ordering information

Table 1. Ordering information

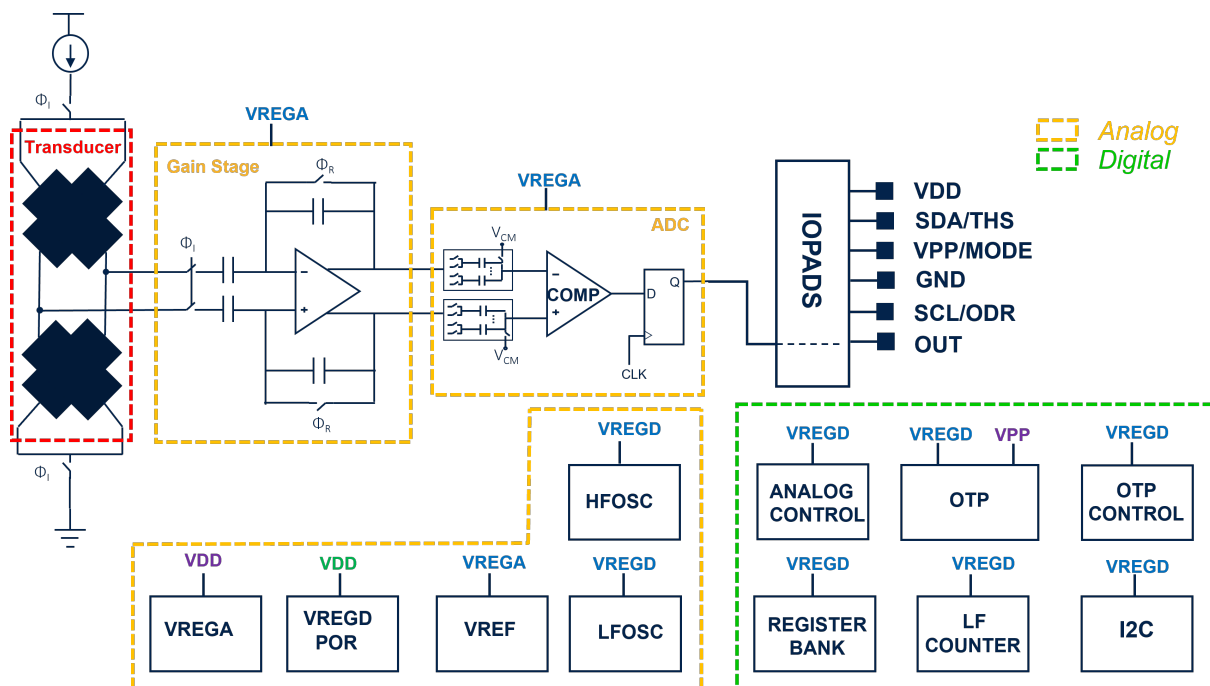
Type number	Package	
	Name	Description
NMH1000	VSON	Very thin small outline package, no leads, 6 terminals, 0.5 mm pitch, 1.4 mm x 1.4 mm x 0.85 mm body

Refer to AN6533 ^[1] for additional information regarding use-case design and manufacturing recommendations.

2 Block diagram

The device consists of a monolithic die holding a Hall effect transducer, conversion, and comparison chain. Supporting blocks are described in [Section 2.1: Block descriptions](#).

Figure 1. Block diagram



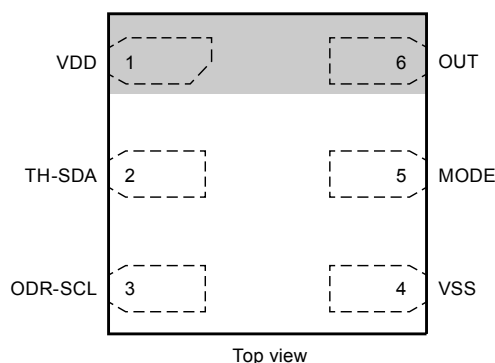
2.1 Block descriptions

- **Transducer:** A hall effect transducer which generates a small charge which is proportional to the proximal magnetic flux density.
- **Analog blocks:**
 - **HF and LF Oscillator:** Configurable frequency (f_{HFO} and f_{LFO}) RC-Relaxation oscillators with independent trim bits for trimming.
 - **Regulators and references:** Regulators to step down the external supply for analog and digital circuits. Bandgap reference and current reference for biasing all analog module.
 - **Gain Stage:** Amplifies the signal from the transducer
 - **ADC:** Converts the analog signal from the gain stage into digital
- **Digital blocks:**
 - **Analog Control:** Control signal generation for regulators and references, gain stage, ADC, oscillators, for example, based on different operational modes.
 - **OTP:** A 16 x 8 bit One Time Programmable array, it requires an external voltage (V_{PPTM}) for programming.
 - **OTP Control:** Generates the signals required to program and read the OTP array.
 - **Register bank:** Provides the registers where users can write configurations or read status values.
 - **LF counter:** Counts the specific time depending on the sample rate (ODR) set by the user.
 - **I²C:** Serial digital communications interface. Includes the address decode logic and interrupt functions.

3 Pinning information

3.1 Pinning

Figure 2. Pin configuration



aaa-040640

Note: Gray area denotes the end of the device where pin 1 is located.

3.2 Pin description

The package and pin assignments are illustrated in Figure 2. In standalone mode, the circuit measures the impedances of the TH-SDA and ODR-SCL pins relative to V_{DD} and V_{SS} to select the absolute magnetic threshold and output sample rate, respectively.

Table 2. Pin description

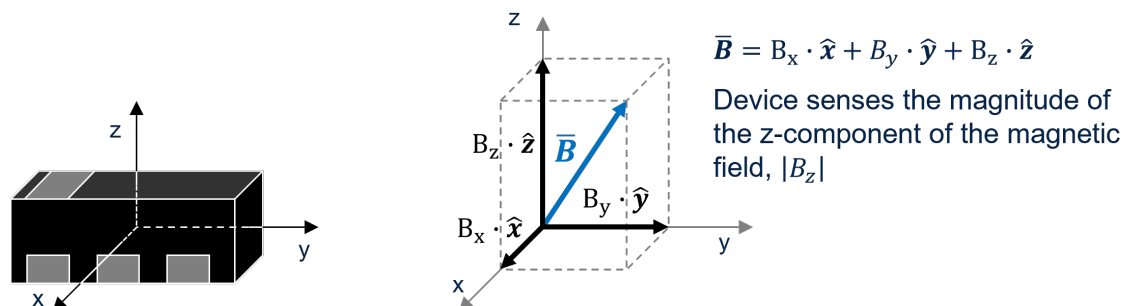
Symbol	Pin	Type	Description
V_{DD}	1	Supply	DC supply voltage
TH-SDA ⁽¹⁾	2	I/O	Standalone mode: Input that selects the threshold I ² C user mode: I ² C serial data
ODR-SCL ⁽²⁾	3	I	Standalone mode: Input that selects the sample rate I ² C user mode: I ² C serial clock
V_{SS}	4	Ground	Main ground
MODE ⁽³⁾	5	I	Selects between Standalone or I ² C modes.
OUT	6	O	Standalone mode: Output asserted high in the absence of a magnetic field and low when exposed to a field of sufficient magnitude I ² C user mode: same as standalone mode but output polarity is selectable

1. Tie to V_{SS} , float, or tie to V_{DD} to select medium, low, or high absolute magnetic threshold, respectively
2. Tie to V_{SS} , float, or tie to V_{DD} for medium, low, or high output sample rate, respectively.
3. Tie to V_{SS} for standalone, tie to V_{DD} for I²C User mode

3.3 Orientation

The NMH1000 senses the component of the magnetic field that is perpendicular to the package surface. In Figure 3, this is B_z .

Figure 3. Magnetic field sensitivity vs. package orientation



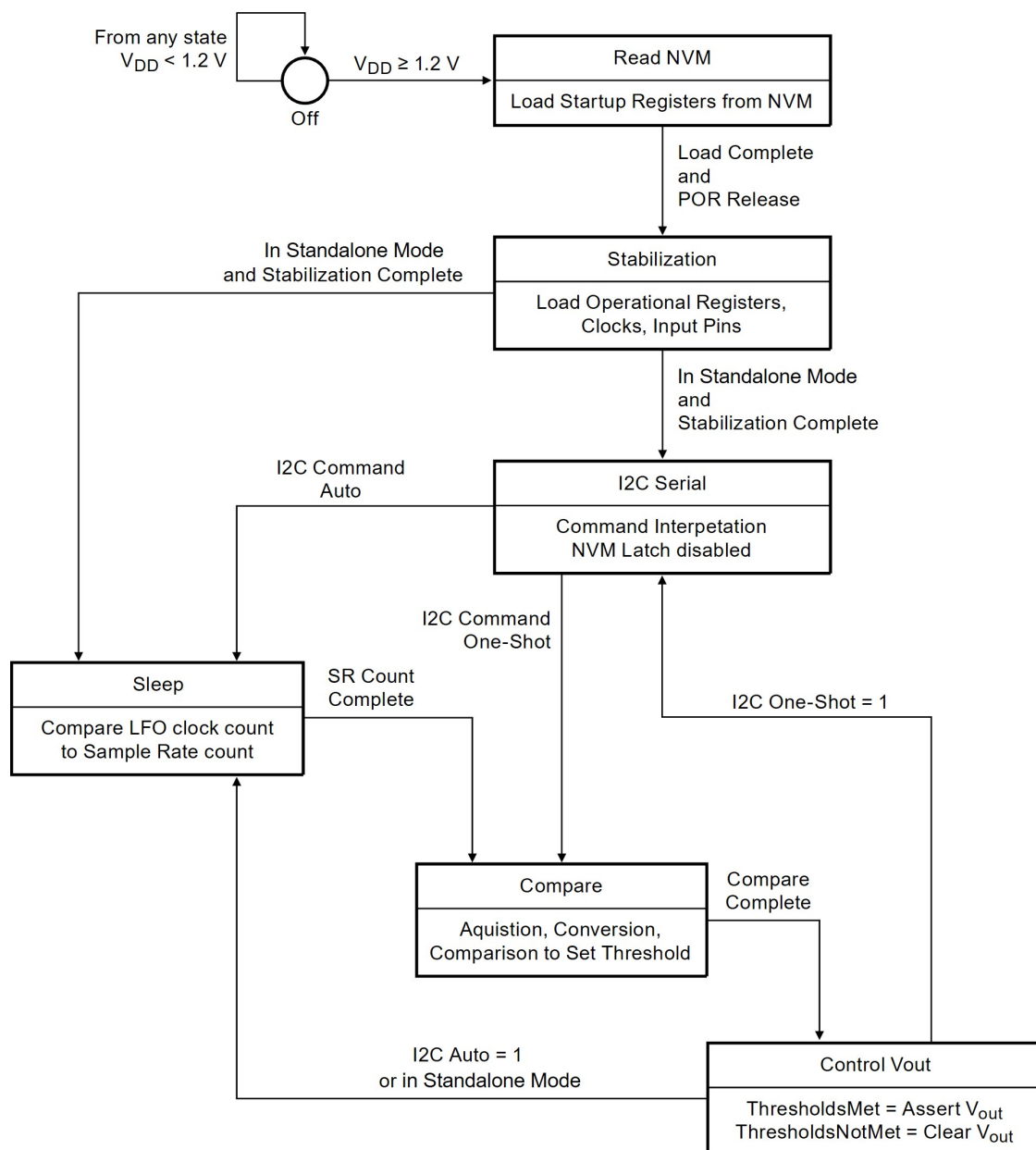
4 Functional description

4.1 Operating modes

4.1.1 Functional states

Figure 4 illustrates the functional states that the device transitions between.

Figure 4. NMH1000 functional state flow diagram



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4.1.2 Operational modes

At power-up, the voltage present on the MODE pin determines which operating mode the device enters. If the logical state of the pin is low, the device enters standalone mode. If high, it enters I²C mode.

4.1.2.1 Standalone mode

The device uses an internal timer to periodically wake up, measure, and update its output status before returning to sleep. The wakeup period and magnetic detection threshold are configured at power-up by sensing how the ODR-SCL and TH-SDA pins are wired. The I²C serial communications link is not active. The only output is the logical state of the hardware output pin OUT.

4.1.2.2 I²C mode

The I²C serial communications link is active making it possible for an external host device to configure the device and read its output and status as necessary.

In addition to the digital output, the hardware output pin, OUT, is available and active. It's the same as it is in standalone mode with one notable difference: the polarity is not fixed. It can be inverted.

In I²C mode, the device can be configured to run autonomously like it could in standalone mode. However, unlike in standalone, the user has much finer control of the magnetic thresholds and sample rates.

A one-shot mode is also available. In this mode, the device only takes measurements only when commanded via the digital interface.

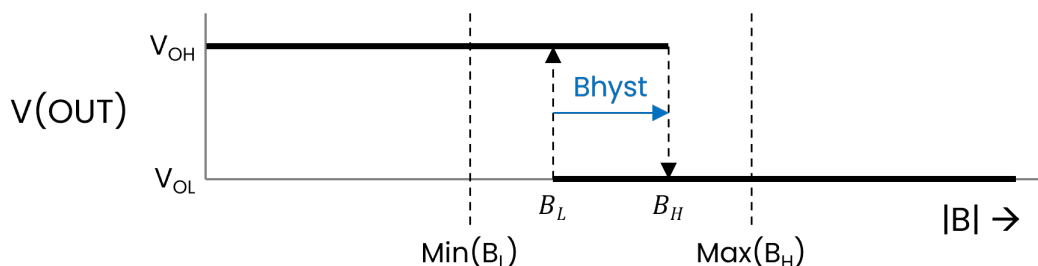
A device that is operating in I²C mode can transition to standalone by writing 1 to I2C_DIS.

4.2 Threshold configurations

4.2.1 In standalone mode

The following figure shows a parametrized transfer characteristic in standalone mode. The independent axis is magnitude of the z-component of the magnetic field while the dependent axis is the voltage on the output pin.

Figure 5. Output pin voltage vs. abs. magnetic field in standalone mode



In the figure, parameters B_H and B_L denote the high and low edges of the hysteresis loop. B_{hyst} is defined as the width of the hysteresis loop, $B_H - B_L$.

B_H and B_L exhibit minor deviations from device to device. $Max(B_H)$ represents the maximum value of B_H of the population of all devices. For magnetic fields that exceed $Max(B_H)$, the output is guaranteed to be low on all devices. Similarly, $Min(B_L)$ is the minimum value of B_L for the population of all devices. For magnetic fields less than $Min(B_L)$, the output will be high on all devices.

In standalone mode, three fixed combinations of threshold and hysteresis are available as detailed in [Table 30. Magnetic transfer function characteristics](#). The selected configuration is determined by how the TH-SDA pin is wired.

[Table 3](#) details how the pin should be wired to select a specific range.

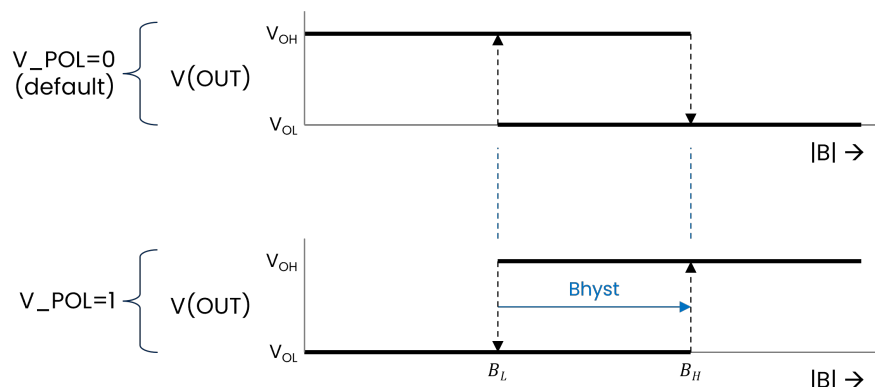
Table 3. Fixed threshold selection

TH-SDA Pin Connection	Max. Abs. High Threshold, "Max(B_H)"	Min. Hysteresis, Min(B_{hyst})
No connection, i.e. <i>floating</i>	Low, 100 G	20 G
Wire to V_{SS}	Medium, 160 G	
Wire to V_{DD}	High, 230 G	

4.2.2 In I²C mode

The following figure shows a parametrized transfer characteristic in I²C mode. The independent axis is magnitude of the z-component of the magnetic field while the dependent axis is the voltage on the output pin.

Figure 6. Output pin voltage vs abs. magnetic field in I²C mode



In I²C mode, the response is similar to standalone mode except for the following two differences:

1. The B_H and B_L values are fully adjustable by writing to the `USER_HIGH_THRESH` and `USER_LOW_THRESH` registers, respectively. To avoid unexpected behavior, it is necessary to ensure that the value of `USER_HIGH_THRESH` is always greater than the value of `USER_LOW_THRESH`. Additionally, to avoid undesired output transitions due to random noise, the hysteresis should be set to a value that is sufficiently high. Refer to `Min(Bhyst)` in [Table 30. Magnetic transfer function characteristics](#).
2. The polarity of the output is selectable by `V_POL` bit.

In I²C mode, the user defined high-side threshold of the hysteresis loop is selected by writing to `USER_HIGH_THRESH` register in units of **0.875 Gauss/LSB**.

In I²C mode, the user-defined low-side threshold of the hysteresis loop is selected by writing to `USER_LOW_THRESH` register in units of **0.875 Gauss/LSB**.

4.3 Sample rate configurations

4.3.1 In standalone mode

In standalone mode, three fixed sample rates are available as detailed in [Section 7.3: Sample rates in standalone mode](#). The selected configuration is determined by how the ODR-SDL pin is wired.

Table 4. [Sample rate selection in standalone mode](#) details how the pin should be wired to select a specific sample rate.

4.3.1.1 Sample rate selection via ODR-SCL pin connection

Table 4. Sample rate selection in standalone mode

ODR-SCL Pin Connection	Sample Rate ⁽¹⁾
No connection, i.e. <i>floating</i>	Low, 0.1 Hz
Wire to VSS	Medium, 1 Hz
Wire to VDD	High, 10 Hz

1. See [Section 7.2: Clocks and rates](#)

4.3.2 In I²C mode

In I²C mode, the user-defined sample rate is selected by writing the USR_ODR[2:0] field in the USER_ODR register. Refer to [Section 7.4: Sample rates in I²C mode](#) for the control codes and resultant sample rates.

4.4 I²C serial data function description

4.4.1 I²C pin functions

Two signals support the I²C-bus:

- Serial Clock Line - SCL.
- Serial Data line - SDA.

SCL is input and used for clocking the data into or out from the SDA data line.

SDA is bidirectional and used for sending and receiving the data.

When the bus is free, both the lines idle high.

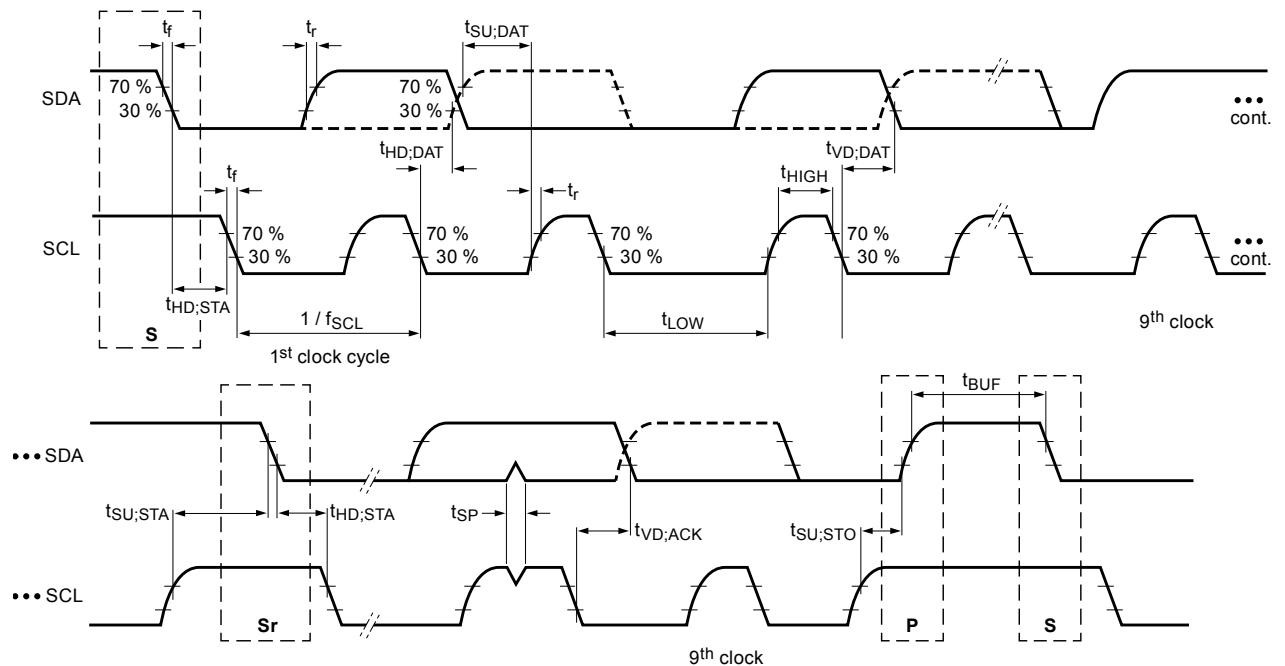
The I²C interface is compliant to the standard mode (100 kHz).

SDA and SCL both expect external pull-up resistors connected to V_{DD}.

- 1 kΩ minimum, board capacitance 20 pF maximum.

4.4.2 I²C timing diagram

Figure 7. I²C timing diagram



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4.4.3 I²C operation

The I²C transaction on the bus is initiated through a start condition (START) signal. START signal is defined as a HIGH to LOW transition on the SDA line while the SCL line is held HIGH. After START is transmitted by the host, the bus is considered busy. The next byte of data transmitted after START contains the device address in the first seven bits, and the eighth bit indicates whether the host is receiving data from the device or transmitting data to the device. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the host. The ninth clock pulse, following the device address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low for it to remain stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited because the internal addressing wraps after \$6D to \$00, continuing to \$6D again, then to \$00, and so forth. The wrapping applies to both write transfers and read transfers. Note that usable addresses stop at \$09, therefore a host may expect random values between \$0A to \$6D. If the host is unable to receive another complete byte of data until it has performed some other function, the host can hold the SCL line low, forcing the transmitter into a wait state. Data transfer continues only when the host is ready for another byte and releases the clock line.

A stop condition (STOP) is defined as a low to high transition on the SDA line while the SCL line is high. Data transfer is terminated by a STOP.

A host may also issue a RESTART during a data transfer. The device expects RESTARTs to randomly read from specific registers.

The bus logic of the device resets on receipt of a START, or RESTART condition. The device anticipates the sending of a device address, even if these START conditions are not positioned or follow proper format.

The device accepts the first bit of an address after each START, or RESTART condition.

The device detects when the SDA line is held low, and in such cases, releases the SDA line when the host issue no more than nine cycles of the SCL line.

The device determines the value in the NVM I²C address register. If the value is not \$00, the device uses this address during I²C transactions. If the address register is \$00, the address defaults to \$60. The reset value of the I²C address register is also \$60.

4.4.4 I²C protocol diagram

Figure 8. I²C write operation

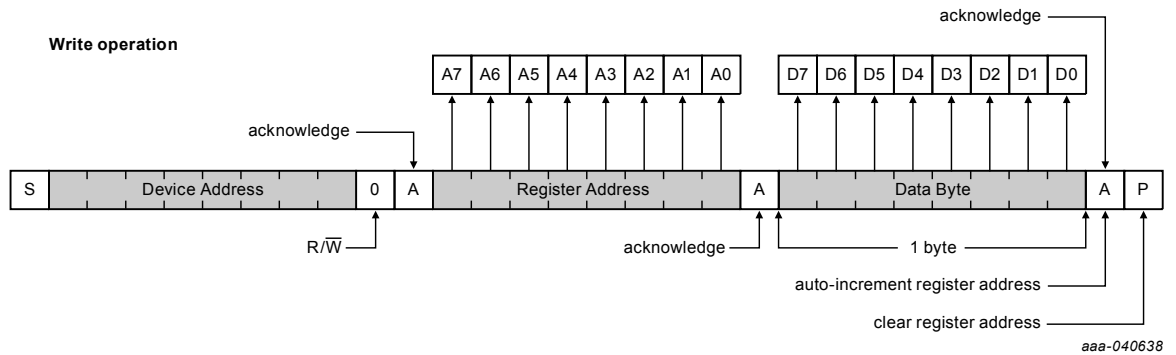
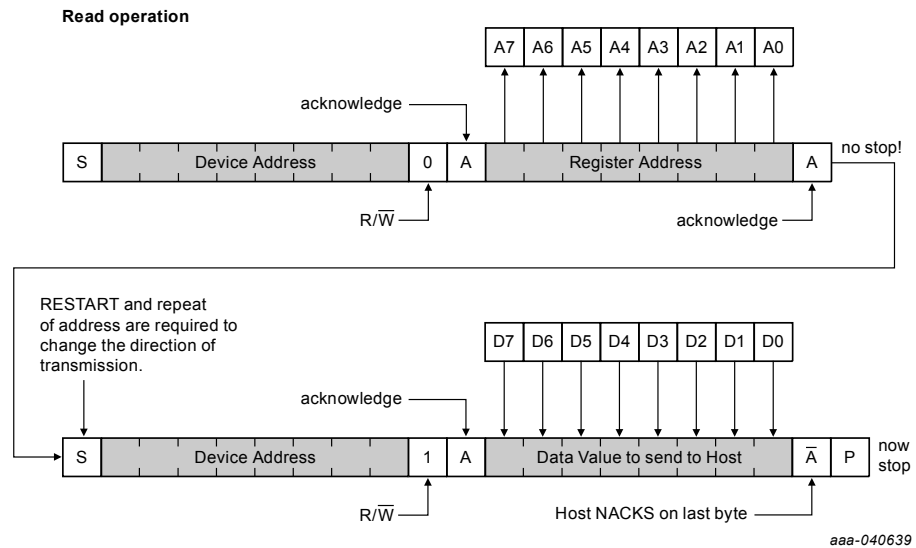


Figure 9. I²C read operation



4.5 Register map

4.5.1 Register overview

Table 5. Register map overview

Address	Name	Description	AO or S ⁽¹⁾	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00	STATUS	Status reporting of modes and selections	S	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	—
\$01	CONTROL_REG1	Control of Operations	S	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
\$02	—	Reserved	—	—	—	—	—	—	—	—	—
\$03	MAG_DATA	Magnitude of the magnetic field	S	MAG_DATA [7:0]							
\$04	USER_LOW_THRESH	User selectable low-side of the hysteresis loop	AO	USER_LOW_THRESH [7:0]							
\$05	USER_HIGH_THRESH	User selectable high-side of the hysteresis loop	AO	USER_HIGH_THRESH [7:0]							
\$06	USER_ODR	User selectable sleep sample output data rates	AO	—	—	—	—	—	USER_ODR[2:0]		
\$07	—	Reserved	—	—	—	—	—	—	—	—	—
\$08	WHO_AM_I	I ² C Configured Identifier	S	WHO_AM_I [7:0]							
\$09	I2C_ADDR	I ² C Configured Address - default after reset = \$60	S	—	ADDR [6:0]						

1. AO - Always On, S - Switched

4.5.2 Register details

4.5.2.1 Status reporting of modes and selections (STATUS) (\$00h)

Table 6. STATUS – Status reporting of modes and selections (address \$00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUTPUT	MDO	MDR	—	OPMODE	—	RST_STAT	—
Reset	1	0	1	—	1	—	1	—
Access	R	R/W	R/W	—	R	—	R	—

Table 7. STATUS – Status reporting of modes and selections (address \$00h) bit descriptions

Bit	Symbol	Access	Value	Description
7	OUTPUT	R		This bit mirrors the logical state of the OUT pin.
			0	The state of OUT is driven to low.
			1	The state of OUT is driven to high; Result of Reset.
6	MDO	R		Magnetic Data Overwrite is a flag used to indicate that the external host missed one, or more MAG_DATA samples, that is, a new a MAG_DATA sample overwrote prior data before it was read by the host. Once MDO is set, it stays set until it is explicitly cleared by the host writing a 0 to the MDO bit of the STATUS register.
			0	MAG_DATA overwrite not detected; Result of reset
			1	MAG_DATA overwrite detected
		W	0	MDO is cleared
			1	No effect. MDO status is unaffected

Bit	Symbol	Access	Value	Description
5	MDR			Magnetic Data Ready is a handshaking flag that an external host can use to collect the sequence of all MAG_DATA samples without replicating or missing any of the samples. MDR is set every time new measurement data is made available in the MAG_DATA register. Once MDR is set, it stays set until it is explicitly cleared by the host writing a 0 to the MDR bit of the STATUS register. In typical use, each time new MAG_DATA is read, the external host writes a 0 to the MDR bit the STATUS register to clear MDR. Subsequently, the host repeatedly polls the MDR flag until it sets which indicates new data is available. The host reads the new data, clears MDR, and repeats the process.
		R	0	MAG_DATA has not been updated since MDR was last cleared
			1	MAG_DATA has been updated since MDR was last cleared; Result of reset
		W	0	MDR is cleared
			1	No effect, MDR state is unaffected
3	OPMODE	R		The read-only OPMODE indicates the mode of the internal state-machine.
			0	Device is in standalone mode.
			1	Device is in I ² C user mode.
1	RST_STAT	R		RST_STAT is a flag that is set on any reset. Once set, it stays set and only clears on read of the STATUS register after an active reset sequence has completed. The flag can be used to detect unexpected reset events that require device re-initialization.
			0	No reset sequence has been initiated since the last time the RST_STAT flag was cleared.
			1	Since the last time the RST_STAT flag was cleared, one, or more, reset sequence(s) has been initiated; Result of reset.

4.5.2.2 Control of operations (CONTROL_Reg1) (\$01h)

Table 8. CONTROL_Reg1 – Control of operations(address \$01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	V_POL	I2C_DIS	AUTO	ONE_SHOT	—	RST
Reset	—	—	0	0	0	0	—	0
Access	—	—	R/W	R/W	R/W	R/W	—	R/W

Table 9. CONTROL_Reg1 – Control of operations (address \$01h) bit description

Bit	Symbol	Access	Value	Description
5	V_POL	R/W		V_POL provides control of the user-defined OUT pin assert / clear polarity.
			0	Assert: OUT pin low, Clear: OUT pin high; Result of reset.
			1	Assert: OUT pin high, Clear: OUT pin low.
4	I2C_DIS	R/W		I2C_DIS provides control of the operating mode "on-the-fly" after the device exits POR or Soft Reset. I2C_DIS allows the user to force the device into standalone mode from the I ² C mode. <i>Note: Writing 1 to I2C_DIS is a one-time-only operation. Bringing the device into I²C mode from standalone requires a full power cycle and release of POR.</i>
			0	Write to 0 has no effect; Read of 0 indicates I ² C mode; Result of reset.
			1	Write to 1 forces the device from I ² C mode to standalone mode; Read of 1 indicates a state machine fault, since the registers are only accessible in the I ² C mode.
3	AUTO			AUTO - Autonomous measurement mode: The device periodically wakes, takes a measurement, compares against thresholds, updates its outputs and returns to sleep. To avoid conflicts, the user should not initiate one-shot measurements when autonomous mode is enabled.

Bit	Symbol	Access	Value	Description
3	AUTO	R	0	Autonomous measurements are disabled, okay to trigger one-shot measurement
			1	Autonomous measurements are enabled
		W	0	Disable autonomous measurements
			1	Enable autonomous measurements
2	ONE_SHOT	R		ONE_SHOT – Single measurement mode: The device executes a single measurement cycle, compares against thresholds, updates its outputs, and then halts. The bit is automatically cleared once the sequence is complete. <i>Note: It is not recommended to trigger ONE_SHOT while AUTO mode is enabled.</i>
			0	One-Shot is not active; Result of reset.
		W	0	It has no effect.
			1	Triggers a one-shot sequence
0	RST	R/W		RST provides I ² C access to force an internal device soft reset:
			0	No reset is forced.
			1	Internal device reset is forced.

4.5.2.3 Magnetic strength report (MAG_DATA) (\$03h)

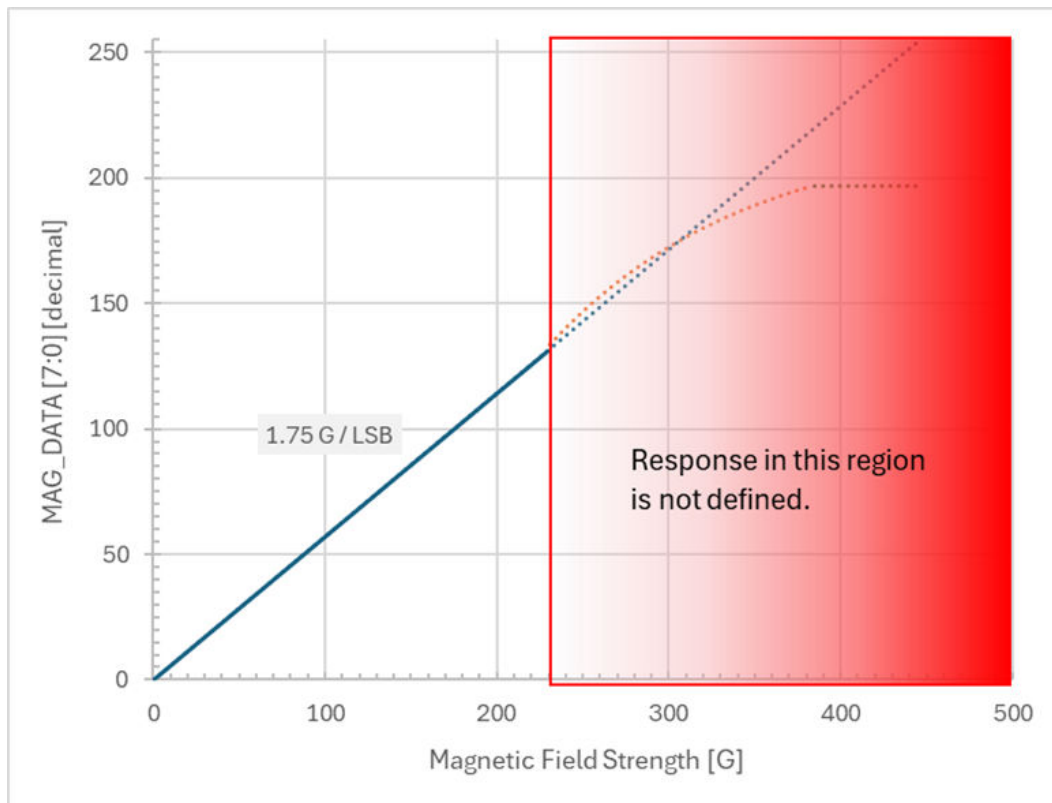
Table 10. MAG_DATA – Magnetic strength report (address \$03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MAG_DATA [7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: The resolution of MAG_DATA is **1.75 G/LSB**. The precision is limited to 3 counts (± 5.25 Gauss).

Table 11. MAG_DATA – Magnetic strength report (address \$03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	MAG_DATA	R/W		MAG_DATA[7:0] indicates the magnitude of the magnetic field strength in units of ΔB of 1.75 G/LSB.
			\$00	0 G; Result of reset.
			\$84	Highest in-range magnetic field strength (≈ 231 Gauss).

Figure 10. Guaranteed In-Spec Region of Operation


Note: The highest in range magnetic field is ≈ 231 Gauss, a reading of $\text{MAG_DATA}[7:0] = 0x84$. Above this field strength, the MAG_DATA register value will continue to trend upward, but neither the linearity nor the saturation level are defined in this region.

4.5.2.4 User selectable output, low threshold, N or S (USER_LOW_THRESH) (\$04h)

Table 12. USER_LOW_THRESH – User selectable output, low threshold, N or S (address \$04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	$\text{USER_LOW_THRESH}[7:0]$							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. USER_LOW_THRESH – User selectable output, low threshold, N or S (address \$04h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	USER_LOW_THRESH	R/W		In I²C mode, $\text{USER_LOW_THRESH}[7:0]$ provides the capability for the user to override the fixed threshold controlling the low-side of hysteresis loop, in units of B_{Δ} in G/LSB. Note: Hysteresis is controlled by appropriate user settings for both USER_LOW_THRESH and USER_HIGH_THRESH registers. Note: The sensitivity of the USER_LOW_THRESH register is fixed at 0.875 Gauss/LSB, unlike the MAG_DATA register, which uses a different scaling. Suppose you want to set the low-side of the hysteresis loop to 56 Gauss. Set USER_LOW_THRESH to 0x40 (64 Dec * 0.875 = 56 Gauss).
			\$00	0 G; Result of reset.

4.5.2.5 User selectable output, high threshold, N or S (USER_HIGH_THRESH) (\$05h)

Table 14. USER_HIGH_THRESH – User selectable output, high threshold, N or S (address \$05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USER_HIGH_THRESH [7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15. USER_HIGH_THRESH – User selectable output, high threshold, N or S (address \$05h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	USER_HIGH_THRESH	R/W		In I ² C mode, USER_HIGH_THRESH[7:0] provides the capability for the user to override the fixed threshold controlling the high-side of hysteresis loop, in units of B_{Δ} in G/LSB. Note: Hysteresis is controlled by appropriate user settings for both USER_ASSERT_THRESH and USER_CLEAR_THRESH registers. Note: The sensitivity of the USER_HIGH_THRESH register is fixed at 0.875 Gauss/LSB, unlike the MAG_DATA register, which uses a different scaling. Suppose you want to set the high-side of the hysteresis loop to 112 Gauss. Set USER_HIGH_THRESH to 0x80 (128 Dec * 0.875 = 112 Gauss).
			\$00	0 G; Result of reset.

4.5.2.6 User selectable sleep sample output data rates (USER_ODR) (\$06h)

Table 16. USER_ODR – User selectable sleep sample output data rates (address \$06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	—	—	—	—	USER_ODR[2:0]		
Reset	—	—	—	—	—	0	0	0
Access	—	—	—	—	—	R/W	R/W	R/W

Table 17. USER_ODR – User selectable sleep sample output data rates (address \$06h) bit description

Bit	Symbol	Access	Value	Description
2 to 0	USER_ODR	R/W		In I ² C mode, USER_ODR[2:0] provides the capability for the user to override the fixed sample rate controlling the sleep-compare-Vout cycle time.
			0 0 0	Low sample rate selected, 0.1 Hz.
			0 0 1	5 x Low sample rate selected, 0.5 Hz.
			0 1 0	Medium sample rate selected, 1 Hz.
			0 1 1	5 x Medium sample rate selected, 5 Hz.
			1 0 0	High sample rate selected, 10 Hz.
			1 0 1	5 x High sample rate selected, 50 Hz.
			1 1 0	10 x High sample rate selected, 100 Hz.
			1 1 1	Undefined.

4.5.2.7 I²C configured identifier (WHO_AM_I) (\$08h)

Table 18. WHO_AM_I - I²C configured identifier (address \$08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WHO_AM_I [7:0]							
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. WHO_AM_I - I²C configured identifier (address \$08h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	WHO_AM_I	R/W		WHO_AM_I[7:0] provides the device identification register. The value is programmed in the NVM at final test. Each variation has its own unique device ID.
			\$00	WHO_AM_I error condition.
			\$01	Generic open market default value.
			\$02 to \$FE	Customer defined unique values.
			\$FF	WHO_AM_I not programmed.

4.5.2.8 I²C configured identifier (I2C_ADDR) (\$09h)

Table 20. I2C_ADDR - I²C configured identifier (address \$09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—	I2C_ADDR [6:0]						
Reset	—	1	1	0	0	0	0	0
Access	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 21. I2C_ADDR - I²C configured identifier (address \$09h) bit description

Bit	Symbol	Access	Value	Description
6 to 0	I2C_ADDR	R/W		I2C_ADDR[6:0] is register mapped and loaded by default value \$60 at boot time. After that, users may write any non-zero value to it. This non-zero value is used until the device is reset. If the device is reset, the same default value of \$60 is reloaded and used again.
			\$60	\$60 = default loaded at exit of reset.
			\$00	\$00 = lowest address value.
			\$7F	\$7F = highest address value.

5 Limiting values

Table 22. Limiting values

Symbol	Description	Condition	Min	Typ	Max	Unit
B _G	Magnetic field	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	—	—	Not limited	G (Gauss)
V _{SUP}	V _{DD} to V _{SS} range	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	−0.3	—	3.6	V
V _{IO}	IO pin voltage, each pin vs V _{DD} / V _{SS}	T _A Min ≤ T _A ≤ T _A Max	V _{SS} − 0.3	—	V _{SUP} + 0.3	V
I _{IO}	IO pin current, each pin vs V _{DD} / V _{SS}	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	−10	—	10	mA
I _{SUBIO}	Substrate current injection, all IO pins, current from pin to V _{SS} − 0.3 V	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	—	100	—	mA
I _{LATCH}	Latch-up current, current to/from pin to V _{DD} /V _{DDA} + 0.3 V	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	−100	—	100	mA
ESD _{HBM}	Electrostatic discharge, Human Body Model (HBM) all pins	T _A = 25 °C, V _{DD} = 1.5 V	−2000	—	2000	V
ESD _{CDM}	Electrostatic discharge, Charged Device Model (CDM) all pins	T _A = 25 °C, V _{DD} = 1.5 V	−500	—	500	V
EOS _{EMIR}	Conducted immunity DPI, until OUT unintentionally changes state or I ² C corruption	T _A = 25 °C, V _{DD} = 1.5 V	—	30	—	dBm
T _{STG}	Unpowered storage temperature range	—	−40	—	150	°C

6 Recommended operating conditions

Table 23. Operating conditions

Symbol	Description	Condition	Min	Typ	Max	Unit
Transitions						
t_{OP}	Power-on initialization	From $V_{DD} > 1.2\text{ V}$ to Operation Ready; $25\text{ }^{\circ}\text{C}$ and 1.5 V .	—	4.8	5.1	ms
t_{BOC-A}	Cleared state to Asserted state phase delay	$T_A\text{ Min} \leq T_A \leq T_A\text{ Max}$, $V_{DD}\text{ Min} \leq V_{DD} \leq V_{DD}\text{ Max}$	—	100	—	μs
Voltages						
V_{DD}	Operating voltage range where Min = $V_{DD}\text{ Min}$, Typ = 1.5 V , Max = $V_{DD}\text{ Max}$	$T_A\text{ Min} \leq T_A \leq T_A\text{ Max}$	1.2	1.5	V_{SUP}	V
Temperatures						
T_A	Operating temperature range where Min = $T_A\text{ Min}$, Typ = $25\text{ }^{\circ}\text{C}$, Max = $T_A\text{ Max}$	$V_{DD}\text{ Min} \leq V_{DD} \leq V_{DD}\text{ Max}$	$-40\text{ }^{\circ}\text{C}$	25	+85	$^{\circ}\text{C}$

7 Characteristics

7.1 Supply currents

Table 24. Supply currents

Symbol	Description	Condition	Min	Typ	Max	Unit
$I_{\text{DDS-LODR}}$	Supply current, Low ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Low ODR stand-alone mode.	—	47.5	187	nA
$I_{\text{DDS-MODR}}$	Supply current, Medium ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the Medium ODR stand-alone mode	—	72.2	234	nA
$I_{\text{DDS-HODR}}$	Supply current, High ODR	Typical value is calculated by a time-weighted average of the consumption during the measurement and sleeping phases while in the High ODR stand-alone mode.	—	319.6	760	nA
$I_{\text{DDS-S}}$	Supply current, Sleep mode	Typ = 25 °C, $V_{\text{DD}} = 1.5 \text{ V}$ Max = T_{A} Min to T_{A} Max and V_{DD} Min to V_{DD} Max	—	42	300	nA
$I_{\text{DDS-M}}$	Supply current, measurement	Typ = 25 °C, $V_{\text{DD}} = 1.5 \text{ V}$ Max = T_{A} Min to T_{A} Max and V_{DD} Min to V_{DD} Max	—	580	650	μA
$I_{\text{DDS-2}}$	Supply current, I ² C command/response	Typ = 25 °C, 1.5 V, Max = T_{A} Min ≤ T_{A} ≤ T_{A} Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	35	45	μA

7.2 Clocks and rates

Table 25. Clocks and rates

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{LFO}	Low frequency oscillator	T_{A} Min ≤ T_{A} ≤ T_{A} Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	2.8	3.2	3.5	kHz
f_{HFO}	High frequency oscillator	T_{A} Min ≤ T_{A} ≤ T_{A} Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	1.7	2	2.3	MHz
f_{SCL}	I ² C input clock	T_{A} Min ≤ T_{A} ≤ T_{A} Max, V_{DD} Min ≤ V_{DD} ≤ V_{DD} Max	—	—	1	MHz

7.3 Sample rates in standalone mode

Table 26. Sample rates in standalone mode

Symbol	Mode	Rate	Min	Typ	Max	Unit
f_{ODR}	Standalone	Low	—	0.1	—	Hz
		Med.	—	1	—	
		High	—	10	—	

7.4 Sample rates in I²C mode

Table 27. Sample rates in I²C mode

Symbol	Mode	USER_ODR[2:0]	Min	Typ	Max	Unit
f _{ODR}	I ² C	000	—	0.1	—	Hz
		001	—	0.5	—	
		010	—	1	—	
		011	—	5	—	
		100	—	10	—	
		101	—	50	—	
		110	—	100	—	
		111	—	Undefined	—	

7.5 I²C pin thresholds

Table 28. I²C pin thresholds

Symbol	Description	Condition	Min	Typ	Max	Unit
V _{IH}	Digital high-level input voltage	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max at I _{IH} max	0.7 x V _{DD}	—	V _{DD} + 0.3	V
V _{IL}	Digital low-level input voltage	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max at I _{IL} Max	V _{SS} - 0.3	—	0.3 x V _{DD}	V
V _{OH}	Digital high-level output voltage	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max at I _{OH} Max	V _{DD} - 0.3	—	—	V
V _{OL}	Digital low-level output voltage	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max at I _{OL} Max	—	—	V _{SS} + 0.3	V
I _{pin}	Digital pin current	T _A = 25 °C, V _{DD} = 1.5 V	—	—	±10	mA

7.6 Serial data timing characteristics

Table 29. Serial data timing characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
C _B	Board capacitive load SDA, SCL	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	—	—	1	μF
t _{BUF}	Bus free time, between stop and start	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	4.7	—	—	μs
t _{HD} to t _{STA}	Restart hold, after this period the first clock may be generated	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	4.0	—	—	μs
t _{SU} to t _{STA}	Restart setup	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	4.7	—	—	μs
t _{SU} to t _{STO}	Stop setup	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	4.0	—	—	μs
t _{HD} to t _{DAT}	SDA hold	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	300	—	—	ns
t _{SU} to t _{DAT}	SDA setup	T _A Min ≤ T _A ≤ T _A Max, V _{DD} Min ≤ V _{DD} ≤ V _{DD} Max	250	—	—	ns

Symbol	Description	Condition	Min	Typ	Max	Unit
t_{LOW}	SCL low	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.7	—	—	μs
t_{HIGH}	SCL high	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	4.0	—	—	μs
t_r	SDA and SCL rise	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	1000	ns
t_f	SDA and SCL fall	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	300	ns

7.7 Magnetic field characteristics

Table 30. Magnetic transfer function characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
Transfer Function, $T_A = 25^\circ C$, $V_{DD} = 1.5 V$						
$B\Delta$	Sensitivity		—	1.75	—	G/LSB
B_{off}	Offset		—	0	—	G
B_{hyst}	Min. hysteresis window ($B_H - B_L$)		20	—	—	G
B_H	High hysteresis threshold in standalone mode	Low	—	70	100	G
		Medium	—	140	160	
		High	—	210	230	
B_L	Low hysteresis threshold in standalone mode	Low	—	42	—	G
		Medium	—	112	—	
		High	—	182	—	

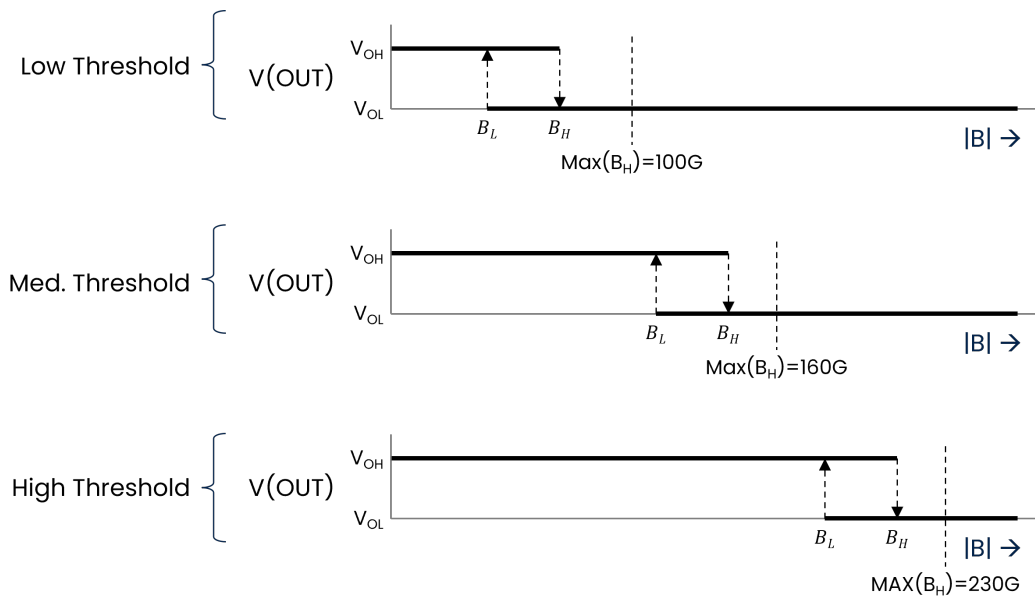


Figure 11. Output voltage vs. abs. magnetic field for each standalone threshold setting

7.8 I²C user mode, output assertion

Table 31. I²C user mode, recommended lowest USER_HIGH_THRESH [7:0]

Symbol	Description	Condition	Min	Typ	Max	Unit
B _{OA-I2C}	Output assertion, magnetic field decaying	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	0x10	—	—	hex

7.9 I²C user mode, output clear

Table 32. I²C user mode, recommended highest USER_LOW_THRESH [7:0]

Symbol	Description	Condition	Min	Typ	Max	Unit
B _{OC-I2C}	Output clear, magnetic field increasing	$T_A \text{ Min} \leq T_A \leq T_A \text{ Max}, V_{DD} \text{ Min} \leq V_{DD} \leq V_{DD} \text{ Max}$	—	—	> 0xF0	hex

8 Application information

Figure 12. Standalone mode, Low threshold, High sample rate

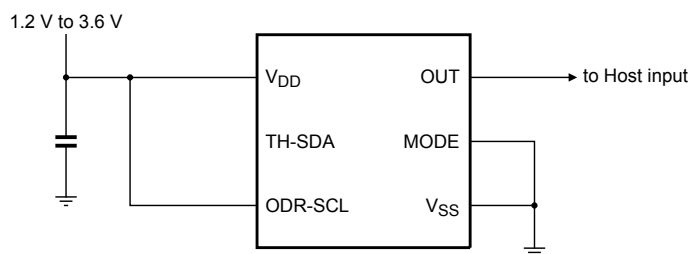


Figure 13. Standalone mode, Medium threshold, High sample rate

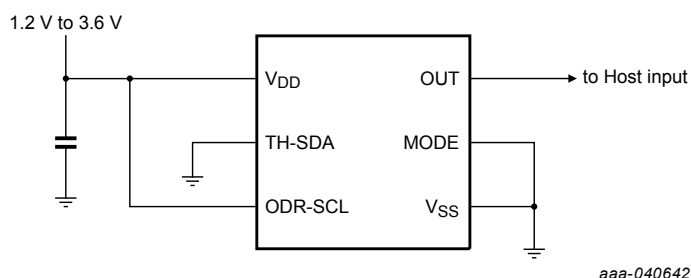


Figure 14. Standalone mode, High threshold, High sample rate

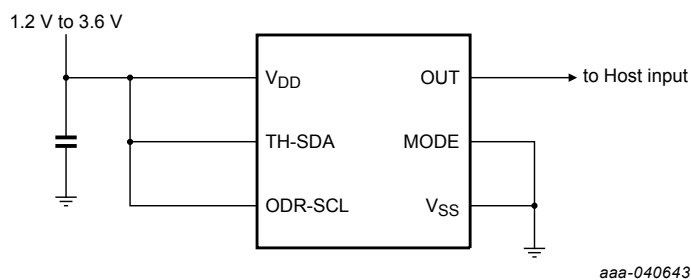


Figure 15. Standalone mode, Low threshold, Medium sample rate

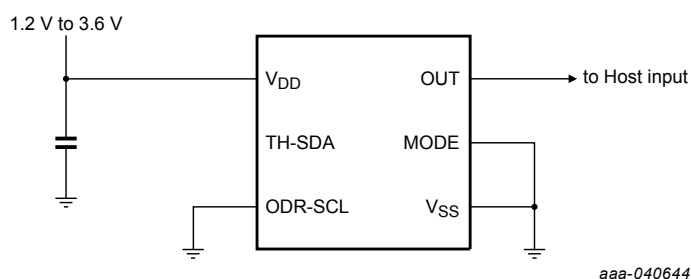


Figure 16. Standalone mode, Medium threshold, Medium sample rate

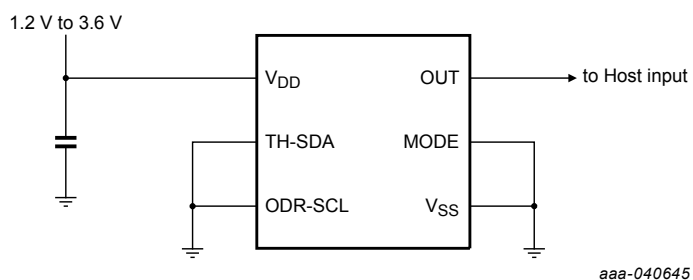


Figure 17. Standalone mode, High threshold, Medium sample rate

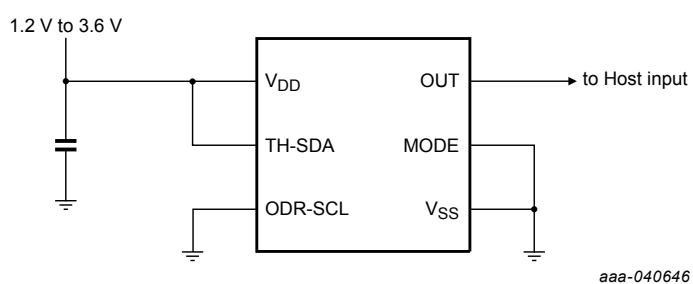


Figure 18. Standalone mode, Low threshold, Low sample rate

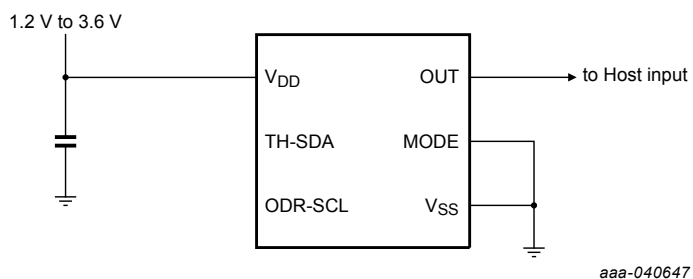


Figure 19. Standalone mode, Medium threshold, Low sample rate

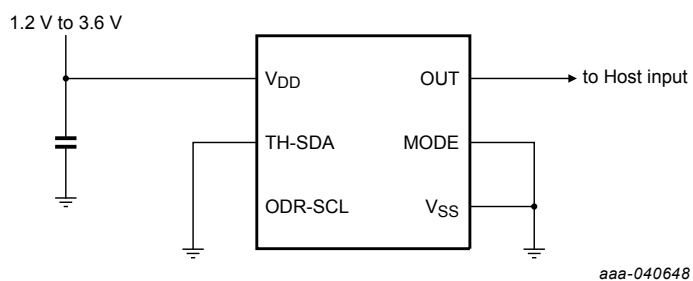


Figure 20. Standalone mode, High threshold, Low sample rate

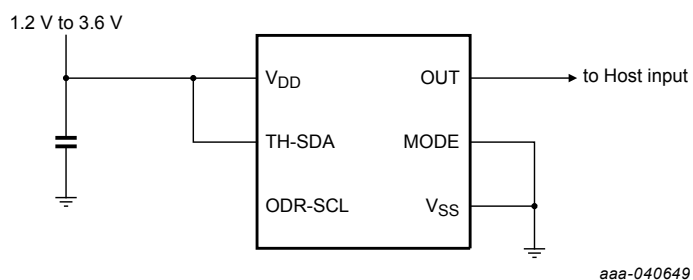
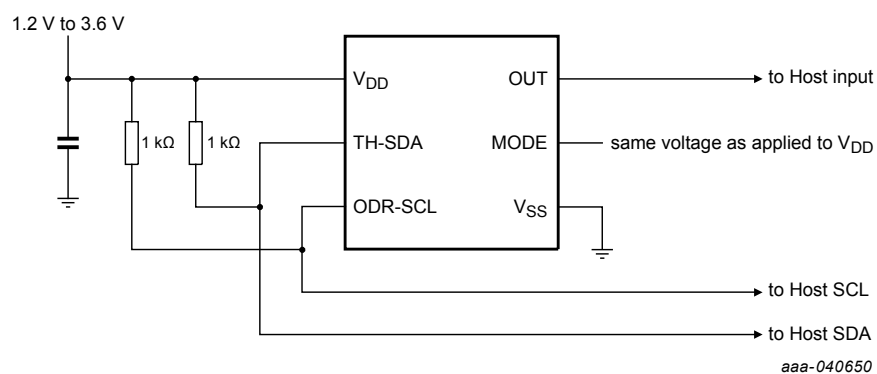


Figure 21. I²C mode



9

Figure 22. Package outline VSON6

PDFN-COL-6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

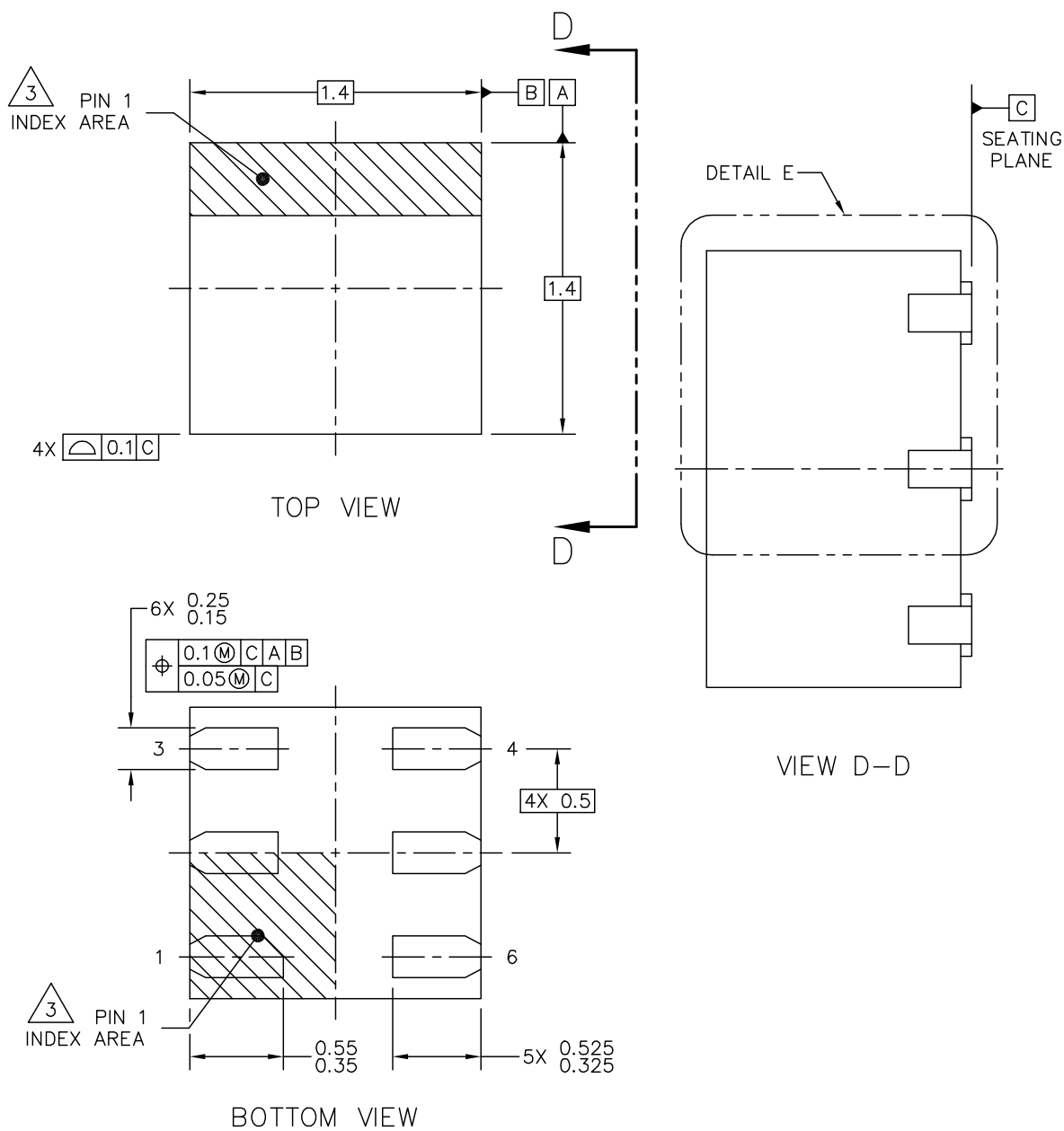
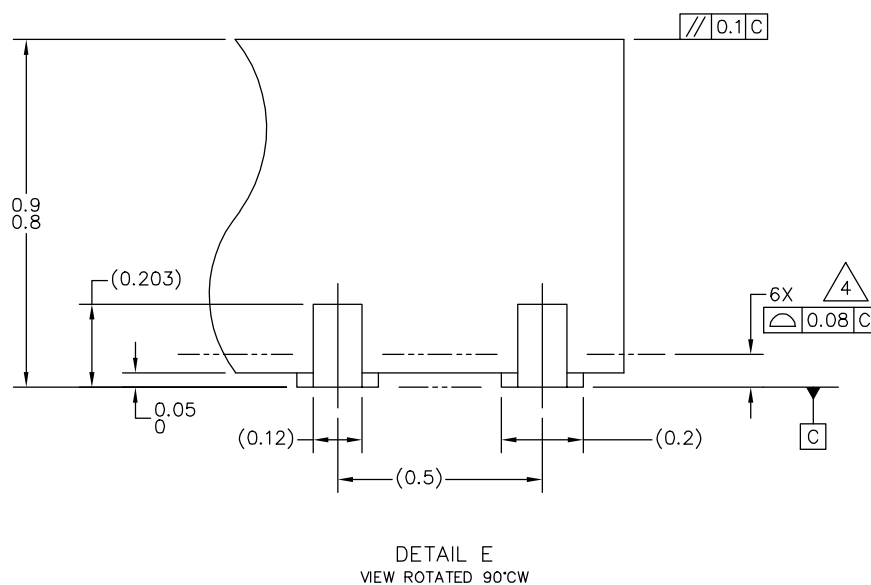


Figure 23. Package outline detail of VSON6

PDFN-COL-6 I/O
 1.4 X 1.4 X 0.85 PKG, 0.5 PITCH


Figure 24. Package outline note VSON6

PDFN-COL-6 I/O
 1.4 X 1.4 X 0.85 PKG, 0.5 PITCH

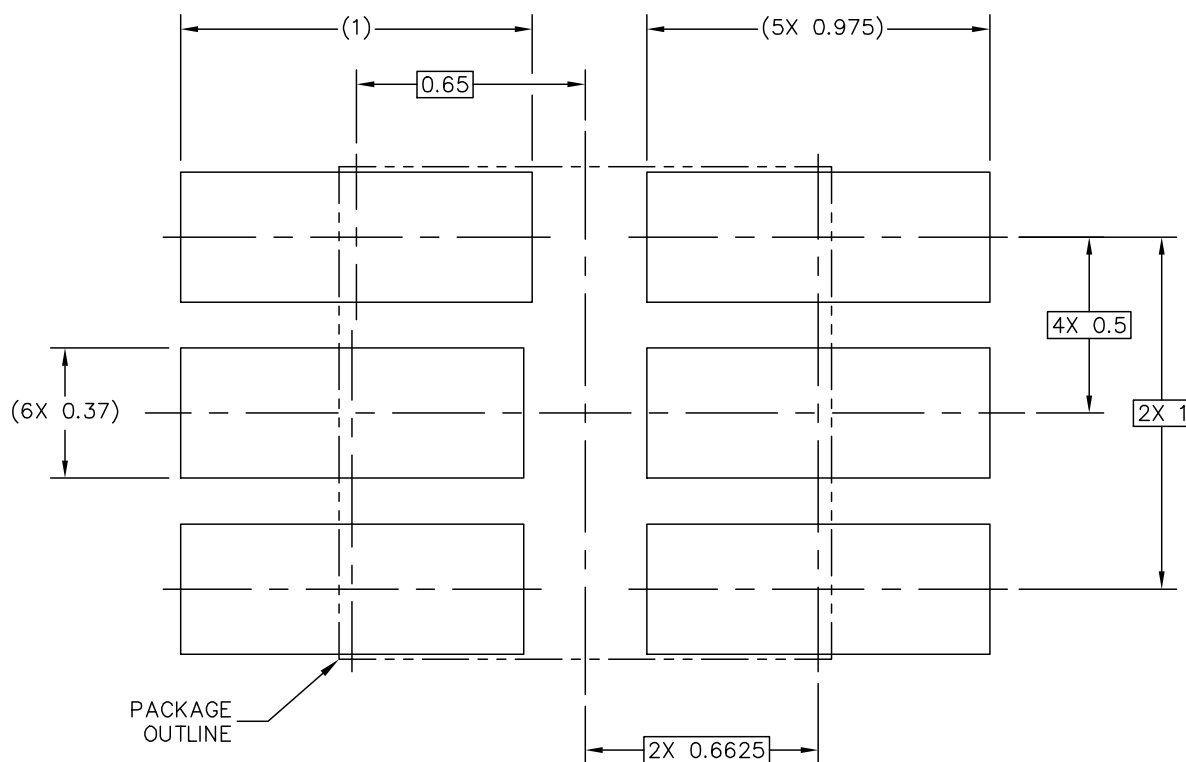
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.
5. MIN. METAL GAP SHOULD BE 0.15 MM.

10 Soldering information

Figure 25. Reflow soldering footprint part 1 for VSON6

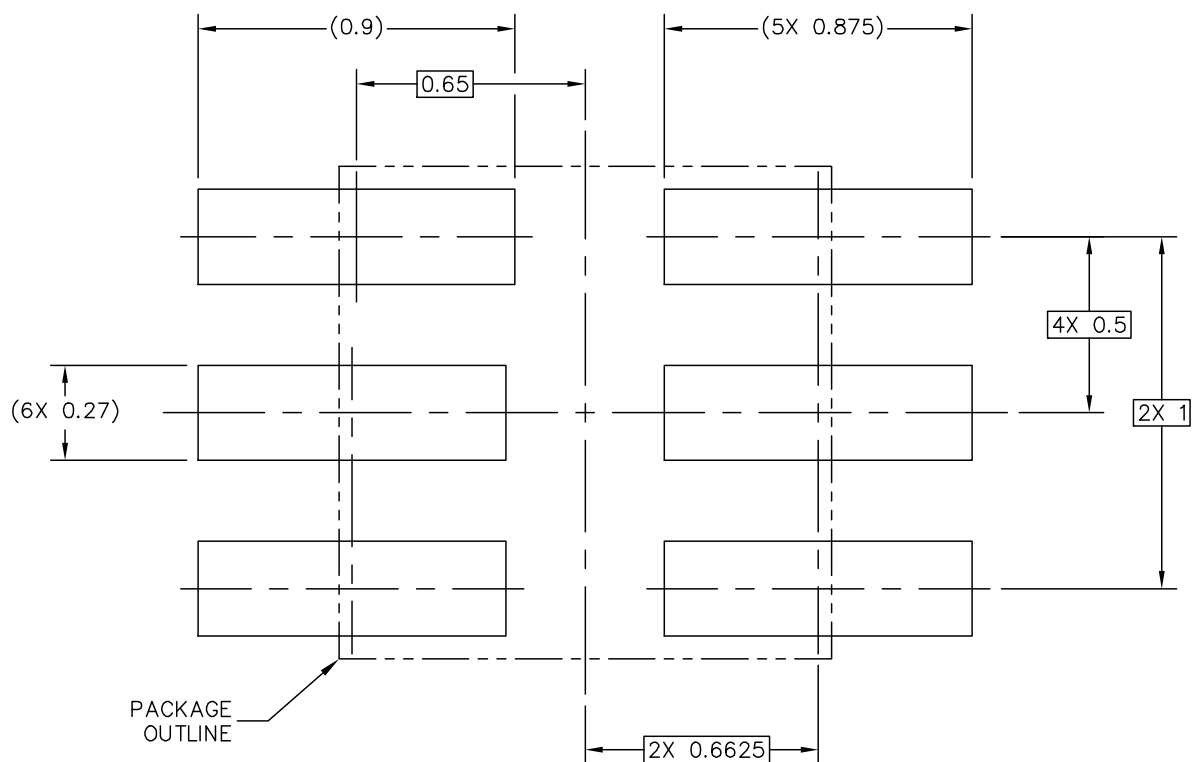
PDFN-COL-6 I/O
 1.4 X 1.4 X 0.85 PKG, 0.5 PITCH



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Figure 26. Reflow soldering footprint part 2 for VSON6

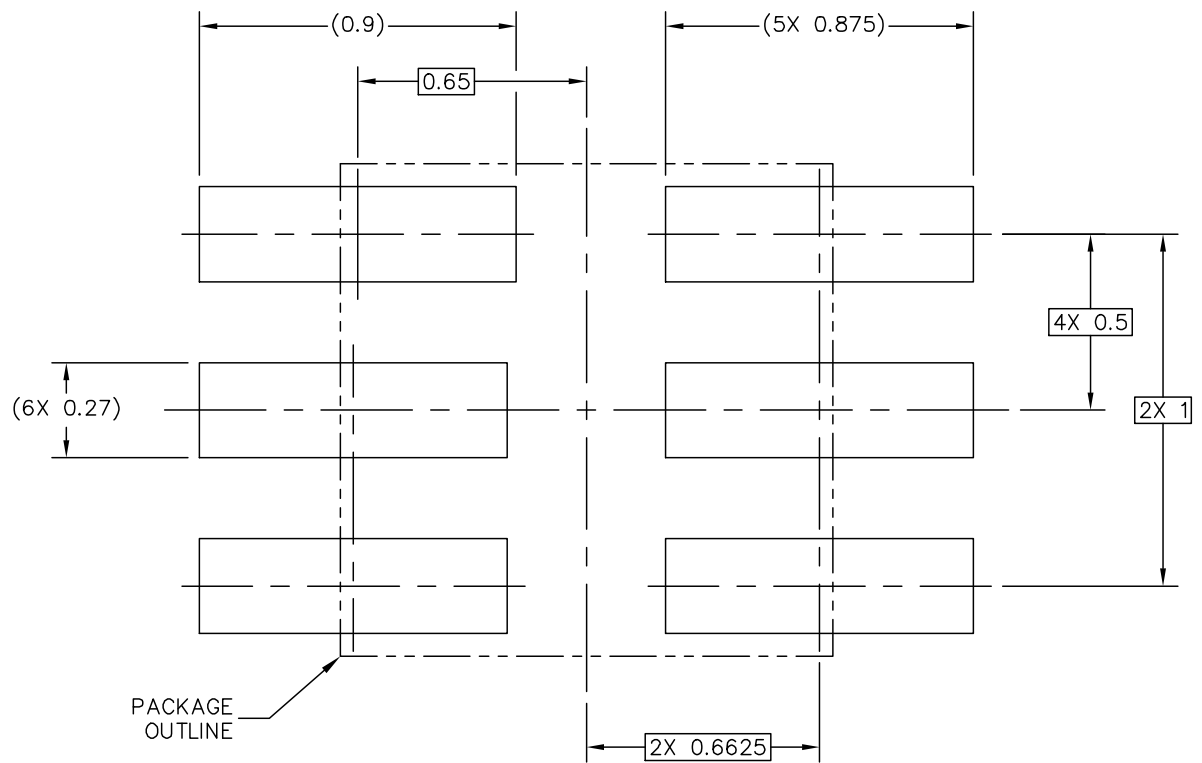
 PDFN-COL-6 I/O
 1.4 X 1.4 X 0.85 PKG, 0.5 PITCH


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Figure 27. Reflow soldering footprint part 3 for VSON6

PDFN-COL-6 I/O
1.4 X 1.4 X 0.85 PKG, 0.5 PITCH



RECOMMENDED STENCIL THICKNESS 0.1

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11 References

- [1] [AN6533](#) — Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages

Revision history

Table 33. Document revision history

Date	Version	Changes
01-Feb-2026	1	Initial release from ST, rebranded NXP document
30-Jul-2026	2	Document restructured; major updates across all sections • Section Features and benefits • Section Description • Figure 1. Block diagram • Section 2.1: Block descriptions • Figure 1. Block diagram • Section 3.2: Pin description • Section 3.3: Orientation • Figure 4. NMH1000 functional state flow diagram • Section 4.1: Operating modes • Section 4.2: Threshold configurations • Section 4.3: Sample rate configurations • Output control function description • Table 5. Register map overview • Table 7. STATUS – Status reporting of modes and selections (address \$00h) bit descriptions • Table 9. CONTROL_Reg1 – Control of operations (address \$01h) bit description • Table 13. USER_LOW_THRESH – User selectable output, low threshold, N or S (address \$04h) bit description • Table 15. USER_HIGH_THRESH – User selectable output, high threshold, N or S (address \$05h) bit description • Section 4.5.2.6: User selectable sleep sample output data rates (USER_ODR) (\$06h) • Table 23. Operating conditions • Table 30. Magnetic transfer function characteristics • Table 30. Magnetic transfer function characteristicsFigure 11. Output voltage vs abs. magnetic field for each standalone threshold setting • Section 7.8: I²C user mode, output assertion • Table 32. I²C user mode, recommended highest USER_LOW_THRESH [7:0]

Contents

1	Ordering information	2
2	Block diagram	3
2.1	Block descriptions	4
3	Pinning information	5
3.1	Pinning	5
3.2	Pin description	5
3.3	Orientation	6
4	Functional description	7
4.1	Operating modes	7
4.1.1	Functional states	7
4.1.2	Operational modes	8
4.2	Threshold configurations	9
4.2.1	In standalone mode	9
4.2.2	In I ² C mode	10
4.3	Sample rate configurations	11
4.3.1	In standalone mode	11
4.3.2	In I ² C mode	11
4.4	I ² C serial data function description	11
4.4.1	I ² C pin functions	11
4.4.2	I ² C timing diagram	12
4.4.3	I ² C operation	12
4.4.4	I ² C protocol diagram	13
4.5	Register map	14
4.5.1	Register overview	14
4.5.2	Register details	14
5	Limiting values	20
6	Recommended operating conditions	21
7	Characteristics	22
7.1	Supply currents	22
7.2	Clocks and rates	22
7.3	Sample rates in standalone mode	22
7.4	Sample rates in I ² C mode	23
7.5	I ² C pin thresholds	23
7.6	Serial data timing characteristics	23
7.7	Magnetic field characteristics	24

7.8	I ² C user mode, output assertion	25
7.9	I ² C user mode, output clear	25
8	Application information	26
9	Package outline	29
10	Soldering information.....	31
11	References	34
	Revision history	35
	List of tables	38
	List of figures.....	39

List of tables

Table 1.	Ordering information.	2
Table 2.	Pin description.	5
Table 3.	Fixed threshold selection	9
Table 4.	Sample rate selection in standalone mode	11
Table 5.	Register map overview	14
Table 6.	STATUS – Status reporting of modes and selections (address \$00h) bit allocation	14
Table 7.	STATUS – Status reporting of modes and selections (address \$00h) bit descriptions	14
Table 8.	CONTROL_Reg1 – Control of operations(address \$01h) bit allocation	15
Table 9.	CONTROL_Reg1 – Control of operations (address \$01h) bit description.	15
Table 10.	MAG_DATA – Magnetic strength report (address \$03h) bit allocation	16
Table 11.	MAG_DATA – Magnetic strength report (address \$03h) bit description	16
Table 12.	USER_LOW_THRESH – User selectable output, low threshold, N or S (address \$04h) bit allocation	17
Table 13.	USER_LOW_THRESH – User selectable output, low threshold, N or S (address \$04h) bit description	17
Table 14.	USER_HIGH_THRESH – User selectable output, high threshold, N or S (address \$05h) bit allocation	18
Table 15.	USER_HIGH_THRESH – User selectable output, high threshold, N or S (address \$05h) bit description	18
Table 16.	USER_ODR – User selectable sleep sample output data rates (address \$06h) bit allocation	18
Table 17.	USER_ODR – User selectable sleep sample output data rates (address \$06h) bit description	18
Table 18.	WHO_AM_I - I ² C configured identifier (address \$08h) bit allocation	19
Table 19.	WHO_AM_I - I ² C configured identifier (address \$08h) bit description	19
Table 20.	I2C_ADDR - I ² C configured identifier (address \$09h) bit allocation	19
Table 21.	I2C_ADDR - I ² C configured identifier (address \$09h) bit description	19
Table 22.	Limiting values	20
Table 23.	Operating conditions	21
Table 24.	Supply currents	22
Table 25.	Clocks and rates	22
Table 26.	Sample rates in standalone mode	22
Table 27.	Sample rates in I ² C mode	23
Table 28.	I ² C pin thresholds.	23
Table 29.	Serial data timing characteristics	23
Table 30.	Magnetic transfer function characteristics	24
Table 31.	I ² C user mode, recommended lowest USER_HIGH_THRESH [7:0]	25
Table 32.	I ² C user mode, recommended highest USER_LOW_THRESH [7:0]	25
Table 33.	Document revision history	35

List of figures

Figure 1.	Block diagram	3
Figure 2.	Pin configuration	5
Figure 3.	Magnetic field sensitivity vs. package orientation.	6
Figure 4.	NMH1000 functional state flow diagram	7
Figure 5.	Output pin voltage vs. abs. magnetic field in standalone mode	9
Figure 6.	Output pin voltage vs abs. magnetic field in I ² C mode	10
Figure 7.	I ² C timing diagram.	12
Figure 8.	I ² C write operation.	13
Figure 9.	I ² C read operation.	13
Figure 10.	Guaranteed In-Spec Region of Operation.	17
Figure 11.	Output voltage vs abs. magnetic field for each standalone threshold setting	24
Figure 12.	Standalone mode, Low threshold, High sample rate	26
Figure 13.	Standalone mode, Medium threshold, High sample rate	26
Figure 14.	Standalone mode, High threshold, High sample rate	26
Figure 15.	Standalone mode, Low threshold, Medium sample rate	26
Figure 16.	Standalone mode, Medium threshold, Medium sample rate	27
Figure 17.	Standalone mode, High threshold, Medium sample rate	27
Figure 18.	Standalone mode, Low threshold, Low sample rate	27
Figure 19.	Standalone mode, Medium threshold, Low sample rate	27
Figure 20.	Standalone mode, High threshold, Low sample rate	28
Figure 21.	I ² C mode	28
Figure 22.	Package outline VSON6	29
Figure 23.	Package outline detail of VSON6	30
Figure 24.	Package outline note VSON6	30
Figure 25.	Reflow soldering footprint part 1 for VSON6	31
Figure 26.	Reflow soldering footprint part 2 for VSON6	32
Figure 27.	Reflow soldering footprint part 3 for VSON6	33

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