

NTD6415AN, NVD6415AN

MOSFET – Power, N-Channel

100 V, 23 A, 55 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|--|------------------------|------------------------|-----------------------------------|-------------|------|
| Drain-to-Source Voltage | | | V _{DSS} | 100 | V |
| Gate-to-Source Voltage – Continuous | | | V _{GS} | ±20 | V |
| Continuous Drain Current R _{θJC} | Steady State | T _C = 25°C | I _D | 23 | A |
| | | T _C = 100°C | | 16 | |
| Power Dissipation R _{θJC} | Steady State | T _C = 25°C | P _D | 83 | W |
| Pulsed Drain Current | t _p = 10 μs | | I _{DM} | 89 | A |
| Operating and Storage Temperature Range | | | T _J , T _{stg} | –55 to +175 | °C |
| Source Current (Body Diode) | | | I _S | 23 | A |
| Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 50 Vdc, V _{GS} = 10 Vdc, I _{L(pk)} = 23 A, L = 0.3 mH, R _G = 25 Ω) | | | E _{AS} | 79 | mJ |
| Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds | | | T _L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---------------------------------------|-----------------|-----|--------------------|
| Junction-to-Case (Drain) Steady State | $R_{\theta JC}$ | 1.8 | $^\circ\text{C/W}$ |
| Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 39 | |

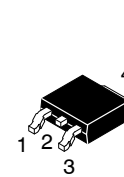
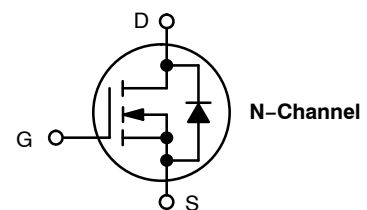
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



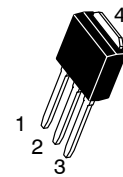
ON Semiconductor®

<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(on)} \text{ MAX}$ | $I_D \text{ MAX}$ (Note 1) |
|---------------|--------------------------|-------------------------------|
| 100 V | 55 mΩ @ 10 V | 23 A |

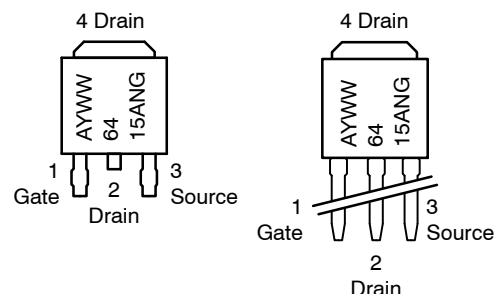


DPACK
CASE 369AA
STYLE 2



IPACK
CASE 369D
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location*
Y = Year
WW = Work Week
6415AN = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NTD6415AN, NVD6415AN

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|--------------------------------------|---|---|-----|------------|-------|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 100 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 113 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 100 V | T _J = 25°C T _J = 125°C | | 1.0 100 | μA |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | ±100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|--|-------------------------------------|---|-----|-----|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 2.0 | | 4.0 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | 7.6 | | mV/°C |
| Drain-to-Source On-Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 23 A | | 47 | 55 | mΩ |
| Forward Transconductance | g _{FS} | V _{GS} = 5 V, I _D = 10 A | | 13 | | S |

CHARGES, CAPACITANCES AND GATE RESISTANCE

| | | | | | | |
|------------------------------|---------------------|---|--|------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | | 700 | | pF |
| Output Capacitance | C _{OSS} | | | 110 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 52 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 80 V, I _D = 23 A | | 29 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 1.2 | | |
| Gate-to-Source Charge | Q _{GS} | | | 5 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 14.6 | | |
| Plateau Voltage | V _{GP} | | | 5.7 | | |
| Gate Resistance | R _G | | | 2.3 | | Ω |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | | |
|---------------------|---------------------|--|--|----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 10 V, V _{DD} = 80 V, I _D = 23 A, R _G = 6.1 Ω | | 10 | | ns |
| Rise Time | t _r | | | 37 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 30 | | |
| Fall Time | t _f | | | 37 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-------------------------|-----------------|---|---|--------------|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 23 A | T _J = 25°C T _J = 125°C | 0.83 0.68 | 1.2 | V |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 23 A | | 65 | | ns |
| Charge Time | T _a | | | 46 | | |
| Discharge Time | T _b | | | 19 | | |
| Reverse Recovery Charge | Q _{RR} | | | 176 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

NTD6415AN, NVD6415AN

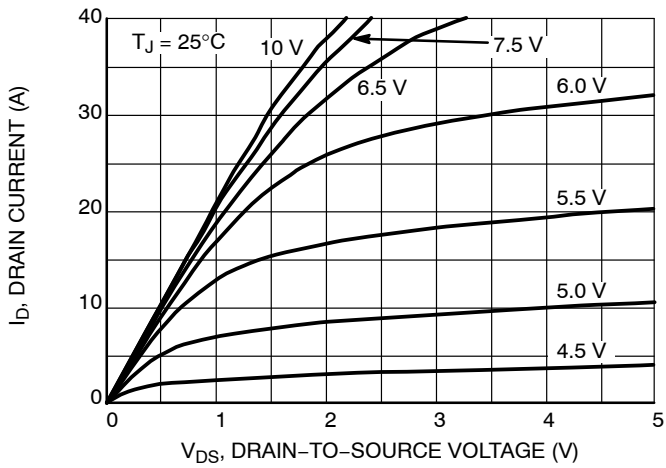


Figure 1. On-Region Characteristics

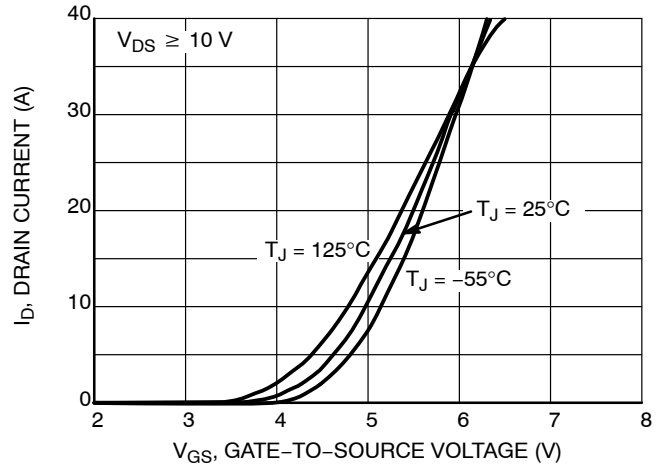


Figure 2. Transfer Characteristics

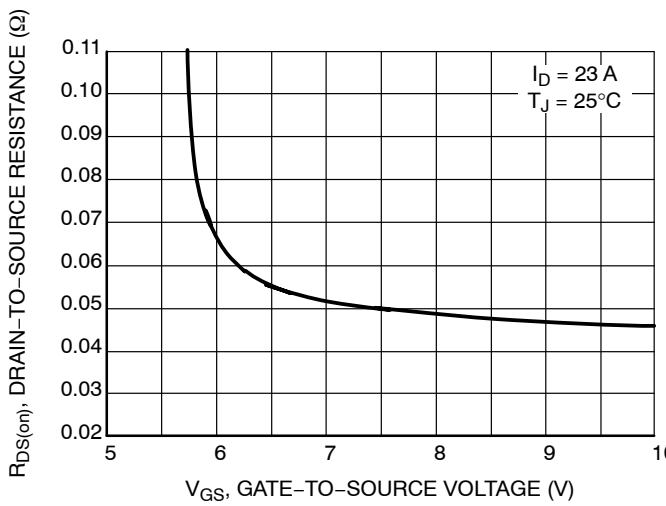


Figure 3. On-Region versus Gate Voltage

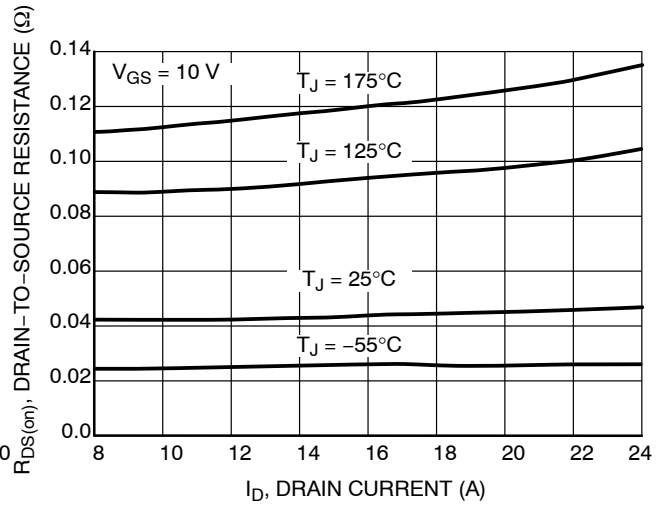


Figure 4. On-Resistance versus Drain Current and Gate Voltage

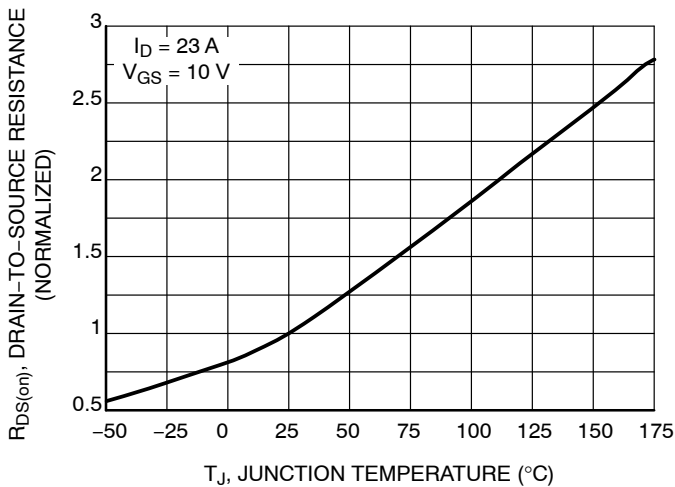


Figure 5. On-Resistance Variation with Temperature

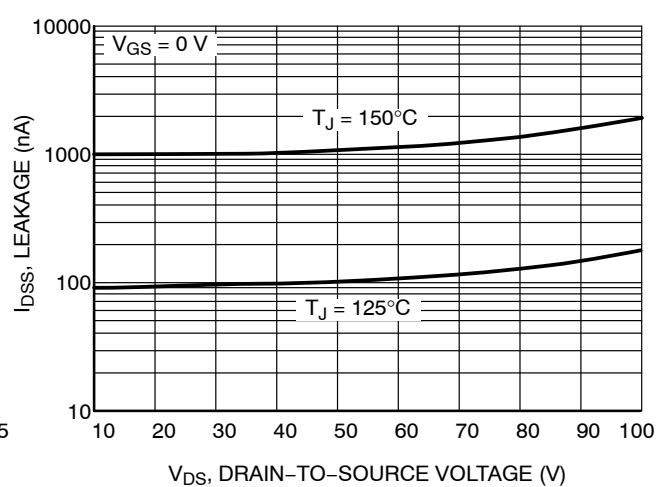


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD6415AN, NVD6415AN

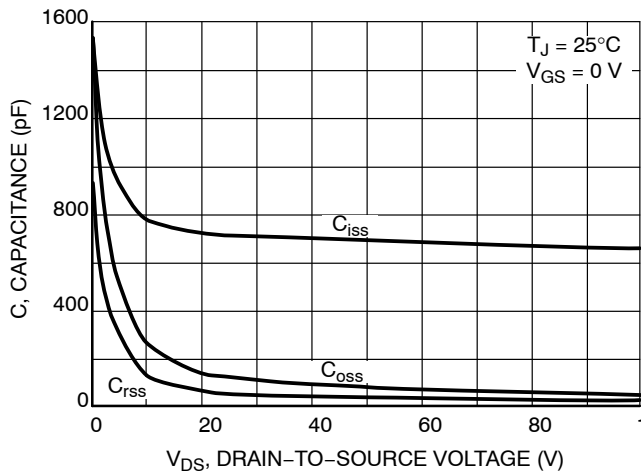


Figure 7. Capacitance Variation

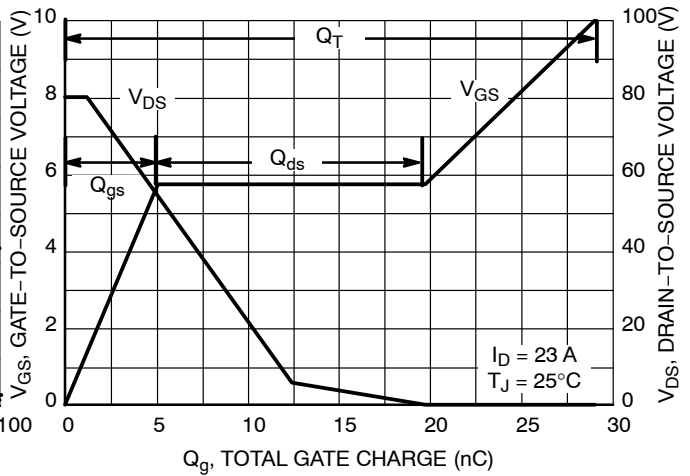


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

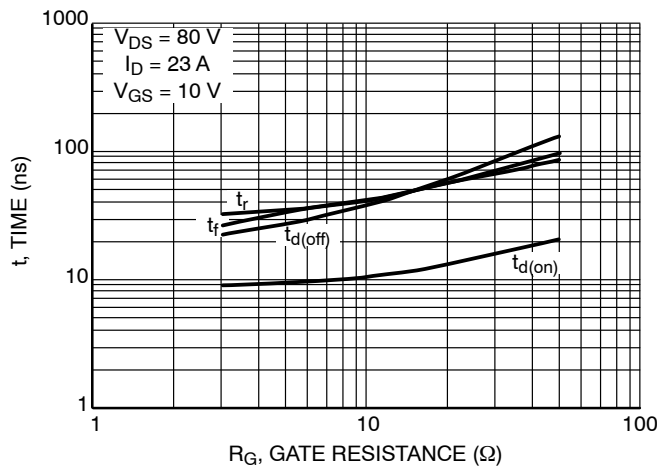


Figure 9. Resistive Switching Time Variation versus Gate Resistance

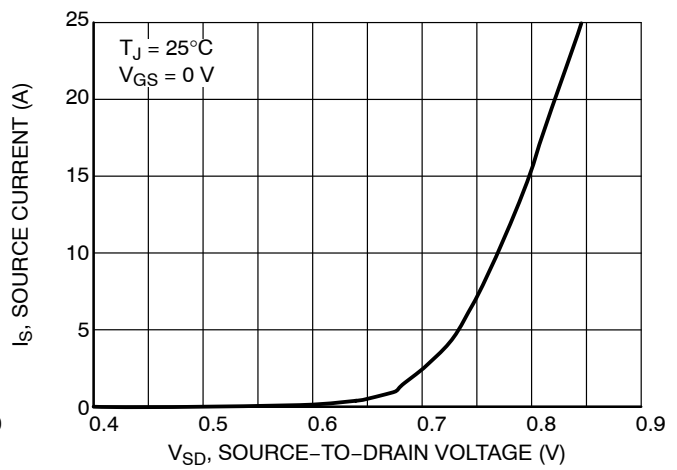


Figure 10. Diode Forward Voltage versus Current

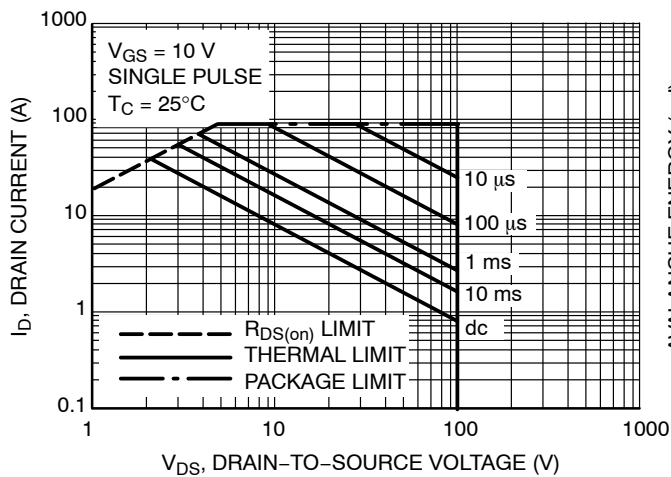


Figure 11. Maximum Rated Forward Biased Safe Operating Area

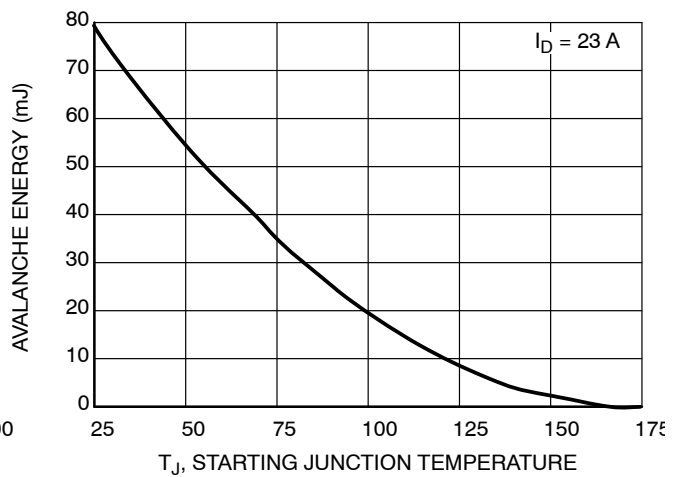


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTD6415AN, NVD6415AN

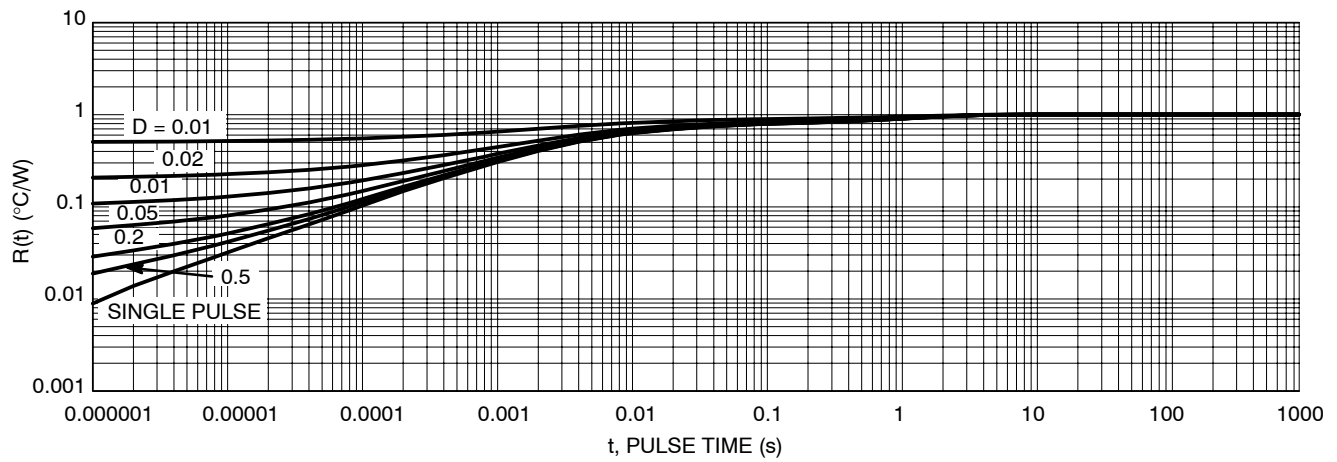


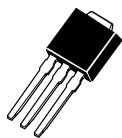
Figure 13. Thermal Response

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|-------------------|--------------------|
| NTD6415ANT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NTD6415AN-1G | IPAK (Pb-Free) | 75 Units / Rail |
| NVD6415ANT4G* | DPAK (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

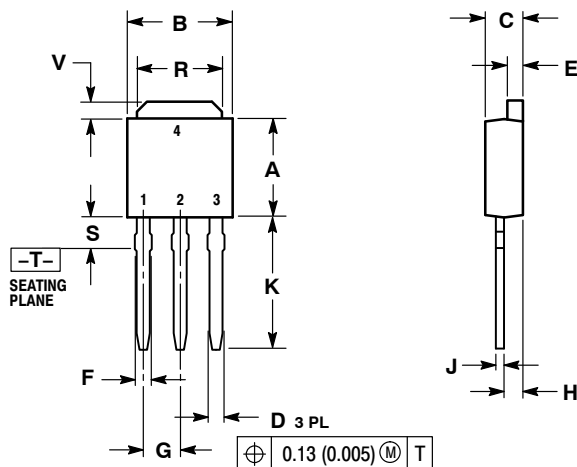
*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.050 | 0.090 | 1.27 | 2.28 |
| V | 0.030 | 0.050 | 0.77 | 1.27 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

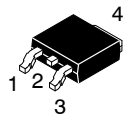
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

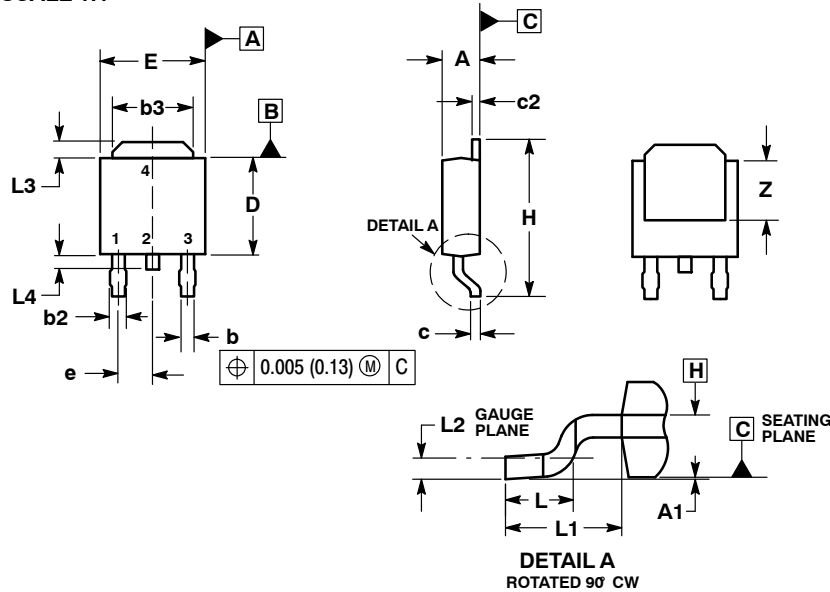
STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

| | | |
|------------------|----------------------|--|
| DOCUMENT NUMBER: | 98ASB42319B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK INSERTION MOUNT | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

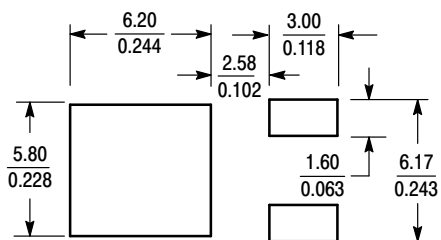
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

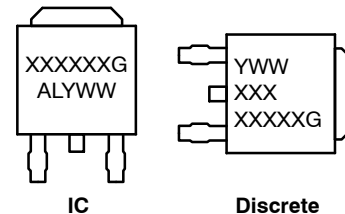
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | | 0.040 | | 1.01 |
| Z | 0.155 | | 3.93 | |

GENERIC
MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
|------------------|---------------------|---|
| DOCUMENT NUMBER: | 98AON13126D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

