

QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1075

CLOCK DIVIDER

Clock Divider/Sine Wave 50 Ohm to CMOS Level Converter

DESCRIPTION

Demonstration circuit 1075 is a clock divider for use with high speed ADCs. Each assembly includes a clock divider followed by a retiming stage used to produce sharp clock edges.

Functionally, the DC1075 receives a high frequency sine wave which is attenuated and routed into the clock divider. The output of the clock divider is then routed to a D flip flop retiming stage. This D flip flop is clocked by the original input. This is critical to ensure signal integrity. The output of this

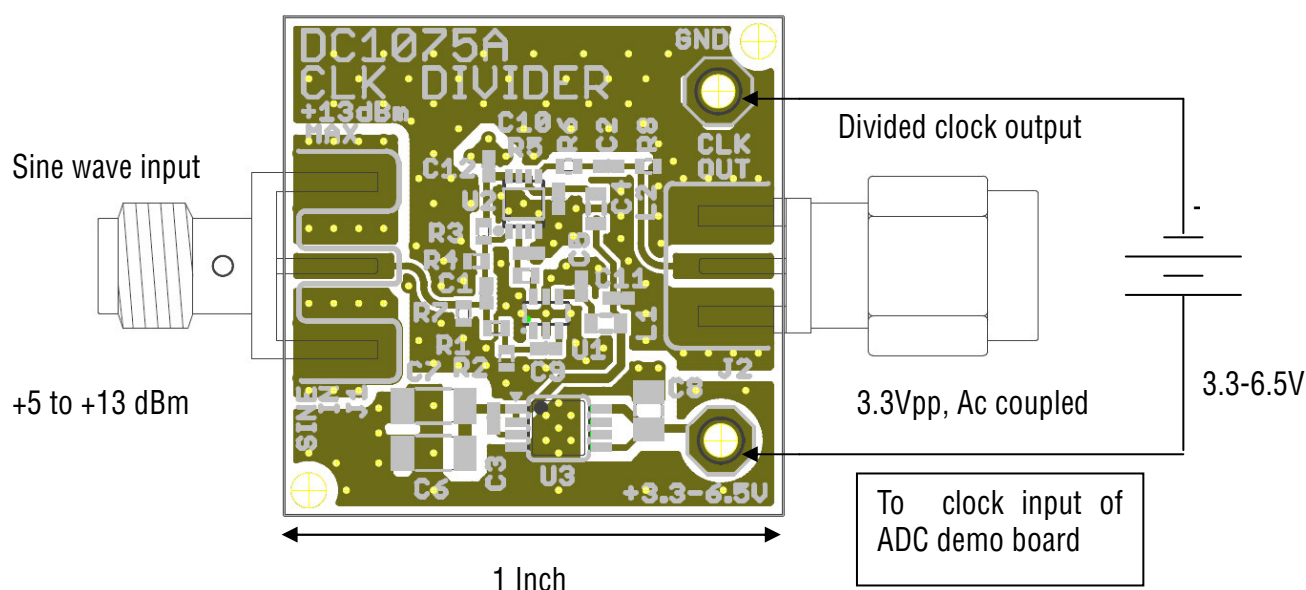
retiming stage is a CMOS signal suitable to be a clock source for high speed ADCs.

This circuit also is a model for designs involving FPGAs which serve as clock dividers. Whenever this is done, a D flip flop retiming stage is required to ensure a low jitter clock signal.

Design files for this circuit board are available. Call the LTC factory.

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QUICK START PROCEDURE



SETUP

The DC1075 requires an external sine wave and an external power supply above 3.3V. The input voltage should not exceed 6.5V. Connect the female SMA connector to the sine wave generator. The input signal should not exceed 13.0dBm. The DC1075 uses a male SMA output connector that can be connected directly to the clock input of ADC demo boards without additional adaptors.

For best results put a bandpass filter between the sine source and the DC1075 to reduce jitter of the input signal.

LINEAR
TECHNOLOGY

REVISION HISTORY

ECO	REV	DESCRIPTION	DATE	APPROVED

CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REPAIRS THE CUSTOMERS RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

CONTRACT NO.

APPROVALS

DRAWN
CHECKED
APPROVED
ENGINEER
DESIGNER
FILENAME: 1075902

TITLE: SCHEMATIC

CLOCK DIVIDER

SIZE DWG NO. **A**

REV: **A2**

DATE: 8/18/2006 01:51:42p

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