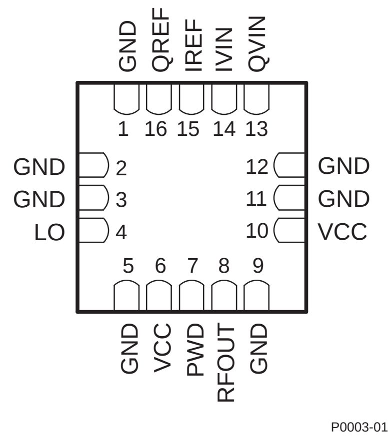
1.5-GHz to 2.5-GHz QUADRATURE MODULATOR

FEATURES

- 71-dBc Single-Carrier WCDMA ACPR at –14-dBm Channel Power
- P1dB of 7 dBm
- Typical Unadjusted Carrier Suppression 35 dBc at 2 GHz
- Typical Unadjusted Sideband Suppression 35 dBc at 2 GHz
- Very Low Noise Floor
- Differential or Single-Ended I, Q Inputs
- Convenient Single-Ended LO Input
- Silicon Germanium Technology

RHC PACKAGE
(TOP VIEW)



APPLICATIONS

- Cellular Base Transceiver Station Transmit Channel
- IF Sampling Applications
- TDMA: GSM, IS-136, EDGE/UWC-136
- CDMA: IS-95, UMTS, CDMA2000
- Wireless Local Loop
- Wireless LAN IEEE 802.11
- LMDS, MMDS
- Wideband Transceivers

DESCRIPTION

The TRF3702 is an ultralow-noise direct quadrature modulator that is capable of converting complex input signals from baseband or IF directly up to RF. An internal analog combiner sums the real and imaginary components of the RF outputs. This combined output can feed the RF preamp at frequencies of up to 2.5 GHz. The modulator is implemented as a double-balanced mixer. An internal local oscillator (LO) phase splitter accommodates a single-ended LO input, eliminating the need for a costly external balun.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

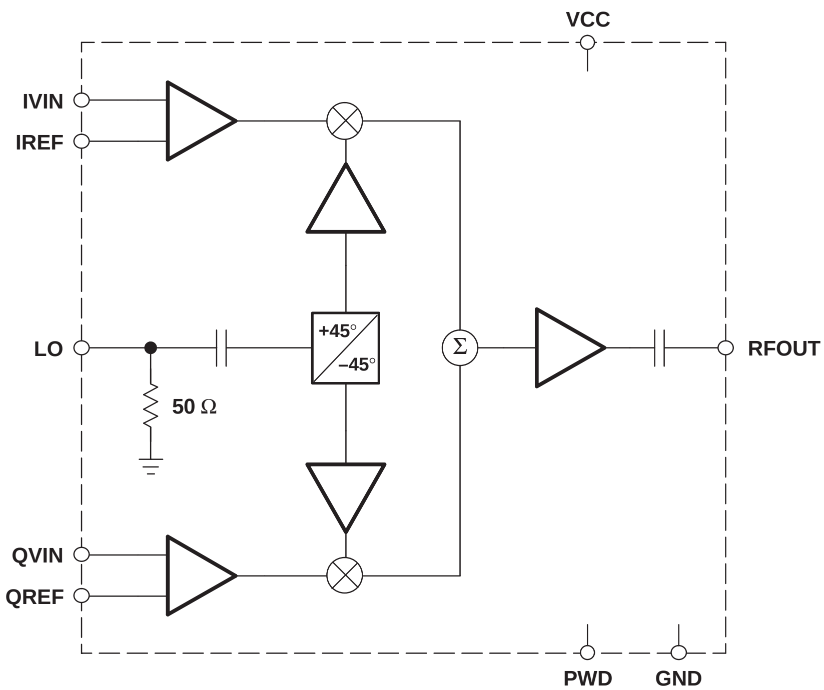
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	4-mm × 4-mm 16-Pin RHC (QFN) Package (1)
–40°C to 85°C	TRF3702IRHC
	TRF3702IRHCR (Tape and reel)

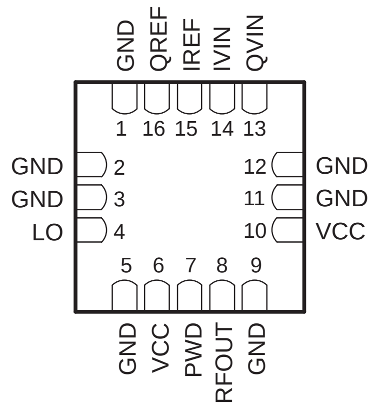
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM



B0002-01

RHC PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1, 2, 3, 5, 9, 11, 12		Ground
IREF	15	I	In-phase (I) reference voltage/differential input
IVIN	14	I	In-phase (I) signal input
LO	4	I	Local oscillator input
PWD	7	I	Power down
QREF	16	I	Quadrature (Q) reference voltage/differential input
QVIN	13	I	Quadrature (Q) signal input
RFOUT	8	O	RF output
VCC	6, 10		Supply voltage

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

V_{CC}	Supply voltage range	–0.5 V to 6 V
	LO input power level	10 dBm
	Baseband input voltage level (single-ended)	3 Vp-p
T_A	Operating free-air temperature range	–40°C to 85°C
	Lead temperature for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to ground

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supplies and References					
V_{CC}	Analog supply voltage	4.5	5	5.5	V
	VCM (IVIN, QVIN, IREF, QREF input common-mode voltage)		3.7		V
	Local Oscillator (LO) Input				
	Input frequency	1500		2500	MHz
	Power level (measured into 50 Ω)	–6	0	6	dBm
	Signal Inputs (IVIN, QVIN)				
	Input bandwidth		700		MHz

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, VCC = 5 V, VCM = 3.7 V, f_{LO} = 2140 MHz at 0 dBm, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
I_{CC}	Total supply current	V(PWD) = 5 V		145	170	mA
		V(PWD) = 0 V		13	30	
	Turnon time			120		ns
	Turnoff time			20		ns
	Power-down input impedance			11		kΩ
Local Oscillator (LO) Input						
	Input impedance (1)			27 + j8		Ω
Signal Inputs (IVIN, QVIN, IREF, QREF)						
	Input bias current	I, Q = VCM = 3.7 V (all inputs tied to VCM)		16		µA
	Input impedance	Single-ended input		260		kΩ
		Differential input		130		

(1) For a listing of impedances at various frequencies, see Table 1.

Table 1. RFOUT and LO Pin Impedance

Frequency (MHz)	Z (RFOUT Pin)	Z (LO Pin)
1500	31 – j 4.7	31.7 – j 8.8
1600	30.9 – j 0.3	29.3 – j 6.2
1700	29.3 + j 3.1	27.3 - j 3.1
1800	27.9 + j 7.2	26.5 – j 0.17
1900	27.6 + j 13	26.1+ – j 2.7
2000	29.4 +j 19.8	26.5 + j 5.4
2100	34.6 + j 27.2	27 + j 7.6
2200	44.2 + j 33	28 + j 9.5
2300	60 + j 33.6	29 + j 10.6
2400	78 + j 21	29.5 + j 11
2500	82 – j 5.8	29.8 + j 12.2

RF OUTPUT PERFORMANCE

Over recommended operating conditions, VCC = 5 V, VCM = 3.7 V, f_{LO} = 1842 MHz at 0 dBm (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Single and Two-Tone Specifications						
	Output power	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz	–5	–2.5		dBm
	Second baseband harmonic (USB or LSB)[2]	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz		–50	–42	dBc
	Third baseband harmonic (USB or LSB)[2]	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz		–57	–50	dBc
	IMD_3	I, Q[1] = 1 Vp-p (two-tone signal, f_{BB1} = 928 kHz, f_{BB2} = 992 kHz)		–59	–53	dBc
	P1dB (output compression point)			7		dBm
NSD	Noise spectral density	I, Q = VCM = 3.7 VDC (all inputs tied to VCM), 6-MHz offset from carrier		–155		dBm/Hz
		6-MHz offset from carrier, P_{out} = 0 dBm, over temperature		–148.5	–146.5[3]	dBm/Hz
	RFOUT pin impedance[4]			28 + j8		Ω
	Carrier suppression	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		30		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, over temperature[5]		44		dBc
	Sideband suppression	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		35		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, over temperature[5]		47		dBc

(1) I , Q = 1 Vp-p implies that the magnitude of the signal at each input pin IVIN, IREF, QVIN, QREF is equal to 500 mVp-p.
(2) USB = upper sideband. LSB = lower sideband.
(3) Maximum noise values are assured by statistical characterization only, not production testing. The values specified are over the entire temperature range, T_A = –40°C to 85°C.
(4) For a listing of impedances at various frequencies, see Table 1.
(5) After optimization at room temperature. See the *Definitions of Selected Specifications* section.

RF OUTPUT PERFORMANCE

Over recommended operating conditions, VCC = 5 V, VCM = 3.7 V, f_{LO} = 1960 MHz at 0 dBm (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Single and Two-Tone Specifications						
	Output power	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz		–3		dBm
	Second baseband harmonic (USB or LSB)[2]	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz		–50		dBc
	Third baseband harmonic (USB or LSB)[2]	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz		–60		dBc
	IMD_3	I, Q[1] = 1 Vp-p (two-tone signal, f_{BB1} = 928 kHz, f_{BB2} = 992 kHz)		–59	–53	dBc
	P1dB (output compression point)			7		dBm
NSD	Noise spectral density	6-MHz offset from carrier, P_{out} = 0 dBm, over temperature		–148	–146.5[3]	dBm/Hz
	RFOUT pin impedance[4]			28 + j15		Ω
	Carrier suppression	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		33		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		dBc
	Sideband suppression	I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		35		dBc
		I, Q[1] = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		dBc

(1) I , Q = 1 Vp-p implies that the magnitude of the signal at each input pin IVIN, IREF, QVIN, QREF is equal to 500 mVp-p.
(2) USB = upper sideband. LSB = lower sideband.
(3) Maximum noise values are assured by statistical characterization only, not production testing. The values specified are over the entire temperature range, T_A = –40°C to 85°C.
(4) For a listing of impedances at various frequencies, see Table 1.

RF OUTPUT PERFORMANCE

Over recommended operating conditions, VCC = 5 V, VCM = 3.7 V, f_{LO} = 2.1 GHz at 0 dBm (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Single and Two-Tone Specifications						
	Output power	I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz	–5	–3		dBm
	Second baseband harmonic (USB or LSB)(2)			–50	–42	dBc
	Third baseband harmonic (USB or LSB)(2)			–60	–51	dBc
	IMD_3	I, Q(1) = 1 Vp-p, fBB = 928 kHz (two-tone signal, f_{BB1} = 928 kHz, f_{BB2} = 992 kHz)		–55	–47	dBc
	P1dB (output compression point)			7		dBm
NSD	Noise spectral density	60-MHz offset from carrier, P_{out} = 0 dBm, over temperature		–151	–148.5(3)	dBm/Hz
	WCDMA ACPR	Single carrier, channel power = –14 dBm		71		dBc
	RFOUT pin impedance(4)			35 + j27		Ω
	Carrier suppression	I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		30		dBc
		I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		
		I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, over temperature(5)		47		
	Sideband suppression	I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, unadjusted		37		dBc
		I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, optimized		55		
		I, Q(1) = 1 Vp-p, f_{BB} = 928 kHz, over temperature(5)		47		

(1) I , Q = 1 Vp-p implies that the magnitude of the signal at each input pin IVIN, IREF, QVIN, QREF is equal to 500 mVp-p.
(2) USB = upper sideband. LSB = lower sideband.
(3) Maximum noise values are assured by statistical characterization only, not production testing. The values specified are over the entire temperature range, T_A = –40°C to 85°C.
(4) For a listing of impedances at various frequencies, see Table 1.
(5) After optimization at room temperature. See the *Definitions of Selected Specifications* section.

THERMAL CHARACTERISTICS

PARAMETER		CONDITION	NOM	UNIT
$R_{\theta JA}$	Thermal resistace, junction to ambient	Soldered pad using four-layer JEDEC board with four thermal vias	42.8	°C/W
$R_{\theta JM}$	Thermal resistance, junction to mounting surface		24.8	°C/W
$R_{\theta JC}$	Thermal resistace, junction to case	Soldered pad using two-layer JEDEC board with four thermal vias	67.6	°C/W

DEFINITIONS OF SELECTED SPECIFICATIONS

Unadjusted Carrier Suppression

This specification measures the amount by which the local oscillator component is attenuated in the output spectrum of the modulator relative to the carrier. It is assumed that the baseband inputs delivered to the pins of the TRF3702 are perfectly matched to have the same dc offset (VCM). This includes all four baseband inputs: IVIN, QVIN, IREF and QREF. Unadjusted carrier suppression is measured in dBc.

Adjusted (Optimized) Carrier Suppression

This differs from the unadjusted suppression number in that the dc offsets of the baseband inputs are iteratively adjusted around their theoretical value of VCM to yield the maximum suppression of the LO component in the output spectrum. Adjusted carrier suppression is measured in dBc.

DEFINITIONS OF SELECTED SPECIFICATIONS (continued)

Unadjusted Sideband Suppression

This specification measures the amount by which the unwanted sideband of the input signal is attenuated in the output of the modulator, relative to the wanted sideband. It is assumed that the baseband inputs delivered to the modulator input pins are perfectly matched in amplitude and are exactly 90° out of phase. Unadjusted sideband suppression is measured in dBc.

Adjusted (Optimized) Sideband Suppression

This differs from the unadjusted sideband suppression in that the baseband inputs are iteratively adjusted around their theoretical values to maximize the amount of sideband suppression. Adjusted sideband suppression is measured in dBc.

Suppressions Over Temperature

This specification assumes that the user has gone through the optimization process for the suppression in question, and set the optimal settings for the I, Q inputs at T_A = 25°C. This specification then measures the suppression when temperature conditions change after the initial calibration is done.

Figure 1 shows a simulated output and illustrates the respective definitions of various terms used in this data sheet. The graph assumes a baseband input of 50 kHz.

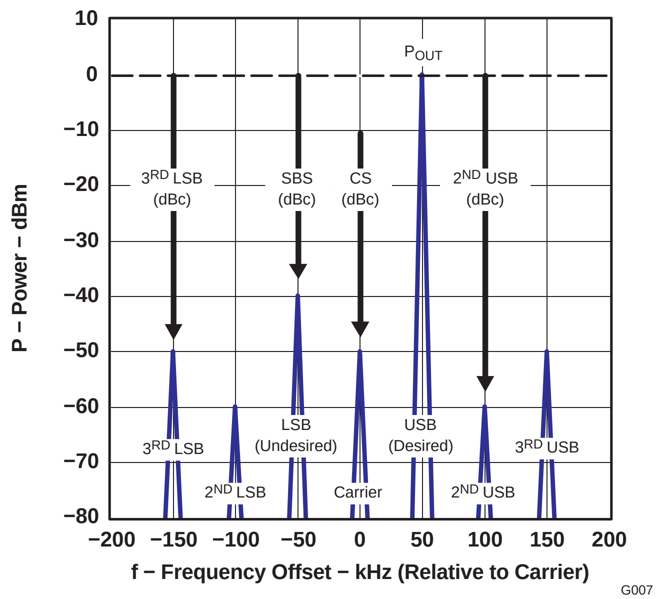


Figure 1. Graphical Illustration of Common Terms

TYPICAL CHARACTERISTICS

For all the performance plots in this section, the following conditions were used, unless otherwise noted: VCC = 5 V, VCM = 3.7 V, P_{LO} = 0 dBm, I and Q inputs driven differentially at a frequency of 50 kHz. In the case of optimized suppressions, the point of optimization is noted and is always at nominal conditions and room temperature. A level of >50 dBc is assumed to be optimized.

TYPICAL CHARACTERISTICS (continued)

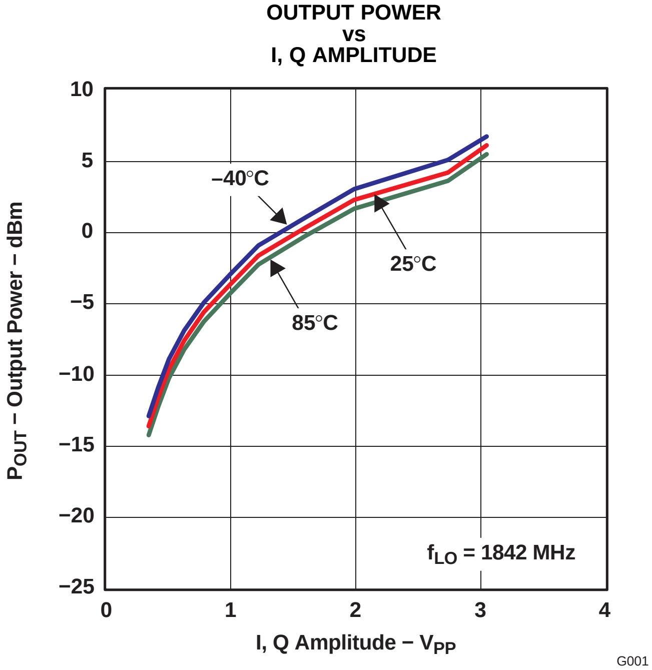


Figure 2.

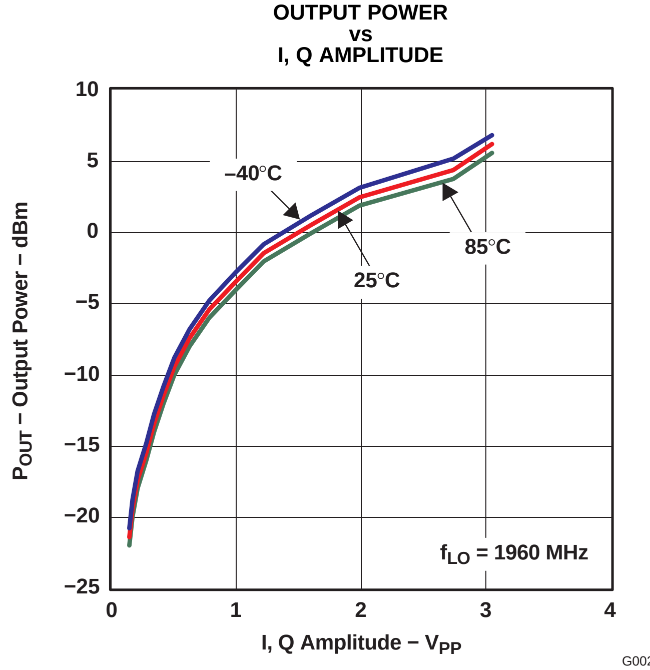


Figure 3.

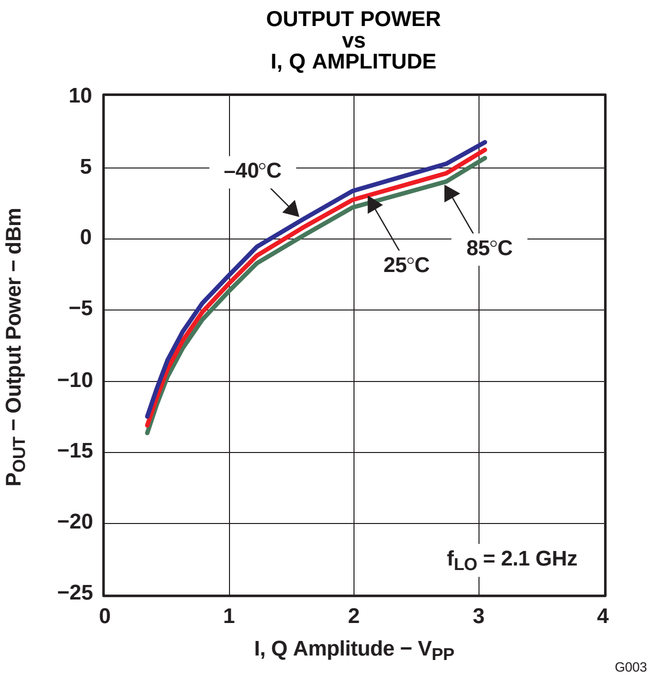


Figure 4.

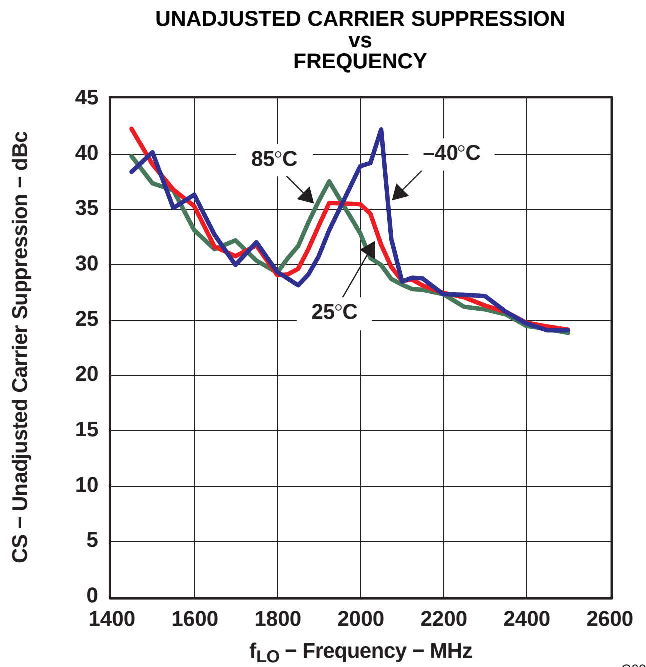


Figure 5.

TYPICAL CHARACTERISTICS (continued)

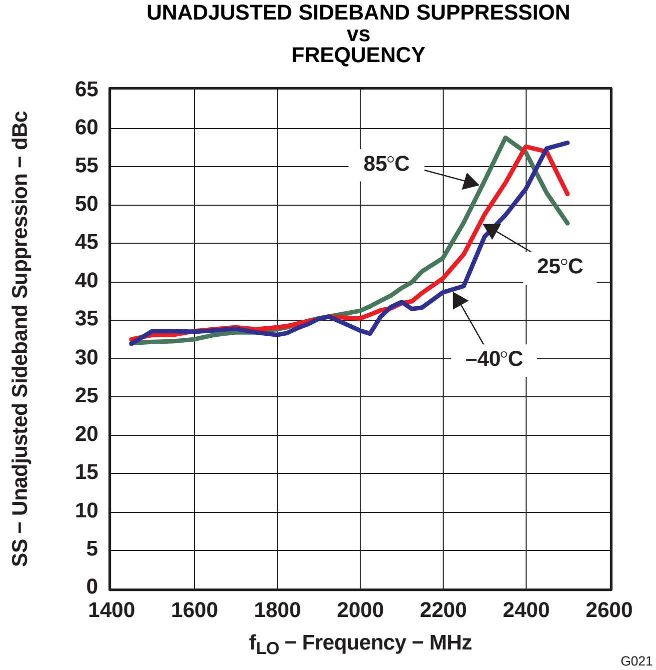


Figure 6.

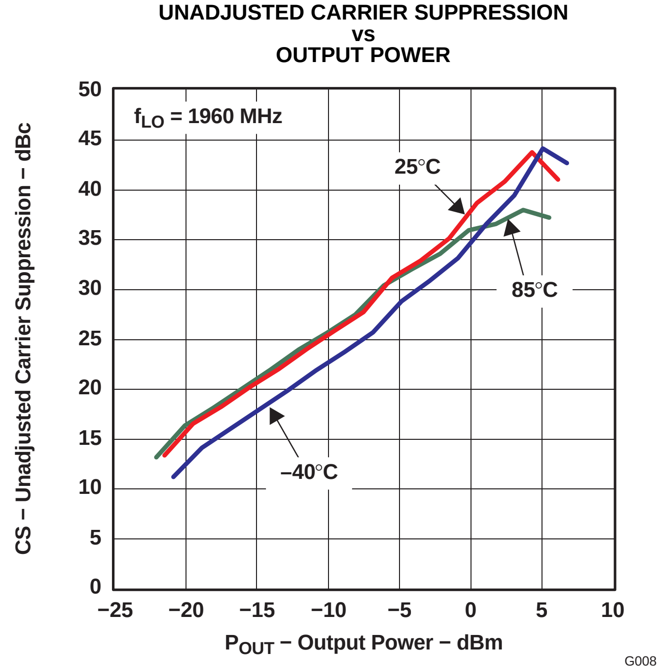


Figure 7.

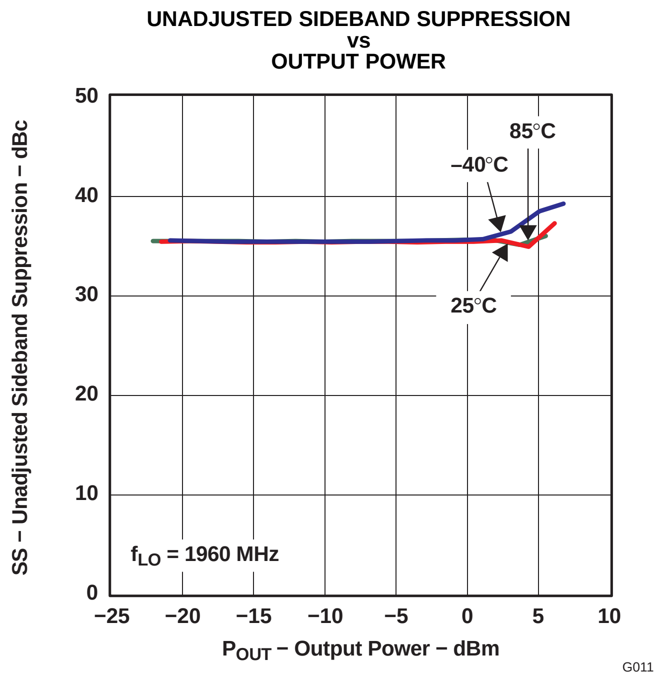


Figure 8.

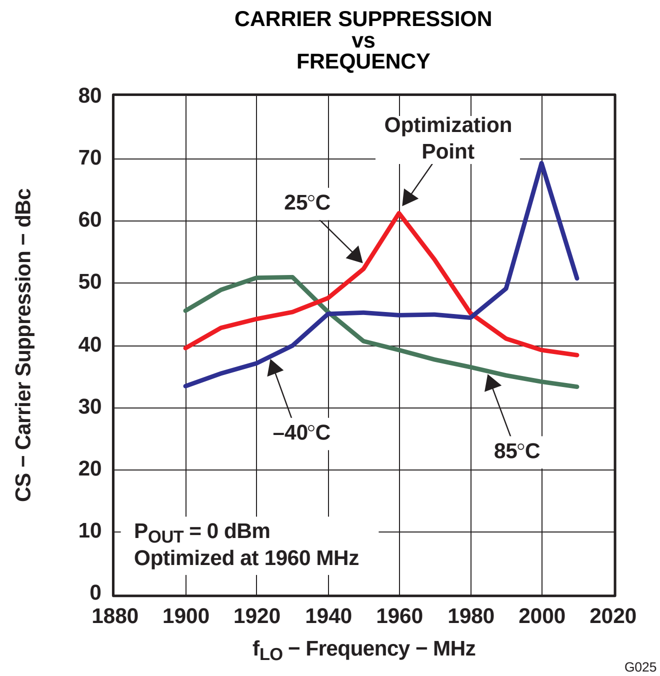


Figure 9.

TYPICAL CHARACTERISTICS (continued)

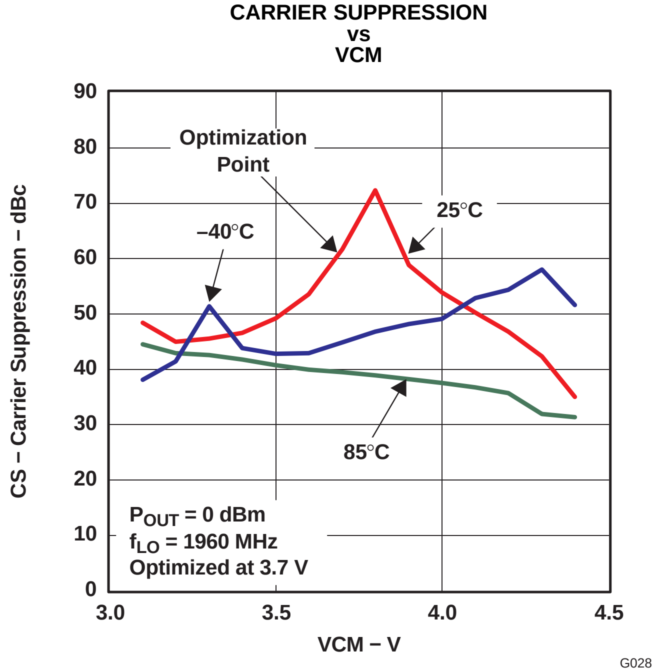


Figure 10.

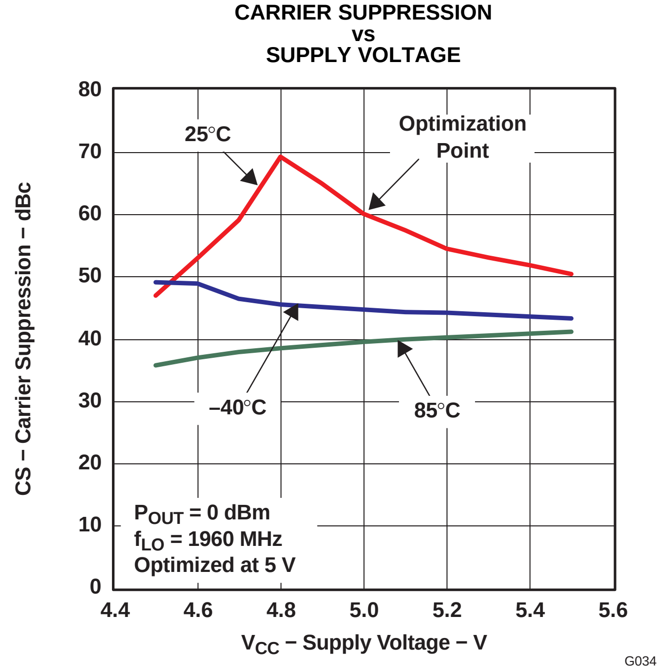


Figure 11.

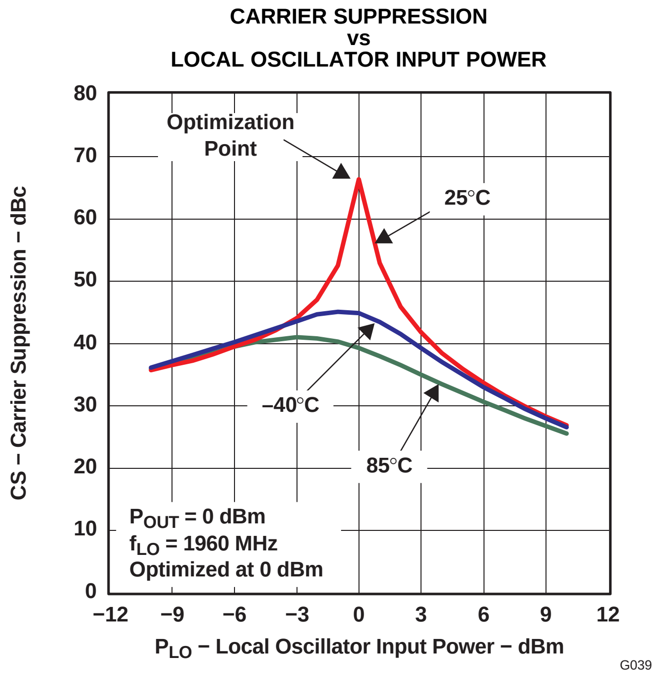


Figure 12.

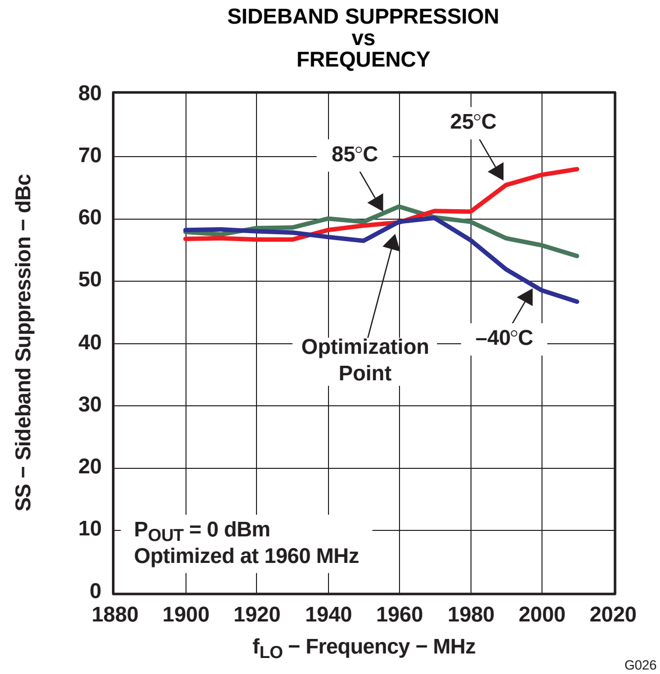


Figure 13.

TYPICAL CHARACTERISTICS (continued)

SIDEBAND SUPPRESSION
vs
VCM

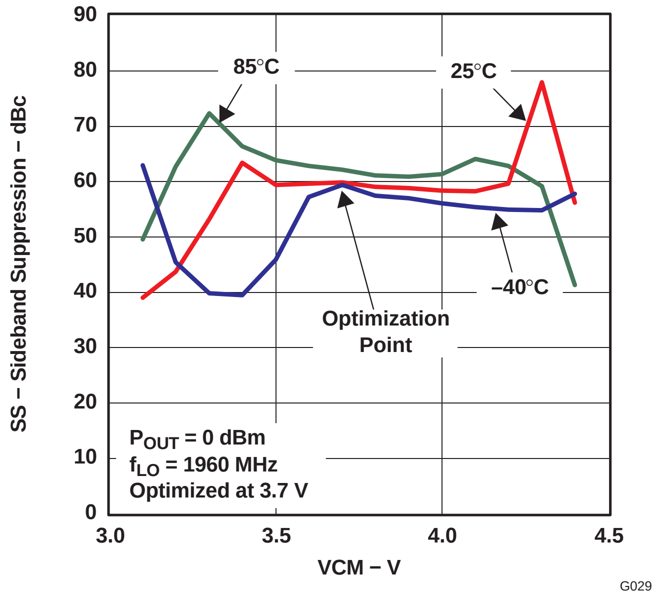


Figure 14.

SIDEBAND SUPPRESSION
vs
SUPPLY VOLTAGE

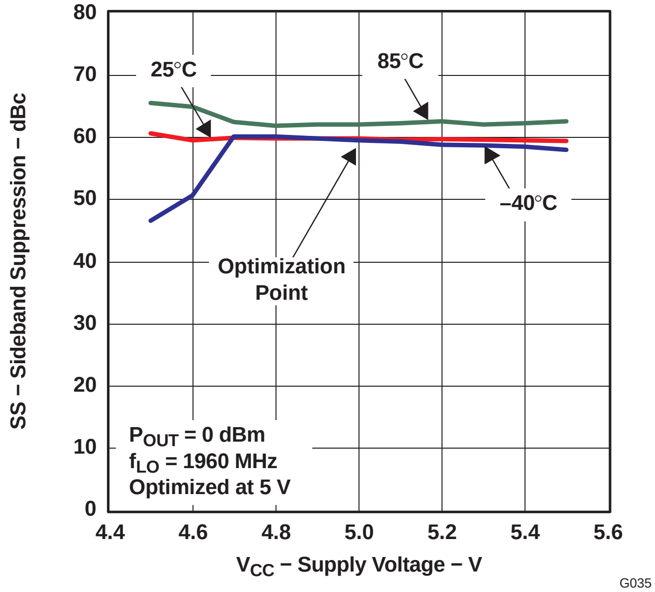


Figure 15.

SIDEBAND SUPPRESSION
vs
LOCAL OSCILLATOR INPUT POWER

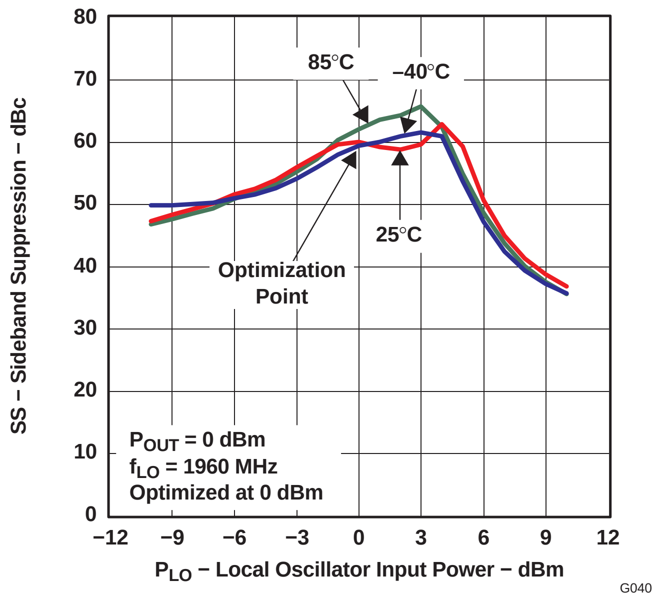


Figure 16.

CARRIER SUPPRESSION
vs
FREQUENCY

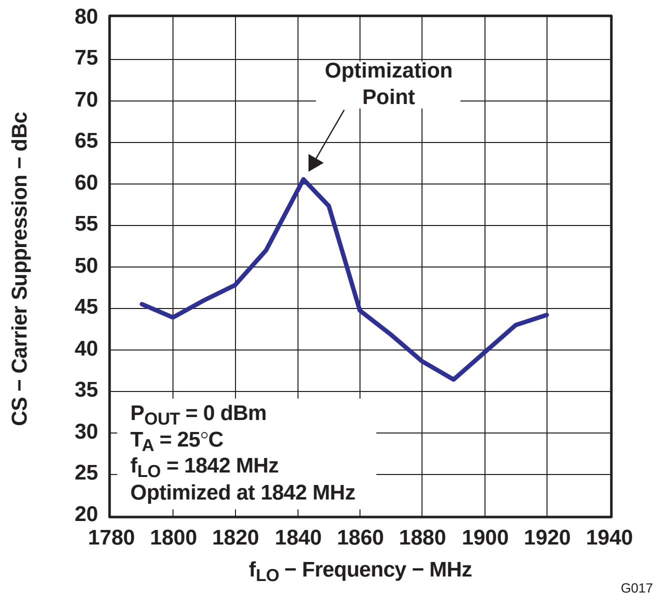


Figure 17.

TYPICAL CHARACTERISTICS (continued)

CARRIER SUPPRESSION
vs
VCM

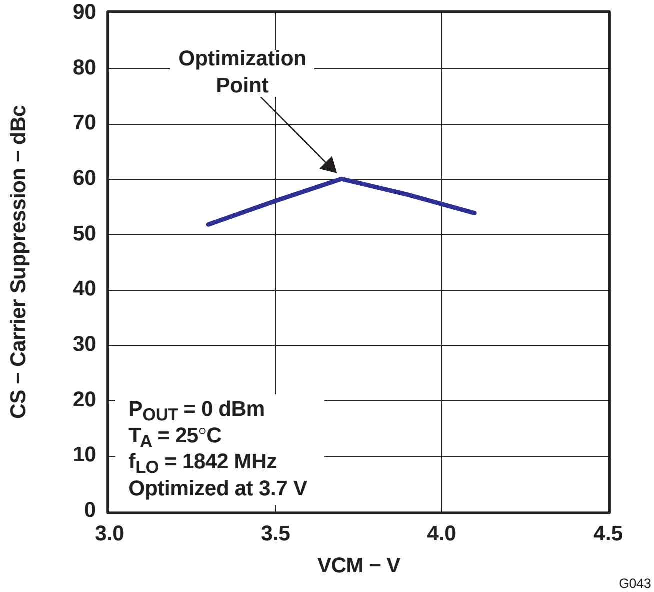


Figure 18.

CARRIER SUPPRESSION
vs
SUPPLY VOLTAGE

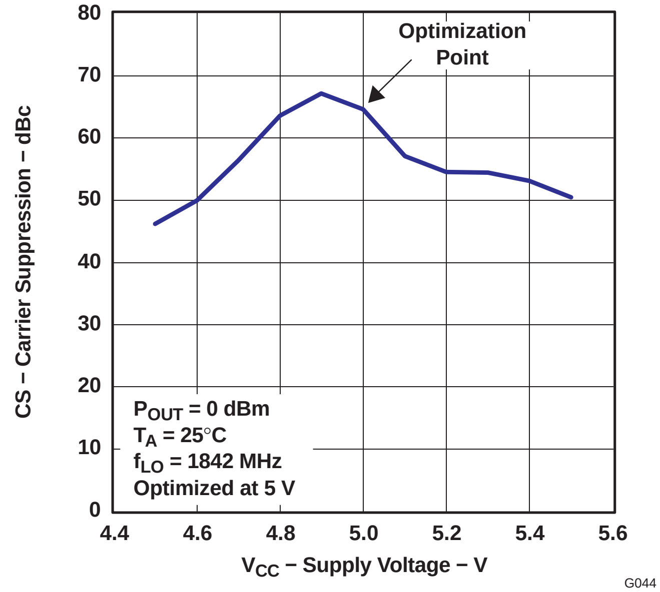


Figure 19.

CARRIER SUPPRESSION
vs
LOCAL OSCILLATOR INPUT POWER

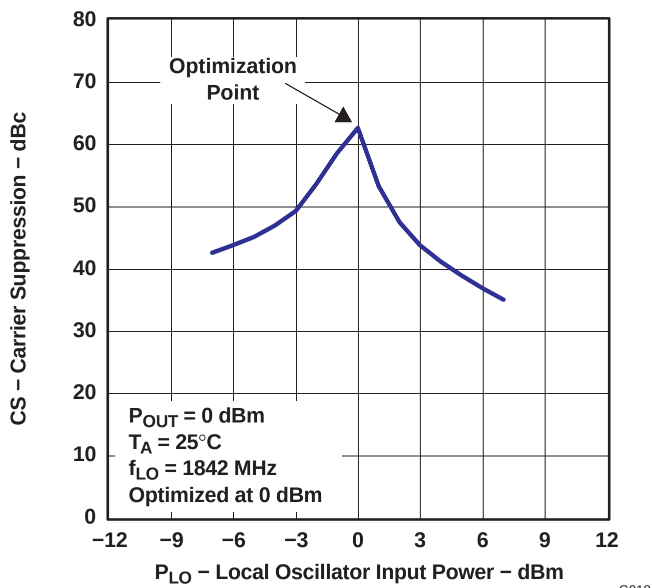


Figure 20.

SIDEBAND SUPPRESSION
vs
FREQUENCY

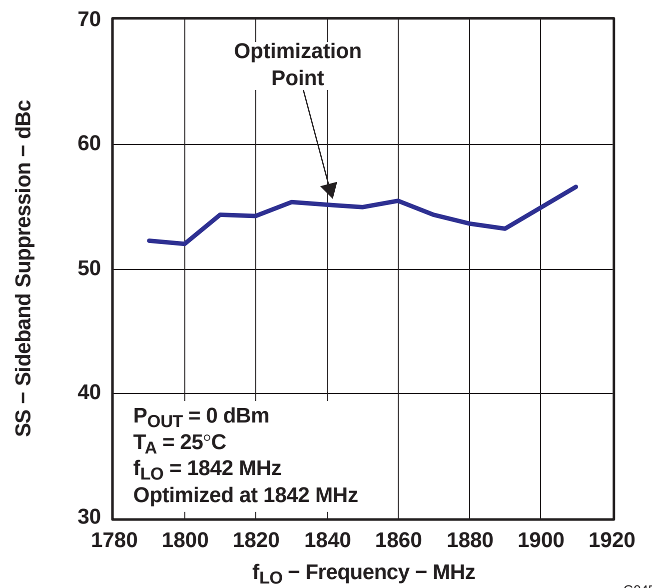


Figure 21.

TYPICAL CHARACTERISTICS (continued)

SIDEBAND SUPPRESSION vs VCM

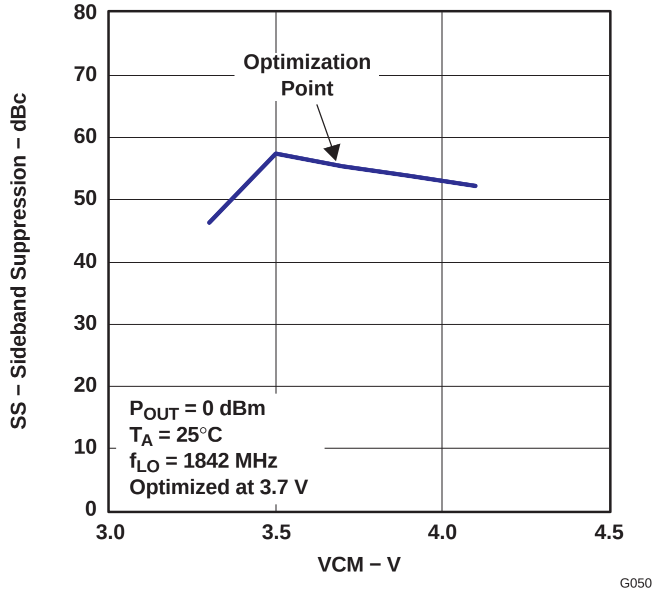


Figure 22.

SIDEBAND SUPPRESSION vs SUPPLY VOLTAGE

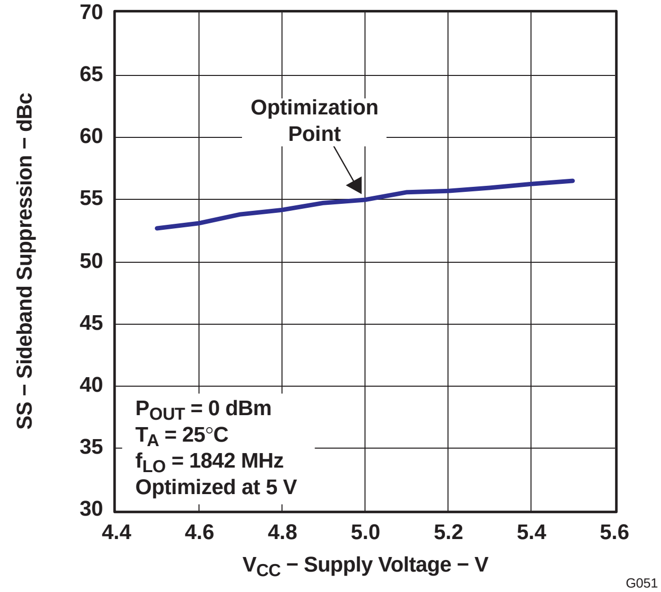


Figure 23.

SIDEBAND SUPPRESSION vs LOCAL OSCILLATOR INPUT POWER

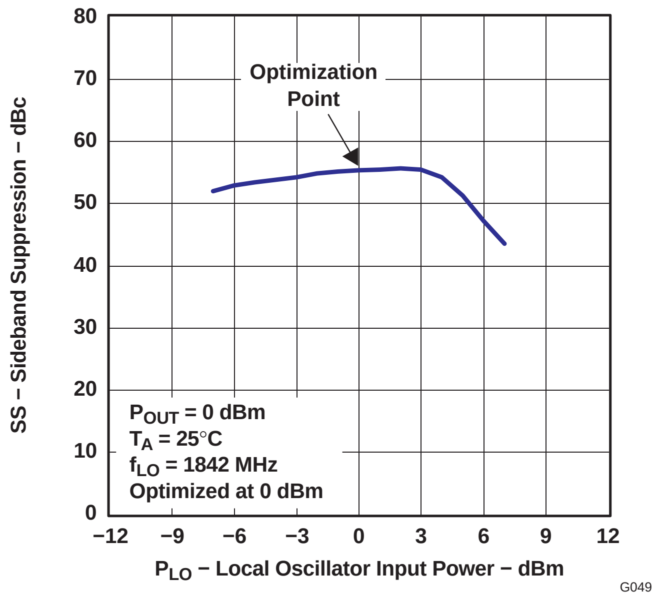


Figure 24.

CARRIER SUPPRESSION vs FREQUENCY

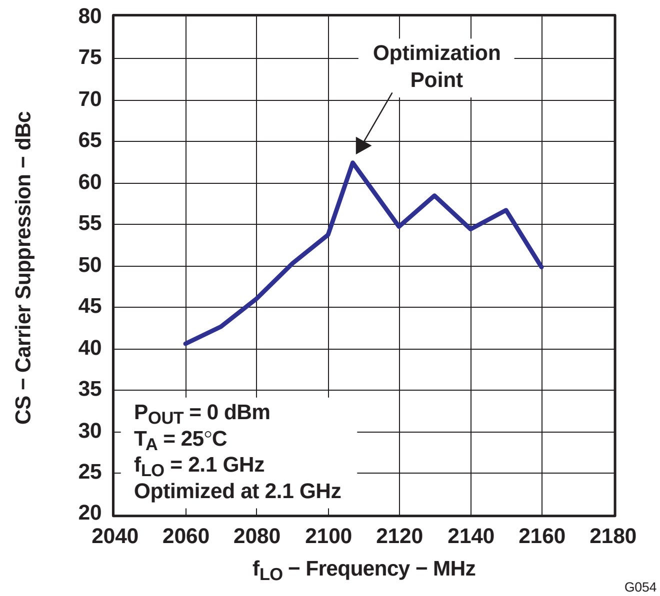


Figure 25.

TYPICAL CHARACTERISTICS (continued)

CARRIER SUPPRESSION
vs
VCM

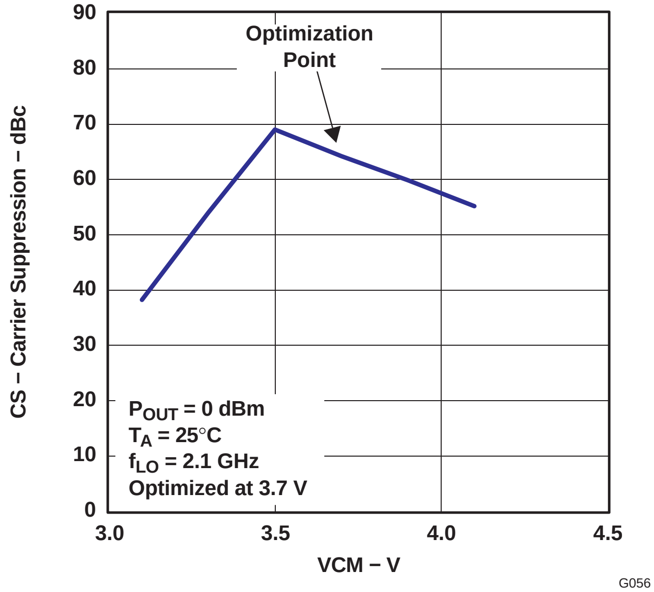


Figure 26.

CARRIER SUPPRESSION
vs
SUPPLY VOLTAGE

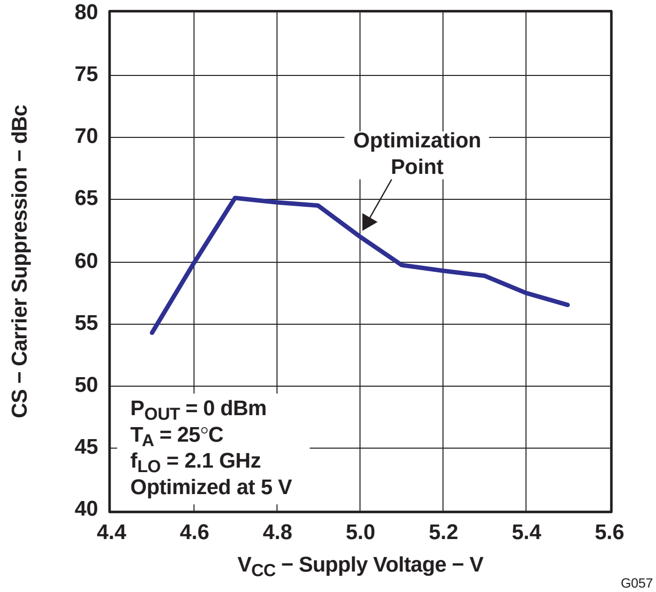


Figure 27.

CARRIER SUPPRESSION
vs
LOCAL OSCILLATOR INPUT POWER

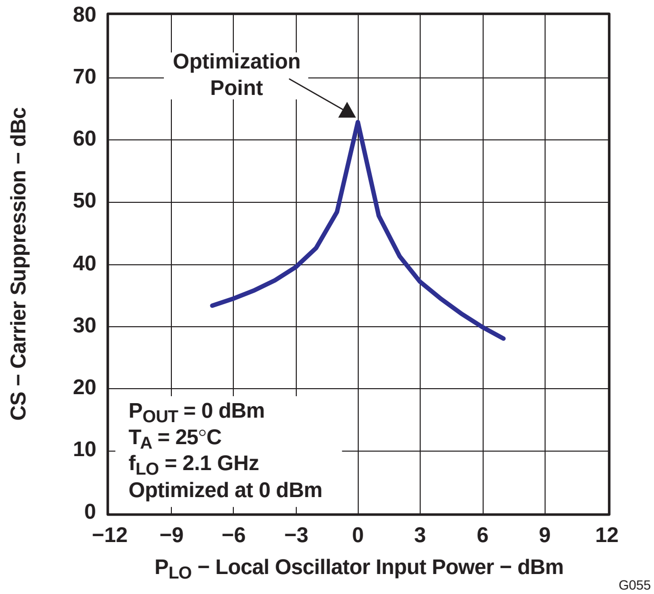


Figure 28.

SIDEBAND SUPPRESSION
vs
FREQUENCY

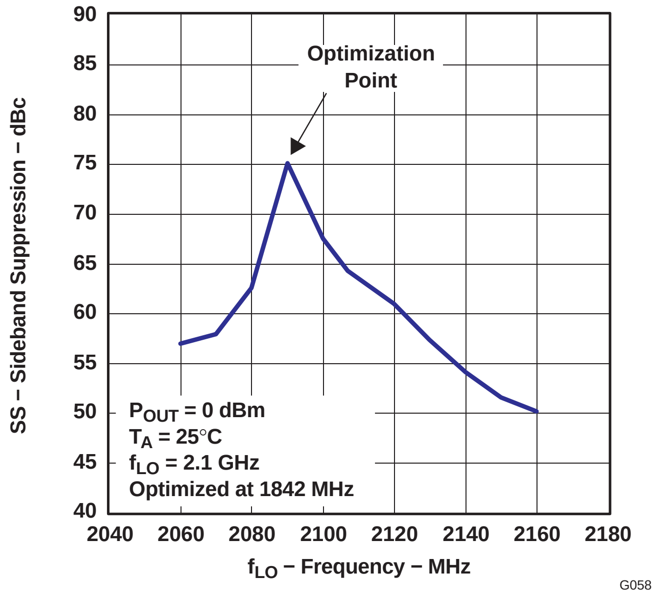


Figure 29.

TYPICAL CHARACTERISTICS (continued)

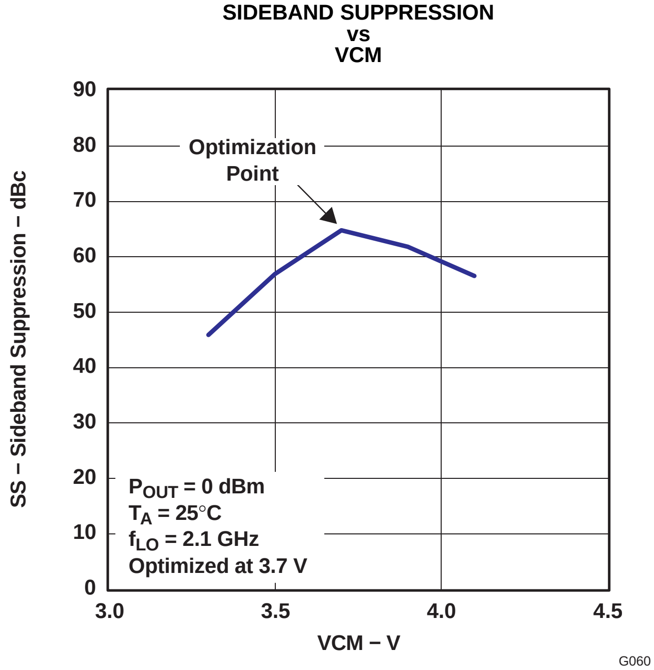
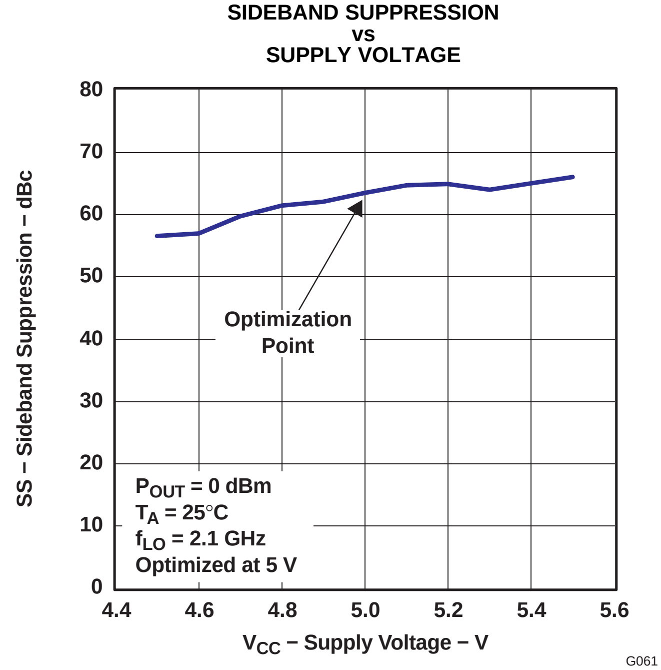


Figure 30.



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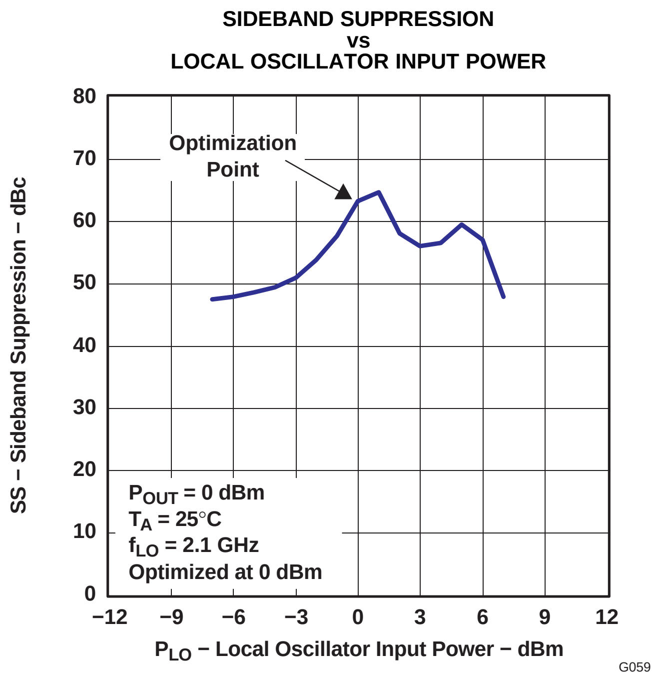

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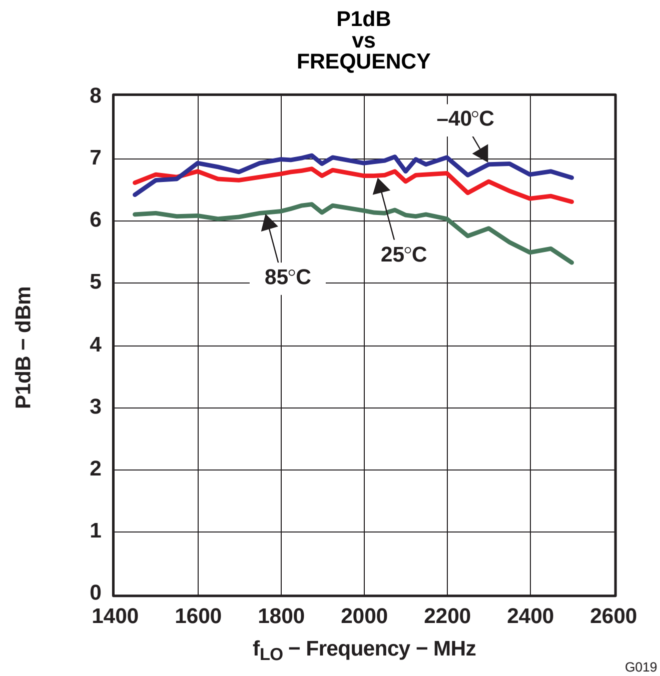

Figure 33.

TYPICAL CHARACTERISTICS (continued)

OUTPUT POWER FLATNESS
vs
FREQUENCY (P_{OUT} = 0, –10 dBm NOMINAL)

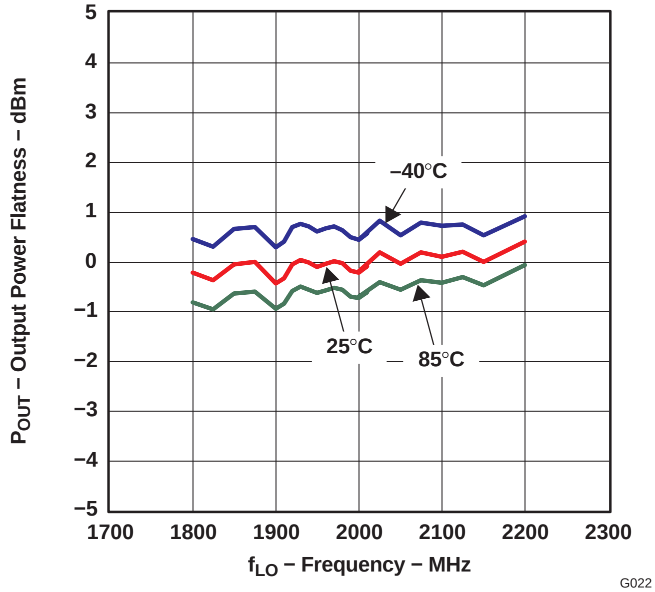

Figure 34.

OUTPUT POWER FLATNESS
vs
VCM (P_{OUT} = 0 dBm NOMINAL)

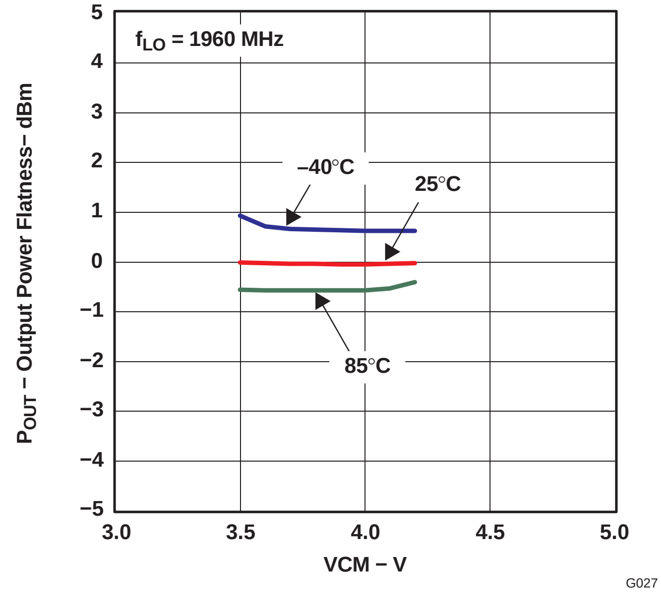

Figure 35.

OUTPUT POWER FLATNESS
vs
LO INPUT POWER (P_{OUT} = 0 dBm NOMINAL)

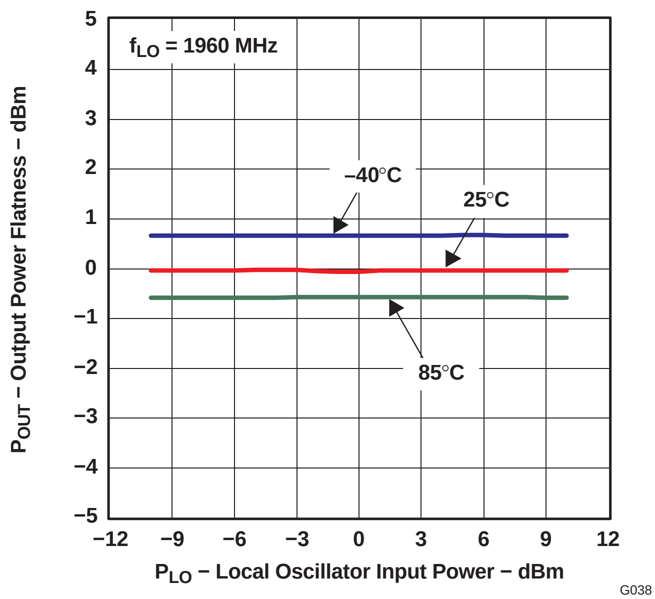

Figure 36.

OUTPUT POWER FLATNESS
vs
SUPPLY VOLTAGE (P_{OUT} = 0 dBm NOMINAL)

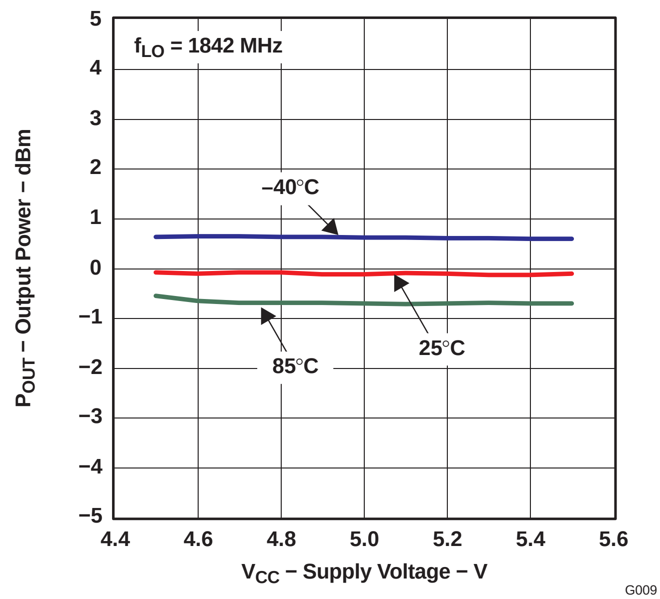

Figure 37.

TYPICAL CHARACTERISTICS (continued)

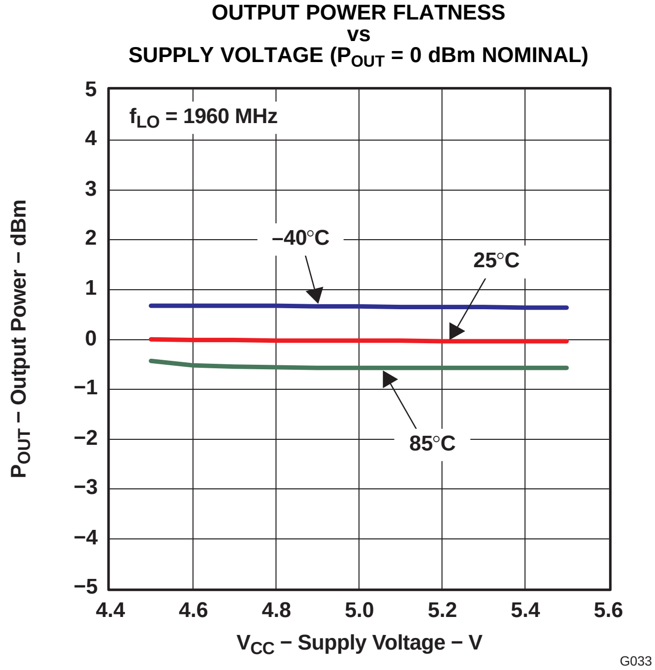

Figure 38.

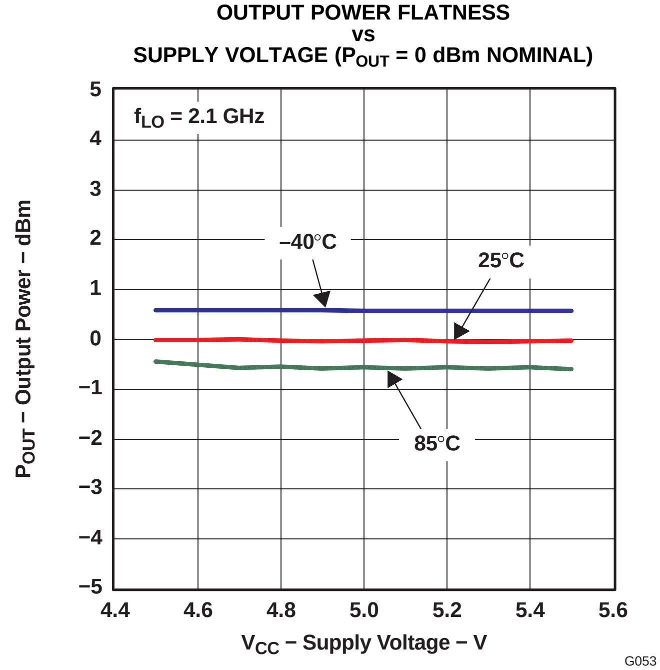

Figure 39.

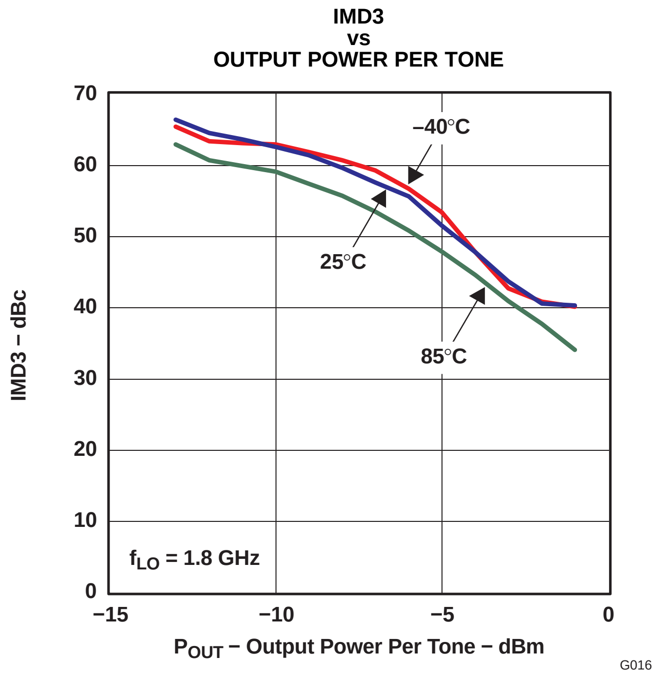

Figure 40.

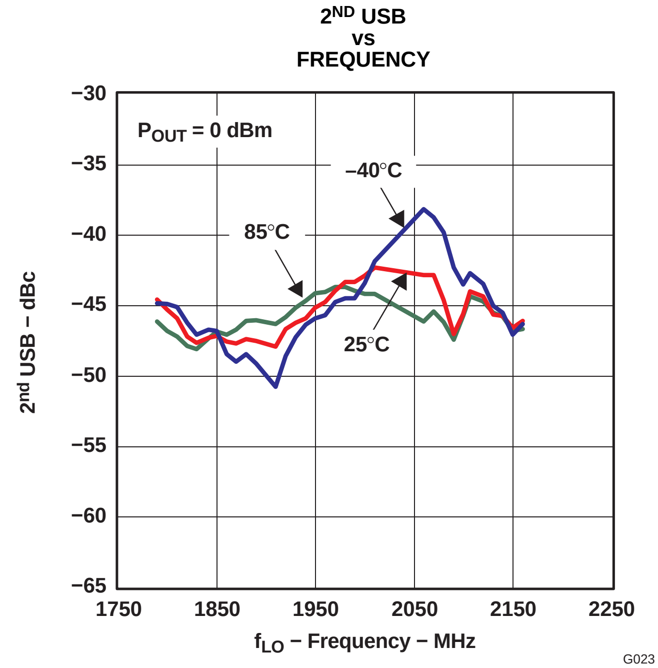

Figure 41.

TYPICAL CHARACTERISTICS (continued)

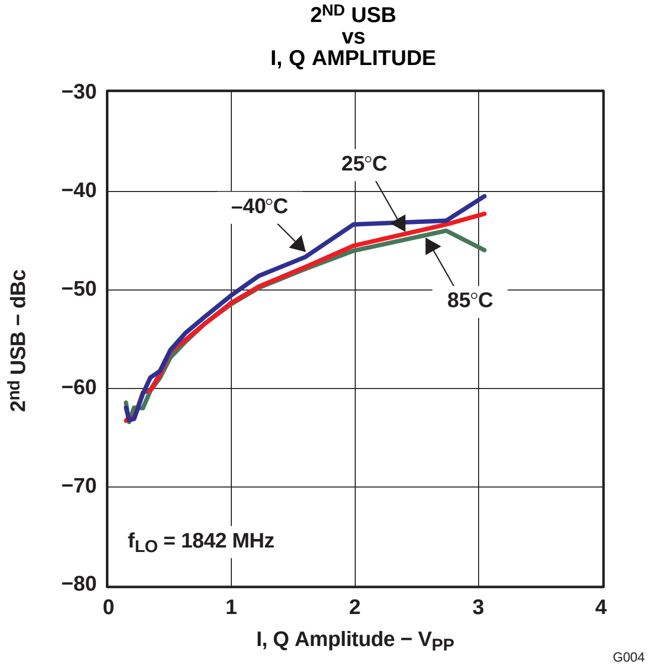

Figure 42.

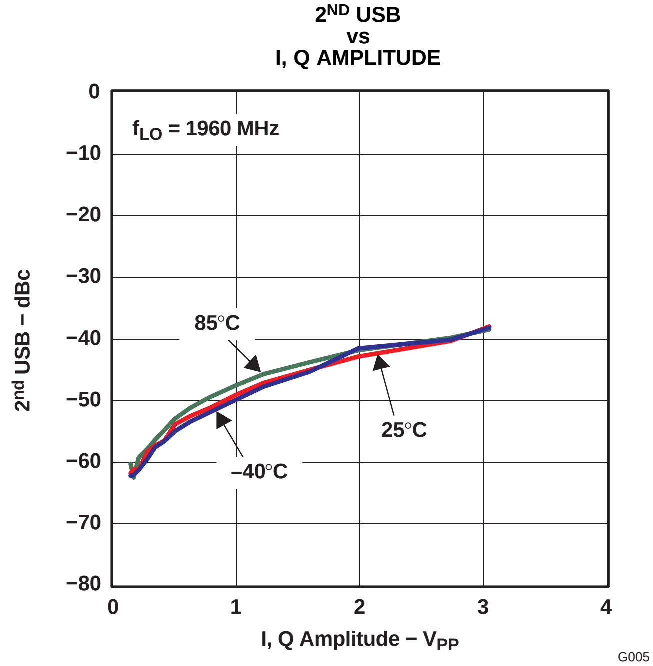

Figure 43.

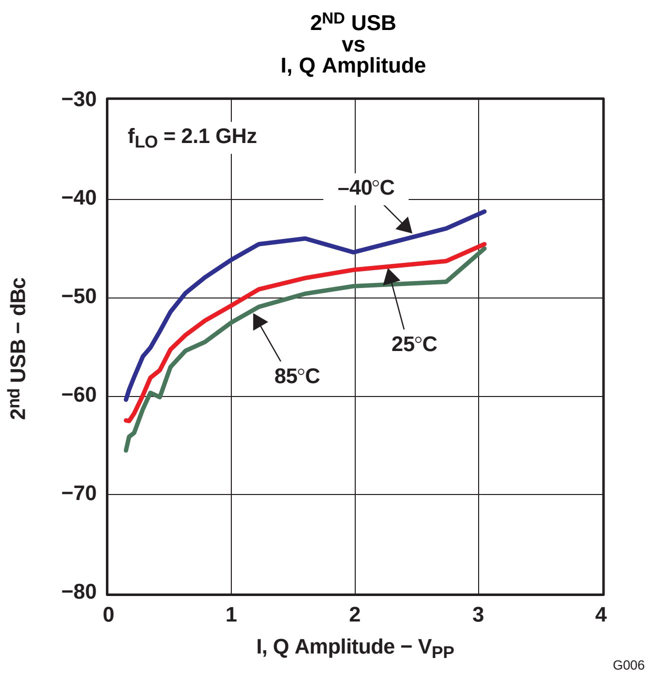

Figure 44.

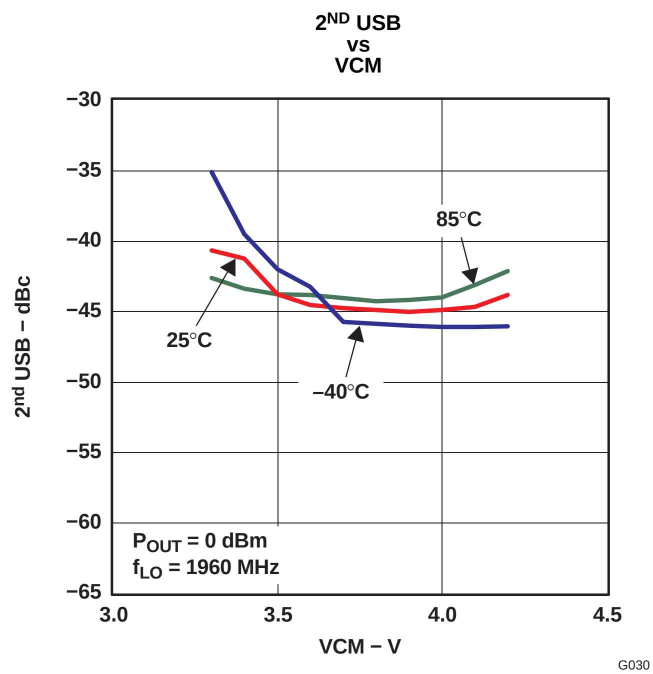

Figure 45.

TYPICAL CHARACTERISTICS (continued)

2ND USB vs SUPPLY VOLTAGE

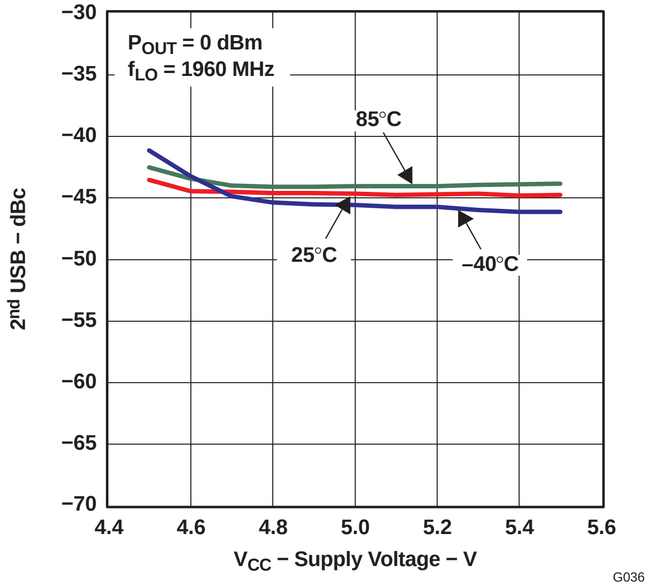

Figure 46.

2ND USB vs LOCAL OSCILLATOR INPUT POWER

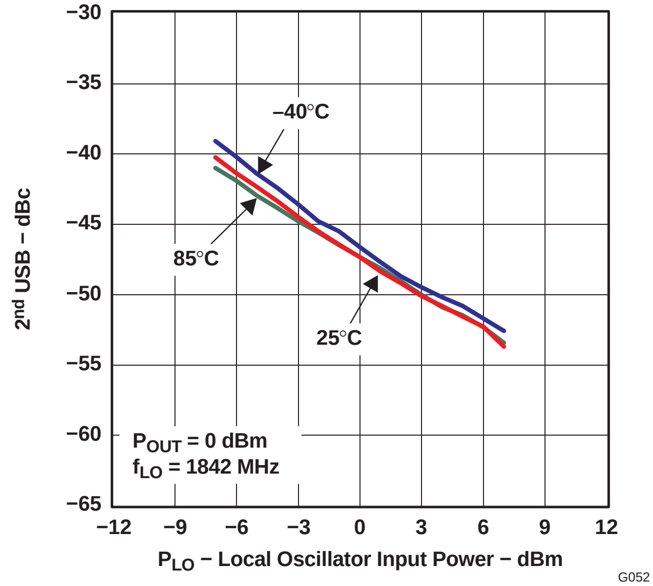

Figure 47.

2ND USB vs LOCAL OSCILLATOR INPUT POWER

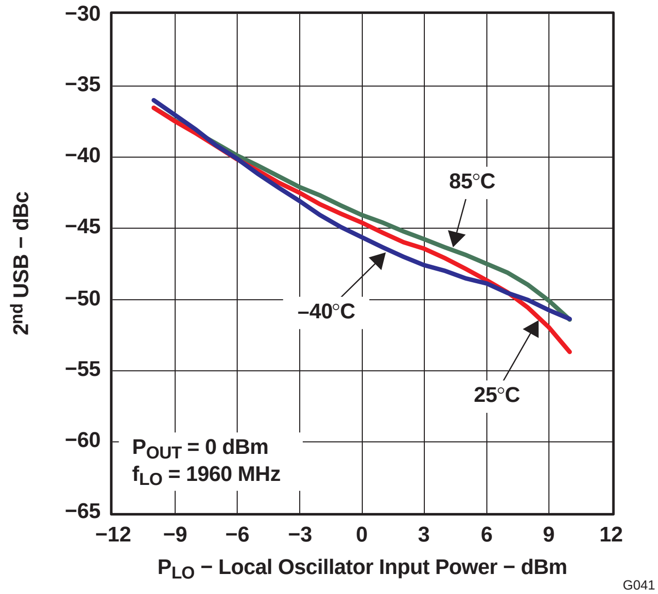

Figure 48.

2ND USB vs LOCAL OSCILLATOR INPUT POWER

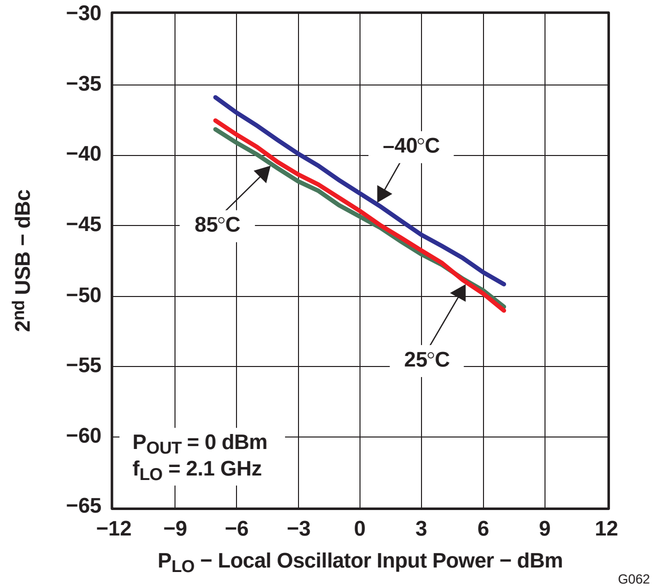

Figure 49.

TYPICAL CHARACTERISTICS (continued)

3RD LSB vs FREQUENCY

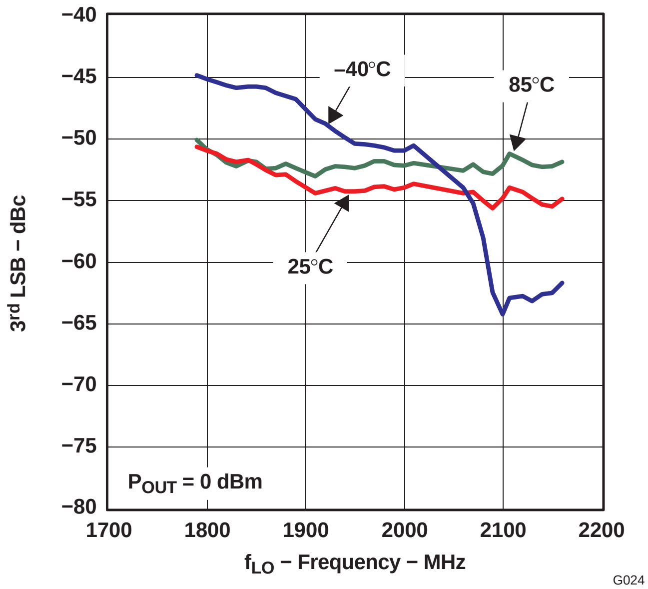

Figure 50.

3RD LSB vs I, Q AMPLITUDE

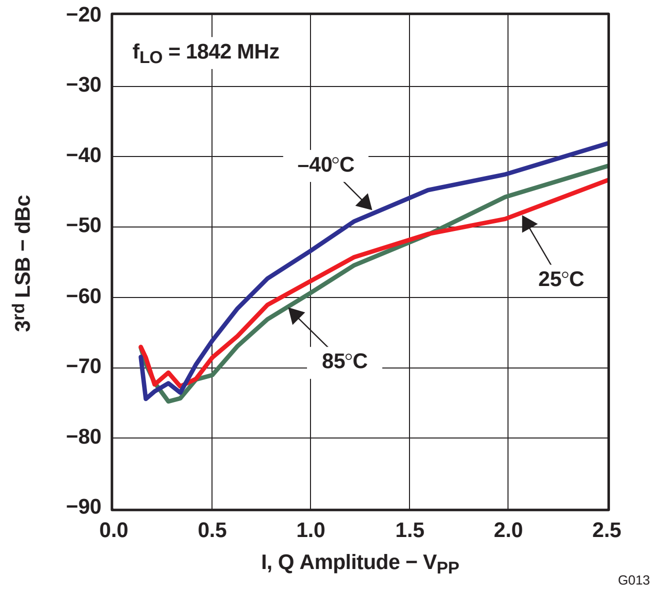

Figure 51.

3RD LSB vs I, Q AMPLITUDE

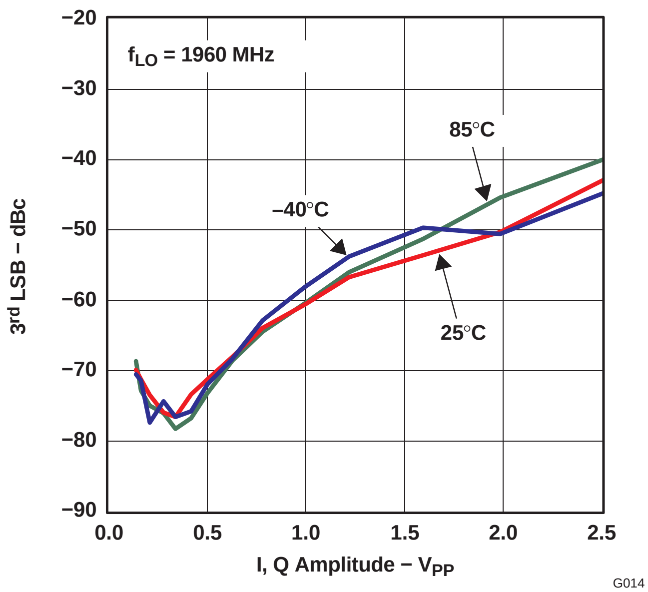

Figure 52.

3RD LSB vs I, Q AMPLITUDE

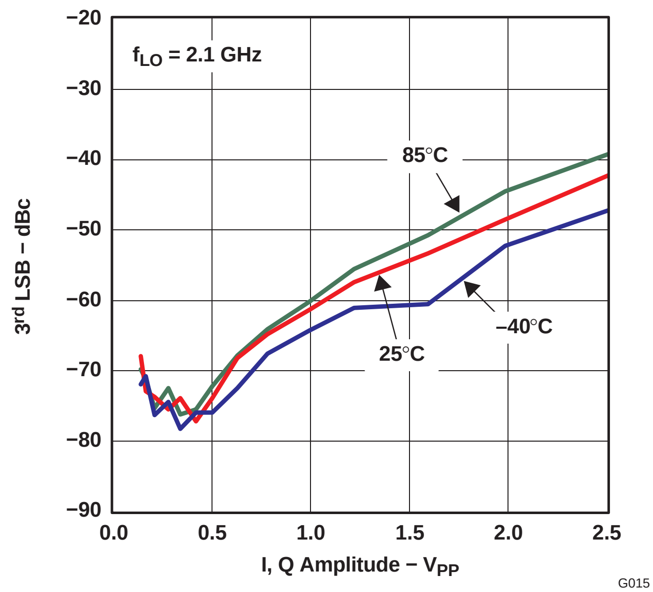

Figure 53.

TYPICAL CHARACTERISTICS (continued)

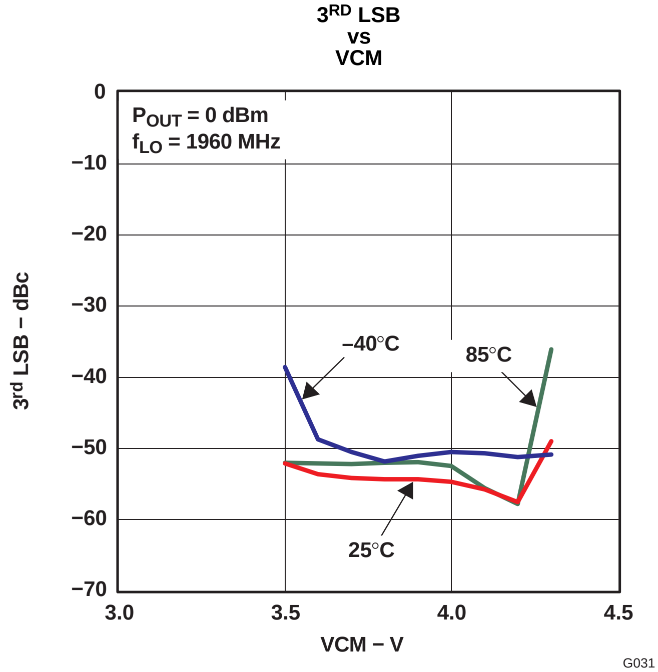

Figure 54.

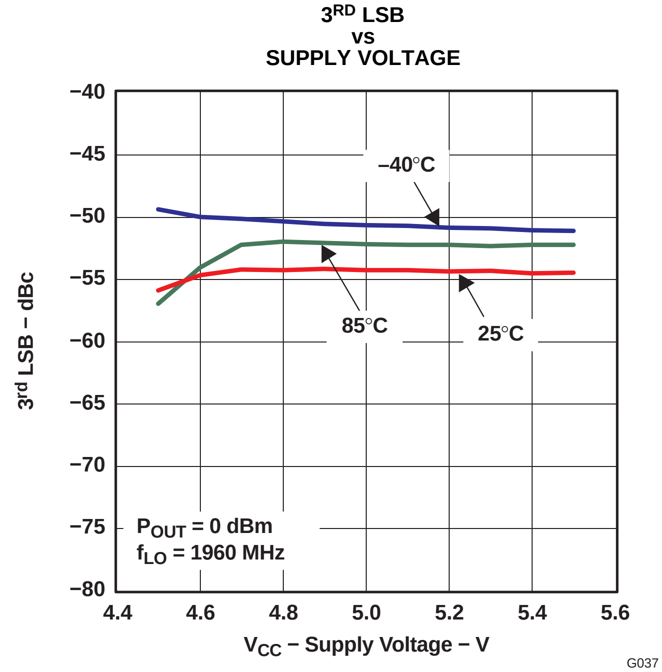

Figure 55.

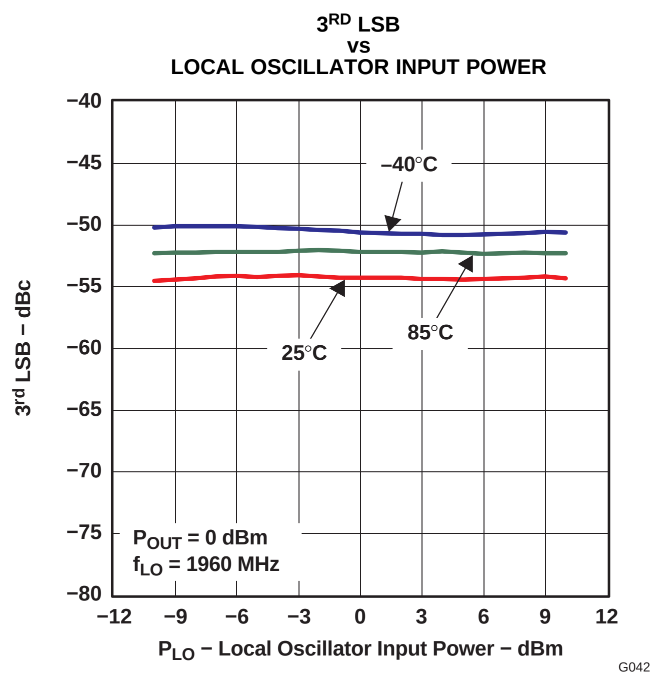

Figure 56.

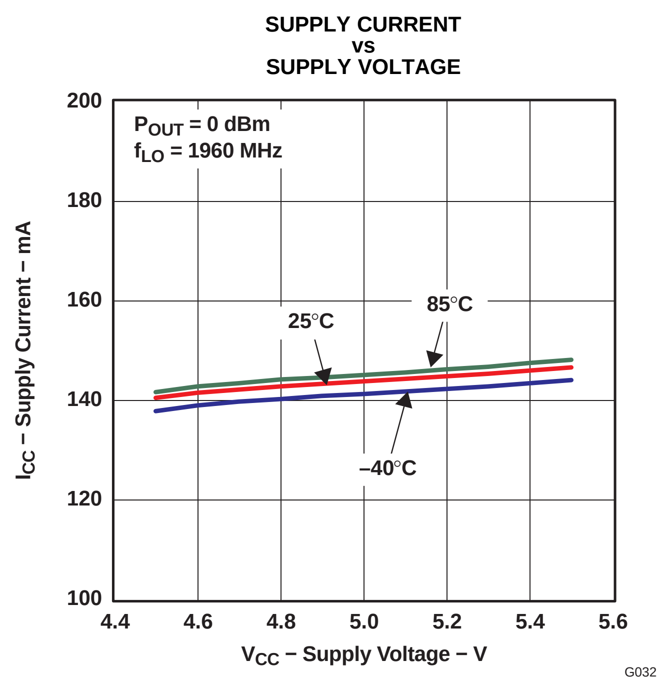

Figure 57.

TYPICAL CHARACTERISTICS (continued)

NOISE AT 6-MHz OFFSET vs OUTPUT POWER

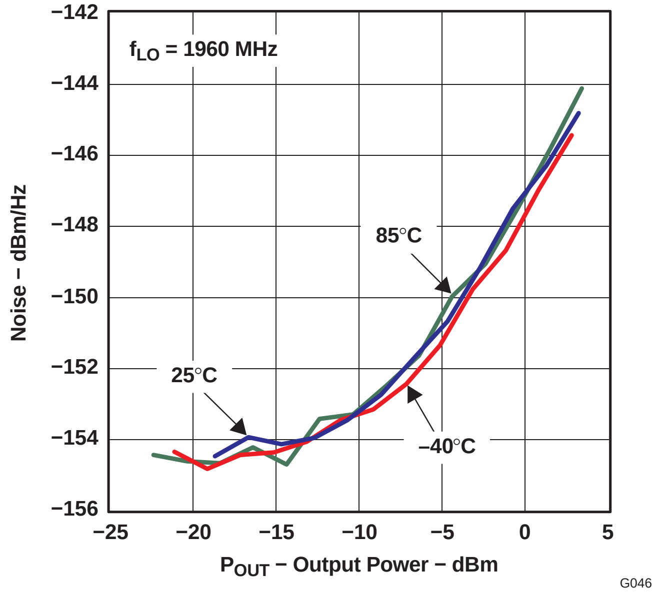

Figure 58.

NOISE AT 60-MHz OFFSET vs OUTPUT POWER

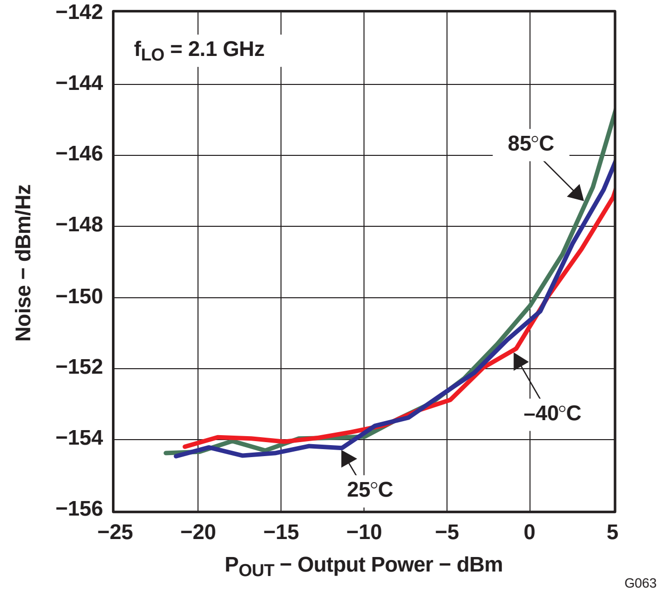

Figure 59.

NOISE DISTRIBUTION AT 6-MHz OFFSET OVER TEMPERATURE

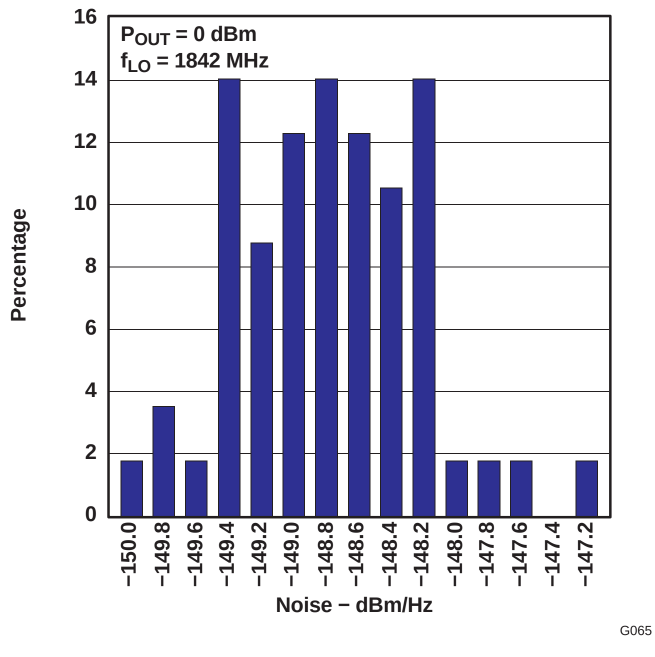

Figure 60.

NOISE DISTRIBUTION AT 6-MHz OFFSET OVER TEMPERATURE

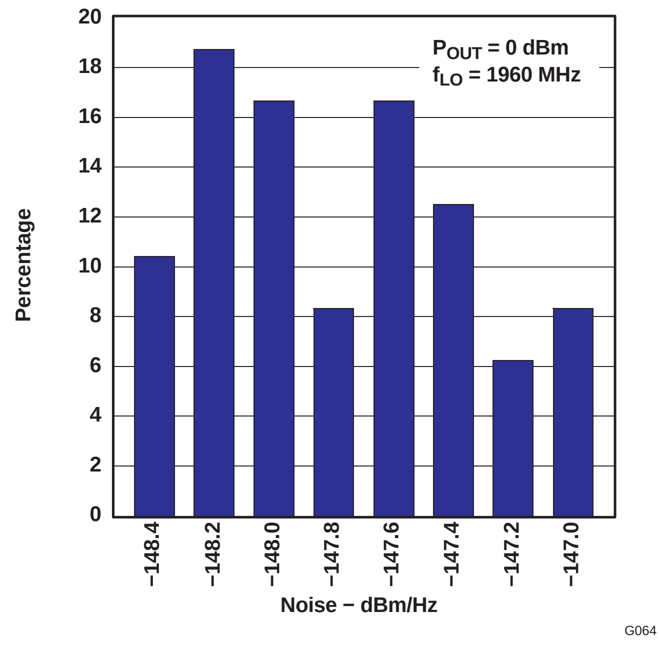

Figure 61.

TYPICAL CHARACTERISTICS (continued)

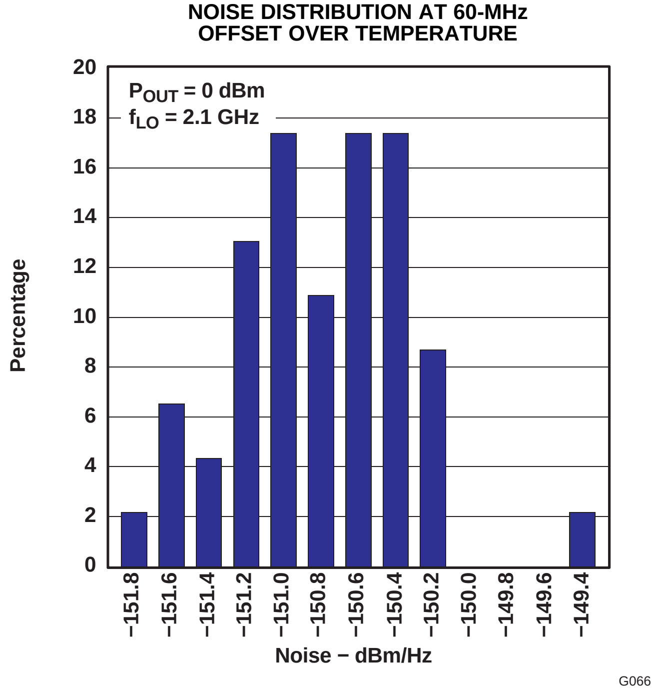

Figure 62.

THEORY OF OPERATION

The TRF3702 employs a double-balanced mixer architecture in implementing the direct I, Q upconversion. The I, Q inputs can be driven single-endedly or differentially, with comparable performance in both cases. The common mode level (VCM) of the four inputs (IVIN, IREF, QVIN, QREF) is typically set to 3.7 V and needs to be driven externally. These inputs go through a set of differential amplifiers and through a V-I converter to feed the double-balanced mixers. The ac-coupled LO input to the device goes through a phase splitter to provide the in-phase and quadrature signals that in turn drive the mixers. The outputs of the mixers are then summed, converted to single-ended signals, and amplified before they are fed to the output port RFOUT. The output of the TRF3702 is ac-coupled and can drive 50-Ω loads.

EQUIVALENT CIRCUITS

Figure 63 through Figure 66 show equivalent schematics for the main inputs and outputs of the device.

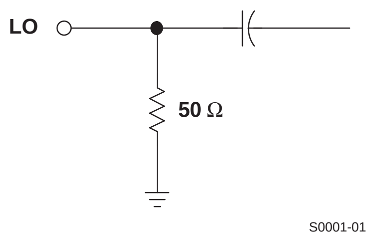

Figure 63. LO Equivalent Input Circuit

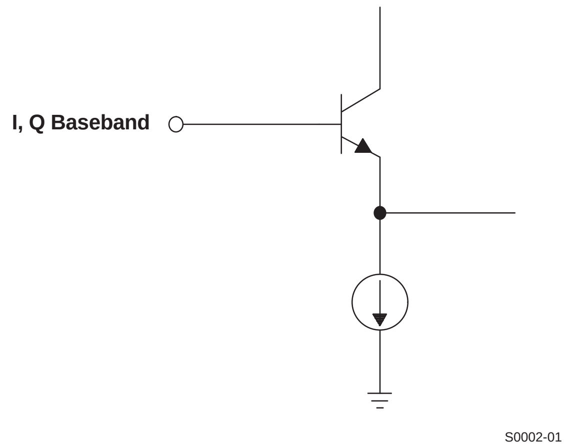

Figure 64. IVIN, QVIN, IREF, QREF Equivalent Circuit

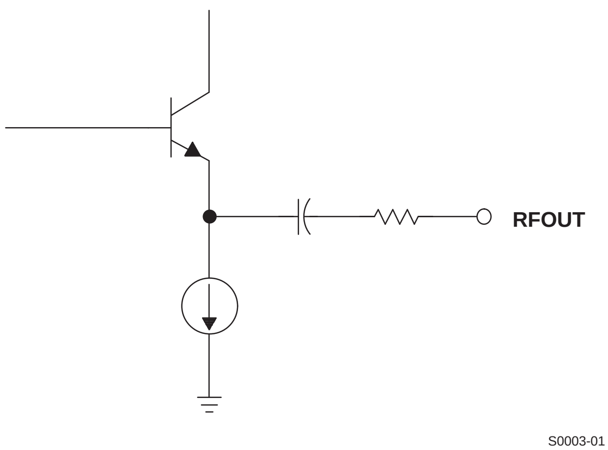

Figure 65. RFOUT Equivalent Circuit

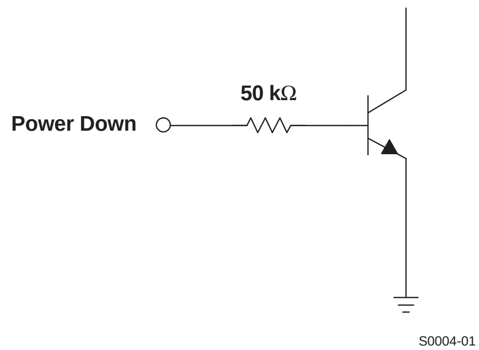

Figure 66. Power-Down (PWD) Equivalent Circuit

APPLICATION INFORMATION

DRIVING THE I, Q INPUTS

There are several ways to drive the four baseband inputs of the TRF3702 to the required amplitude and dc offset. The optimal configuration depends on the end application requirements and the signal levels desired by the designer.

The TRF3702 is by design a differential part, meaning that ideally the user should provide fully complementary signals. However, similar performance in every respect can be achieved if the user only has single-ended signals available. In this case, the IREF and QREF pins just need to have the VCM dc offset applied.

Implementing a Single-to-Differential Conversion for the I, Q inputs

In case differential I, Q signals are desired but not available, the THS4503 family of wideband, low-distortion, fully differential amplifiers can be used to provide a convenient way of performing this conversion. Even if differential signals are available, the THS4503 can provide gain in case a higher voltage swing is required. Besides featuring high bandwidth and high linearity, the THS4503 also provides a convenient way of applying the VCM to all four inputs to the modulator through the VOCM pin (pin 2). The user can further adjust the dc levels for optimum carrier suppression by injecting extra dc at the inputs to the operational amplifier, or by individually adding it to the four outputs. Figure 67 shows a typical implementation of the THS4503 as a driver for the TRF3702. Gain can be easily incorporated in the loop by adjusting the feedback resistors appropriately. For more details, see the THS4503 data sheet at www.ti.com.

APPLICATION INFORMATION (continued)

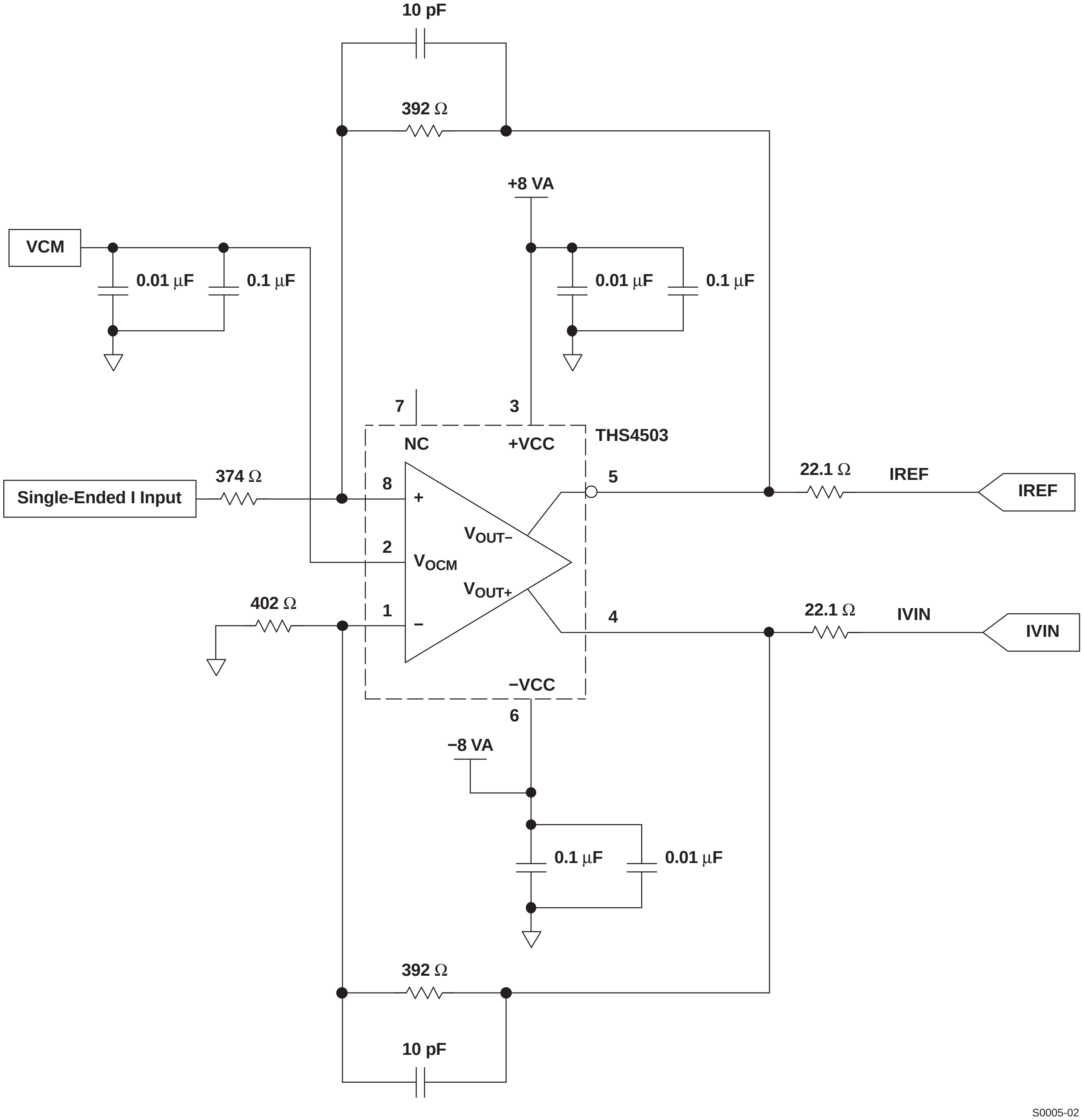

Figure 67. Using the THS4503 to Condition the Baseband Inputs to the TRF3702 (I Channel Shown)

APPLICATION INFORMATION (continued)

DRIVING THE LOCAL OSCILLATOR INPUT

The LO pin is internally terminated to 50 Ω, thus enabling easy interface to the LO source without the need for external impedance matching. The power level of the LO signal should be in the range of –6 dBm to 6 dBm. For characterization purposes, a power level of 0 dBm was chosen. An ideal way of driving the LO input of the TRF3702 is by using the TRF3750, an ultralow-phase-noise integer-N PLL from Texas Instruments. Combining the TRF3750 with an external VCO can complete the loop and provide a flexible, convenient, and cost-effective solution for the local oscillator of the transmitter. Figure 68 shows a typical application for the LO driver network that incorporates the TRF3750 integer-N PLL synthesizer into the design. Depending on the VCO output and the amount of signal loss, an optional gain stage may be added to the output of the VCO before it is applied to the TRF3702 LO input.

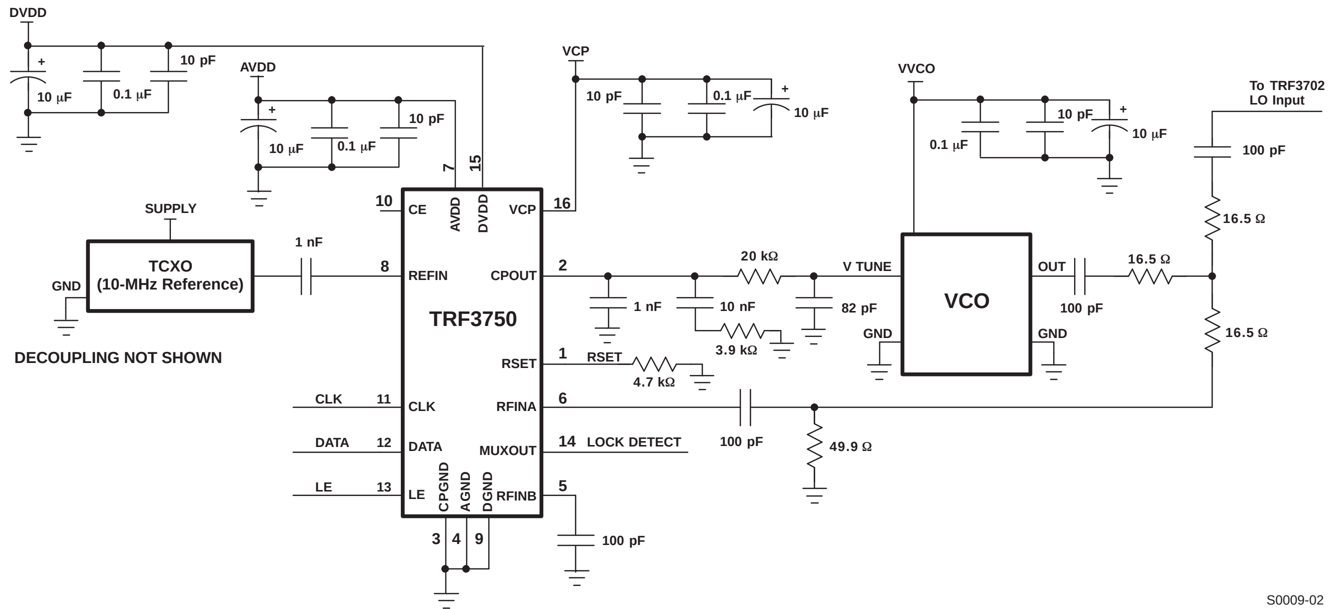

Figure 68. Typical Application Circuit for Generating the LO Signal for the TRF3702 Modulator

PCB LAYOUT CONSIDERATIONS

The TRF3702 is a high-performance RF device; hence, care should be taken in the layout of the PCB in order to ensure optimum performance. Proper decoupling with low-ESR ceramic chip capacitors is needed for the VCC supplies (pins 6 and 10). Typical values used are in the order of 1 pF parallel to 0.1 µF, with the lower-valued capacitors placed closer to the device pins. In addition, a larger tank capacitor in the order of 10 µF should be placed on the supply line as layout permits. At least a 4-layer board is recommended for the PCB. If possible, a solid ground plane and a ground pour is also recommended, as is a power plane for the supplies. Because the balance of the four I, Q inputs to the modulator can be critical to device performance, care should be taken to ensure that the trace runs for all four inputs are equal in length. In the case of single-ended drive of the I, Q inputs, the two unused pins IREF and QREF are fed with the VCM dc voltage only, and should be decoupled with a 0.1-µF capacitor (or smaller). The LO input trace should be minimized in length and have controlled impedance of 50 Ω. No external matching components are needed because there is an internal 50-Ω termination. The RFOUT pin should also have a relatively small trace to minimize parasitics and coupling, and should also be controlled to 50 Ω. An impedance-matching network can be used to optimize power transfer, but is not critical. All the results shown in the data sheet were taken with no impedance matching network used (RFOUT directly driving an external 50-Ω load).

The exposed thermal and ground pad on the bottom of the TRF3702 should be soldered to ground to ensure optimum electrical and thermal performance. The landing pattern on the PCB should include a solid pad and 4 thermal vias. These vias typically have 1,2-mm pitch and 0,3-mm diameter. The vias can be arranged in a 2×2 array. The thermal pad on the PCB should be at least 1,65×1,65 mm. A suggested layout is shown in Figure 69.

APPLICATION INFORMATION (continued)

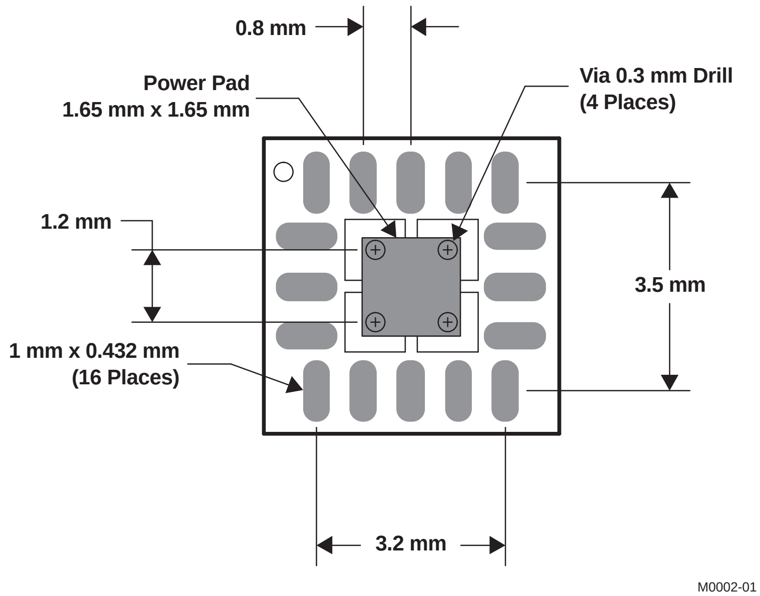

Figure 69. Board Layout for the TRF3702 Device

IMPLEMENTING A DIRECT UPCONVERSION TRANSMITTER USING A TI DAC

The TRF3702 is ideal for implementing a direct upconversion transmitter, where the input I, Q data can originate from an ASIC or a DAC. Texas Instruments' line of digital-to-analog converters (DAC) is ideally suited for interfacing to the TRF3702. Such DACs include, among others, the DAC290x series, DAC5672, and DAC5686.

This section illustrates the use of the DAC5686, which offers a unique set of features that make interfacing to the TRF3702 easy and convenient. The DAC5686 is a 16-bit, 500 MSPS, 2×–16× interpolating dual-channel DAC, and it features I, Q adjustments for optimal interface to the TRF3702. User-selectable, 11-bit offset and 12-bit gain adjustments can optimize the carrier and sideband suppression of the modulator, resulting in enhanced performance and relaxed filtering requirements at RF. The preferred mode of operation of the DAC5686 for direct interface with the TRF3702 at baseband is the dual-DAC mode. The user also has the flexibility of selecting any one of the four possible complex spectral bands to be fed into the TRF3702. For details on the available modes and programming, see the DAC5686 data sheet available at www.ti.com.

Figure 70 shows the DAC5686 in dual-DAC mode, which is best-suited for zero-IF interface to the TRF3702. In this mode, a seamless, passive interface between the DAC output and the input to the modulator is used, so that no extra components are needed between the two devices. The optimum dc offset level for the inputs to the TRF3702 (VCM) is approximately 3.7 V. The output of the DAC should be centered around 3.3 V or less (depending on signal swing), in order to ensure that its output compliance limits are not exceeded. The resistive network shown in Figure 70 allows for this dc offset transition while still providing a dc path between the DAC output and the modulator. This ensures that the dc offset adjustments on the DAC5686 can still be applied to optimize the carrier suppression at the modulator output. The combination of the DAC5686 and the TRF3702 provides a unique signal-chain solution with state-of-the-art performance for wireless infrastructure applications.

APPLICATION INFORMATION (continued)

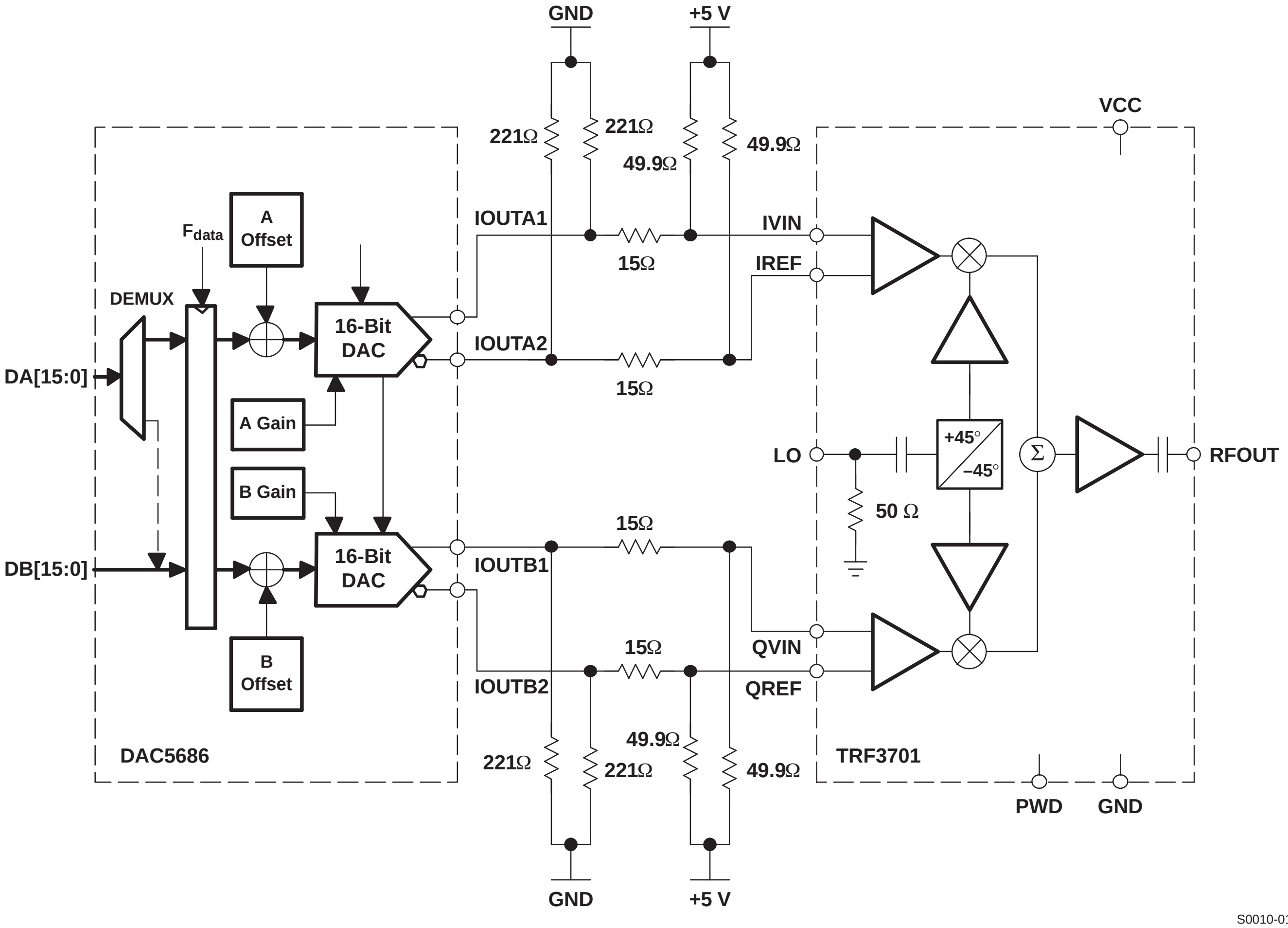

Figure 70. DAC5686 in Dual-DAC Mode With Quadrature Modulator

GSM Applications

The TRF3702 is ideally suited for GSM applications, because it combines high linearity with low noise levels. Figure 60 and Figure 61 show the distribution of noise vs output power for the TRF3702 over the entire recommended temperature range. The level of noise attained in combination with the superior IMD3 performance shown in Figure 40 means that the user can reach superior levels of C/N while maintaining high linearity. This combination offers the capability of delivering low levels of EVM, meeting the stringent requirements imposed by the GSM/EDGE standards. Figure 71 shows the spectral mask compliance for the device versus channel power, for both 400-kHz and 600-kHz offsets.

APPLICATION INFORMATION (continued)

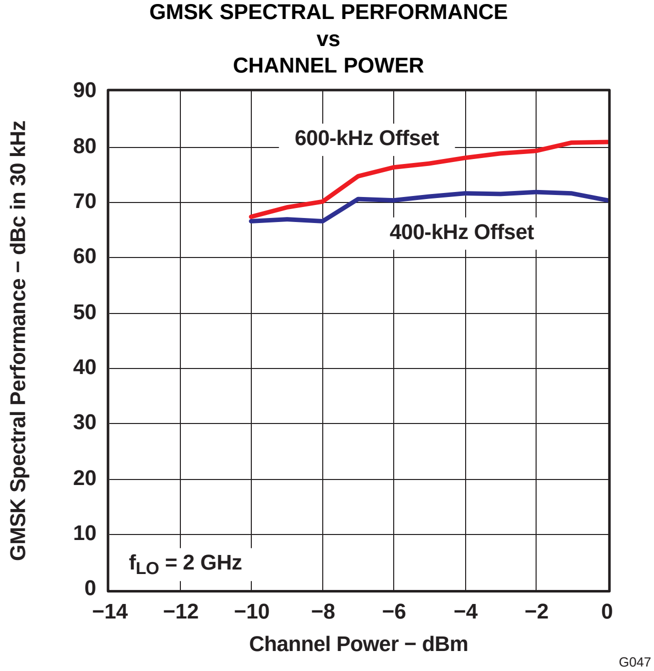

Figure 71.

WCDMA Applications

The TRF3702 is also optimized for WCDMA applications, where both adjacent-channel power ratio (ACPR) and noise density are critically important. Figure 62 shows the noise performance of the modulator at a 60-MHz offset over temperature. In addition, Figure 72 shows the 60-MHz offset noise measured at the output of the TRF3702 versus WCDMA channel power. Using Texas Instruments' DAC568x series of high-performance digital-to-analog converters in the configuration depicted in Figure 70, state-of-the-art levels of ACPR have been measured. In each case, test model 1 was used with 64 active channels as the baseband input to the TRF3702. Figure 73 shows the performance attained for a single WCDMA carrier at 2.14 GHz, with a measured ACPR of 71.2 dBc for a channel power of –14 dBm. This unprecedented level of ACPR along with the low levels of noise at 60-MHz offset makes the TRF3702 an optimum choice for such applications. Figure 74 shows the single-carrier WCDMA ACPR performance versus channel power; it is important to note that even at high output power levels, the TRF3702 maintains great linearity, offering 64 dBc of ACPR at an output-channel power of –8 dBm.

APPLICATION INFORMATION (continued)

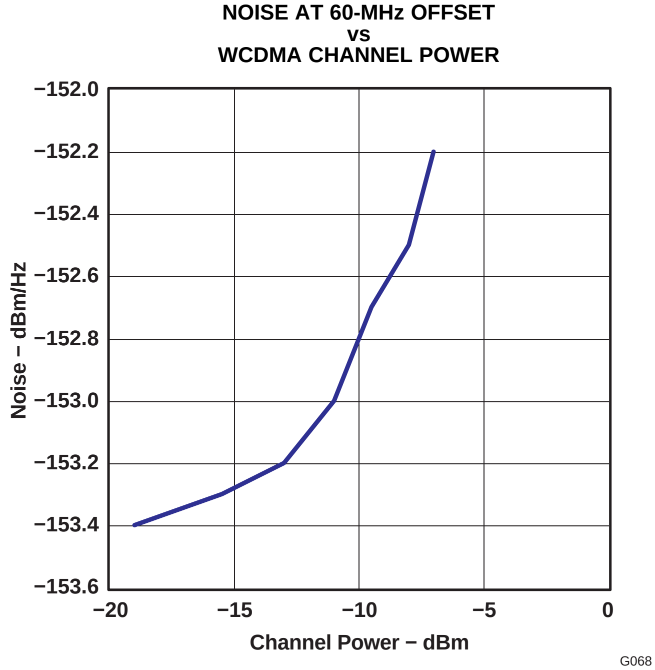

Figure 72.

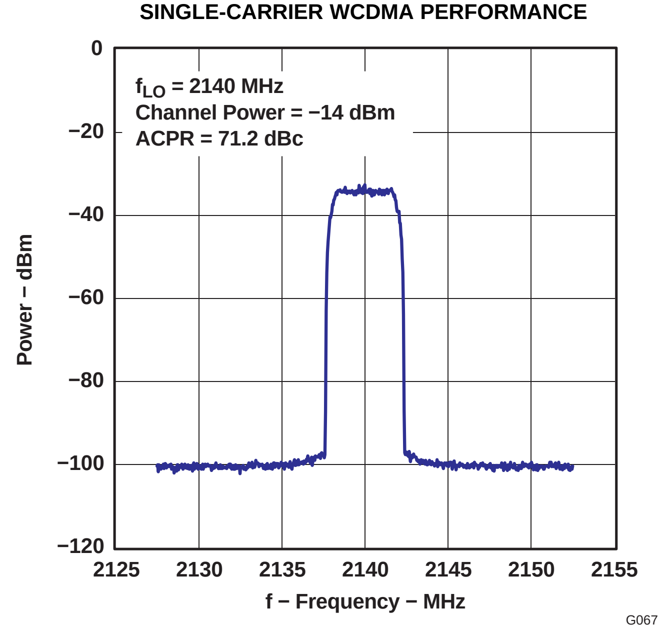

Figure 73.

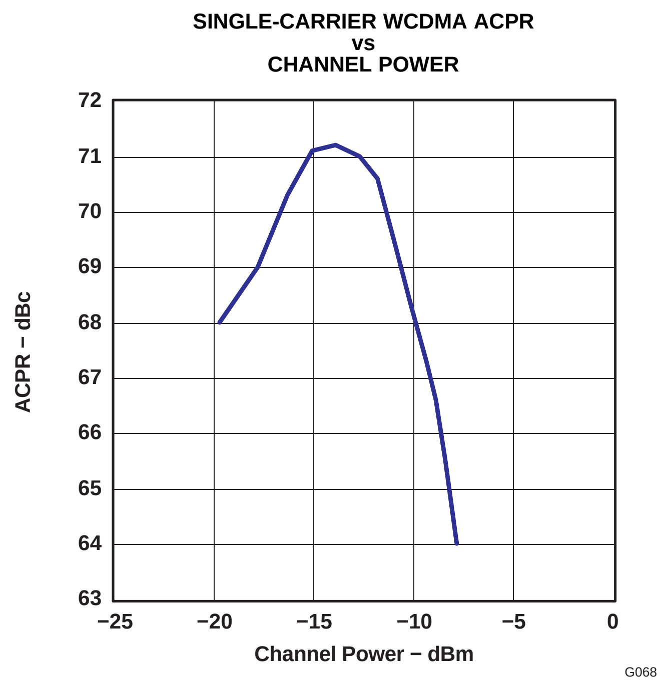

Figure 74.

APPLICATION INFORMATION (continued)

The TRF3702 can also be used for multicarrier applications, as is illustrated in Figure 75. For a 4-carrier case at a total output power of –16.7 dBm, an ACPR of almost 63 dBc can be reached. Figure 76 shows the ACPR profile for a 4-carrier WCDMA application versus per-carrier channel power. Further improvements in performance can be achieved by including a low-pass filter between the output of the DAC and the input to the TRF3702, based on the frequency planning and specific requirements of a given design. The combination of the TRF3702, the DAC568x, and the TRF3750 provides a unique signal-chain chipset capable of delivering state-of-the-art levels of performance for the most challenging WCDMA applications.

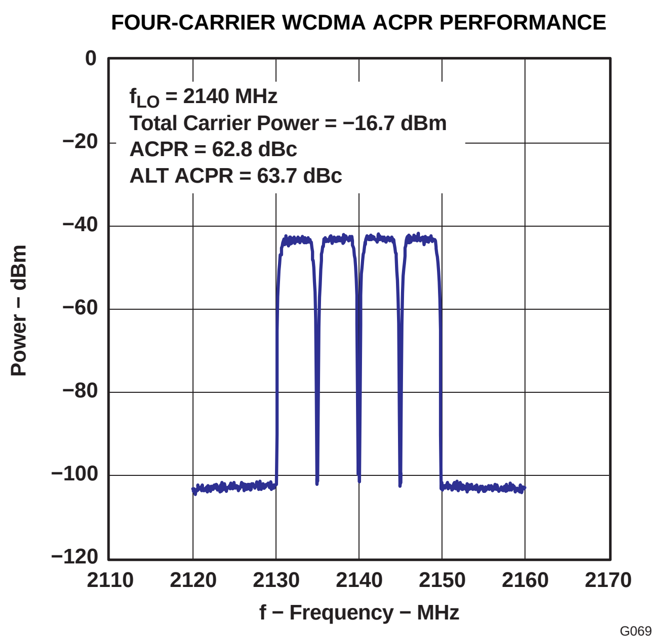

Figure 75.

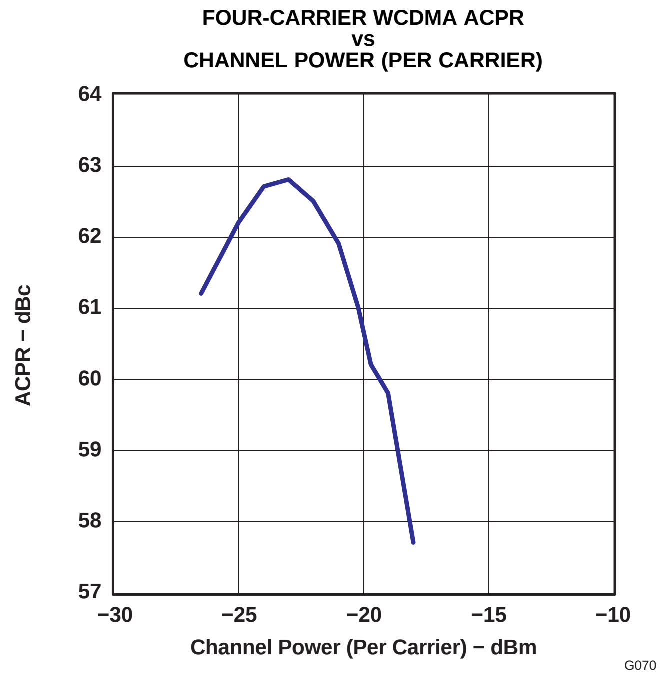

Figure 76.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3702IRHC	LIFEBUY	VQFN	RHC	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3702 TRF	
TRF3702IRHCG4	LIFEBUY	VQFN	RHC	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3702 TRF	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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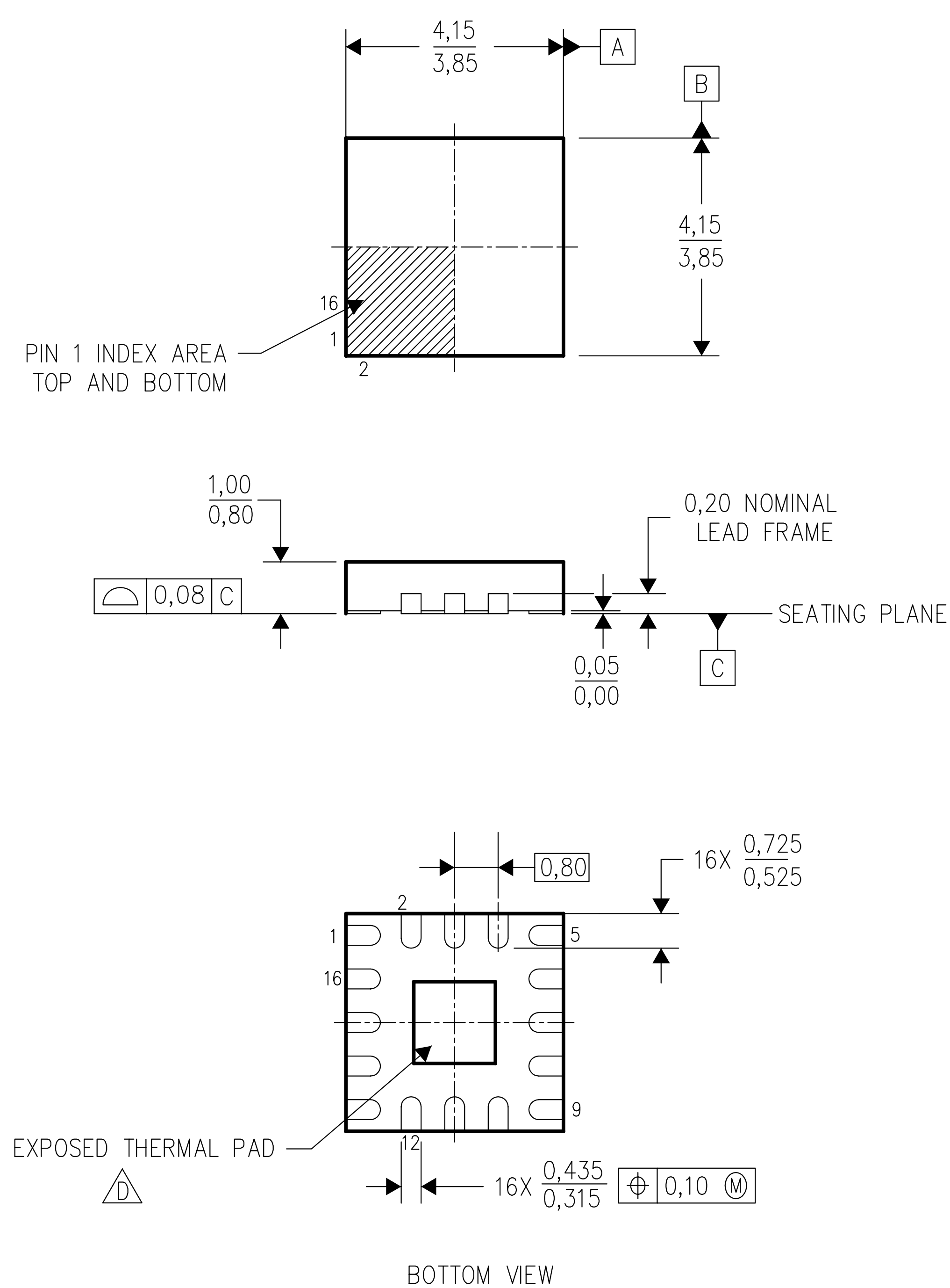
RHC (S–PQFP–N16) (CUSTOM PACKAGE) PLASTIC QUAD FLATPACK



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

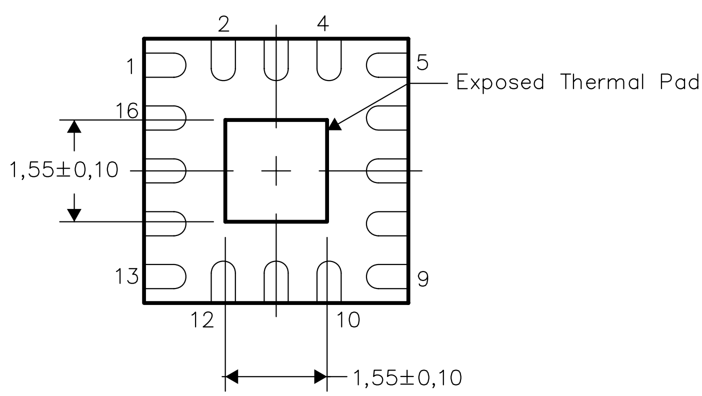
RHC (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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