

LMV331 Single, LMV393 Dual, LMV339 Quad General-purpose Low-voltage Comparators

1 Features

- 2.7-V and 5-V Performance
- Low Supply Current
 - LMV331 130 μ A Typ
 - LMV393 210 μ A Typ
 - LMV339 410 μ A Typ
- Input Common-Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV Typical
- Open-Collector Output for Maximum Flexibility

2 Applications

- Hysteresis Comparators
- Oscillators
- Window Comparators
- Industrial Equipment
- Test and Measurement

3 Description

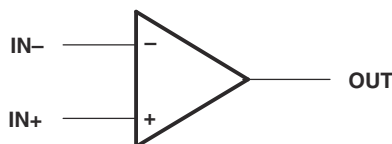
The LMV393 and LMV339 devices are low-voltage (2.7 V to 5.5 V) versions of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331 is the single-comparator version.

The LMV331, LMV339, and LMV393 are the most cost-effective solutions for applications where low-voltage operation, low power, and space saving are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

Device Information

PART NUMBER	PACKAGE (PIN) ⁽¹⁾	BODY SIZE (NOM)
LMV339	SOIC (14)	8.65 mm x 3.90 mm
LMV393	SOIC (8)	4.90 mm x 3.90 mm
LMV331	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (January 2015) to Revision U (October 2020) Page

- Updated the numbering format for tables, figures and cross-references throughout the document..... **1**

Changes from Revision S (October 2012) to Revision T (January 2015) Page

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... **1**
- Deleted *Ordering Information* table..... **1**

Changes from Revision R (May 2012) to Revision S (October 2012) Page

- Updated operating temperature range..... **4**

Changes from Revision N (April 2011) to Revision O (February 2012) Page

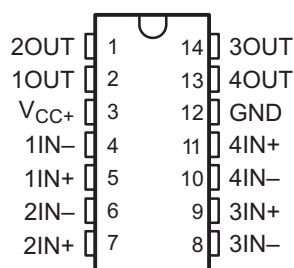
- Changed V_I in the *Absolute Maximum Ratings* from 5.5 V to V_{CC+} **4**

Changes from Revision M (November 2005) to Revision N (April 2011) Page

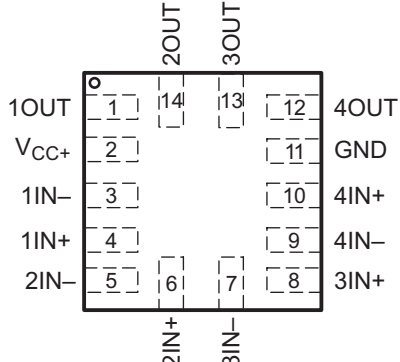
- Changed document format from Quicksilver to DocZone..... **1**
- Added RUC package pin out drawing..... **3**

5 Pin Configuration and Functions

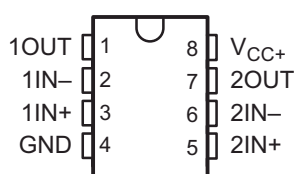
**LMV339 . . . D OR PW PACKAGE
(TOP VIEW)**



**LMV339 . . . RUC PACKAGE
(TOP VIEW)**



**LMV393 . . . D, DDU, DGK OR PW PACKAGE
(TOP VIEW)**



**LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)**

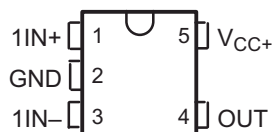


Table 5-1. Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	LMV331 DBV or DCK	LMV393 D, DDU, DGK or PW	LMV339 D or PW	RUC		
1IN-, 2IN-, 3IN-, 4IN-	3	2, 6	4, 6, 8, 10	3, 5, 7, 9	I	Comparator(s) negative input pin(s)
1IN+, 2IN+, 3IN+, 4IN+	1	3, 5	5, 7, 9, 11	4, 6, 8, 10	I	Comparator(s) positive input pin(s)
GND	2	4	12	11	I	Ground
1OUT, 2OUT, 3OUT, 4OUT	4	1, 7	2, 1, 14, 13	1, 14, 13, 12	O	Comparator(s) output pin(s)
VCC+	5	8	3	2	I	Supply Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		5.5	V
V _{ID}	Differential input voltage ⁽³⁾		±5.5	V
V _I	Input voltage range (either input)	0	V _{CC+}	V
	Duration of output short circuit (one amplifier) to ground ⁽⁴⁾	At or below T _A = 25°C, V _{CC} ≤ 5.5 V		Unlimited
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.

(3) Differential voltages are at IN+ with respect to IN–.

(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
V _{OUT}	Output voltage	V _{CC+} + 0.3		V
T _A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMV339			LMV393				LMV331		UNIT
		D	PW	RUC	D	DDU	DGK	PW	DBV	DCK	
		14 PINS			8 PINS				5 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	86	113	216	97	210	172	149	206	252	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	—	—	51.3	—	—	—	—	—	—	
R _{θJB}	Junction-to-board thermal resistance	—	—	59.0	—	—	—	—	—	—	
Ψ _{JT}	Junction-to-top characterization parameter	—	—	1.2	—	—	—	—	—	—	
Ψ _{JB}	Junction-to-board characterization parameter	—	—	59.0	—	—	—	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics, $V_{CC+} = 2.7\text{ V}$

$V_{CC+} = 2.7\text{ V}$, $GND = 0\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage		25°C		1.7	7	mV
α_{VIO} Average temperature coefficient of input offset voltage		–40°C to 125°C		5		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		15	250	nA
		–40°C to 125°C			400	
I_{IO} Input offset current		25°C		5	50	nA
		–40°C to 125°C			150	
I_O Output current (sinking)	$V_O \leq 1.5\text{ V}$	25°C	5	23		mA
Output Leakage Current		25°C		0.003		μA
		–40°C to 125°C			1	
V_{ICR} Common-mode input voltage range		25°C		–0.1 to 2		V
V_{SAT} Saturation voltage	$I_O \leq 1.5\text{ mA}$	25°C		200		mV
I_{CC} Supply current	LMV331	25°C		40	100	μA
	LMV393 (both comparators)	25°C		70	140	
	LMV339 (all four comparators)	25°C		140	200	

6.6 Electrical Characteristics, $V_{CC+} = 5\text{ V}$

$V_{CC+} = 5\text{ V}$, $GND = 0\text{ V}$, at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage		25°C		1.7	7	mV
		–40°C to 125°C			9	
α_{VIO} Average temperature coefficient of input offset voltage		25°C		5		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current		25°C		25	250	nA
		–40°C to 125°C			400	
I_{IO} Input offset current		25°C		2	50	nA
		–40°C to 125°C			150	
I_O Output current (sinking)	$V_O \leq 1.5\text{ V}$	25°C	10	84		mA
Output Leakage Current		25°C		0.003		μA
		–40°C to 125°C			1	
V_{ICR} Common-mode input voltage range		25°C		–0.1 to 4.2		V
A_{VD} Large-signal differential voltage gain		25°C	20	50		V/mV
V_{SAT} Saturation voltage	$I_O \leq 4\text{ mA}$	25°C		200	400	mV
		–40°C to 125°C			700	
I_{CC} Supply current	LMV331	25°C		60	120	μA
		–40°C to 125°C			150	
	LMV393 (both comparators)	25°C		100	200	
		–40°C to 125°C			250	
	LMV339 (all four comparators)	25°C		170	300	
		–40°C to 125°C			350	

6.7 Switching Characteristics, $V_{CC+} = 2.7\text{ V}$

$T_A = 25^\circ\text{C}$, $V_{CC+} = 2.7\text{ V}$, $R_L = 5.1\text{ k}\Omega$, $GND = 0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{PHL} Propagation delay high to low level output switching	Input overdrive = 10 mV	1000	ns
	Input overdrive = 100 mV	350	
t_{PLH} Propagation delay low to high level output switching	Input overdrive = 10 mV	500	ns
	Input overdrive = 100 mV	400	

6.8 Switching Characteristics, $V_{CC+} = 5\text{ V}$

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{ V}$, $R_L = 5.1\text{ k}\Omega$, $\text{GND} = 0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{PHL} Propagation delay high to low level output switching	Input overdrive = 10 mV	600	ns
	Input overdrive = 100 mV	200	
t_{PLH} Propagation delay low to high level output switching	Input overdrive = 10 mV	450	ns
	Input overdrive = 100 mV	300	

6.9 Typical Characteristics

Unless otherwise specified, $V_S = +5\text{V}$, single supply, $T_A = 25^\circ\text{C}$

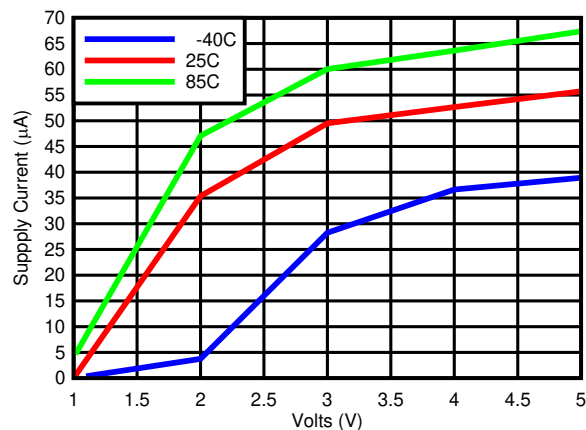


Figure 6-1. Supply Current vs Supply Voltage Output High (LMV33x)

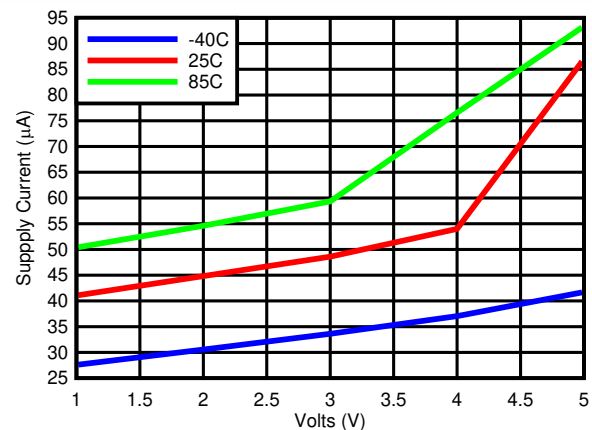


Figure 6-2. Supply Current vs Supply Voltage Output Low (LMV33x)

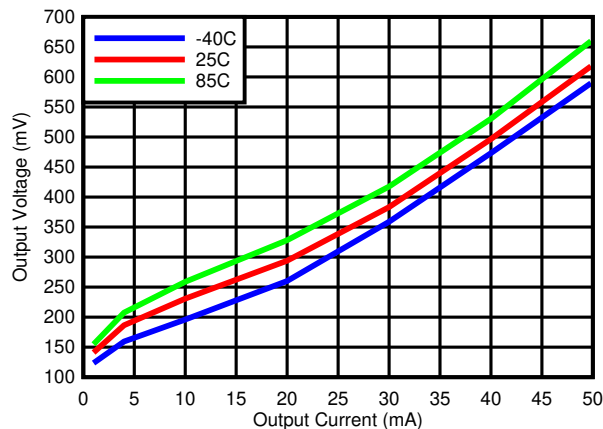


Figure 6-3. Output Voltage vs Output Current

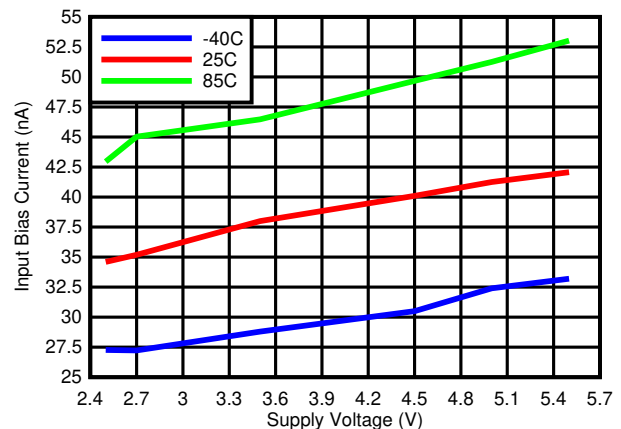
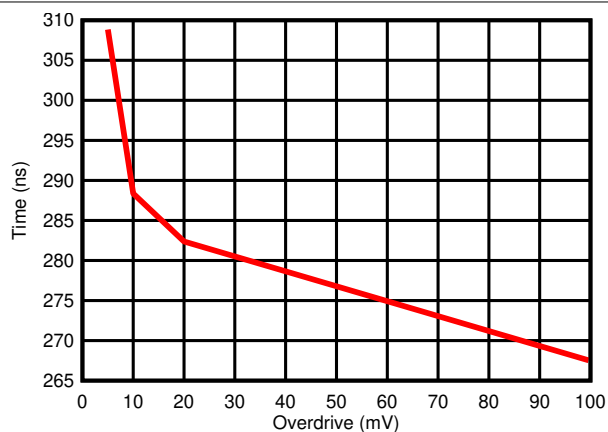
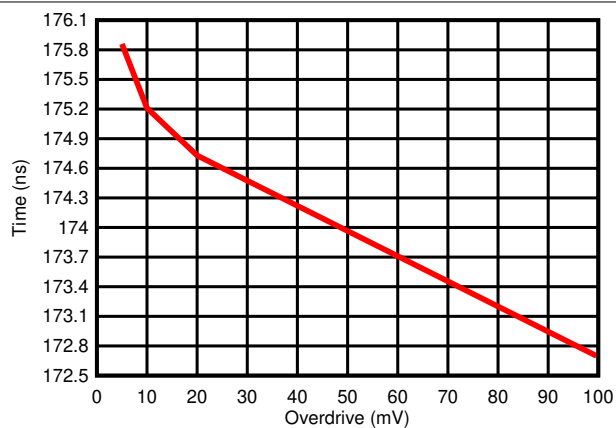


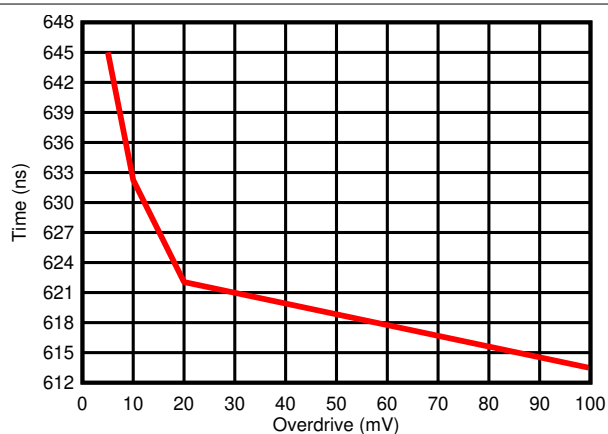
Figure 6-4. Input Bias Current vs Supply Voltage



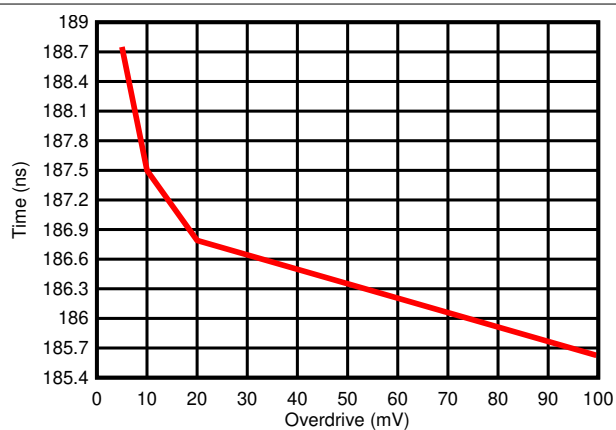
**Figure 6-5. Response Time vs Input Overdrives
Negative Transition ($V_{CC}=5$ V)**



**Figure 6-6. Response Time vs Input Overdrives
Positive Transition ($V_{CC} = 5$ V)**



**Figure 6-7. Response Time vs Input Overdrives
Negative Transition ($V_{CC} = 2.7$ V)**



**Figure 6-8. Response Time vs Input Overdrives
Positive Transition ($V_{CC} = 2.7$ V)**

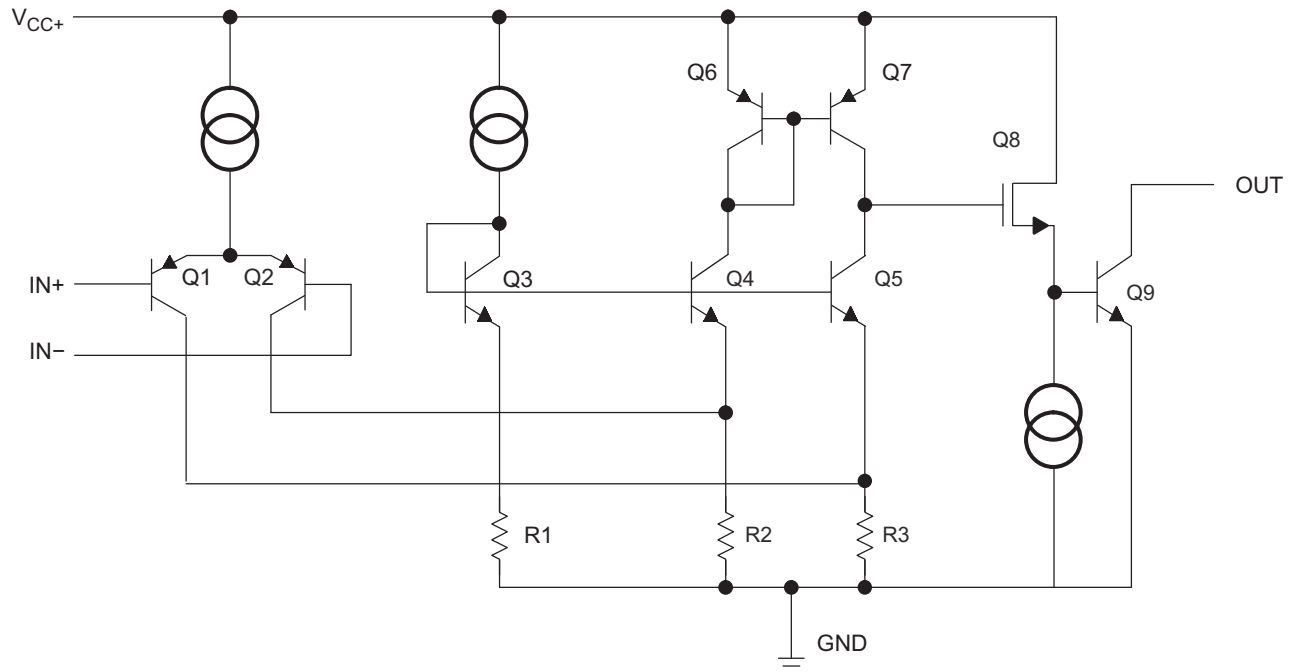
7 Detailed Description

7.1 Overview

The LMV331, LMV393 and LMV339 family of comparators have the ability to operate up to 5 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its low I_q and fast response.

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram



7.3 Feature Description

The LMV331, LMV393 and LMV339 consists of a PNP input, whose V_{be} creates a limit on the input common mode voltage capability, allowing LMV33x to accurately function from ground to $V_{CC} - V_{be}$ (~700mV) differential input. This enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The V_{OL} is resistive and will scale with the output current. Please see [Figure 6-3](#) for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LMV33x operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputs a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LMV331, LMV393, and LMV339 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMV331, LMV393, and LMV339 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

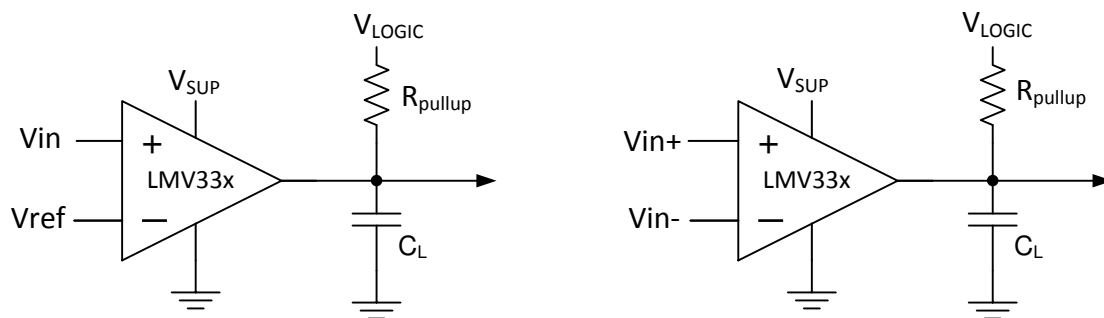


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#) as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 4.2 V
Supply Voltage	2.7 V to 5V
Logic Supply Voltage (R_{PULLUP} Voltage)	1 V to 5 V
Output Current (V_{LOGIC}/R_{PULLUP})	1 μ A to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

8.2.2 Detailed Design Procedure

When using LMV331, LMV393, and LMV339 in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If operating temperature is above or below 25°C the V_{ICR} can range from 0 V to $V_{CC} - 0.7$ V. This limits the input voltage range to as high as $V_{CC} - 0.7$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a possible list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
 - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison; the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 8-2](#) show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the pull-up resistance (R_{pullup}) and V_{logic} voltage, refer to [Figure 8-1](#). The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use [Figure 6-3](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (T_P) is approximately $T_P \sim R_{PULLUP} \times C_L$
- The negative response time (T_N) is approximately $T_N \sim R_{CE} \times C_L$
 - R_{CE} can be determine by taking the slope of [Figure 6-3](#) in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic} , $R_{PULLUP} = 5.1$ k Ω , and 50 pF scope probe.

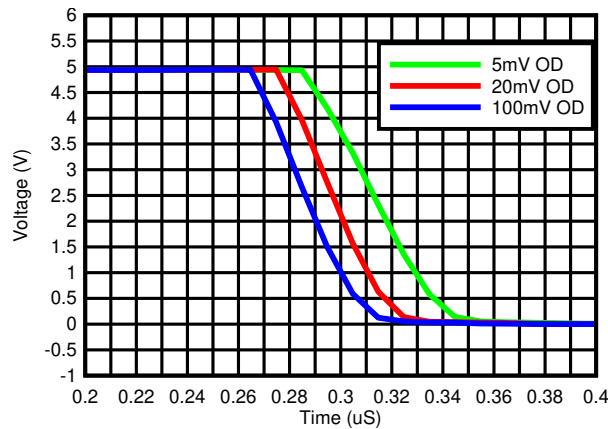


Figure 8-2. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation cause temporary fluctuations in the comparator's input common mode range and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

10.2 Layout Example

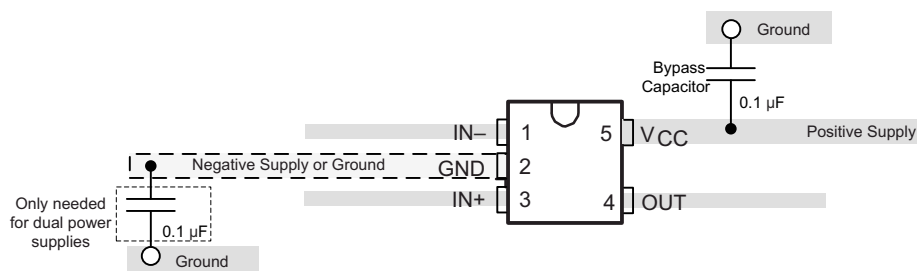


Figure 10-1. LMV331 Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV331	Click here	Click here	Click here	Click here	Click here
LMV393	Click here	Click here	Click here	Click here	Click here
LMV339	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV331IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R1IF, R1IK)
LMV331IDBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	(R1IF, R1IK)
LMV331IDCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R2F, R2K, R2R)
LMV331IDCKT	Obsolete	Production	SC70 (DCK) 5	-	-	Call TI	Call TI	-40 to 125	(R2F, R2R)
LMV339ID	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 125	LMV339I
LMV339IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV339I
LMV339IPW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 125	MV339I
LMV339IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV339I
LMV393ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 125	MV393I
LMV393IDDUR	Obsolete	Production	VSSOP (DDU) 8	-	-	Call TI	Call TI	-40 to 125	RABR
LMV393IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(R9B, R9Q, R9R)
LMV393IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 125	MV393I
LMV393IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I
LMV393IPWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV393I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV331, LMV393 :

- Automotive : [LMV331-Q1](#), [LMV393-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


*All dimensions are nominal

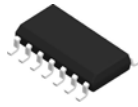
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.17	3.23	1.37	4.0	8.0	Q3
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV339IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV393IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LMV393IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV393IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

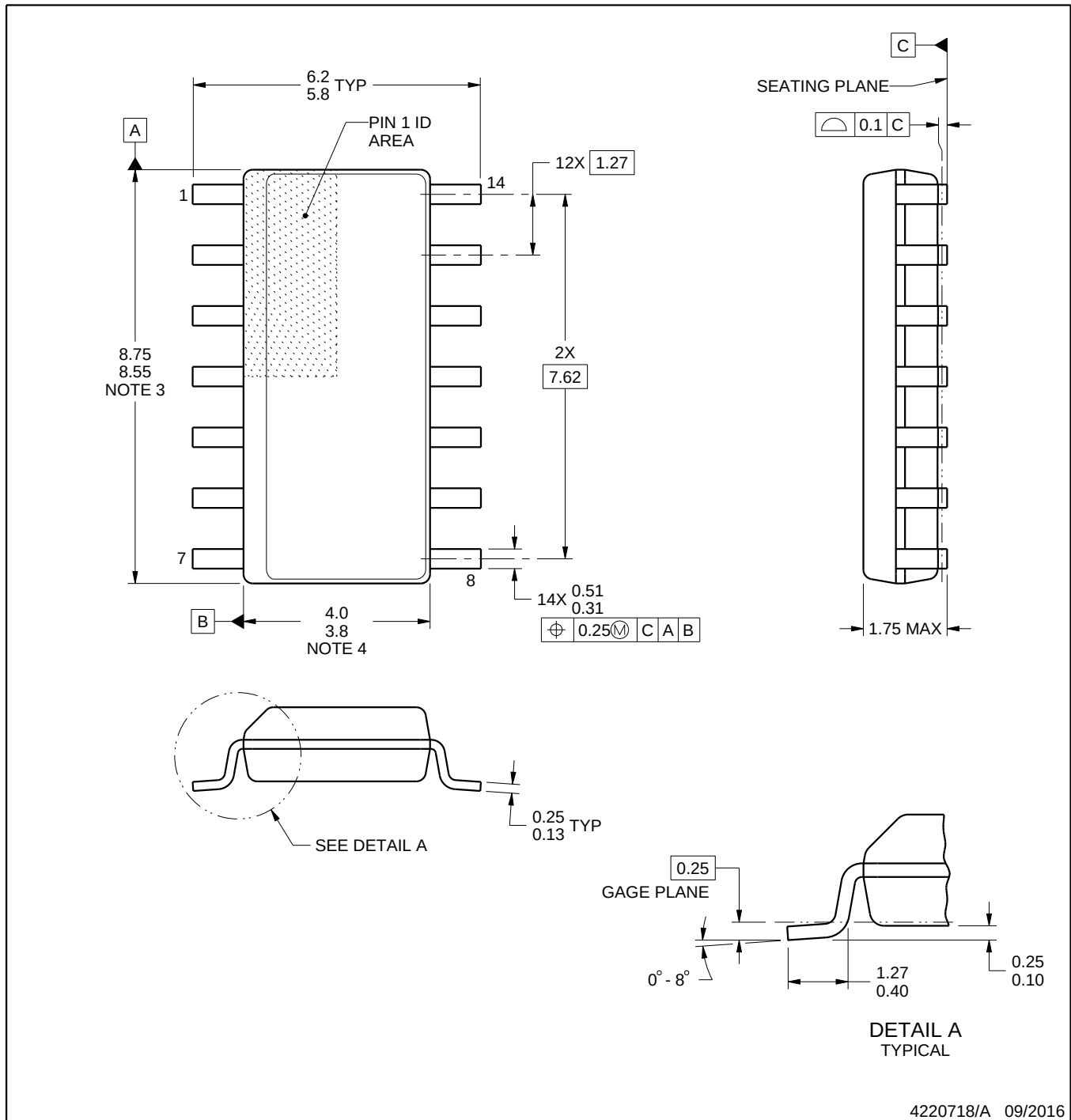


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV331IDBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
LMV331IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV331IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV339IDR	SOIC	D	14	2500	356.0	356.0	35.0
LMV339IDR	SOIC	D	14	2500	353.0	353.0	32.0
LMV339IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LMV393IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV393IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LMV393IDR	SOIC	D	8	2500	353.0	353.0	32.0
LMV393IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LMV393IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LMV393IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

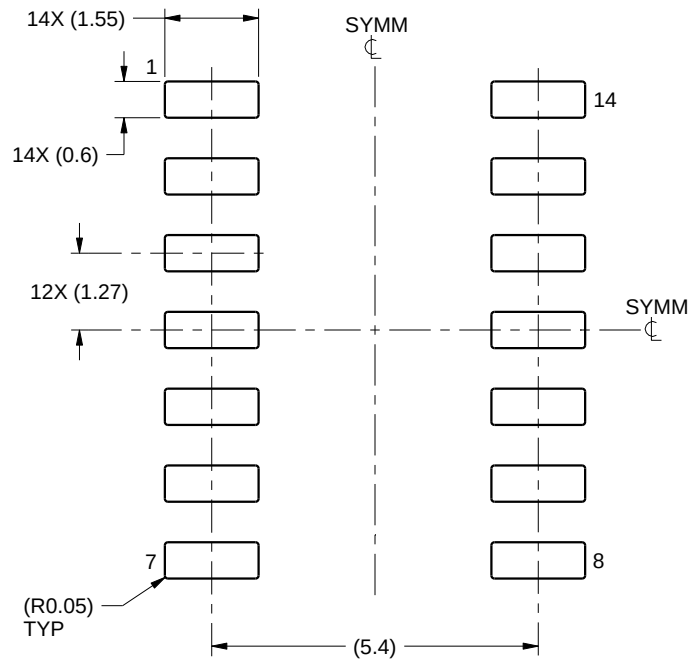
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

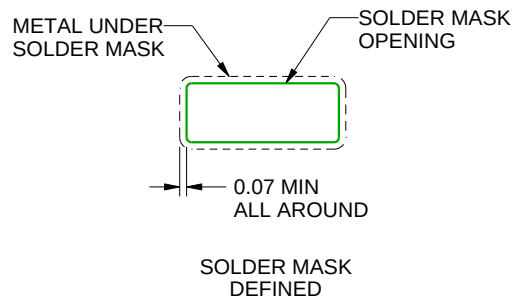
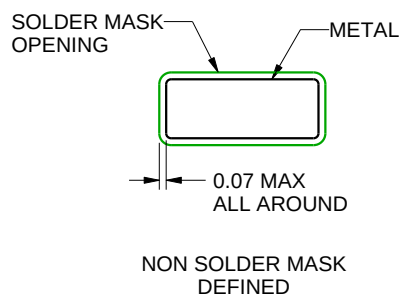
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

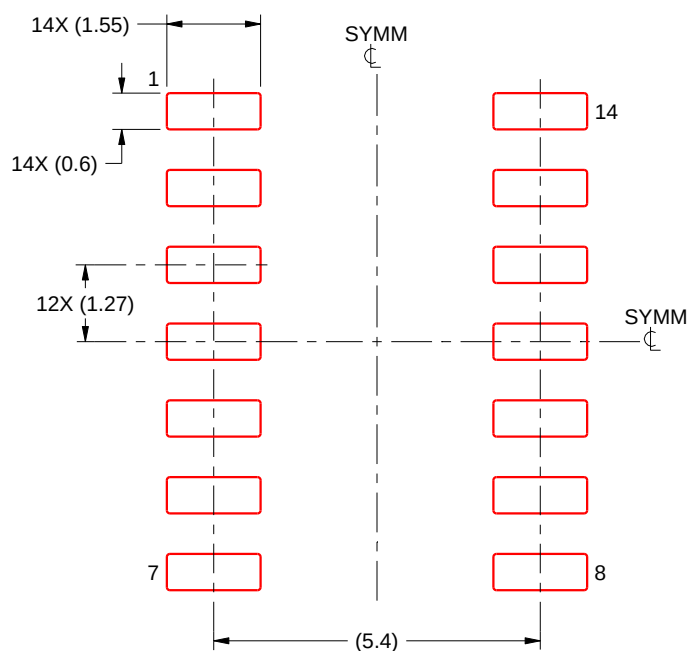
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

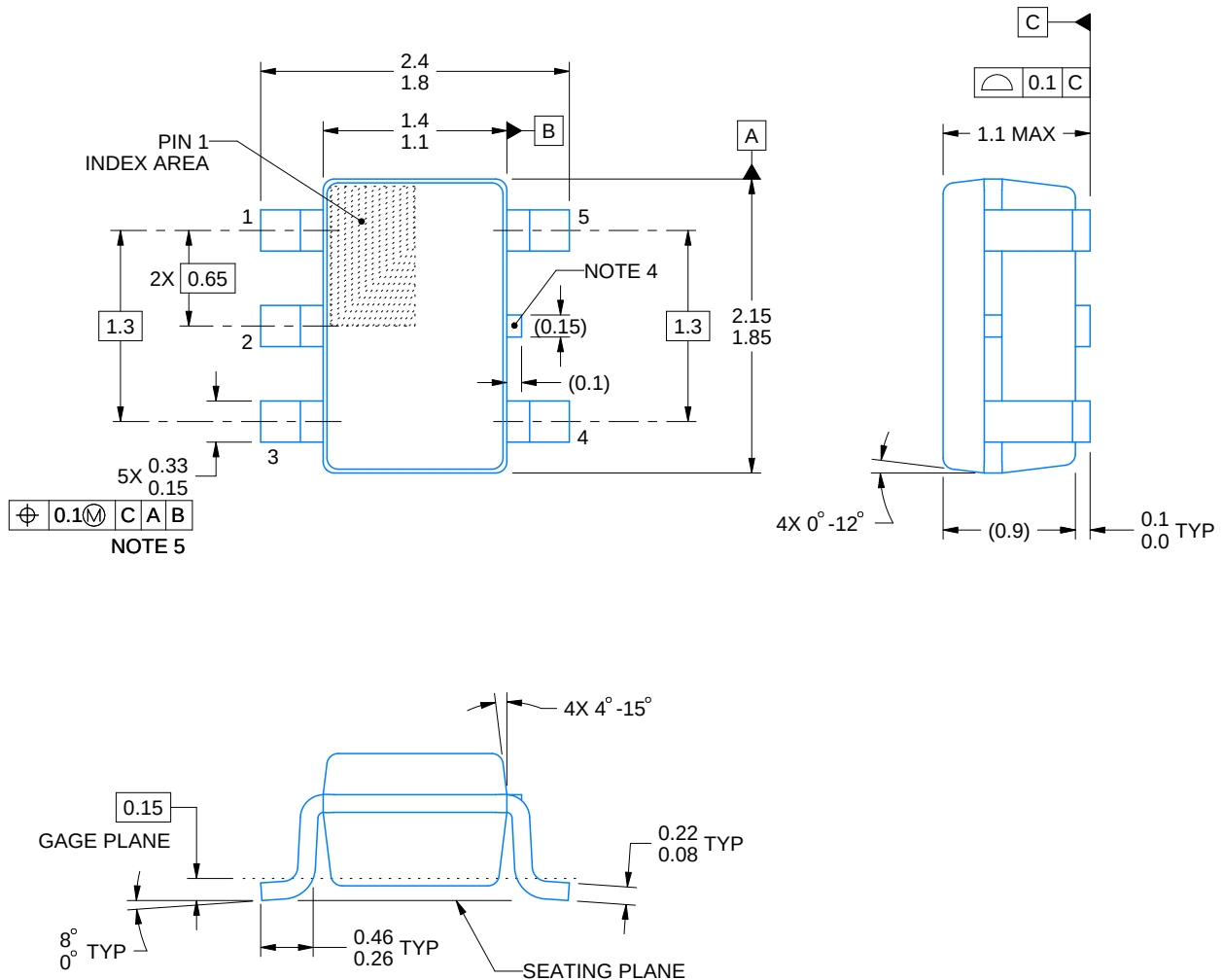
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

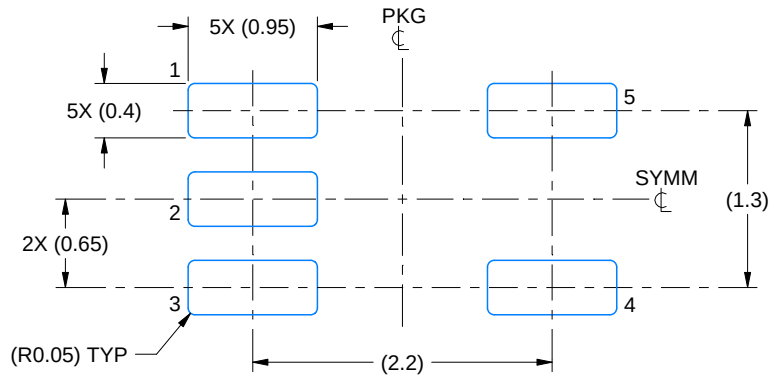
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

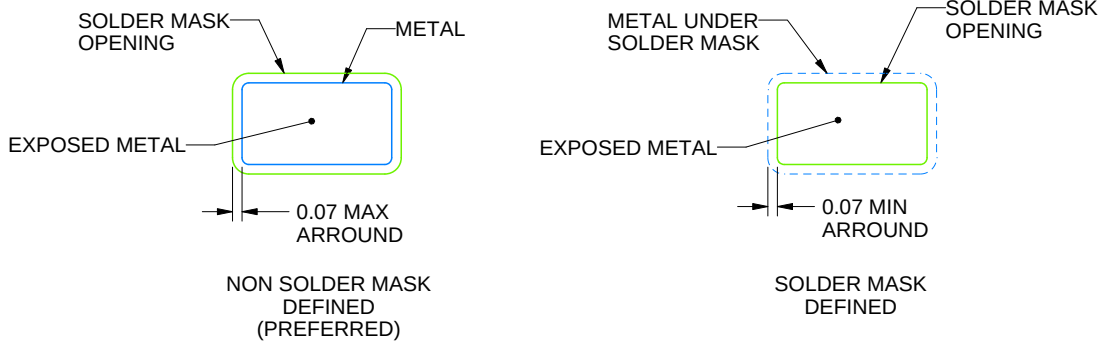
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

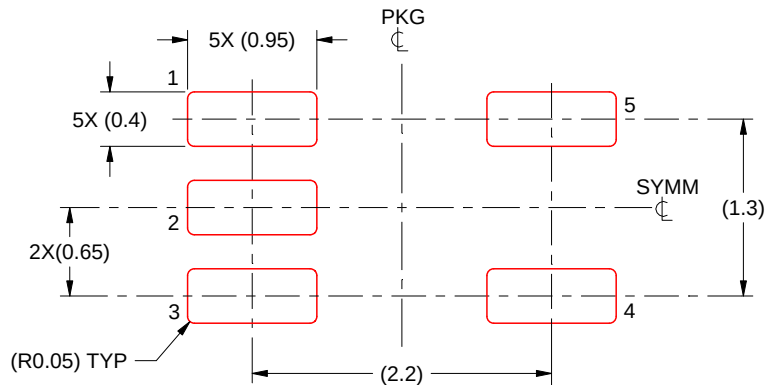
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

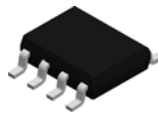


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

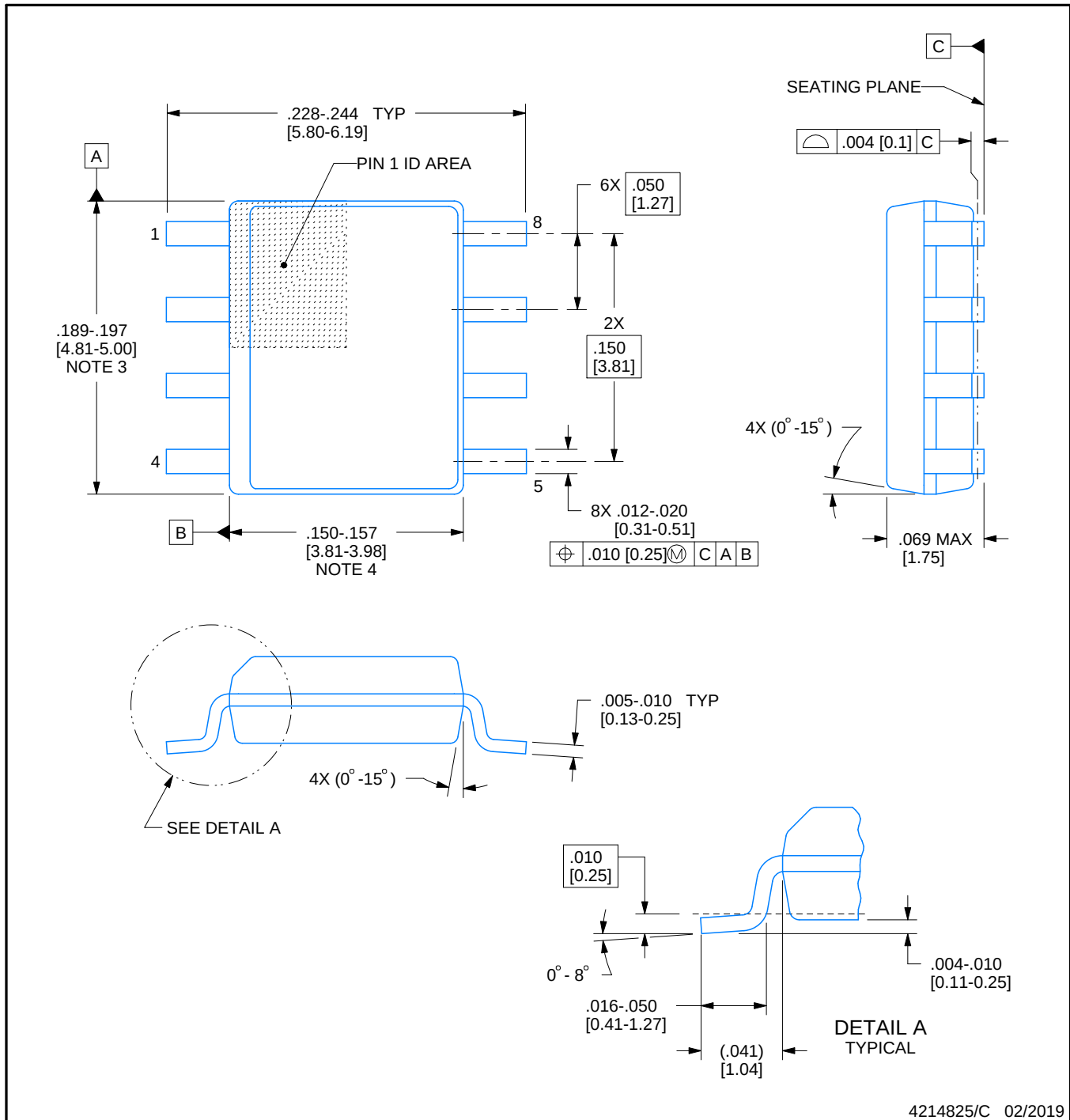


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

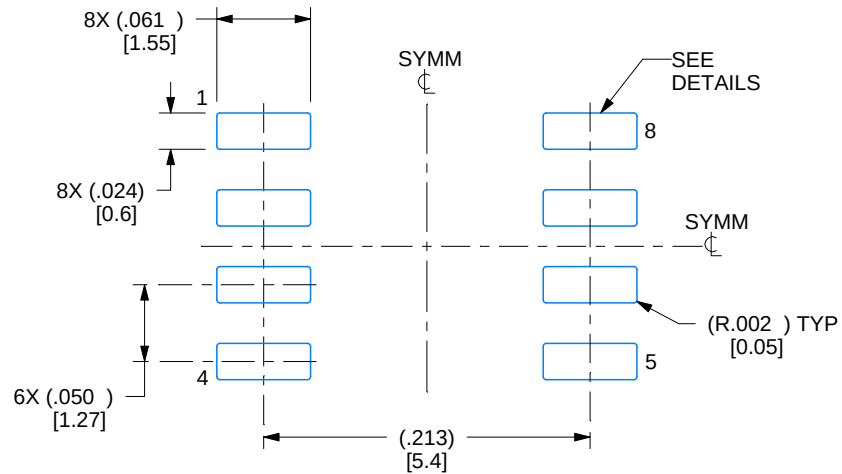
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

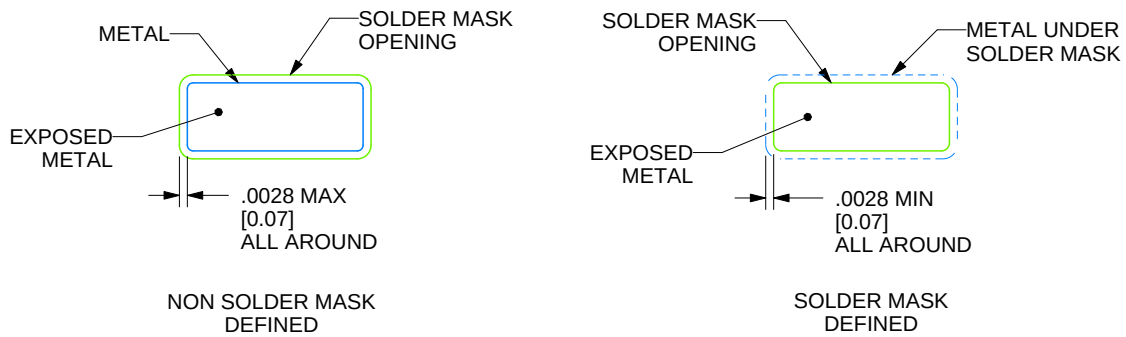
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

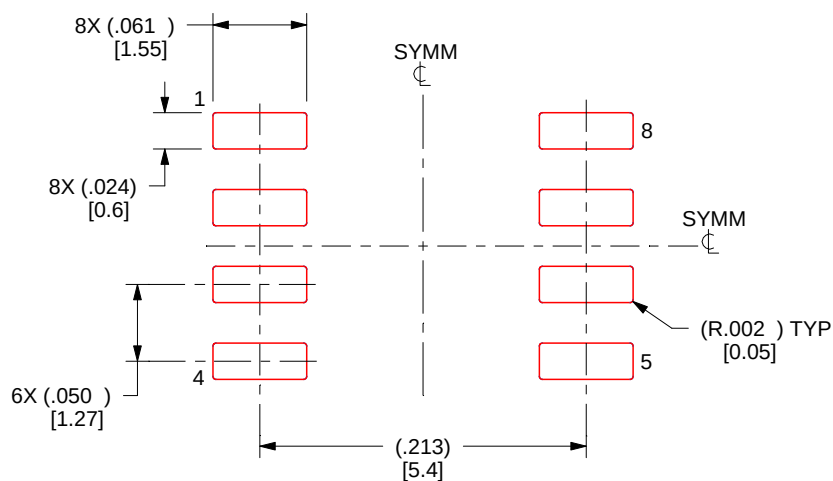
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

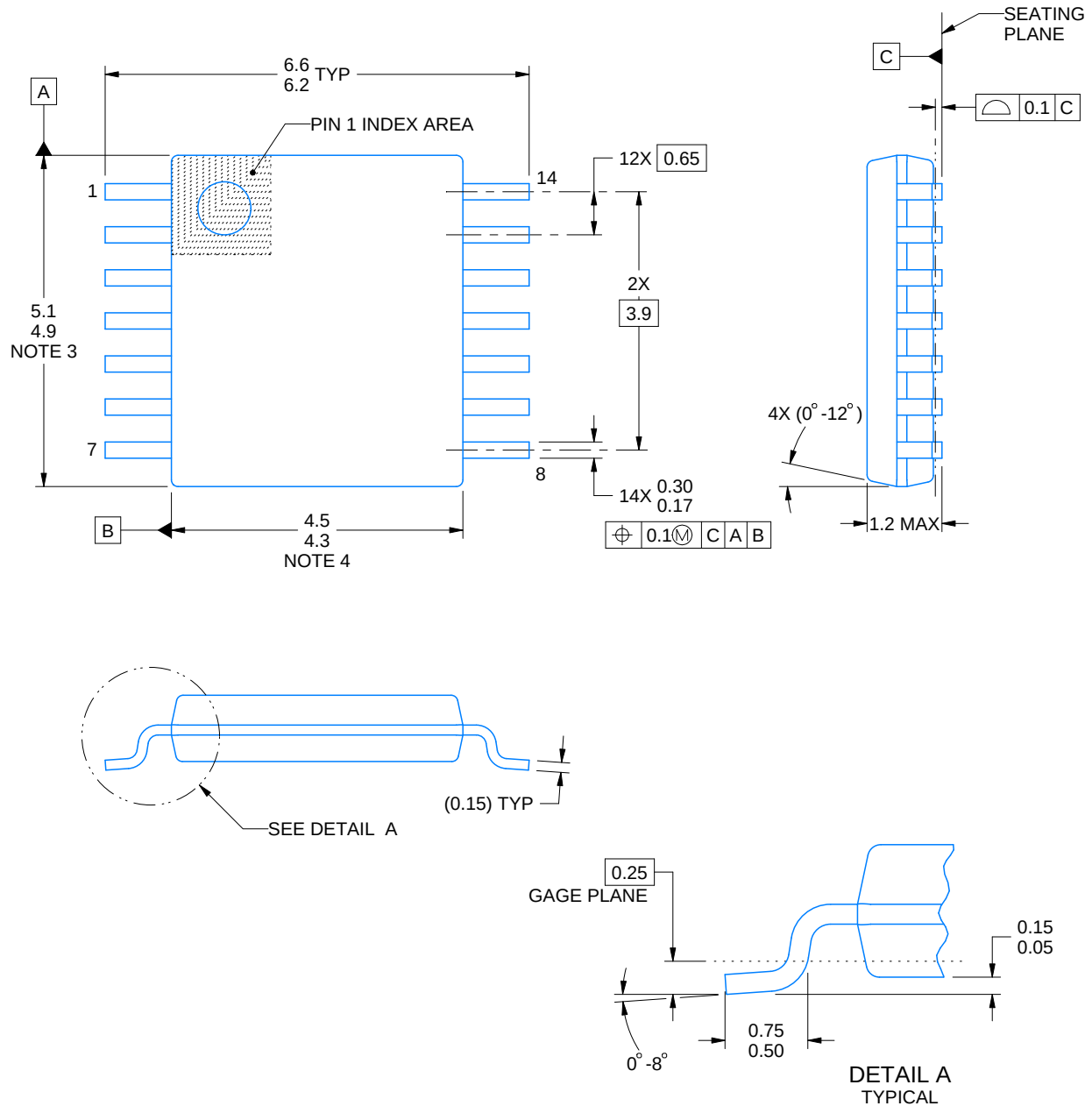
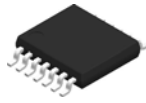


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

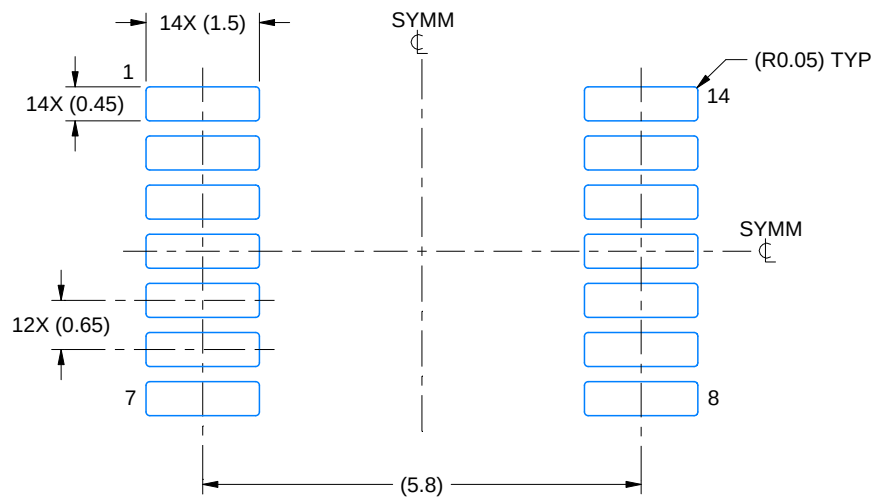
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

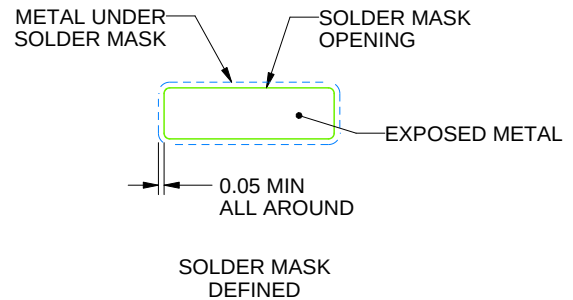
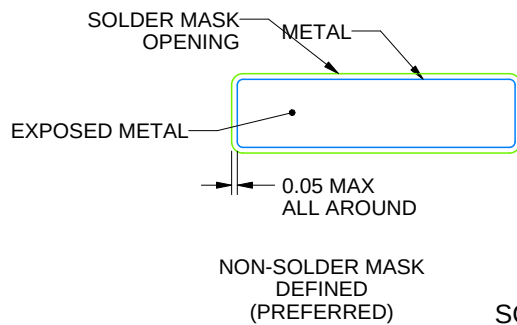
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

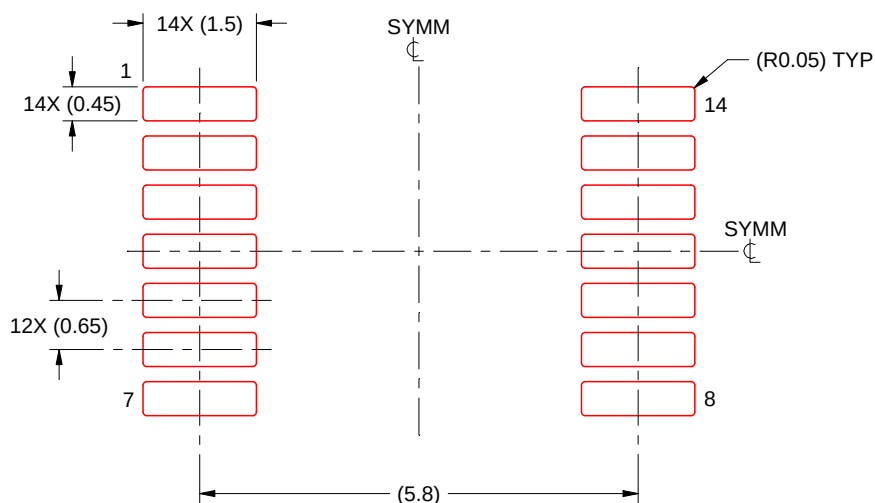
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

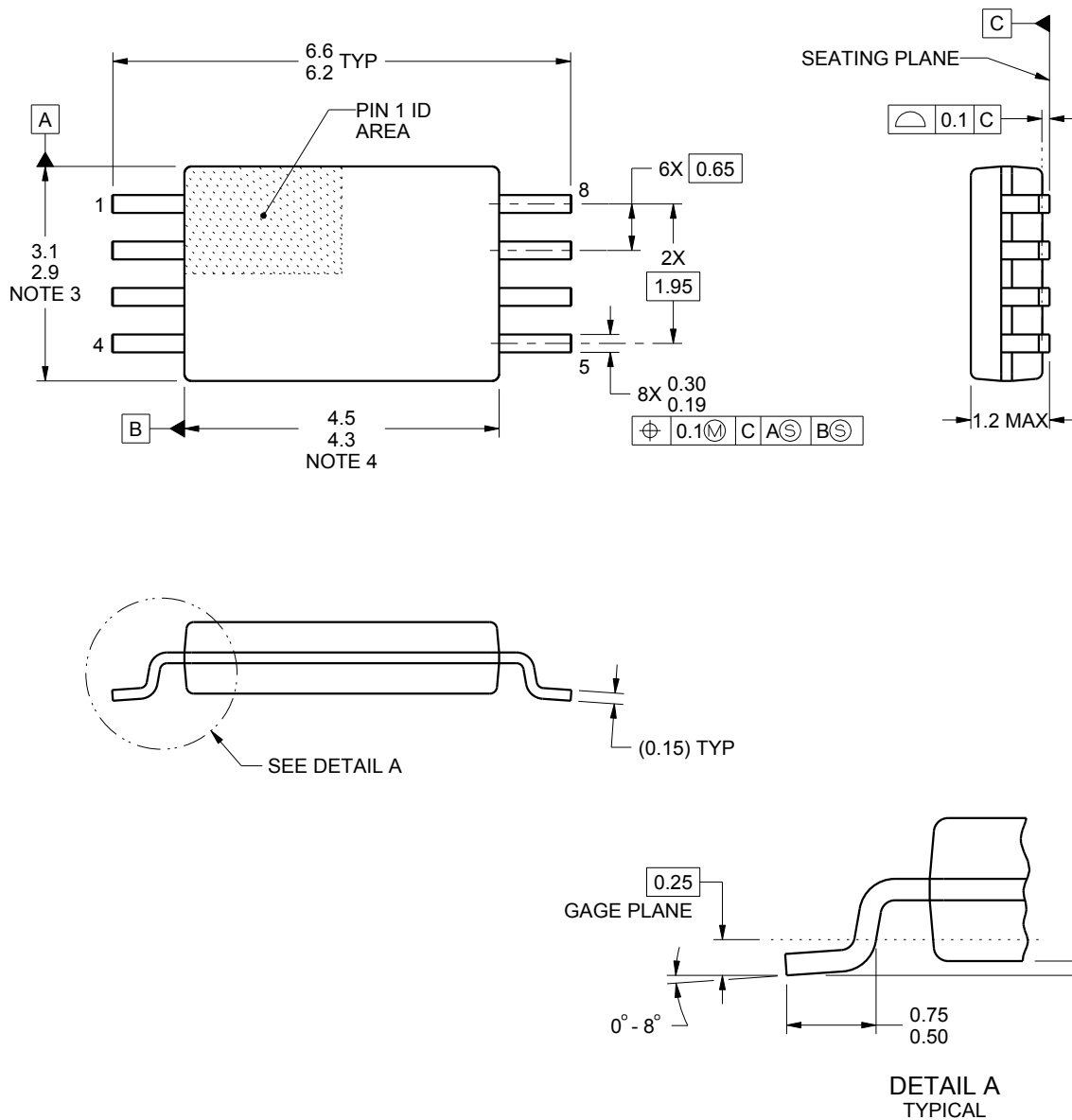
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

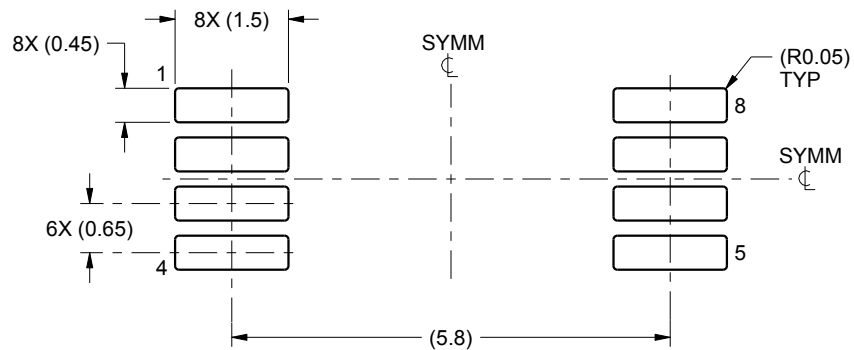
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

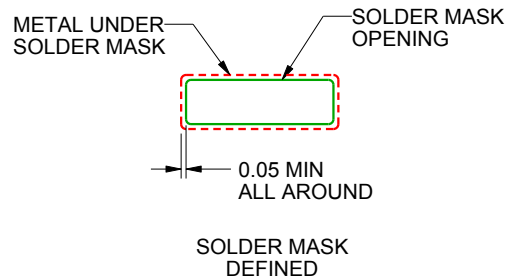
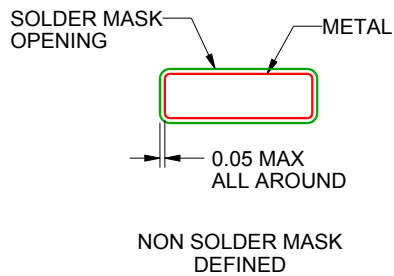
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

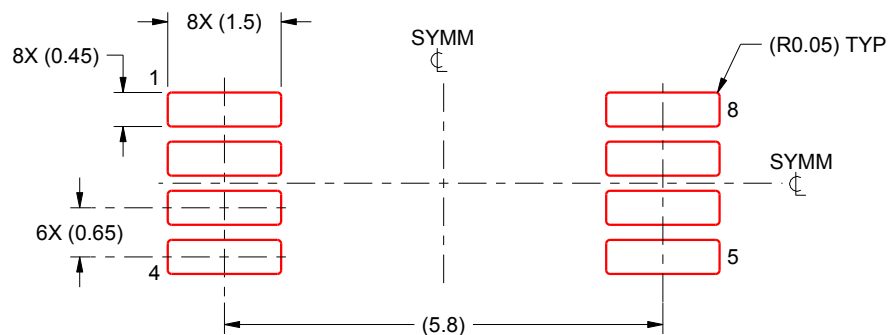
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

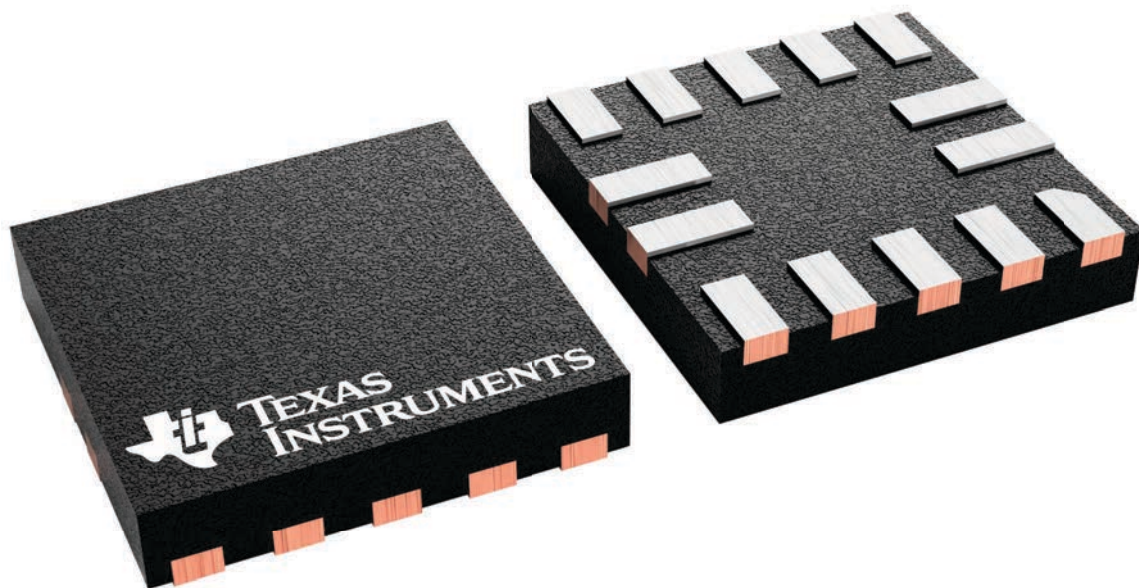
RUC 14

X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229871/A

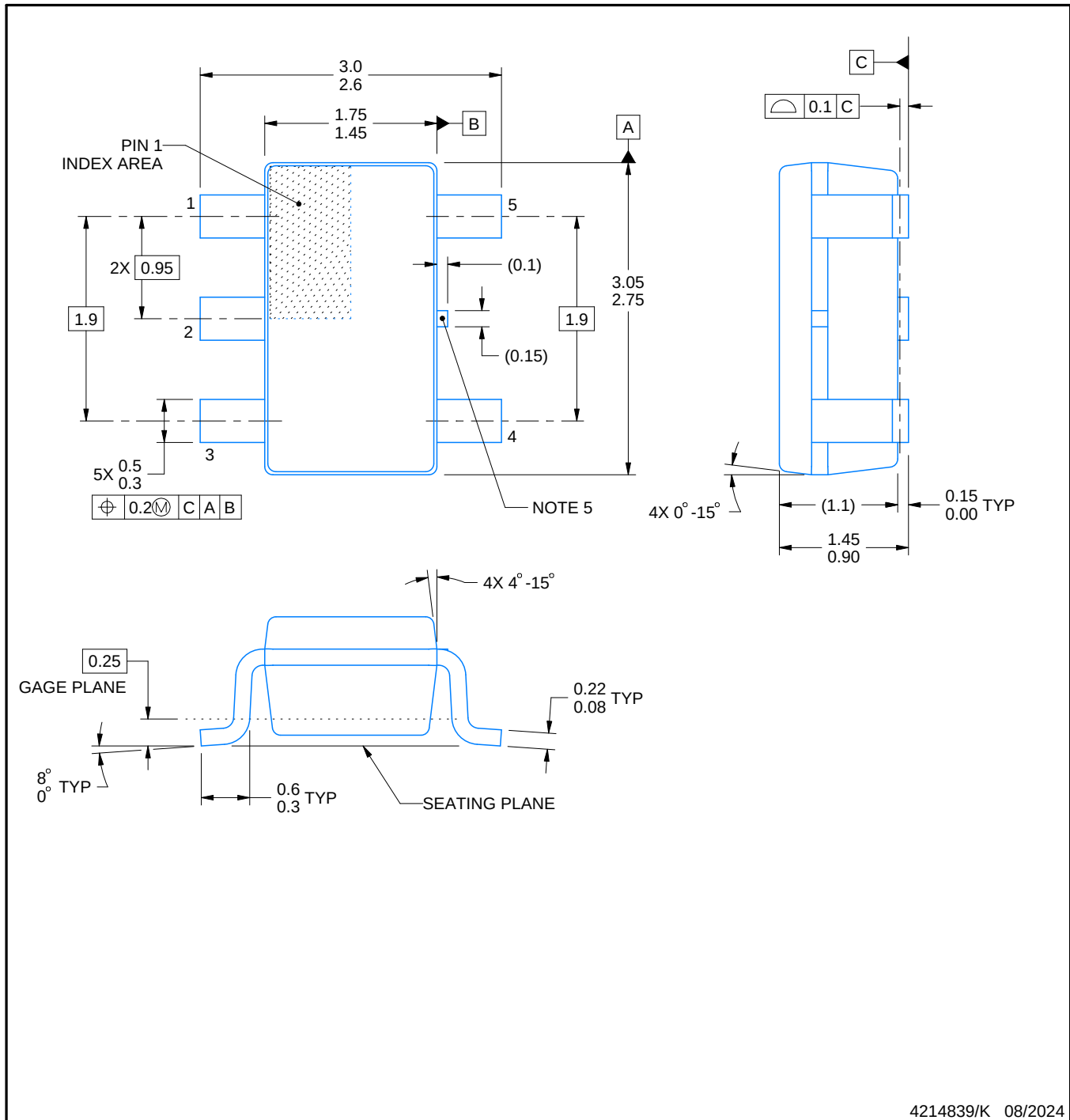
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

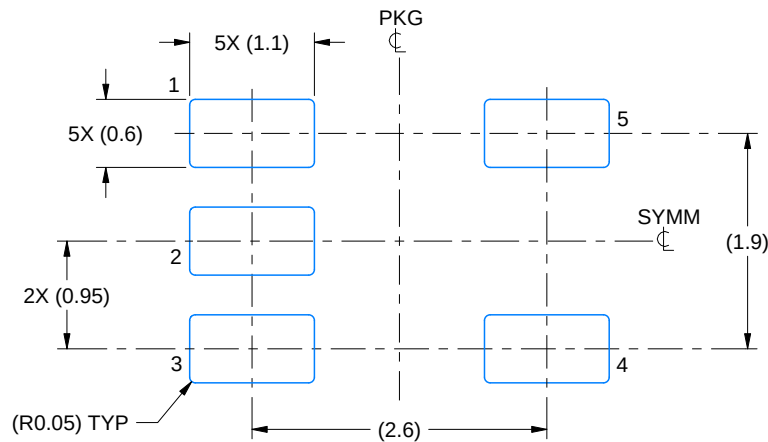
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

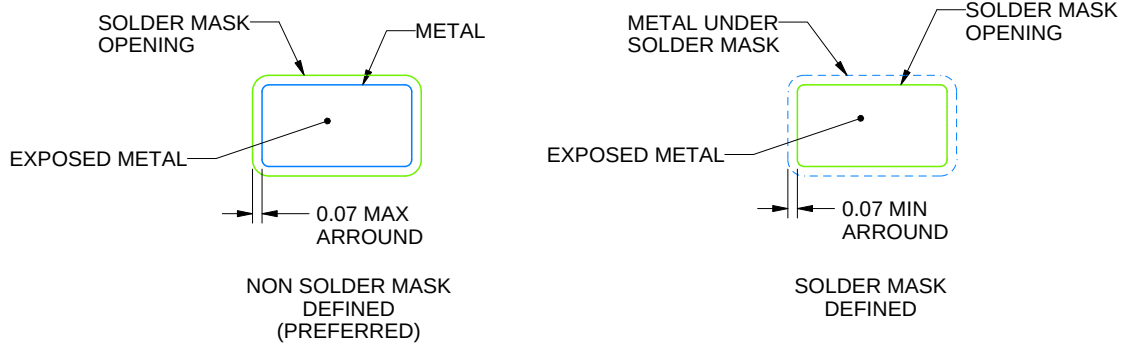
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

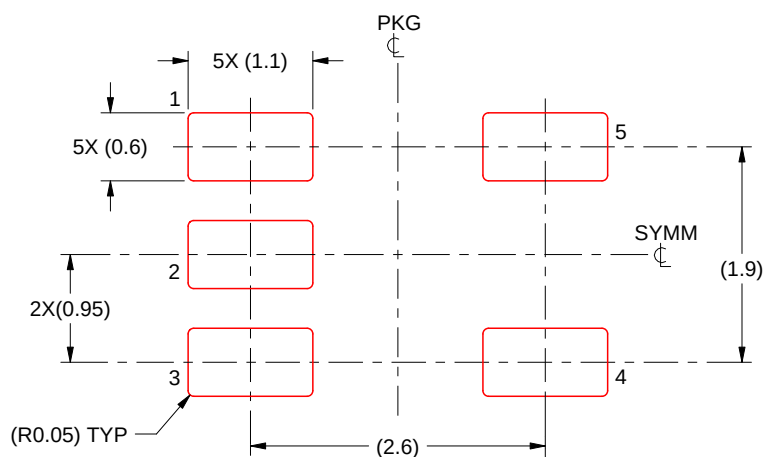
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

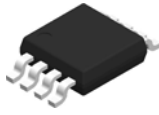


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

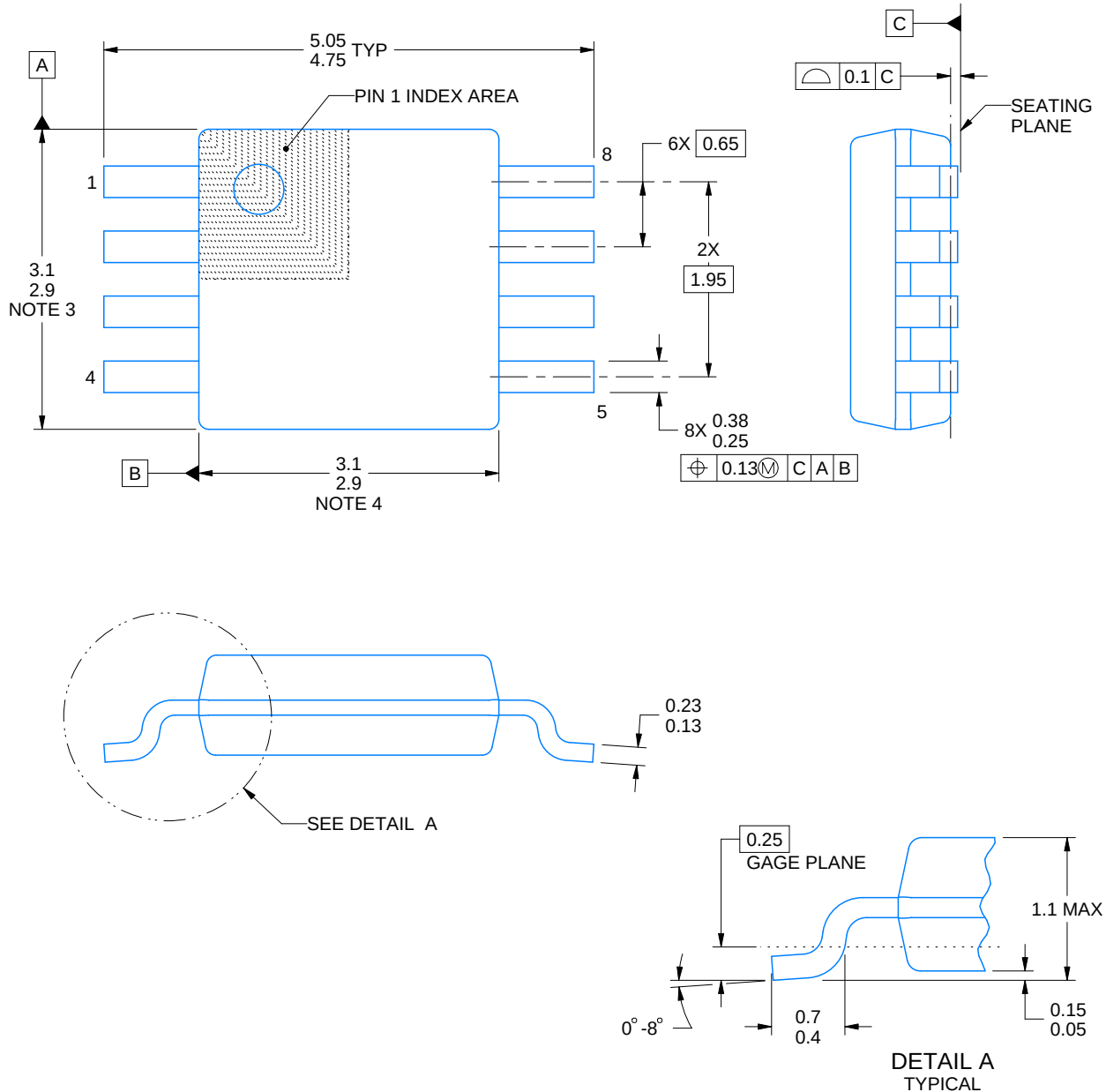
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

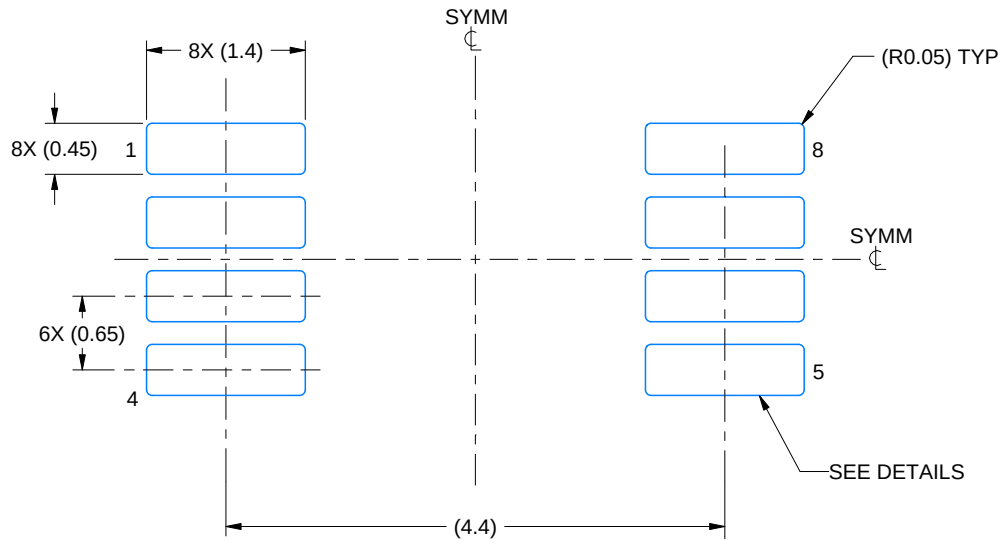
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

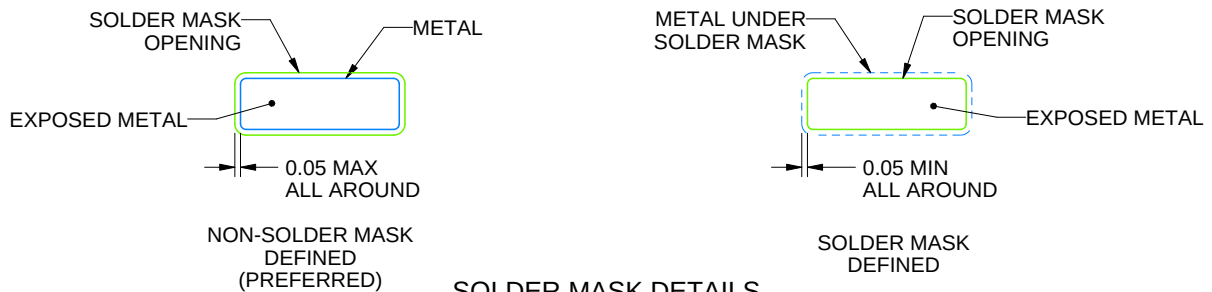
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

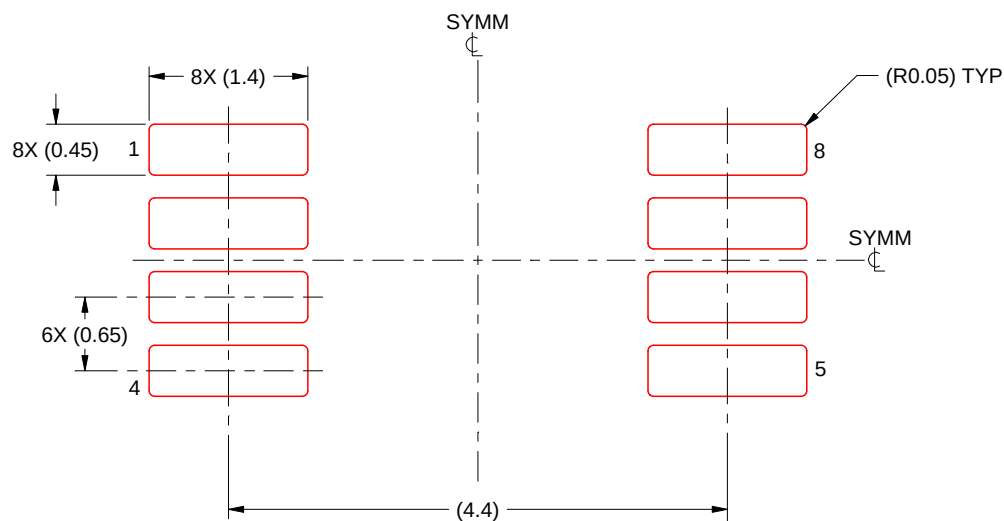
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

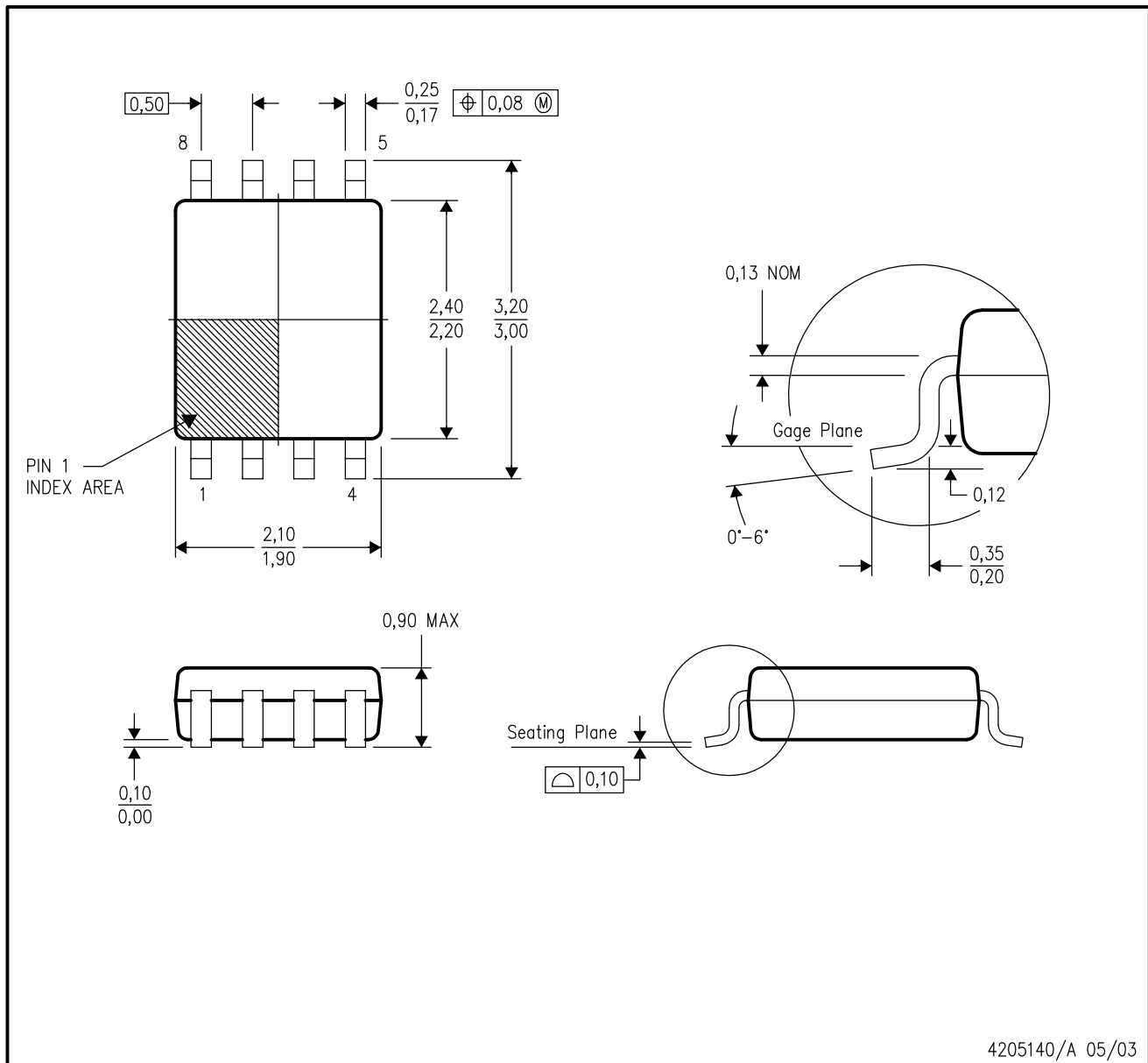
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

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