

## N-channel 900 V, 1.90 $\Omega$ typ., 3 A MDmesh™ K5 Power MOSFET in a TO-220 package

Datasheet - production data

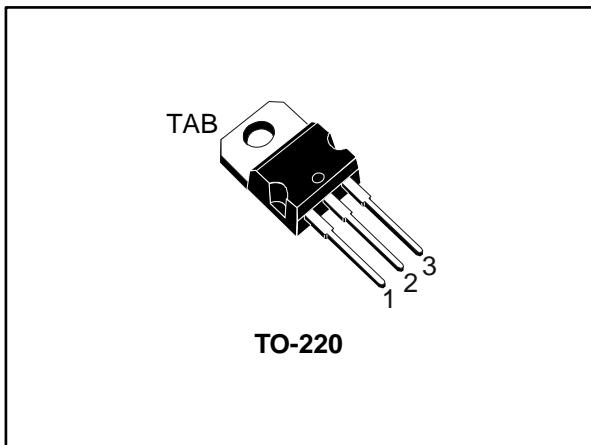
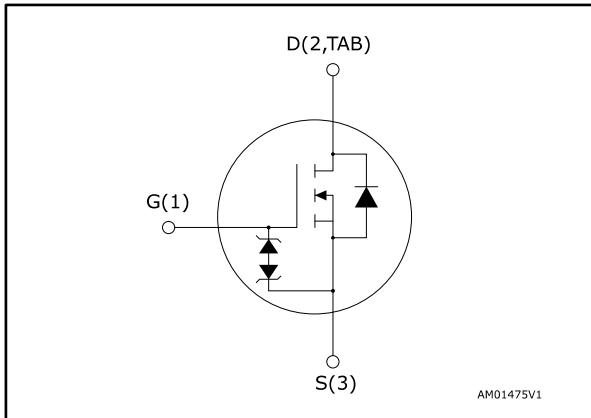


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$	$R_{DS(on)} \text{ max.}$	$I_D$
STP4N90K5	900 V	2.10 $\Omega$	3 A

- Industry's lowest  $R_{DS(on)} \times \text{area}$
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STP4N90K5	4N90K5	TO-220	Tube

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
2.1	Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
4.1	TO-220 package information.....	10
<b>5</b>	<b>Revision history .....</b>	<b>12</b>

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	3	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.9	A
$I_D^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_j$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

(1)Pulse width limited by safe operating area

(2) $I_{SD} \leq 3$  A,  $di/dt \leq 100$  A/ $\mu\text{s}$ ;  $V_{DS}$  peak  $< V_{(BR)DSS}$ ,  $V_{DD} = 450$  V.(3) $V_{DS} \leq 720$  V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50$ V)	160	mJ

## 2 Electrical characteristics

$T_C = 25^\circ\text{C}$  unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 1 \text{ mA}$	900			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 900 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0 \text{ V}$ , $V_{DS} = 900 \text{ V}$ $T_C = 125^\circ\text{C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DD} = V_{GS}$ , $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 1.5 \text{ A}$		1.90	2.10	$\Omega$

**Notes:**

(1) Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0 \text{ V}$	-	173	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	17.9	-	$\text{pF}$
$C_{rss}$	Reverse transfer capacitance		-	1	-	$\text{pF}$
$C_{o(\text{tr})}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{DS} = 0 \text{ to } 720 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	29	-	$\text{pF}$
$C_{o(\text{er})}$ <sup>(2)</sup>	Equivalent capacitance energy related		-	11	-	$\text{pF}$
$R_g$	Intrinsic gate resistance	$f = 1 \text{ MHz}$ , $I_D = 0 \text{ A}$	-	15.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 720 \text{ V}$ , $I_D = 3 \text{ A}$ $V_{GS} = 10 \text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	5.3	-	$\text{nC}$
$Q_{gs}$	Gate-source charge		-	1.45	-	$\text{nC}$
$Q_{gd}$	Gate-drain charge		-	2.8	-	$\text{nC}$

**Notes:**

(1) Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

(2) Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450 \text{ V}$ , $I_D = 1.50 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <i>Figure 14: "Test circuit for resistive load switching times"</i> and <i>Figure 19: "Switching time waveform"</i> )	-	10.5	-	ns
$t_r$	Rise time		-	11.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	26.4	-	ns
$t_f$	Fall time		-	25.5	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i> )	-	289		ns
$Q_{rr}$	Reverrse recovery charge		-	1.56		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	10.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 3 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150^\circ\text{C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i> )	-	494		ns
$Q_{rr}$	Reverse recovery charge		-	2.45		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	9.9		A

**Notes:**

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

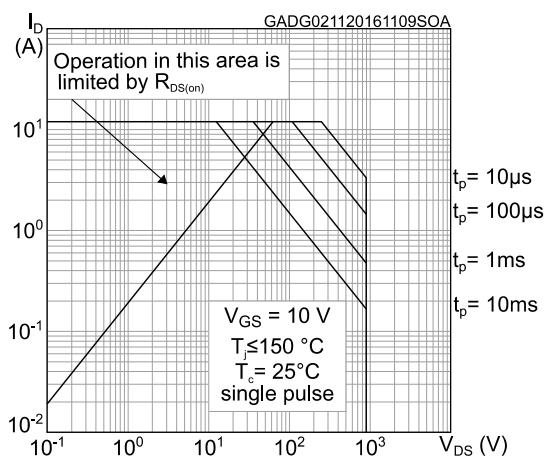


Figure 3: Thermal impedance

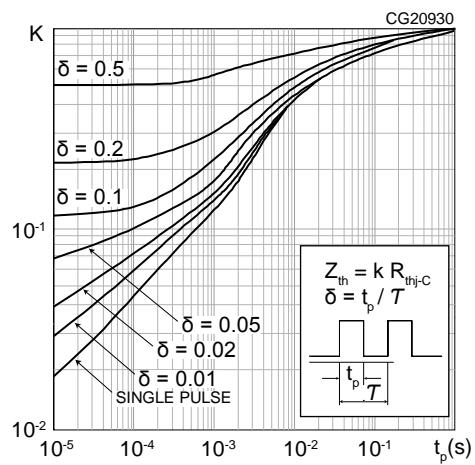


Figure 4: Output characteristics

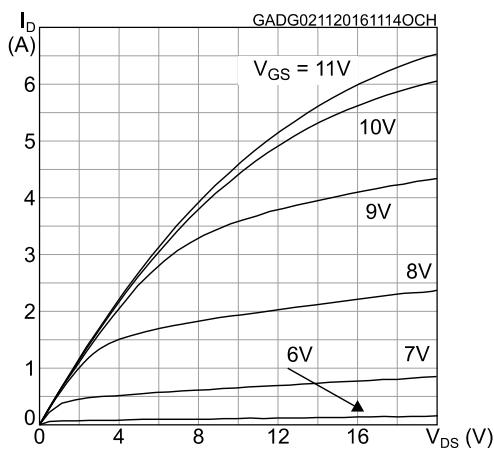


Figure 5: Transfer characteristics

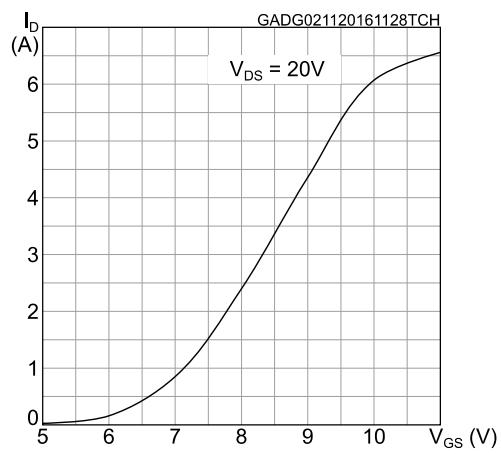


Figure 6: Gate charge vs gate-source voltage

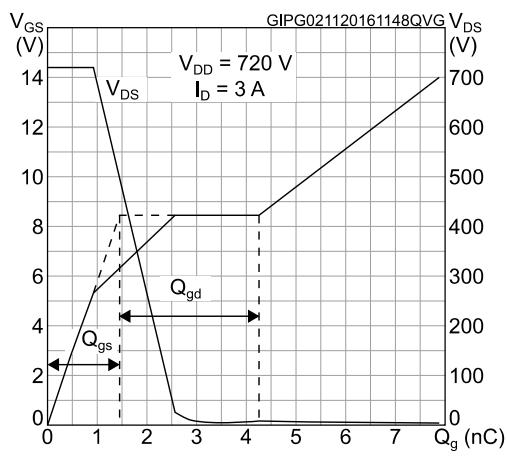
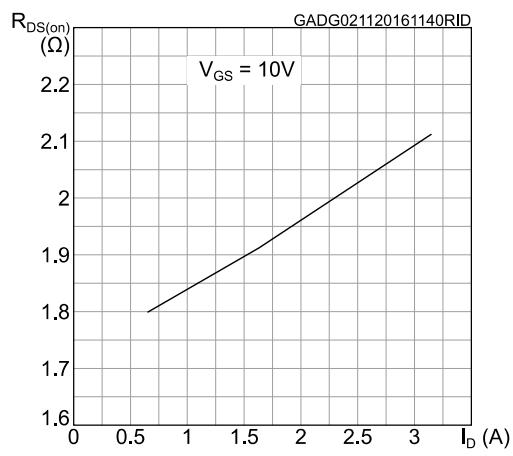
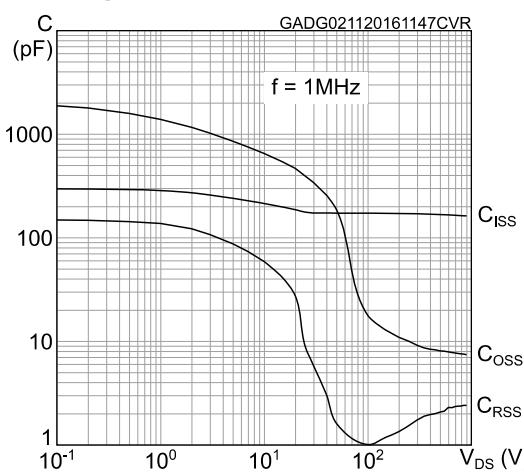
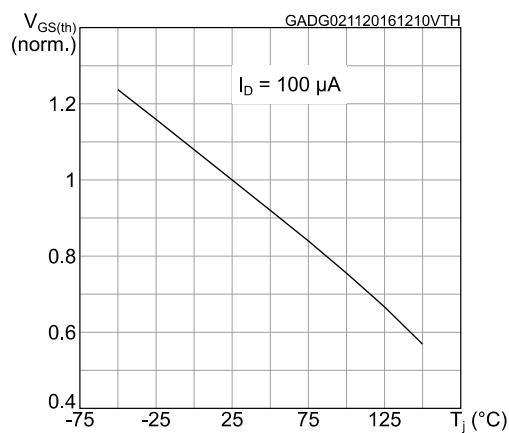
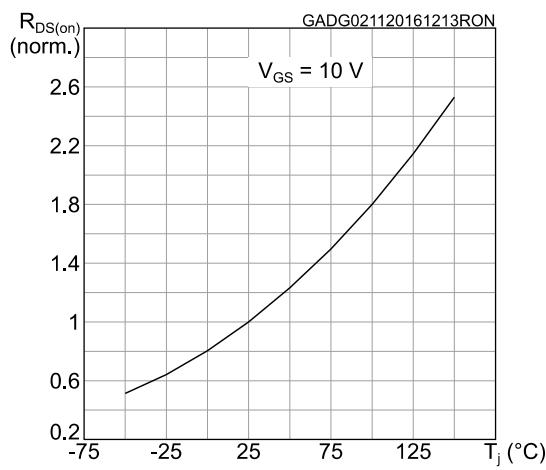
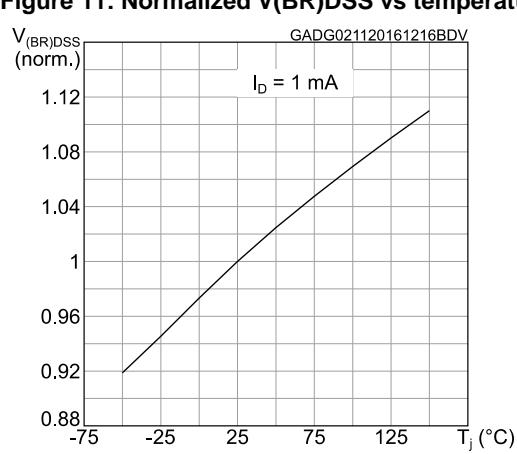
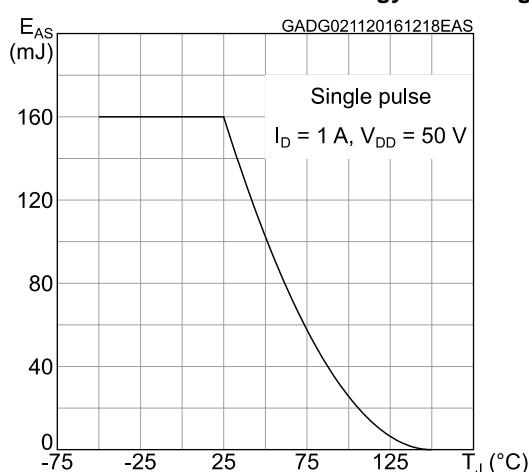
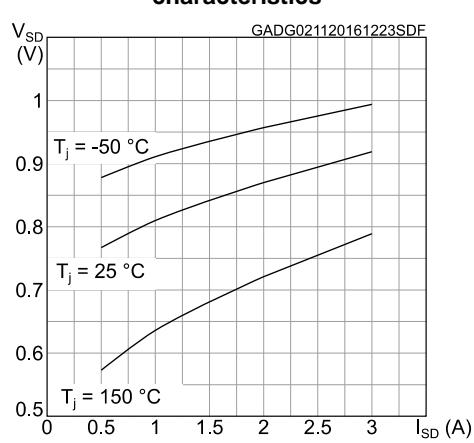


Figure 7: Static drain-source on-resistance



**Figure 8: Capacitance variations****Figure 9: Normalized gate threshold voltage vs temperature****Figure 10: Normalized on-resistance vs temperature****Figure 11: Normalized V(BR)DSS vs temperature****Figure 12: Maximum avalanche energy vs starting TJ****Figure 13: Source-drain diode forward characteristics**

### 3 Test circuits

Figure 14: Test circuit for resistive load switching times

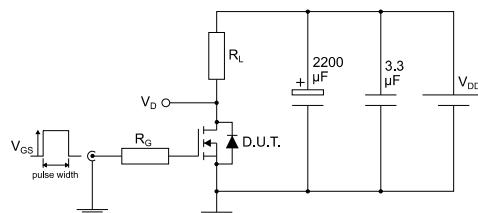


Figure 15: Test circuit for gate charge behavior

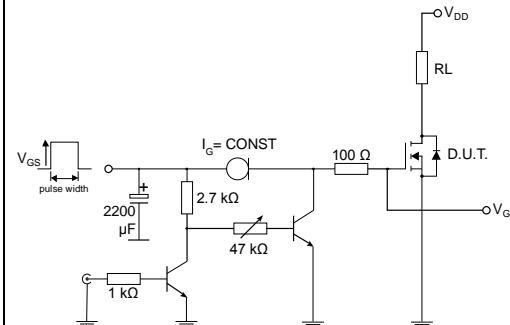


Figure 16: Test circuit for inductive load switching and diode recovery times

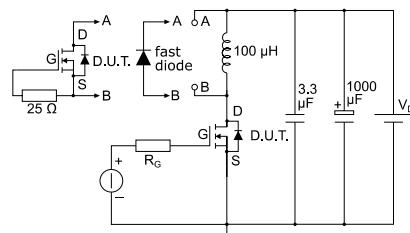


Figure 17: Unclamped inductive load test circuit

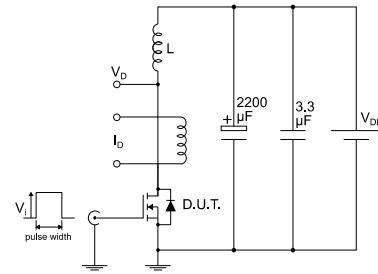


Figure 18: Unclamped inductive waveform

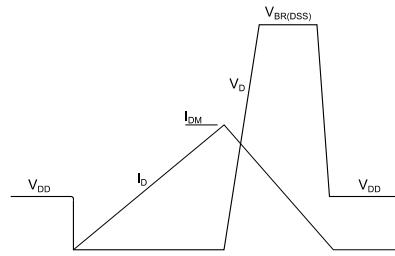
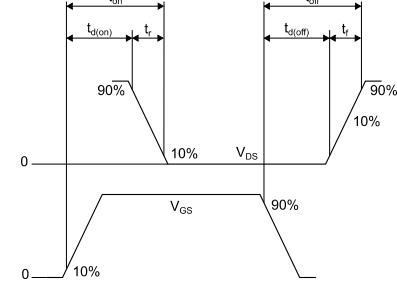


Figure 19: Switching time waveform



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 TO-220 package information

Figure 20: TO-220 type A package outline

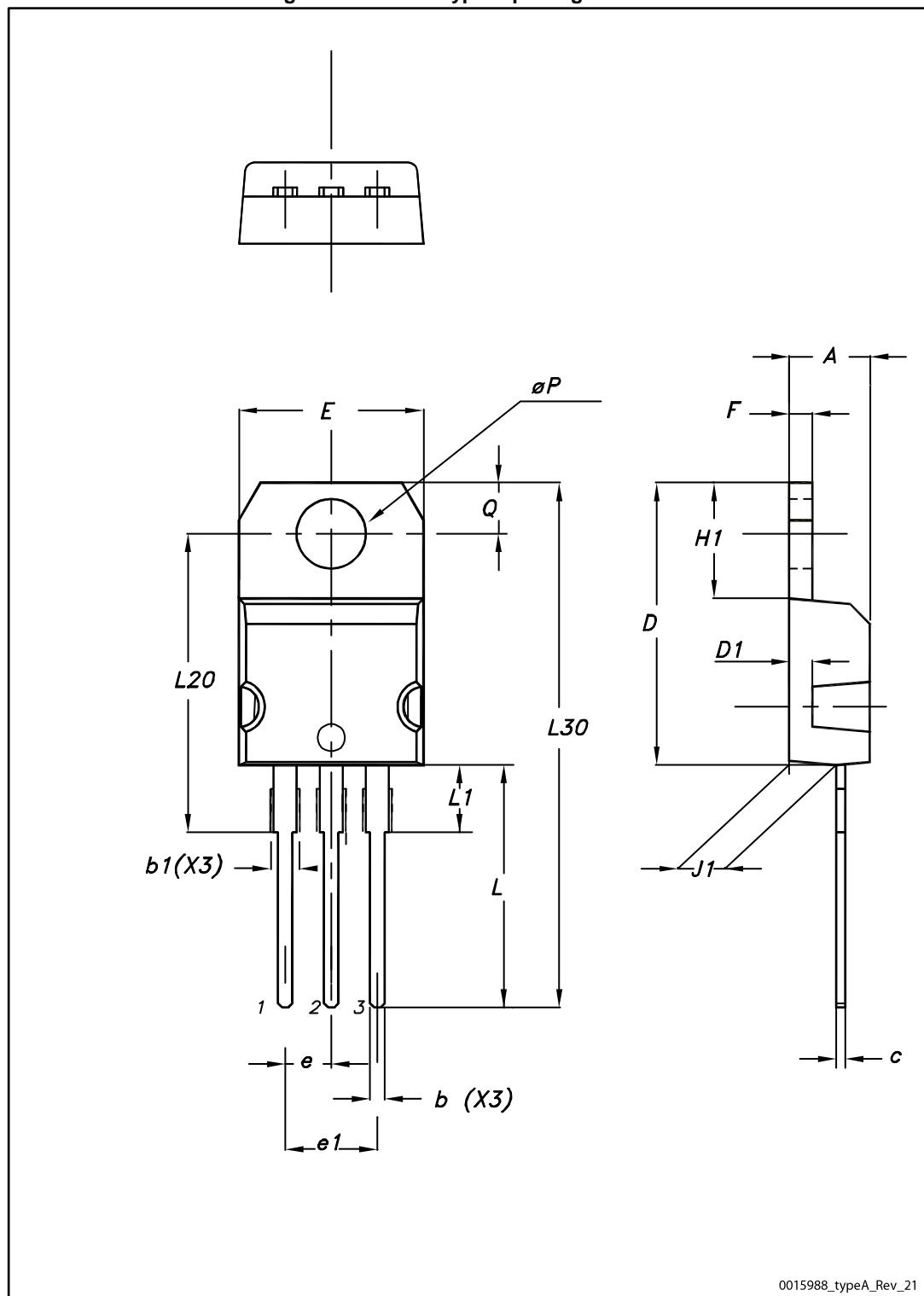


Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-Nov-2016	1	First release.

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