![Texas Instruments logo]

TSDxx Unidirectional TVS Diodes in SOD-323

1 Features

- IEC 61000-4-2 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 25-60A (8/20µs)
- IO capacitance < 20 (typical)
- Ultra low leakage current: 50nA (maximum)
- Industrial temperature range: –55°C to +150°C
- Industry standard SOD-323 leaded package (2.65mm × 1.3mm)

2 Applications

- USB VBUS
- GPIO
- Push buttons
- Grid infrastructure
- EPOS
- Portable electronics

3 Description

The TSDxx are a family of unidirectional TVS protection diodes designed for clamping harmful transients such as ESD and surge. The TSDxx is rated to dissipate ESD strikes up to ±30kV (contact and air gap discharge) and also meets the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

Combining the robust clamping performance and low capacitance of this device, TSDxx is an excellent TVS diode to protect both data and power lines in many different applications.

The TSDxx is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

Package Information

PART NUMBER	PACKAGE [1]	PACKAGE SIZE [2]
TSDxx	DYF (SOD-323, 2)	2.65mm × 1.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

ID Area
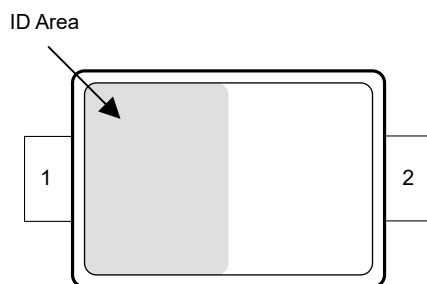
Figure 4-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel
2	GND	GND	Ground. Connect to ground.

(1) I = input, O = output. GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

PARAMETER		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 power (t_p – 8/20μs) at 25°C	TSD03		170	W
		TSD05		529	W
I_{PP}	IEC 61000-4-5 current (t_p – 8/20μs) at 25°C	TSD03		25	A
		TSD05		60	A
T_A	Ambient Operating Temperature		-55	150	°C
T_{stg}	Storage Temperature		-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002 [2]	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufactuuring with a standard ESD control proccess
(2) JEDEC document JEP157 states that 250V CDM allows safe manufactuuring with a standard ESD control proccess.

5.3 ESD Ratings - IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC [1]		TSD03	TSD05	UNIT
		DYF (SOD-323)	DYF (SOD-323)	
		2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	739.2	672.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	287.7	230.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	605.5	541.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	118.4	64.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	591.1	527.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics - TSD03

At TA = 25°C unless otherwise noted [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50nA, across operating temperature range			3.6	V
V_{BR}	Breakdown voltage	I_{IO} = 1mA, IO to GND	4.5			V
I_{LEAK}	Reverse leakage current	V_{IO} = 3.6V, IO to GND		5	50	nA
V_{FWD}	Forward voltage	I_{IO} = 1mA, GND to IO		0.8		V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs [2]	I_{PP} = 12A, IO to GND		6.3		V
		I_{PP} = 25A, IO to GND		7.7		V
		I_{PP} = 12A, GND to IO		3		V
		I_{PP} = 25A, GND to IO		4.9		V
	TLP clamping voltage, t_p = 100ns	I_{PP} = 16A, IO to GND		6.5		V
		I_{PP} = 16A, GND to IO		3.4		V
C_L	Line capacitance	V_{IO} = 0V, V_{p-p} = 30mV, f = 1MHz, IO to GND		4.5		pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20µs exponentially decaying waveform according to IEC 61000-4-5

5.7 Electrical Characteristics - TSD05

At TA=25℃ (unless otherwise noted) [1]

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <50nA, across operating temperature range			5.5	V
V_{BR}	Break-down voltage	I_{IO} = 1mA, IO to GND	6			V
I_{LEAK}	Reverse leakage current	V_{IO} = 5.5V, IO to GND		5	50	nA
V_{FWD}	Forward voltage	I_{IO} = 1mA, GND to IO		0.7		V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20μs [2]	I_{PP} = 24A, IO to GND		8	11.5	V
		I_{PP} = 60A, IO to GND		9	15	V
		I_{PP} = 60A, GND to IO		5.5		V
	TLP clamping voltage, t_p = 100ns	I_{PP} = 16A, IO to GND		7.5		V
		I_{PP} =16A, GND to IO		2.5		V
C_L	Line capacitance	V_{IO} = 0V; f = 1MHz, IO to GND		19		pF

(1)   Typical parameters are measured at 25℃
(2)   Nonrepetitive current pulse 8 to 20μs exponentially decaying waveform according to IEC 61000-4-5

Product Folder Links: *TSD03 TSD05*

5.8 Typical Characteristics
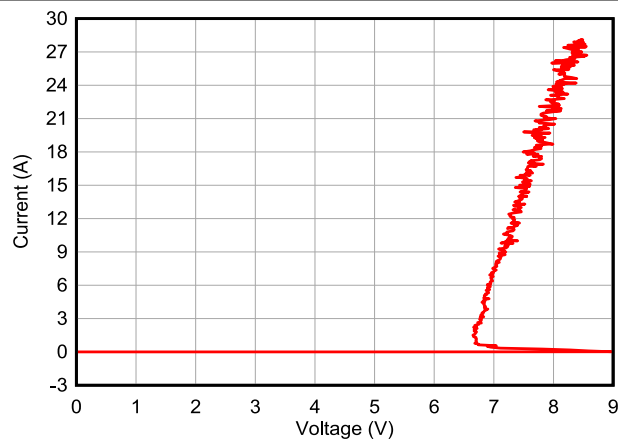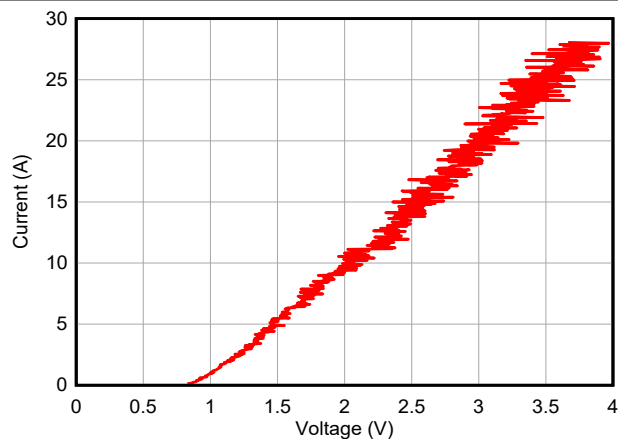

Figure 5-1. Positive TLP Curve

Figure 5-2. Negative TLP Curve

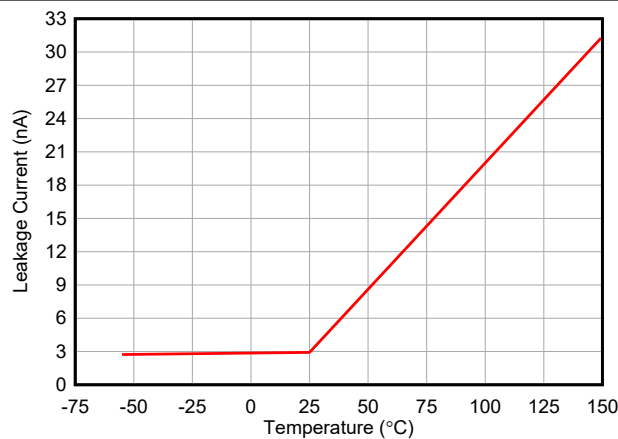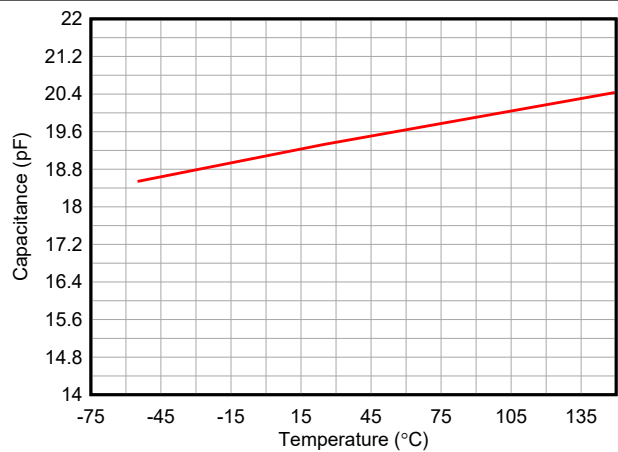**Figure 5-3. Temperature vs Leakage Current**

Figure 5-4. Temperature vs Capacitance
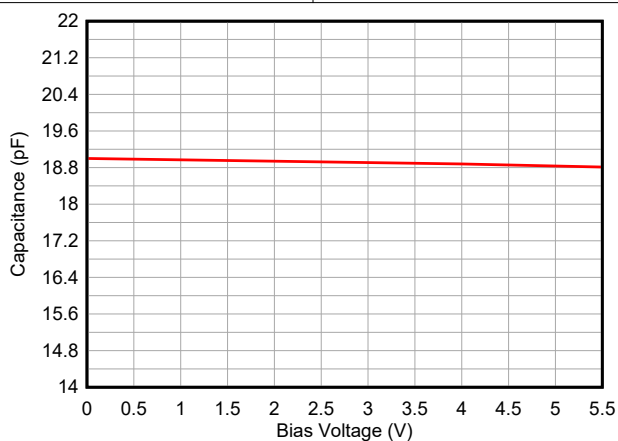
Figure 5-5. Bias Voltage vs Capacitance

Product Folder Links: *TSD03 TSD05*

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The TSDxx are TVS diodes that provide a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. The small voltage drop is presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

Product Folder Links: *TSD03 TSD05*

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:
• Texas Instruments, *ESD Layout Guide* application reports
• Texas Instruments, *Generic ESD Evaluation Module* user's guide
• Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2023	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Tape and Reel Information

REEL DIMENSIONS

TAPE DIMENSIONS

| A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
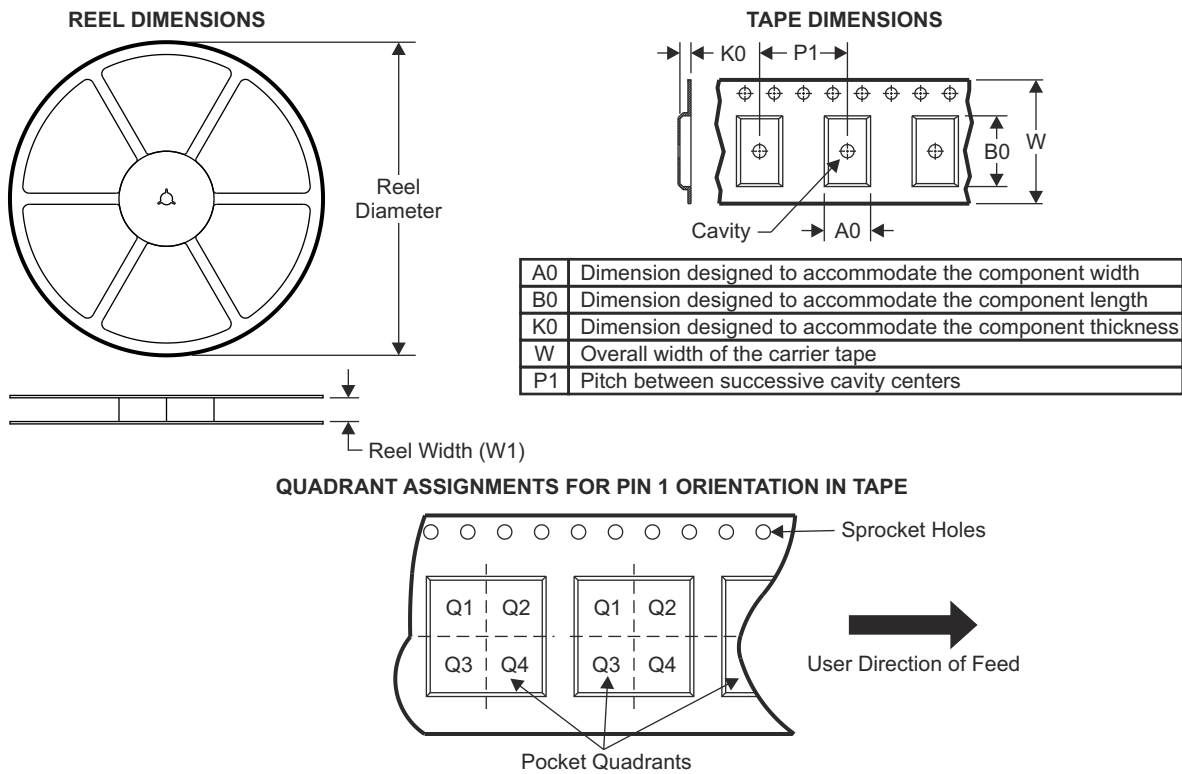
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD05DYFR	SOD-323	DYF	2	15000	178	8.4	0.36	0.66	0.33	0.2	8	Q1

Product Folder Links: *TSD03 TSD05*

TAPE AND REEL BOX DIMENSIONS
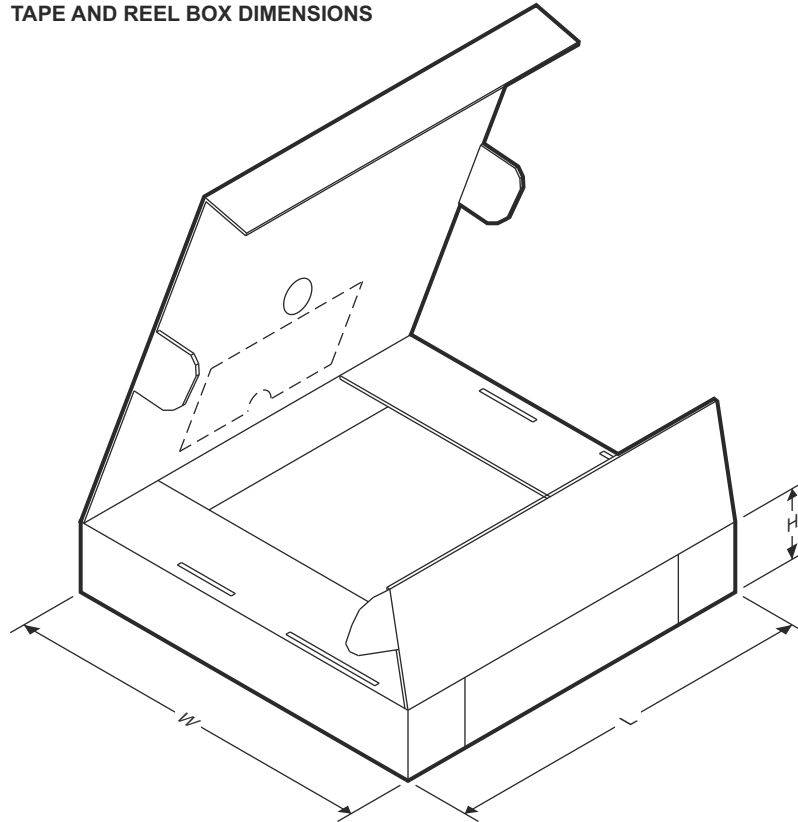
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD05DYFR	SOD-323	DYF	2	15000	205	200	33

9.2 Mechanical Data

PACKAGE OUTLINE

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR

2.75
2.55

1.8
1.6

1.4
1.2

1 (-)   2 (+)

2X 0.35
    0.25

PIN 1 ID

1 MAX

(0.85)   0.1 TYP
            0.0

(0.475)

0.2
GAGE PLANE

0°-8° TYP

0.40 TYP
0.25

0.15 TYP
0.08

4228484/A   02/2022
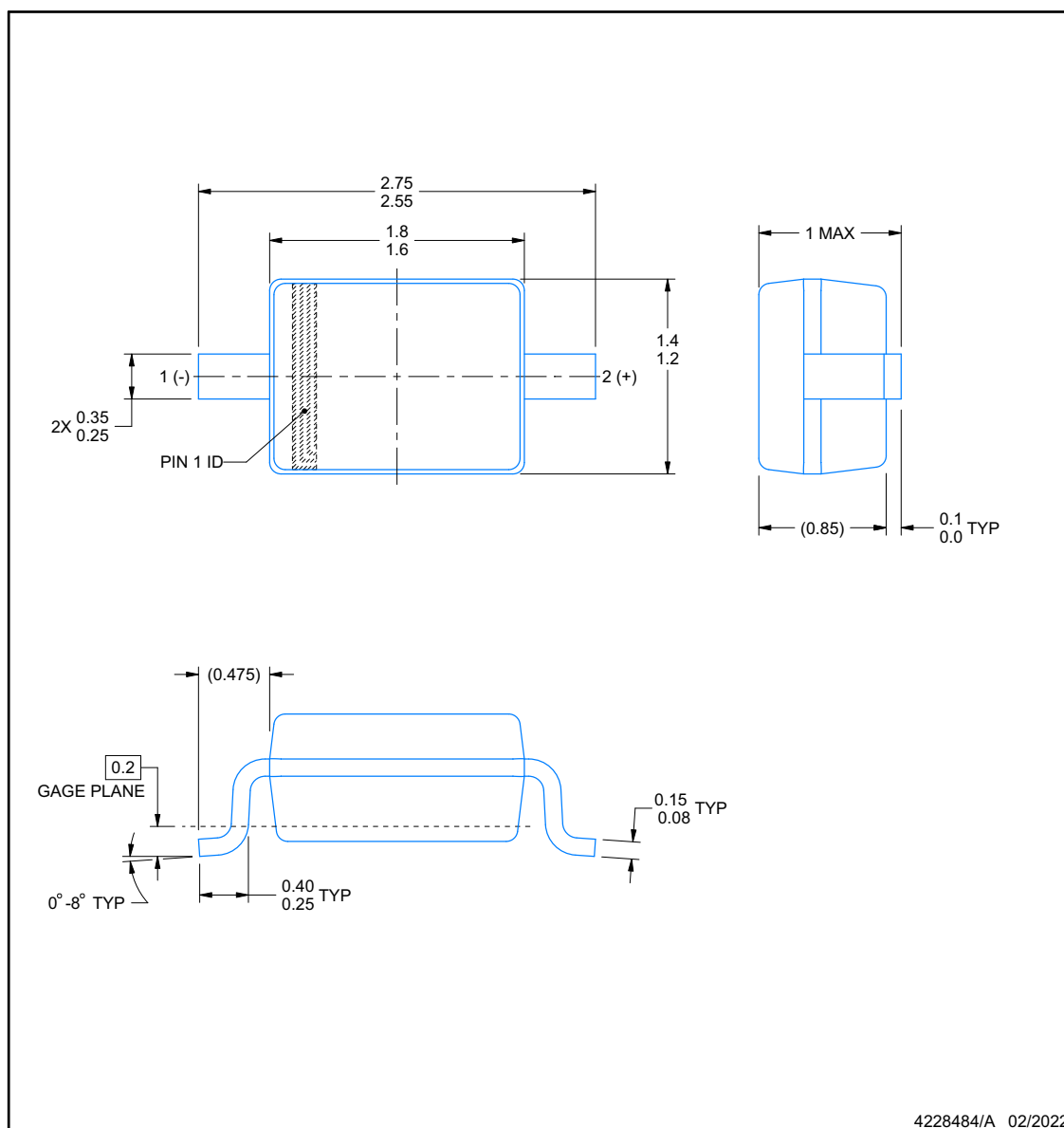
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

TEXAS INSTRUMENTS
www.ti.com

Product Folder Links: *TSD03 TSD05*

EXAMPLE BOARD LAYOUT
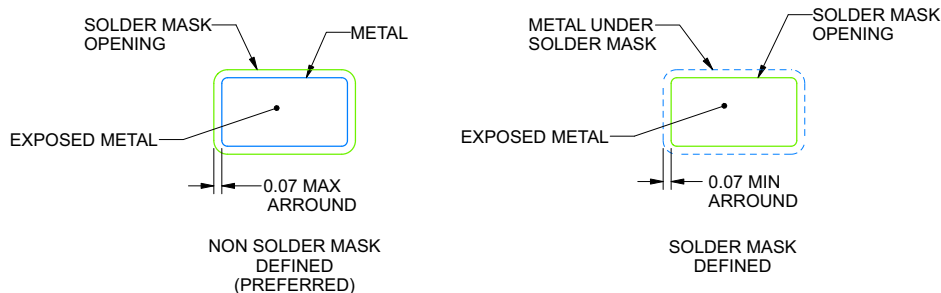
DYF0002A   SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR
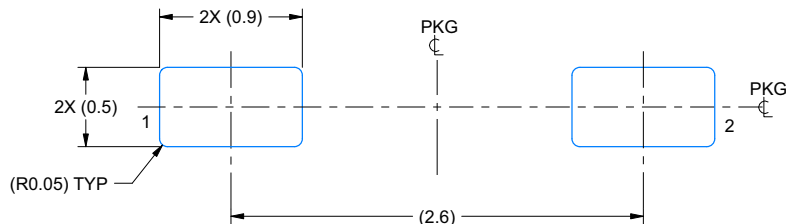
LAND PATTERN EXAMPLE
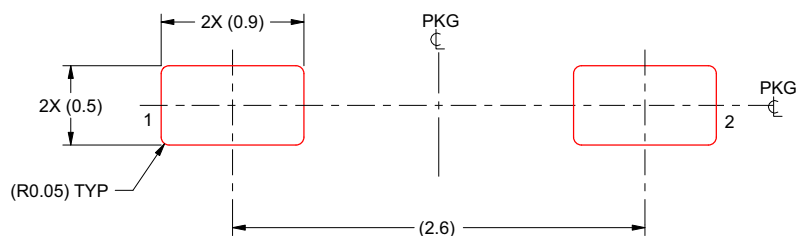EXPOSED METAL SHOWN
SCALE:25X

SOLDER MASK DETAILS

4228484/A   02/2022

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Product Folder Links: *TSD03 TSD05*

EXAMPLE STENCIL DESIGN

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4228484/A   02/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

TEXAS INSTRUMENTS
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Product Folder Links: *TSD03 TSD05*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSD03DYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR		3N5F	Samples
TSD05DYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33MF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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