REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Drawing updated to reflect current requirements. Editorial changes throughout. - gap	00-10-12	Raymond Monnin
F	Added device to cover 12 ns access time. Updated boilerplate, editorial changes throughout. - ksr	02-08-16	Raymond Monnin
G	Boilerplate update and part of five year review. - tcr	07-11-01	Robert M. Heber
H	Update boilerplate for current MIL-PRF-38535 requirements. - llb	16-03-17	Charles F. Saffle
J	Five Year Review boilerplate update to Section 508 Compliance and current MIL-PRF-38535 requirements. – llb	23-07-05	James R. Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
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DRAWING APPROVAL DATE
88-06-03

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

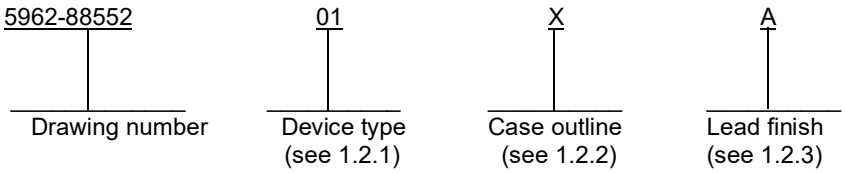
MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 32K X 8 STATIC RANDOM ACCESS MEMORY (SRAM) LOW POWER, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL J	SIZE A	CAGE CODE **67268**	**5962-88552**
		SHEET	1 OF 18	

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		32K x 8 low power CMOS SRAM	100 ns
02, 07			70 ns
03, 08			55 ns
04, 09			45 ns
05			35 ns
06			25 ns
10			20 ns
11			17 ns
12			15 ns
13			12 ns

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP3-F28	28	Flat pack
U	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
T	CDFP4-T28	28	Flat pack
M	CQCC3-N28	28	Rectangular leadless chip carrier
N	GDFP2-F28	28	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 2/
Input voltage range	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 3/
Power dissipation (P_D)	1.0 W
Junction temperature (soldering, 10 seconds)	+260°C

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
2/ All voltages referenced to V_{CC}.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc 4/
Ground voltage (V_{SS})	0 V dc
Input high voltage (V_{IH})	+2.2 V dc to V_{CC} +0.5 V dc
Input low voltage (V_{IL})	-0.5 V dc to 0.8 V dc
Case operating temperature (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

4/ All voltages referenced to V_{CC}.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = max, V_{IN} = GND to V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = max, V_{OUT} = GND to V_{CC} $\overline{CE} \ge V_{IH}$; $\overline{WE} \le V_{IL}$	1, 2, 3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Data retention voltage	V_{DR}		1, 2, 3	All	2.0		V
Operating supply current (active)	I_{CC1}	V_{CC} = 5.5 V, f = f max 1/, $\overline{CE}$ = V_{IL}, outputs open, all other inputs at V_{IL}	1, 2, 3	01, 02, 07,13		100	mA
				03, 08		125	
				04, 09		135	
				05		145	
				06, 11		155	
				10		150	
				12		160	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open V_{CC} = 5.5 V, f = 0 MHz	1, 2, 3	01 – 04		3	mA
				05 – 09, 13		5	
				10 – 12		10	
Standby power supply current (CMOS)	I_{CC3}	$\overline{CE} \ge (V_{CC}-0.2\ V)$, outputs open, all other inputs ≤ 0.2 V or ≥ (V_{CC}-0.2 V)	1, 2, 3	05, 07 – 09, 13		350	µA
				01-04, 06		800	
				10-12		750	
Data retention current	I_{CC4} 2/	V_{CC} = 3.0 V, $\overline{CE} \ge (V_{CC}-0.2\ V)$, f = 0 MHz, outputs open, all other inputs ≤ 0.2 V, or ≥ (V_{CC}-0.2 V)	1, 2, 3	05, 07 – 09, 13		350	µA
				01-04, 06		800	
				10-12		750	
Input capacitance	C_I 2/	V_I = 5.0 V or GND, f = 1 MHz, T_C = +25°C, See 4.3.1c	4	All		12	pF
Output capacitance	C_O 2/	V_O = 5.0 V or GND, f = 1 MHz, T_C = +25°C, See 4.3.1c	4	All		12	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}	3/	9, 10, 11	01	100		ns
				02,07	70		
				03,08	55		
				04,09	45		
				05	35		
				06	25		
				10	20		
				11	17		
				12	15		
				13	12		
Address access time	t_{AVQV}		9, 10, 11	01		100	ns
				02,07		70	
				03,08		55	
				04,09		45	
				05		35	
				06		25	
				10		20	
				11		17	
				12		15	
				13		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip-enable access time	t_{ELQV}		9, 10, 11	01		100	ns
				02,07		70	
				03,08		55	
				04,09		45	
				05		35	
				06		25	
				10		20	
				11		17	
				12		15	
				13		12	
Output hold from address change	t_{OLQV}		9, 10, 11	01 – 12	3		ns
				13	2		
Output enable to output valid	t_{OLQV}		9, 10, 11	01		60	ns
				02 – 04, 07 - 09		35	
				05, 06		20	
				10, 11		10	
				12		8	
				13		6	
Chip select to output in low Z	t_{ELQX} 2/ 4/		9, 10, 11	01 – 12	3		ns
				13	2		
Chip deselect to output in high Z	t_{EHQZ} 2/ 4/		9, 10, 11	01 – 04, 07, 09		35	ns
				05, 06		20	
				10 – 12		10	
				13		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output disable to output in high Z	t_{OHQZ} 2/ 4/		9, 10, 11	01		50	ns
				02 – 04, 07, 09		35	
				05, 06		20	
				10 – 12		10	
				13		7	
Write enable to output in high Z	t_{WLQZ} 2/ 4/		9, 10, 11	01		50	ns
				02 – 04, 07, 09		35	
				05, 06		20	
				10 – 12		10	
				13		7	
Output enable to output in low Z	t_{OLQX} 2/ 4/		9, 10, 11	All	0		ns
Retention time	t_{CDR}	$\overline{CE} \ge V_{CC}$-0.2 V	9, 10, 11	All	0		ns
Operation recovery time	t_R	$\overline{CE} \ge V_{CC}$-0.2 V	9, 10, 11	All	t_{AVAV}		ns
Data valid to end of write	t_{DVWH} t_{DVEH}		9, 10, 11	01 – 04, 07 – 09	35		ns
				05, 06	15		
				10 – 12	10		
				13	8		
Data hold time	t_{WHDX} t_{EHDX}		9, 10, 11	01 – 09	3		ns
				10 – 13	0		
Output active from end of write	t_{WHQX} 2/ 4/		9, 10, 11	01 – 09	3		ns
				10 – 13	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t_{AVAV}		9, 10, 11	01	100		ns
				02, 07	70		
				03, 08	55		
				04, 09	45		
				05	35		
				06	25		
				10, 11	20		
				12	15		
				13	12		
Chip select to end of write	t_{ELWH}	3/	9, 10, 11	01	90		ns
				02, 07	60		
				03, 08	50		
				04, 09	40		
				05	30		
				06	20		
				10, 11	15		
				12	12		
				13	10		
Address valid to end of write	t_{AVWH}		9, 10, 11	01	85		ns
				02, 07	60		
				03, 08	50		
				04, 09	40		
				05	30		
				06	20		
				10, 11	15		
				12	12		
				13	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address-setup time	t_{AVEL} t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	01	55		ns
				02, 07	45		
				03, 08	40		
				04, 09	35		
				05	30		
				06	25		
				10, 11	15		
				12	12		
				13	9		
Write recovery time	t_{WHAX} t_{EHAX}		9, 10, 11	01 – 09	7		ns
				10 – 13	0		

1/ f max = $1/t_{AVAV}$.
2/ This parameter tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For output load circuits see figure 3 and for timing waveforms see figure 4.
4/ Transition is measured ±500 mV from steady state voltage.

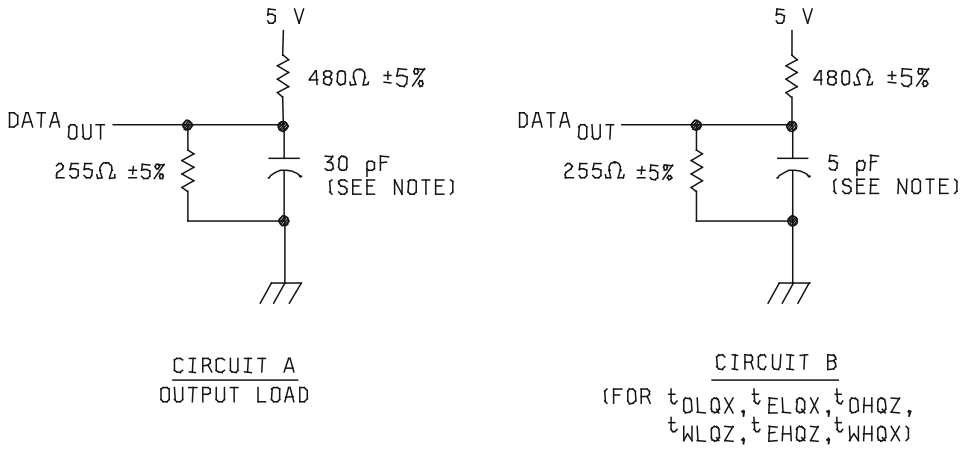
All device types		
Case outlines	**X, Z, U, T, M, and N**	**Y**
Terminal numbers	Terminal symbol	
1	A_{14}	NC
2	A_{12}	A_{14}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	I/O_1	A_0
12	I/O_2	NC
13	I/O_3	I/O_1
14	GND	I/O_2
15	I/O_4	I/O_3
16	I/O_5	GND
17	I/O_6	NC
18	I/O_7	I/O_4
19	I/O_8	I/O_5
20	$\overline{CE}$	I/O_6
21	A_{10}	I/O_7
22	$\overline{OE}$	I/O_8
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	$\overline{WE}$	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	$\overline{WE}$
32	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Function
H	X	X	High Z	Standby (I_{CC2})
≥ V_{CC} -0.2 V	X	X	High Z	Standby (I_{CC3})
L	H	H	High Z	Output disable
L	H	L	Data out	Read
L	L	X	Data in	Write

FIGURE 2. Truth table.



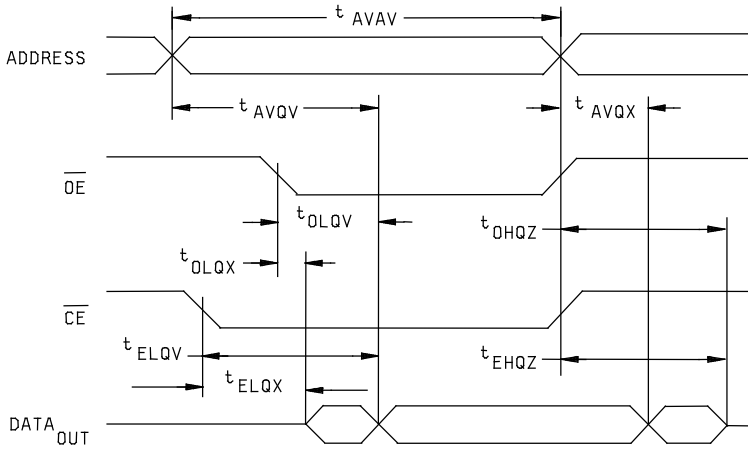
NOTE: Including scope and jig. (minimum values)

AC test conditions

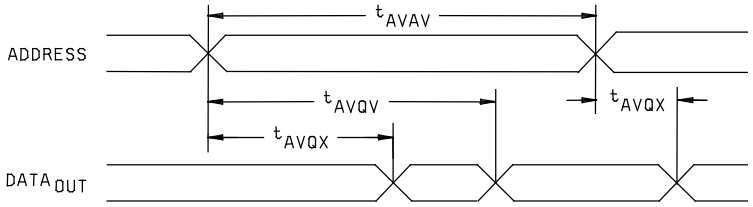
Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit.

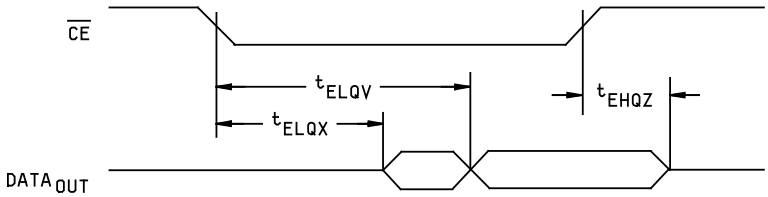
Timing waveform of read cycle number 1 (see note 1)



Timing waveform of read cycle number 2 (see notes 1, 2, and 4)



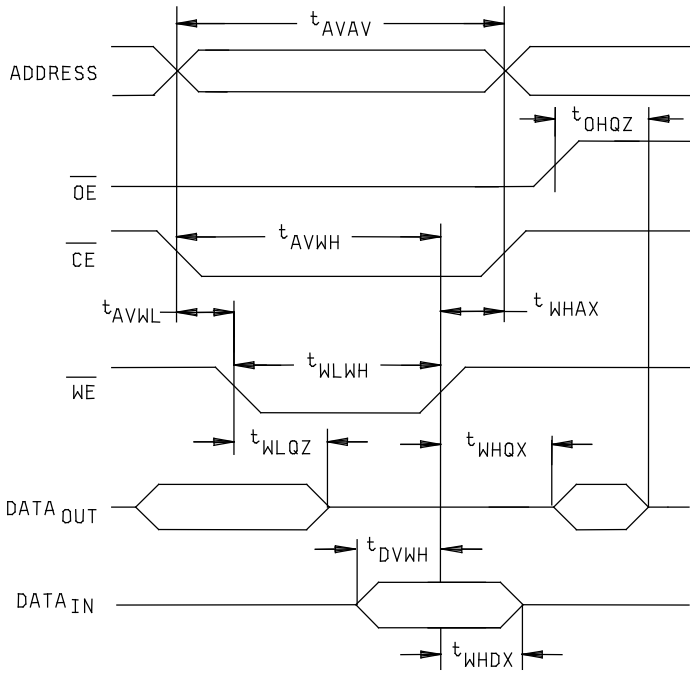
Timing waveform of read cycle number 3 (see notes 1, 3, and 4)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$- V_{IL}.
5. Transition is measured ±500 mV from steady state with 5 pF load (including scope and jig).

FIGURE 4. Timing waveforms.

Timing waveform of write cycle number 1 ($\overline{WE}$ controlled timing) (see notes 1, 2, 3, 6, and 7)



Timing waveform of write cycle number 2 ($\overline{CE}$ controlled timing) (see notes 1, 2, 3, and 5)

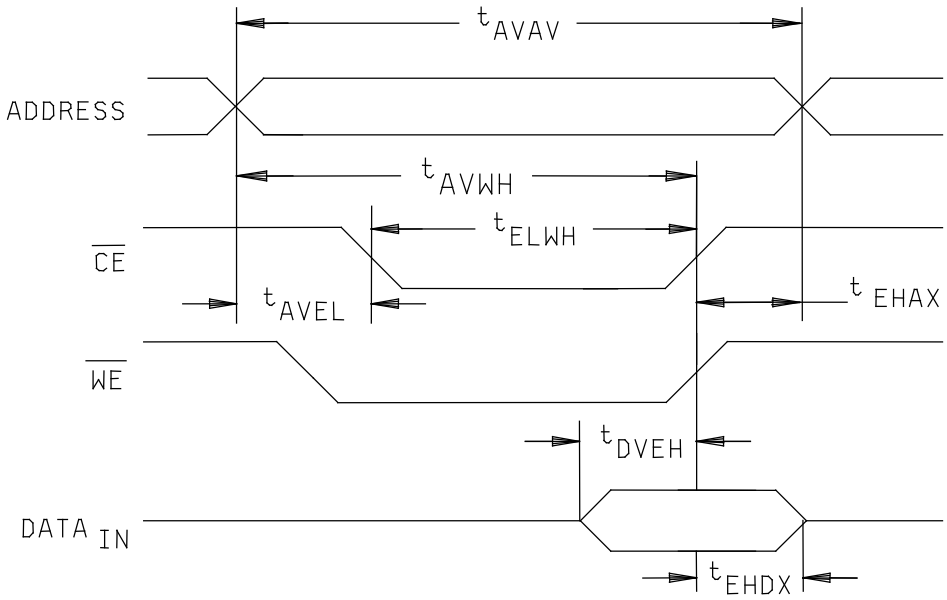


FIGURE 4. Timing waveforms - Continued.

NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for required t_{DVWH}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 4. Timing waveforms - Continued.

Low V_{CC} retention waveform

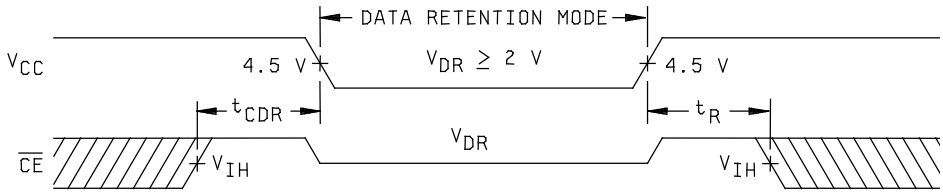


FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883 and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A, 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1.
** See 4.3.1c.
*** See 4.3.1d.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7, 8A, and 8B shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-07-05

Approved sources of supply for SMD 5962-88552 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855201MA	3DTT2	P4C1256L-100L28MB
	3/	IDT71256L100L28B
5962-8855201NA	3/	IDT71256L100XEB
	0C7V7	QP7C199L-100KMB
	3DTT2	P4C1256L-100FMB
5962-8855201TA	3DTT2	P4C1256L-100FSSMB
5962-8855201UA	8QEK4	IDT71256L100TDB
	0C7V7	QP7C199L-100DMB
	3DTT2	P4C1256L-100CMB
5962-8855201XA	3/	EDI8833LP100CB
	8QEK4	IDT71256L100DB
	0C7V7	QP7C198L-100DMB
	3DTT2	P4C1256L-100CWMB
5962-8855201YA	3/	EDI8833LP100LB
	3/	IDT71256L100L32B
	0C7V7	QP7C198L-100LMB
	3DTT2	P4C1256L-100L32MB
5962-8855201ZA	3/	IDT71256L100EB
	3DTT2	P4C1256L-100FSMB
5962-8855202MA	3/	IDT71256L70L28B
	3DTT2	P4C1256L-70L28MB
5962-8855202NA	0C7V7	QP7C199L-70KMB
	3/	IDT71256L70TDB
	3DTT2	P4C1256L-70FMB
	3/	IDT71256L70XEB
5962-8855202TA	3DTT2	P4C1256L-70FSSMB
5962-8855202UA	0C7V7	QP7C199L-70DMB
	8QEK4	IDT71256L70DB
	3DTT2	P4C1256L-70CMB
5962-8855202XA	3/	EDI8833LP70CB
	8QEK4	IDT71256L70DB
	3/	MC51256L-70/B
	0C7V7	QP7C198L-70DMB
	3DTT2	P4C1256L-70CWMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855202YA	0C7V7	QP7C198L-70LMB
	3DTT2	P4C1256L-70L32MB
	3/	EDI8833LP70LB
	3/	IDT71256L70L32B
	3/	MR51256L-70/B
5962-8855202ZA	3DTT2	P4C1256L-70FSMB
	3/	IDT71256L70EB
5962-8855203MA	3DTT2	P4C1256L-55L28MB
	3/	IDT71256L55L28B
	3/	L7C199KMB55L
5962-8855203NA	0C7V7	QP7C199L-55KMB
	3DTT2	P4C1256L-55FMB
	3/	IDT71256L55XEB
	3/	L7C199MMB55L
5962-8855203TA	3DTT2	P4C1256L-55FSSMB
5962-8855203UA	0C7V7	QP7C199L-55DMB
	8QEK4	IDT71256L55TDB
	3DTT2	P4C1256L-55DMB
5962-8855203XA	0C7V7	QP7C198L-55DMB
	8QEK4	IDT71256L55DB
	3DTT2	P4C1256L-55DWMB
	3/	L7C199HMB55L
5962-8855203YA	0C7V7	QP7C198L-55LMB
	3DTT2	P4C1256L-55L32MB
	3/	IDT71256L55L32B
	3/	L7C199TMB55L
5962-8855203ZA	3DTT2	P4C1256L-55FSMB
	3/	IDT71256L55EB
	3/	L7C199CMB55L
5962-8855204MA	3DTT2	P4C1256L-45L28MB
	3/	IDT71256L45L28B
	3/	L7C199KMB45L
5962-8855204NA	0C7V7	QP7C199L-45KMB
	3DTT2	P4C1256L-45FMB
	3/	IDT71256L45XEB
	3/	L7C199CMB45L
5962-8855204TA	3DTT2	P4C1256L-45FSSMB
5962-8855204UA	0C7V7	QP7C199L-45DMB
	8QEK4	IDT71256L45TDB
	3DTT2	P4C1256L-45DMB
	3/	L7C199CMB45L

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855204XA	0C7V7	QP7C198L-45DMB
	8QEK4	IDT71256L45DB
	3DTT2	P4C1256L-45DWMB
	3/	L7C199IMB45L
	3/	MC51256L-45/B
5962-8855204YA	0C7V7	QP7C198L-45LMB
	3/	IDT71256L45L32B
	3DTT2	P4C1256L-45L32MB
	3/	L7C199TMB45L
	3/	MR51256L-45/B
5962-8855204ZA	3DTT2	P4C1256L-45FSMB
	3/	IDT71256L45EB
5962-8855205MA	0C7V7	QP7C199L-35LMB
	3DTT2	P4C1256L-35L28MB
	57300	AS5C2568EC-35L/883C
	3/	L7C199CMB35L
5962-8855205NA	0C7V7	QP7C199L-35KMB
	3DTT2	P4C1256L-35FMB
	3/	L7C199CMMB45L
5962-8855205TA	0C7V7	QP7C199L-35FMB
	3DTT2	P4C1256L-35FSSMB
	57300	AS5C2568F-35L/883C
	3/	EDI8833LP35FB
5962-8855205UA	0C7V7	QP7C199L-35DMB
	3DTT2	P4C1256L-35CMB
	57300	AS5C2568C-35L/883C
	3/	EDI8833LPA35QB
	3/	IDT71256L35TCB
	3/	L7C199CMB35L
5962-8855205XA	0C7V7	QP7C198L-35DMB
	3DTT2	P4C1256L-35DWMB
	57300	AS5C2568CW-35L/883C
	3/	EDI8833LP35CB
	3/	IDT71256L35DB
	3/	L7C199IMB35L
5962-8855205YA	0C7V7	QP7C198L-35LMB
	3DTT2	P4C1256L-35L32MB
	57300	AS5C2568ECW-35L/883C
	3/	EDI8833LP35LB
	3/	IDT71256L35L32B
	3/	L7C199TMB35L

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855205ZA	3DTT2	P4C1256L-35FSMB
	3/	IDT71256L35EB
5962-8855206MA	0C7V7	QP7C199L-25LMB
	3DTT2	P4C1256L-25L28MB
	57300	AS5C2568EC-25L/883C
	3/	IDT71256L25L28B
	3/	L7C199KMB25L
5962-8855206NA	0C7V7	QP7C199L-25KMB
	3DTT2	P4C1256L-25FMB
	3/	IDT71256L25XEB
	3/	L7C199MMB25L
5962-8855206TA	0C7V7	QP7C199L-25FMB
	3DTT2	P4C1256L-25FSSMB
	57300	AS5C2568F-25L/883C
5962-8855206UA	0C7V7	QP7C199L-25DMB
	8QEK4	IDT71256L25TDB
	3DTT2	P4C1256L-25DMB
	57300	AS5C2568C-25L/883C
	3/	L7C199CMB25L
5962-8855206XA	0C7V7	QP7C198L-25DMB
	8QEK4	IDT71256L25DB
	3DTT2	P4C1256L-25DWMB
	57300	AS5C2568CW-25L/883C
	3/	L7C199IMB25L
5962-8855206YA	0C7V7	QP7C198L-25LMB
	3/	IDT71256L25L32B
	3DTT2	P4C1256L-25L32MB
	57300	AS5C2568ECW-25L/883C
	3/	L7C199TMB25L
5962-8855206ZA	3DTT2	P4C1256L-25FSMB
	3/	IDT71256L25EB
5962-8855207MA	0C7V7	QP7C199L-70LMB
	3DTT2	P4C1256L-70L28MB
	57300	AS5C2568EC-70L/883C
5962-8855207NA	0C7V7	QP7C199L-70KMB
	3DTT2	P4C1256L-70FMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855207TA	0C7V7	QP7C199L-70FMB
	3DTT2	P4C1256L-70FSSMB
	57300	AS5C2568F-70L/883C
	3/	EDI8833LP70FB
5962-8855207UA	0C7V7	QP7C199L-70DMB
	3DTT2	P4C1256L-70DMB
	57300	AS5C2568C-70L/883C
	3/	EDI8833LPA70QB
	3/	IDT71256L70TCB
5962-8855207XA	0C7V7	QP7C198L-70DMB
	3DTT2	P4C1256L-70DWMB
	57300	AS5C2568CW-70L/883C
	3/	EDI8833LP70CB
	3/	IDT71256L70DB
5962-8855207YA	0C7V7	QP7C198L-70LMB
	3DTT2	P4C1256L-70L32MB
	57300	AS5C2568ECW-70L/883C
	3/	EDI8833LP70LB
	3/	IDT71256L70L32B
5962-8855207ZA	3DTT2	P4C1256L-70FSMB
	3/	IDT71256L70EB
5962-8855208MA	0C7V7	QP7C199L-55LMB
	3DTT2	P4C1256L-55L28MB
	57300	AS5C2568EC-55L/883C
	3/	L7C199KMB55L
5962-8855208NA	0C7V7	QP7C199L-55KMB
	3DTT2	P4C1256L-55FMB
	3/	L7C199MMB55L
5962-8855208TA	0C7V7	QP7C199L-55FMB
	3DTT2	P4C1256L-55FSSMB
	57300	AS5C2568F-55L/883C
	3/	EDI8833LP55FB
5962-8855208UA	0C7V7	QP7C199L-55DMB
	3DTT2	P4C1256L-55DMB
	57300	AS5C2568C-55L/883C
	3/	EDI8833LPA55QB
	3/	IDT71256L55TCB
	3/	L7C199CMB55L

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855208XA	3DTT2	P4C1256L-55DWMB
	0C7V7	QP7C198L-55DMB
	57300	AS5C2568CW-55L/883C
	3/	EDI8833LP55CB
	3/	IDT71256L55DB
	3/	L7C199IMB55L
5962-8855208YA	0C7V7	QP7C198L-55LMB
	3DTT2	P4C1256L-55L32MB
	57300	AS5C2568ECW-55L/883C
	3/	EDI8833LP55LB
	3/	IDT71256L55L32B
	3/	L7C199TMB55L
5962-8855208ZA	3DTT2	P4C1256L-55FSMB
	3/	IDT71256L55EB
5962-8855209MA	0C7V7	QP7C199L-45LMB
	3DTT2	P4C1256L-45L28MB
	57300	AS5C2568EC-45L/883C
	3/	L7C199KMB45L
5962-8855209NA	0C7V7	QP7C199L-45KMB
	3DTT2	P4C1256L-45FMB
	3/	L7C199MMB45L
5962-8855209TA	0C7V7	QP7C199L-45FMB
	3DTT2	P4C1256L-45FSSMB
	57300	AS5C2568F-45L/883C
	3/	EDI8833LP45FB
5962-8855209UA	0C7V7	QP7C199L-45DMB
	3DTT2	P4C1256L-45DMB
	57300	AS5C2568C-45L/883C
	3/	EDI8833LPA45QB
	3/	IDT71256L45TCB
	3/	L7C199CMB45L
5962-8855209XA	0C7V7	QP7C198L-45DMB
	3DTT2	P4C1256L-45DWMB
	57300	AS5C2568CW-45L/883C
	3/	EDI8833LP45CB
	3/	IDT71256L45DB
	3/	L7C199IMB45L

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855209YA	0C7V7	QP7C198L-45LMB
	3DTT2	P4C1256L-45L32MB
	57300	AS5C2568ECW-45L/883C
	3/	EDI8833LP45LB
	3/	IDT71256L45L32B
	3/	L7C199TMB45L
5962-8855209ZA	3DTT2	P4C1256L-45FSMB
	3/	IDT71256L45EB
5962-8855210MA	0C7V7	QP7C199L-20LMB
	3DTT2	P4C1256L-20L28MB
	57300	AS5C2568EC-20L/883C
	3/	L7C199KMB20L
5962-8855210NA	0C7V7	QP7C199L-20KMB
	3DTT2	P4C1256L-20FMB
	3/	L7C199MMB20L
5962-8855210TA	0C7V7	QP7C199L-20FMB
	3DTT2	P4C1256L-20FSSMB
	57300	AS5C2568F-20L/883C
5962-8855210UA	0C7V7	QP7C199L-20DMB
	3DTT2	P4C1256L-20CMB
	57300	AS5C2568C-20L/883C
	3/	PDM41256LA20DB
5962-8855210XA	0C7V7	QP7C198L-20DMB
	3DTT2	P4C1256L-20DWMB
	57300	AS5C2568CW-20L/883C
	3/	L7C199IMB20L
5962-8855210YA	0C7V7	QP7C198L-20LMB
	3DTT2	P4C1256L-20L32MB
	57300	AS5C2568ECW-20L/883C
	3/	PDM41256LA20L32B
5962-8855211MA	0C7V7	QP7C199L-17LMB
	3DTT2	P4C1256L-17L28MB
	57300	AS5C2568EC-17L/883C
	3/	L7C199KMB17L
5962-8855211NA	0C7V7	QP7C199L-17KMB
	3DTT2	P4C1256L-17FMB
	3/	L7C199MMB17L
5962-8855211TA	0C7V7	QP7C199L-17FMB
	3DTT2	P4C1256L-17FSSMB
	57300	AS5C2568F-17L/883C

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855211UA	0C7V7	QP7C199L-17DMB
	3DTT2	P4C1256L-17DMB
	57300	AS5C2568C-17L/883C
	3/	PDM41256LA17DB
5962-8855211XA	0C7V7	QP7C198L-17DMB
	3DTT2	P4C1256L-17CWMB
	57300	AS5C2568CW-17L/883C
	3/	L7C199IMB17L
5962-8855211YA	0C7V7	QP7C198L-17LMB
	3DTT2	P4C1256L-17L32MB
	57300	AS5C2568ECW-17L/883C
	3/	PDM41256LA17L32B
5962-8855211ZA	3DTT2	P4C1256L-17FSMB
5962-8855212MA	0C7V7	QP7C199L-15LMB
	3DTT2	P4C1256L-15L28MB
	57300	AS5C2568EC-15L/883C
	3/	L7C199KMB15L
5962-8855212NA	0C7V7	QP7C199L-15KMB
	3DTT2	P4C1256L-15FMB
	3/	L7C199MMB15L
5962-8855212TA	0C7V7	QP7C199L-15FMB
	3DTT2	P4C1256L-15FSSMB
	57300	AS5C2568F-15L/883C
5962-8855212UA	0C7V7	QP7C199L-15DMB
	3DTT2	P4C1256L-15DMB
	57300	AS5C2568C-15L/883C
	3/	PDM41256LA15DB
5962-8855212XA	0C7V7	QP7C199L-15DMB
	3DTT2	P4C1256L-15DWMB
	57300	AS5C2568CW-15L/883C
	3/	PDM41256LA15DB
5962-8855212YA	0C7V7	QP7C198L-15LMB
	3DTT2	P4C1256L-15L32MB
	57300	AS5C2568ECW-15L/883C
	3/	PDM41256LA15L32B
5962-8855212ZA	3DTT2	P4C1256L-15FSMB
5962-8855213MA	0C7V7	QP7C199L-12LMB
	3DTT2	P4C1256L-12L28M8
	57300	AS5C2568EC-12L/883C
5962-8855213NA	0C7V7	QP7C199L-12KMB
	3DTT2	P4C1256L-12FMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8855213TA	0C7V7	QP7C199L-12FMB
	3DTT2	P4C1256L-12FSSMB
	57300	AS5C2568F-12L/883C
5962-8855213UA	0C7V7	QP7C199L-12DMB
	3DTT2	P4C1256L-12DMB
	57300	AS5C2568C-12L/883C
5962-8855213XA	0C7V7	QP7C198L-12DMB
	3DTT2	P4C1256L-12DWMB
	57300	AS5C2568CW-12L/883C
5962-8855213YA	0C7V7	QP7C198L-12LMB
	3DTT2	P4C1256L-12L32MB
	57300	AS5C2568ECW-12L/883C
5962-8855213ZA	3DTT2	P4C1256L-12FSMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	Teledyne e2v, Inc. 765 Sycamore Drive Milpitas, CA 95035
8QEK4	Renesas Electronics America, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138
57300	Micross Components 7725 N. Orange Blossom Trail Orlando, FL 32810-2696
3DTT2	Pyramid Semiconductor Corporation 1249 Reamwood Avenue Sunnyvale, CA 94089

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.