S-93L46A/56A/66A

LOW VOLTAGE OPERATION 3-WIRE SERIAL E^2PROM

www.ablicinc.com

© ABLIC Inc., 2004-2015

The S-93L46A/56A/66A is a low voltage operation, high speed, low current consumption, 3-wire serial E^2PROM with a wide operating voltage range. The S-93L46A/56A/66A has the capacity of 1 K-bit, 2 K-bit and 4 K-bit, and the organization is 64-word × 16-bit, 128-word × 16-bit, and 256-word × 16-bit. It is capable of sequential read, at which time addresses are automatically incremented in 16-bit blocks.
The communication method is by the Microwire bus.

■ Features

- Operating voltage range: Read 1.6 V to 5.5 V
  Write 1.8 V to 5.5 V (WRITE, ERASE)
  2.7 V to 5.5 V (WRAL, ERAL)
- Operation frequency: 2.0 MHz (V_{CC} = 4.5 V to 5.5 V)
- Write time: 8.0 ms max.
- Sequential read capable
- Write protect function during the low power supply voltage
- Function to protect against write due to erroneous instruction recognition
- Endurance: 10^6 cycles / word*1 (Ta = +85°C)
- Data retention: 100 years (Ta = +25°C)
  20 years (Ta = +85°C)
- Memory capacity: S-93L46A: 1 K-bit
  S-93L56A: 2 K-bit
  S-93L66A: 4 K-bit
- Initial delivery state: FFFFh
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free, Sn 100%, halogen-free*2

***1.** For each address (Word: 16-bit)
***2.** Refer to "■ **Product Name Structure**" for details.

■ Packages

- 8-Pin SOP (JEDEC)
- 8-Pin TSSOP
- TMSOP-8
- SNT-8A

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Pin Configurations

1. 8-Pin SOP (JEDEC)

8-Pin SOP (JEDEC)
Top view

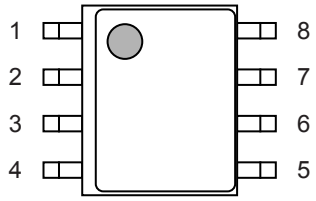


Figure 1

S-93L46AD0I-J8T1x
S-93L56AD0I-J8T1x
S-93L66AD0I-J8T1x

Table 1

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

8-Pin SOP (JEDEC) (Rotated)
Top view

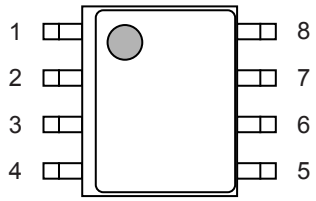


Figure 2

S-93L46AR0I-J8T1x
S-93L56AR0I-J8T1x
S-93L66AR0I-J8T1x

Table 2

Pin No.	Symbol	Description
1	NC	No connection
2	VCC	Power supply
3	CS	Chip select input
4	SK	Serial clock input
5	DI	Serial data input
6	DO	Serial data output
7	GND	Ground
8	TEST*1	Test

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark 1. Refer to the "**Package drawings**" for the details.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

2. 8-Pin TSSOP

8-Pin TSSOP
Top view

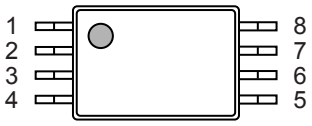


Figure 3

S-93L46AD0I-T8T1x
S-93L56AD0I-T8T1x
S-93L66AD0I-T8T1x

Table 3

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

3. TMSOP-8

TMSOP-8
Top view

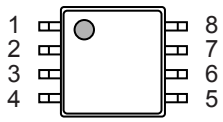


Figure 4

S-93L46AD0I-K8T3U
S-93L56AD0I-K8T3U
S-93L66AD0I-K8T3U

Table 4

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

4. SNT-8A

SNT-8A
Top view

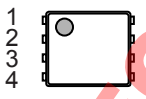


Figure 5

S-93L46AD0I-I8T1U
S-93L56AD0I-I8T1U
S-93L66AD0I-I8T1U

Table 5

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark 1. Refer to the "**Package drawings**" for the details.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Block Diagram

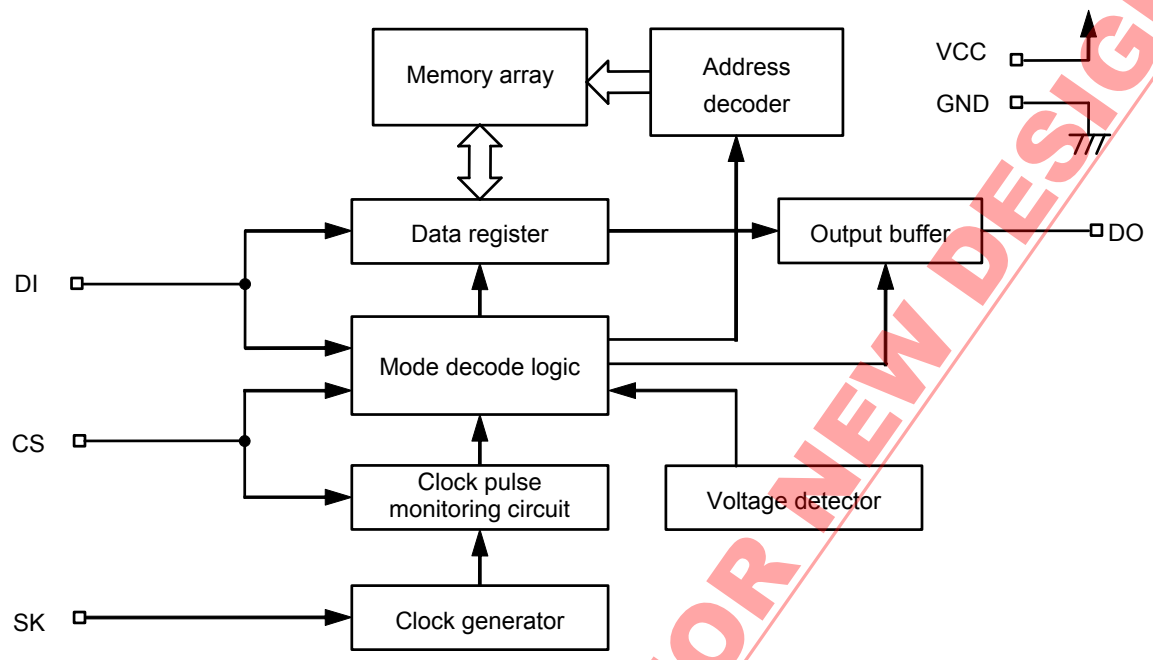


Figure 6

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Instruction Sets

1. S-93L46A

Table 6

Instruction SK input clock	Start Bit	Operation Code		Address						Data
	1	2	3	4	5	6	7	8	9	10 to 25
READ (Read data)	1	1	0	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

2. S-93L56A

Table 7

Instruction SK input clock	Start Bit	Operation Code		Address								Data
	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Read data)	1	1	0	x	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	x	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	x	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

3. S-93L66A

Table 8

Instruction SK input clock	Start Bit	Operation Code		Address								Data
	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Read data)	1	1	0	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	A7	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Absolute Maximum Ratings

Table 9

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operation ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 10

Item	Symbol	Conditions	Ta = −40°C to +85°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	READ, EWDS	1.6	5.5	V
		WRITE, ERASE, EWEN	1.8	5.5	V
		WRAL, ERAL	2.7	5.5	V
High level input voltage	V_{IH}	V_{CC} = 4.5 V to 5.5 V	2.0	V_{CC}	V
		V_{CC} = 2.7 V to 4.5 V	0.8 × V_{CC}	V_{CC}	V
		V_{CC} = 1.6 V to 2.7 V	0.8 × V_{CC}	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V to 5.5 V	0.0	0.8	V
		V_{CC} = 2.7 V to 4.5 V	0.0	0.2 × V_{CC}	V
		V_{CC} = 1.6 V to 2.7 V	0.0	0.15 × V_{CC}	V

■ Pin Capacitance

Table 11

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Conditions	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	10	pF

■ Endurance

Table 12

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	NW	Ta = −40°C to +85°C	10^6	—	Cycles / word*1

*1. For each address (Word: 16-bit)

■ Data Retention

Table 13

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data Retention	—	Ta = +25°C	100	—	year
		Ta = −40°C to +85°C	20	—	year

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ DC Electrical Characteristics

Table 14

Item	Symbol	Conditions	Ta = −40°C to +85°C						Unit
			V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 1.6 V to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	0.8	—	0.5	—	0.4	mA

Table 15

Item	Symbol	Conditions	Ta = −40°C to +85°C				Unit
			V_{CC} = 4.5 V to 5.5 V		V_{CC} = 1.8 V to 4.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	2.0	—	1.5	mA

Table 16

Item	Symbol	Conditions	Ta = −40°C to +85°C						Unit
			V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 1.6 V to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other input pins are V_{CC} or GND	—	1.5	—	1.5	—	1.5	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	—	—	—	V
		I_{OL} = 100 μA	—	0.1	—	0.1	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = −400 μA	2.4	—	—	—	—	—	V
		I_{OH} = −100 μA	V_{CC} − 0.3	—	V_{CC} − 0.3	—	—	—	V
		I_{OH} = −10 μA	V_{CC} − 0.2	—	V_{CC} − 0.2	—	V_{CC} − 0.2	—	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	—	1.5	—	1.5	—	V

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ AC Electrical Characteristics

Table 17 Measurement Conditions

Input pulse voltage	0.1 × V_{CC} to 0.9 × V_{CC}
Output reference voltage	0.5 × V_{CC}
Output load	100 pF

Table 18

Item	Symbol	Ta = −40°C to +85°C						Unit
		V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 1.6 V to 2.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
CS setup time	t_{CSS}	0.2	—	0.4	—	1.0	—	µs
CS hold time	t_{CSH}	0	—	0	—	0	—	µs
CS deselect time	t_{CDS}	0.2	—	0.2	—	0.4	—	µs
Data setup time	t_{DS}	0.1	—	0.2	—	0.4	—	µs
Data hold time	t_{DH}	0.1	—	0.2	—	0.4	—	µs
Output delay time	t_{PD}	—	0.4	—	0.8	—	2.0	µs
Clock frequency*1	f_{SK}	0	2.0	0	1.0	0	0.25	MHz
SK clock time "L" *1	t_{SKL}	0.1	—	0.25	—	1.0	—	µs
SK clock time "H" *1	t_{SKH}	0.1	—	0.25	—	1.0	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.15	0	0.5	0	1.0	µs
Output enable time	t_{SV}	0	0.15	0	0.5	0	1.0	µs

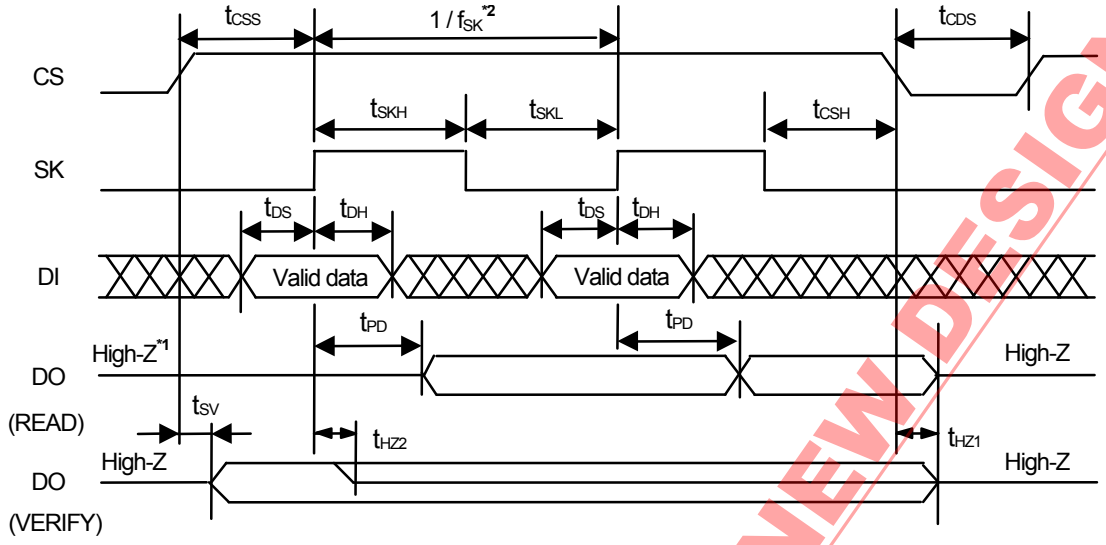
*1. The clock cycle of the SK clock (frequency: f_{SK}) is 1 / f_{SK} µs. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle (1 / f_{SK}) cannot be made equal to t_{SKL} (min.) + t_{SKH} (min.).

Table 19

Item	Symbol	Ta = −40°C to +85°C			Unit
		V_{CC} = 1.8 V to 5.5 V			
		Min	Typ.	Max.	
Write time	t_{PR}	—	4.0	8.0	ms

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.



***1.** Indicates high impedance.

***2.** $1 / f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1 / f_{SK}$) cannot be made equal to t_{SKL} (min.) + t_{SKH} (min.).

Figure 7 Timing Chart

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Initial Delivery State

Initial delivery state of all addresses is “FFFFh”.

■ Operation

All instructions are executed by inputting DI in synchronization with the rising edge of SK after CS goes high. An instruction set is input in the order of start bit, instruction, address, and data.
Instruction input finishes when CS goes low. A low level must be input to CS between commands during t_{CDS}. While a low level is being input to CS, the S-93L46A/56A/66A is in standby mode, so the SK and DI inputs are invalid and no instructions are allowed.

■ Start Bit

A start bit is recognized when the DI pin goes high at the rise of SK after CS goes high. After CS goes high, a start bit is not recognized even if the SK pulse is input as long as the DI pin is low.

1. Dummy clock

SK clocks input while the DI pin is low before a start bit is input are called dummy clocks. Dummy clocks are effective when aligning the number of instruction sets (clocks) sent by the CPU with those required for serial memory operation. For example, when a CPU instruction set is 16 bits, the number of instruction set clocks can be adjusted by inserting a 7-bit dummy clock for the S-93L46A and a 5-bit dummy clock for the S-93L56A/66A.

2. Start bit input failure

- When the output status of the DO pin is high during the verify period after a write operation, if a high level is input to the DI pin at the rising edge of SK, the S-93L46A/56A/66A recognizes that a start bit has been input. To prevent this failure, input a low level to the DI pin during the verify operation period (refer to “**4. 1 Verify operation**”).

- When a 3-wire interface is configured by connecting the DI input pin and DO output pin, a period in which the data output from the CPU and the serial memory collide may be generated, preventing successful input of the start bit. Take the measures described in “**■ 3-Wire Interface (Direct Connection between DI and DO)**”.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

3. Reading (READ)

The READ instruction reads data from a specified address.
After CS has gone high, input an instruction in the order of the start bit, read instruction, and address. Since the last input address (A_0) has been latched, the output status of the DO pin changes from high impedance (High-Z) to low, which is held until the next rise of SK. 16-bit data starts to be output in synchronization with the next rise of SK.

3. 1 Sequential read

After the 16-bit data at the specified address has been output, inputting SK while CS is high automatically increments the address, and causes the 16-bit data at the next address to be output sequentially. The above method makes it possible to read the data in the whole memory space. The last address (A_n ••• A_1 A_0 = 1 ••• 1 1) rolls over to the top address (A_n ••• A_1 A_0 = 0 ••• 0 0).

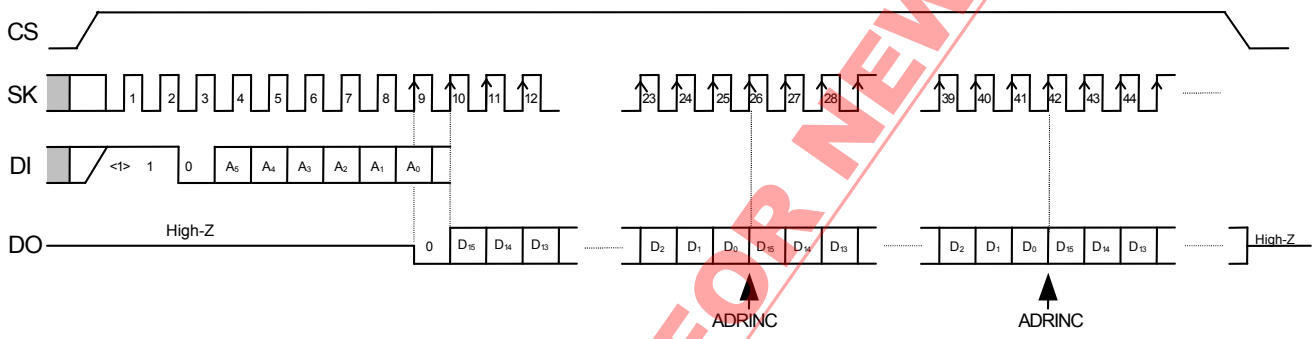


Figure 8 Read Timing (S-93L46A)

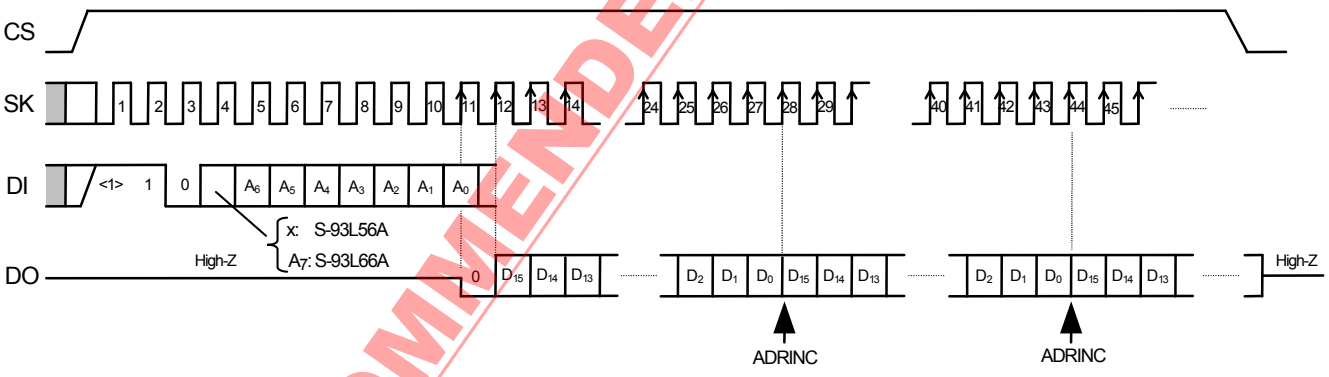


Figure 9 Read Timing (S-93L56A, S-93L66A)

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

4. Writing (WRITE, ERASE, WRAL, ERAL)

A write operation includes four write instructions: data write (WRITE), data erase (ERASE), chip write (WRAL), and chip erase (ERAL).
A write instruction (WRITE, ERASE, WRAL, ERAL) starts a write operation to the memory cell when a low level is input to CS after a specified number of clocks have been input. The SK and DI inputs are invalid during the write period, so do not input an instruction.
Input an instruction while the output status of the DO pin is high or high impedance (High-Z).
A write operation is valid only in program enable mode (refer to "**5. Write enable (EWEN) and write disable (EWDS)**").

4. 1 Verify operation

A write operation executed by any instruction is completed within 8 ms (write time t_{PR}: typically 4 ms), so if the completion of the write operation is recognized, the write cycle can be minimized. A sequential operation to confirm the status of a write operation is called a verify operation.

4. 1. 1 Operation

After the write operation has started (CS = low), the status of the write operation can be verified by confirming the output status of the DO pin by inputting a high level to CS again. This sequence is called a verify operation, and the period that a high level is input to the CS pin after the write operation has started is called the verify operation period.
The relationship between the output status of the DO pin and the write operation during the verify operation period is as follows.

- DO pin = low: Writing in progress (busy)
- DO pin = high: Writing completed (ready)

4. 1. 2 Operation example

There are two methods to perform a verify operation: Waiting for a change in the output status of the DO pin while keeping CS high, or suspending the verify operation (CS = low) once and then performing it again to verify the output status of the DO pin. The latter method allows the CPU to perform other processing during the wait period, allowing an efficient system to be designed.

Caution 1. Input a low level to the DI pin during a verify operation.
2. If a high level is input to the DI pin at the rise of SK when the output status of the DO pin is high, the S-93L46A/56A/66A latches the instruction assuming that a start bit has been input. In this case, note that the DO pin immediately enters a high-impedance (High-Z) state.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

4. 2 Writing data (WRITE)

To write 16-bit data to a specified address, change CS to high and then input the WRITE instruction, address, and 16-bit data following the start bit. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRITE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

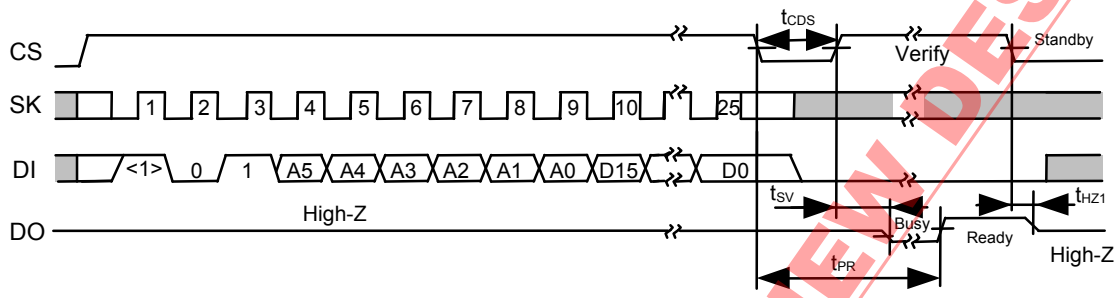


Figure 10 Data Write Timing (S-93L46A)

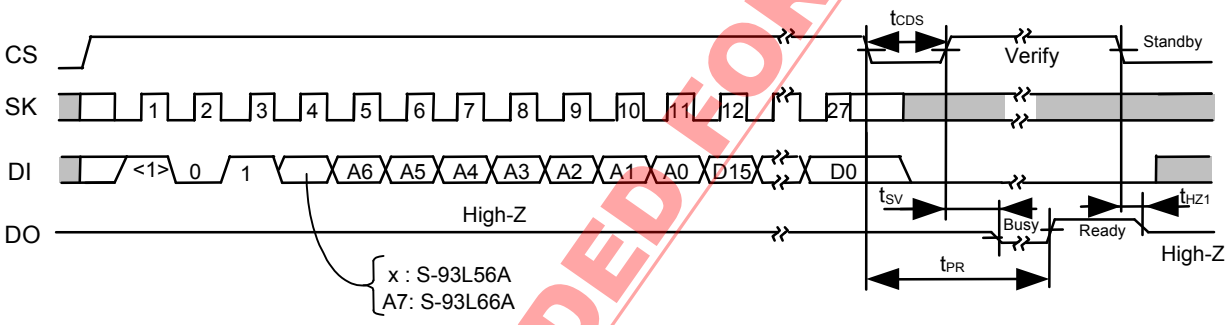


Figure 11 Data Write Timing (S-93L56A, S-93L66A)

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

4. 3 Erasing data (ERASE)

To erase 16-bit data at a specified address, set all 16 bits of the data to 1, change CS to high, and then input the ERASE instruction and address following the start bit. There is no need to input data. The data erase operation starts when CS goes low. If the clocks have been input more than the specified number, the clock pulse monitoring circuit cancels the ERASE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

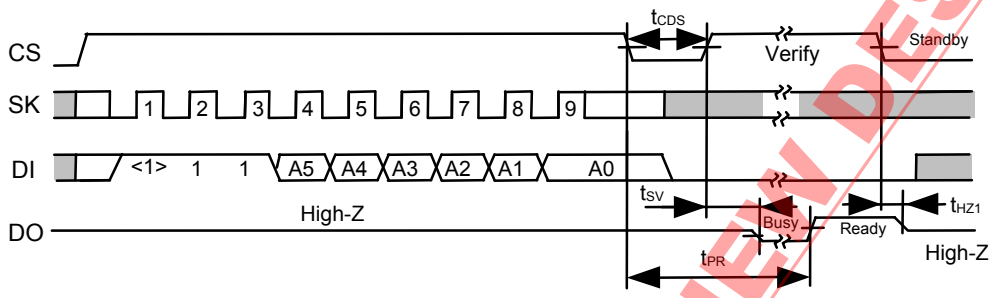


Figure 12 Data Erase Timing (S-93L46A)

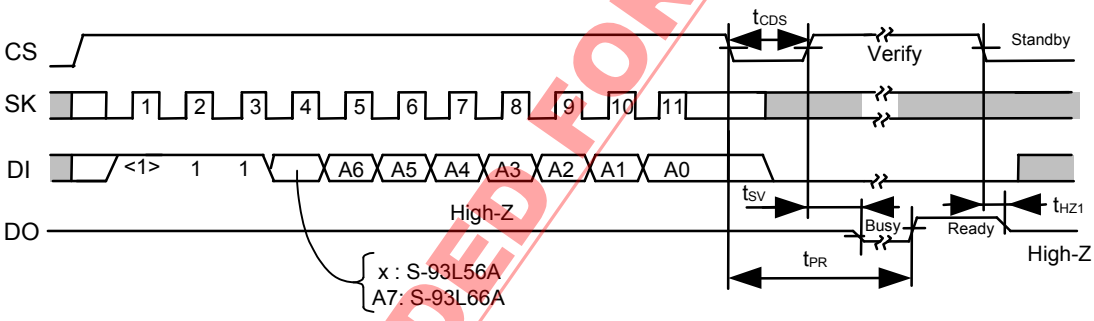


Figure 13 Data Erase Timing (S-93L56A, S-93L66A)

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

4. 4 Writing to chip (WRAL)

To write the same 16-bit data to the entire memory address space, change CS to high, and then input the WRAL instruction, an address, and 16-bit data following the start bit. Any address can be input. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

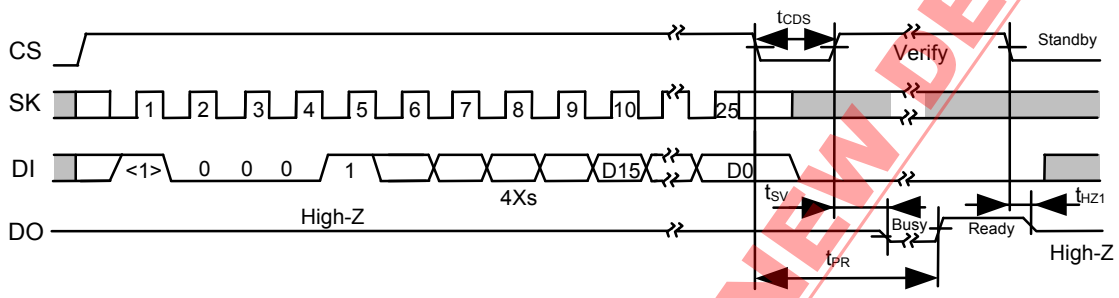


Figure 14 Chip Write Timing (S-93L46A)

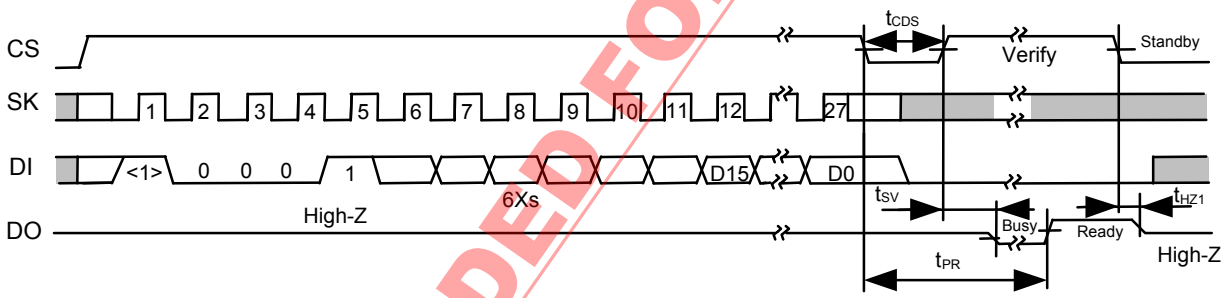


Figure 15 Chip Write Timing (S-93L56A, S-93L66A)

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

4. 5 Erasing chip (ERAL)

To erase the data of the entire memory address space, set all the data to 1, change CS to high, and then input the ERAL instruction and an address following the start bit. Any address can be input. There is no need to input data. The chips erase operation starts when CS goes low. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

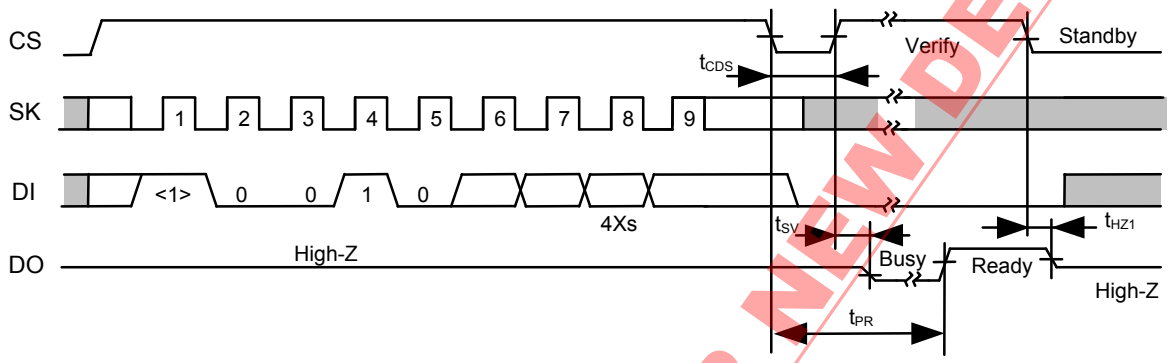


Figure 16 Chip Erase Timing (S-93L46A)

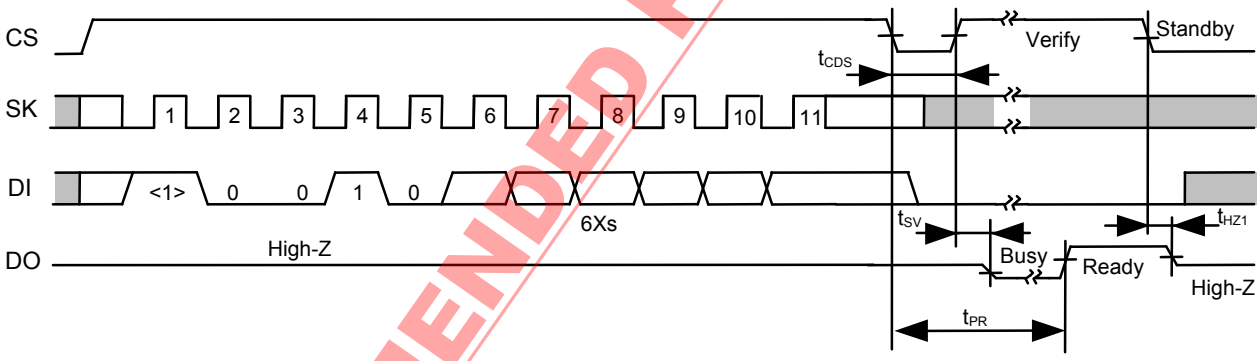


Figure 17 Chip Erase Timing (S-93L56A, S-93L66A)

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

5. Write enable (EWEN) and write disable (EWDS)

The EWEN instruction is an instruction that enables a write operation. The status in which a write operation is enabled is called the program enable mode.
The EWDS instruction is an instruction that disables a write operation. The status in which a write operation is disabled is called the program disable mode.
After CS goes high, input an instruction in the order of the start bit, EWEN or EWDS instruction, and address (optional). Each mode becomes valid by inputting a low level to CS after the last address (optional) has been input.

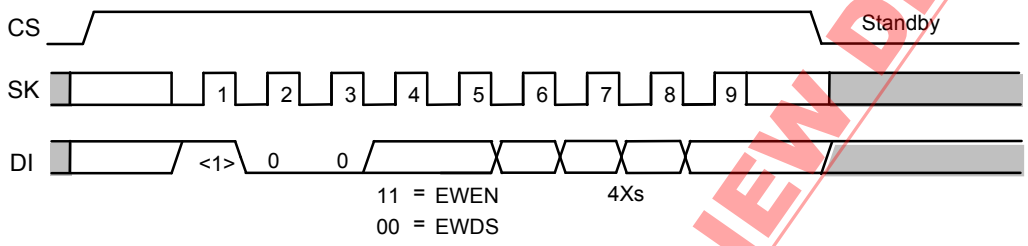


Figure 18 Write Enable / Disable Timing (S-93L46A)

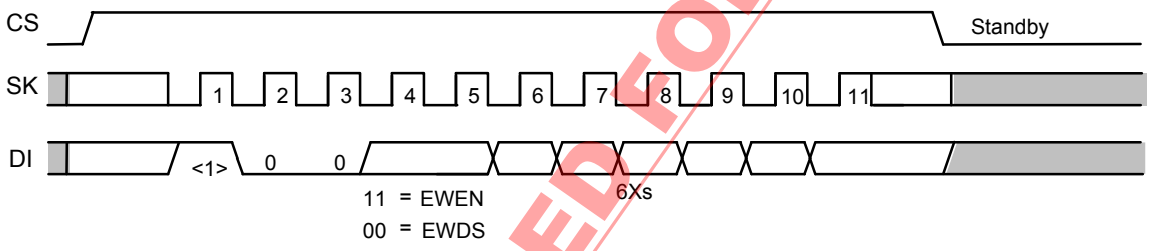


Figure 19 Write Enable / Disable Timing (S-93L56A, S-93L66A)

Remark It is recommended to execute an EWDS instruction for preventing an incorrect write operation if a write instruction is erroneously recognized when executing instructions other than write instruction, and immediately after power-on and before power-off.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Write Protect Function during the Low Power Supply Voltage

The S-93L46A/56A/66A provides a built-in detection circuit to detect a low power supply voltage. When the power supply voltage is low or at power-on, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable state (EWDS) is automatically set. The detection voltage and the release voltage are 1.4 V typ. (refer to **Figure 20**).

Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.

When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

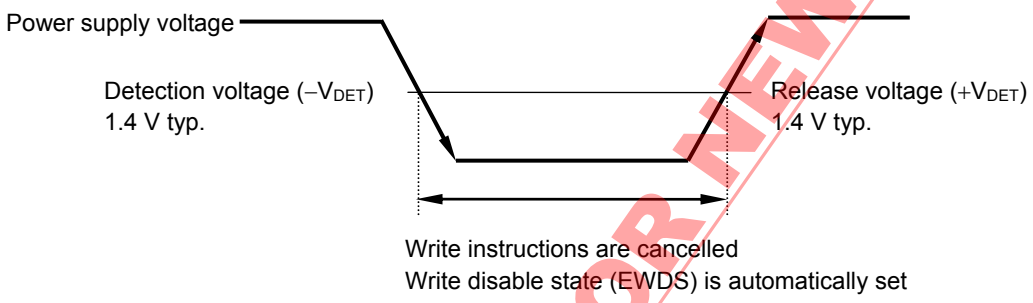


Figure 20 Operation during Low Power Supply Voltage

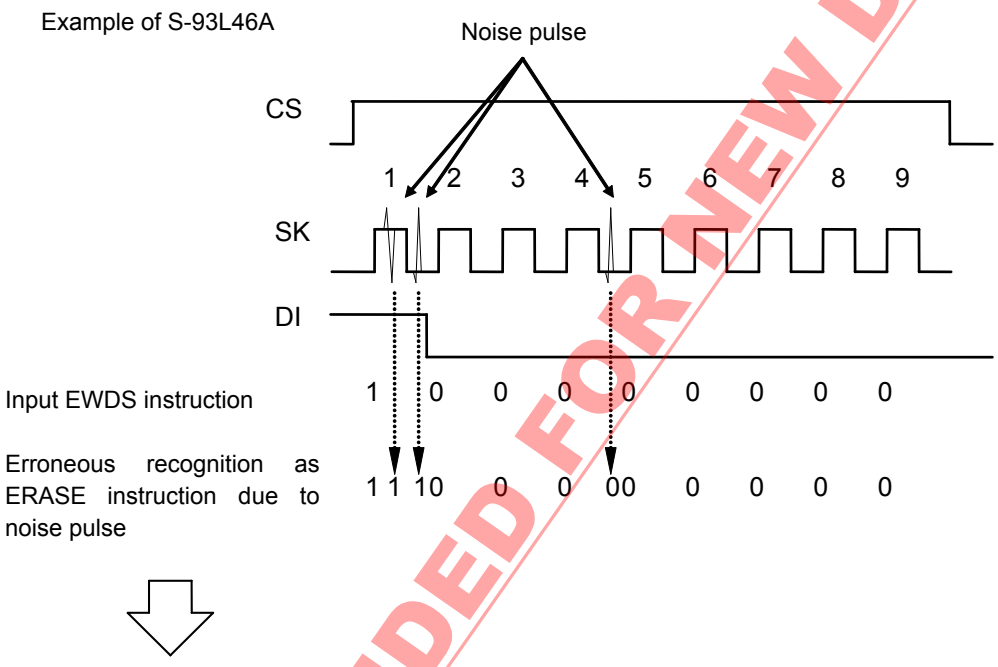
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Function to Protect Against Write due to Erroneous Instruction Recognition

The S-93L46A/56A/66A provides a built-in clock pulse monitoring circuit which is used to prevent an erroneous write operation by canceling write instructions (WRITE, ERASE, WRAL, and ERAL) recognized erroneously due to an erroneous clock count caused by the application of noise pulses or double counting of clocks.
Instructions are cancelled if a clock pulse more or less than specified number decided by each write operation (WRITE, ERASE, WRAL, or ERAL) is detected.

<Example> Erroneous recognition of program disable instruction (EWDS) as erase instruction (ERASE)



In products that do not include a clock pulse monitoring circuit, FFFFh is mistakenly written on address 00h. However the S-93L46A detects the overcount and cancels the instruction without performing a write operation.

Figure 21 Example of Clock Pulse Monitoring Circuit Operation

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ 3-Wire Interface (Direct Connection between DI and DO)

There are two types of serial interface configurations: a 4-wire interface configured using the CS, SK, DI, and DO pins, and a 3-wire interface that connects the DI input pin and DO output pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI and DO pins of the S-93L46A/56A/66A via a resistor (10 kΩ to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (refer to **Figure 22**).

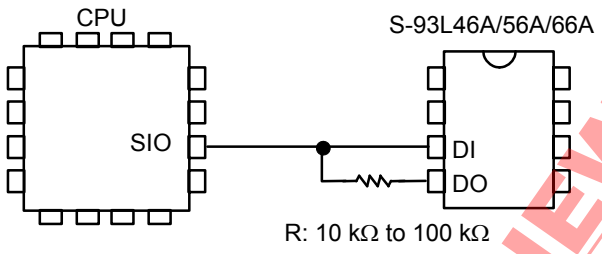


Figure 22 Connection of 3-Wire Interface

■ Input Pin and Output Pin

1. Connection of input pins

All input pins in S-93L46A/56A/66A have the CMOS structure. Do not set these pins in high impedance during operation when you design. Especially, set the CS pin to "L" at power-on, power-off, and during standby. The error write does not occur as long as the CS pin is "L". Set the CS pin to GND via a resistor (the pull-down resistor of 10 kΩ to 100 kΩ).
To prevent the error for sure, it is recommended to use equivalent pull-down resistors for input pins other than the CS pin.

2. Equivalent circuit of input pin and output pin

The following shows the equivalent circuits of input pins of the S-93L46A/56A/66A. None of the input pins incorporate pull-up and pull-down resistors, so special care must be taken when designing to prevent a floating status.
Output pins are high-level / low-level / high-impedance tri-state outputs.
The TEST pin is disconnected from the internal circuit by a switching transistor during normal operation.
As long as the absolute maximum rating is satisfied, the TEST pin and internal circuit will never be connected.

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

2. 1 Input pin

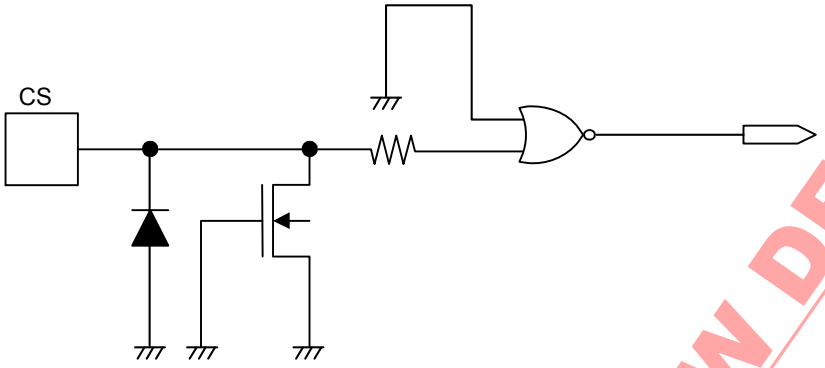


Figure 23 CS Pin

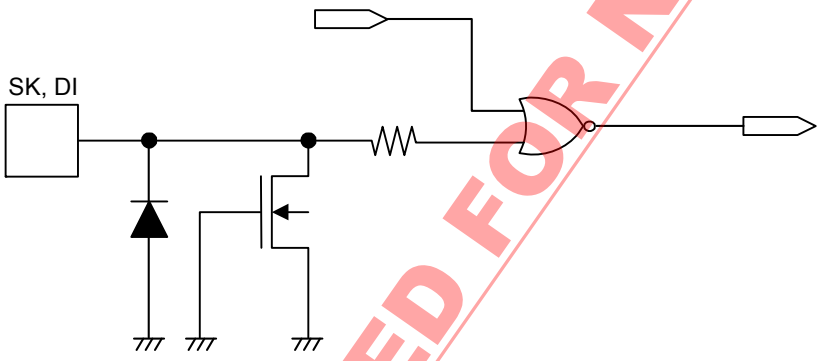


Figure 24 SK, DI Pin

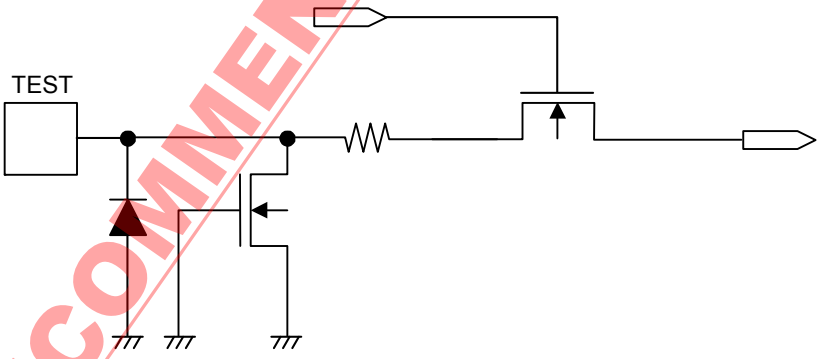


Figure 25 TEST Pin

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

2. 2 Output pin

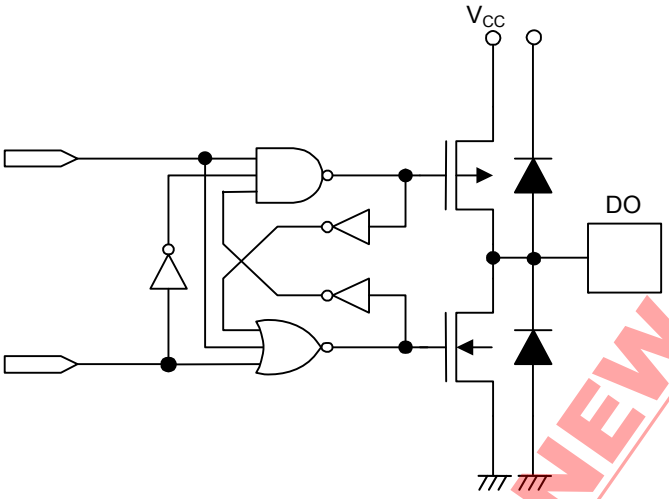


Figure 26 DO Pin

3. Input pin noise suppression time

This IC has a built-in low-pass filter at the SK pin, the DI pin and the CS pin to suppress noise. If the supply voltage is 5.0 V, noise with a pulse width of 20 ns or less at room temperature can be suppressed by the low-pass filter.
Note that noise with a pulse width of more than 20 ns is recognized as a pulse since the noise can not be suppressed if the voltage exceeds V_{IH} / V_{IL}.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

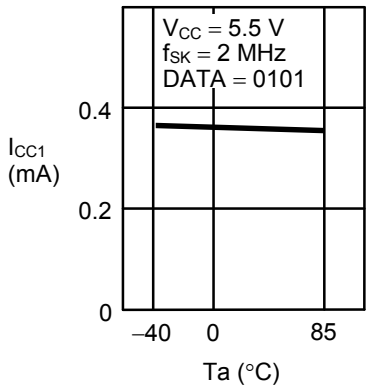
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

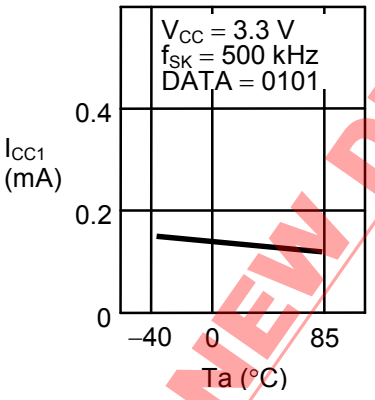
■ Characteristics (Typical Data)

1. DC Characteristics

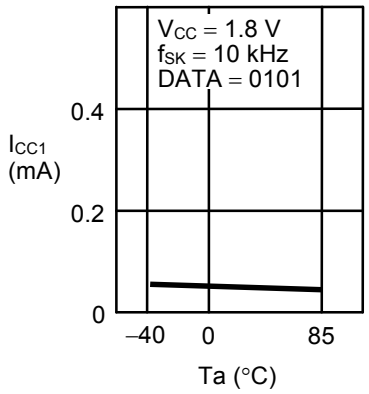
1. 1 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



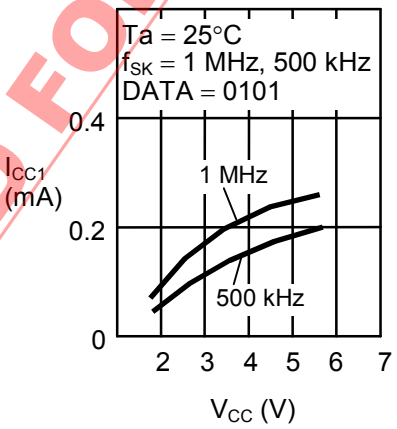
1. 2 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



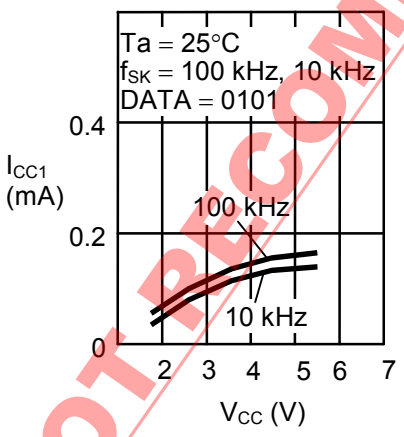
1. 3 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



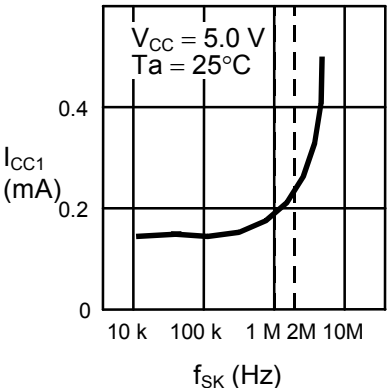
1. 4 Current consumption (READ) I_{CC1} vs. power supply voltage V_{CC}



1. 5 Current consumption (READ) I_{CC1} vs. power supply voltage V_{CC}



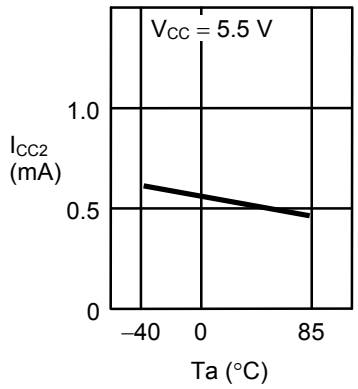
1. 6 Current consumption (READ) I_{CC1} vs. Clock frequency f_{SK}



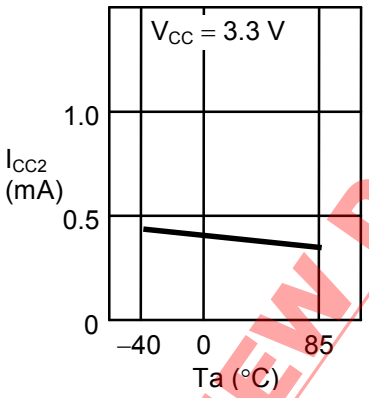
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

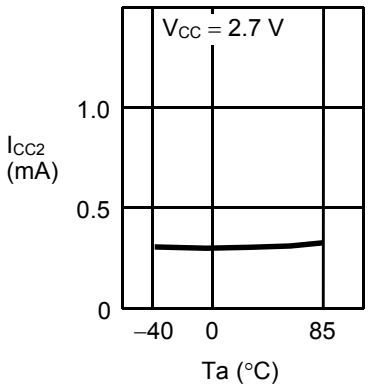
1. 7 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



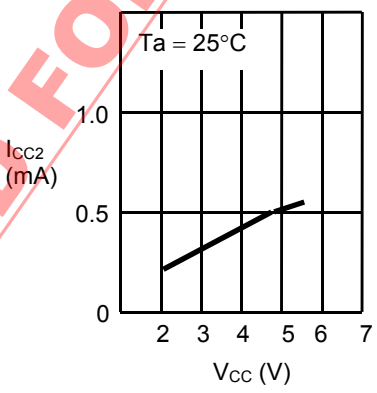
1. 8 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



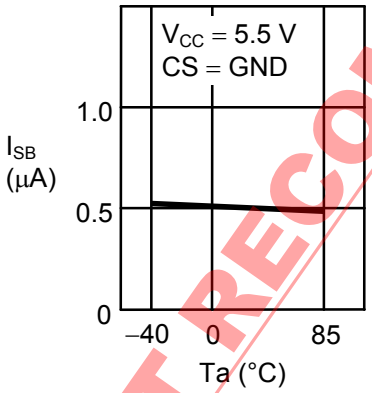
1. 9 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



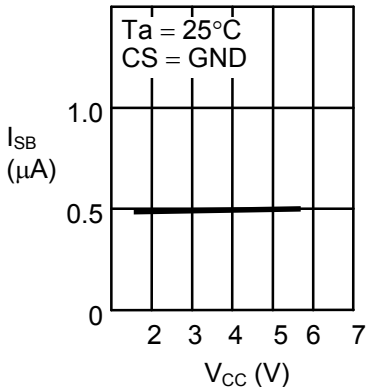
1. 10 Current consumption (WRITE) I_{CC2} vs. power supply voltage V_{CC}



1. 11 Current consumption in standby mode I_{SB} vs. ambient temperature Ta



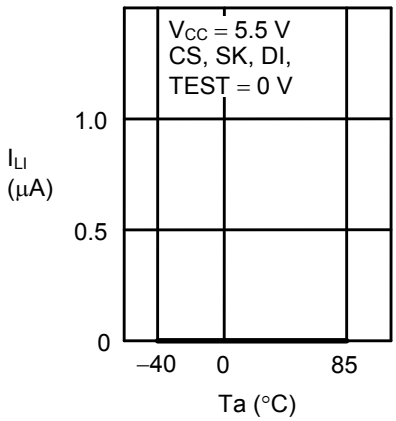
1. 12 Current consumption in standby mode I_{SB} vs. power supply voltage V_{CC}



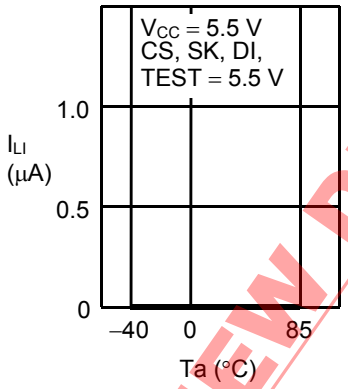
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

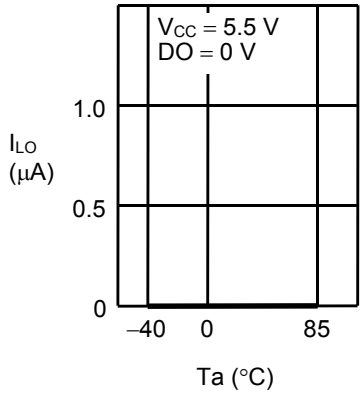
1. 13 Input leakage current I_{LI} vs. ambient temperature Ta



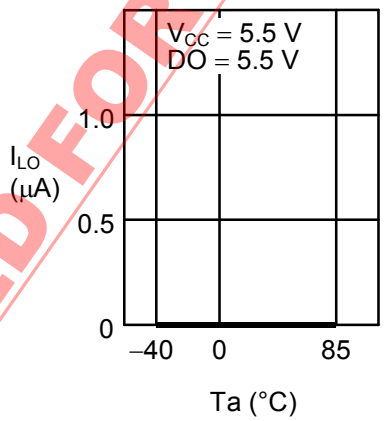
1. 14 Input leakage current I_{LI} vs. ambient temperature Ta



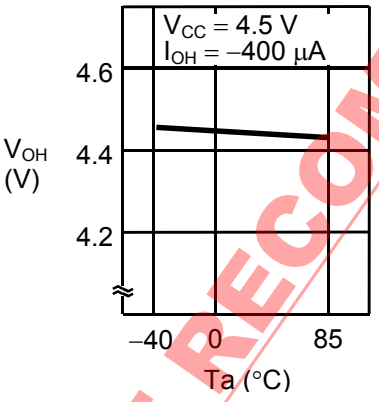
1. 15 Output leakage current I_{LO} vs. ambient temperature Ta



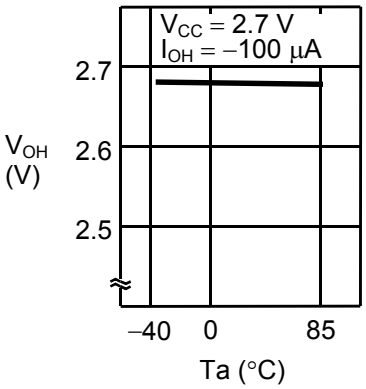
1. 16 Output leakage current I_{LO} vs. ambient temperature Ta



1. 17 High-level output voltage V_{OH} vs. ambient temperature Ta



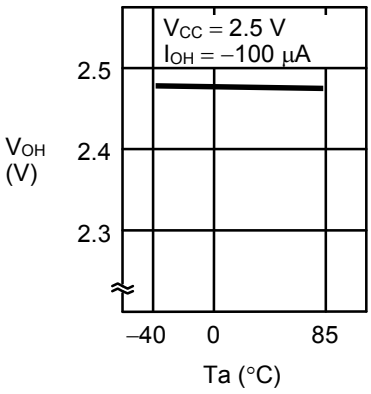
1. 18 High-level output voltage V_{OH} vs. ambient temperature Ta



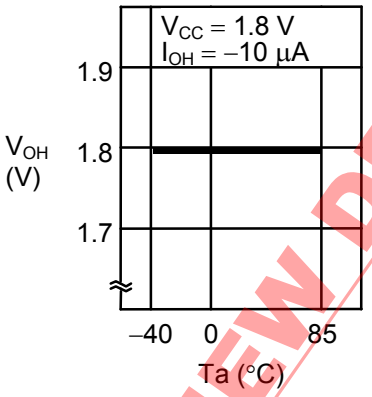
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

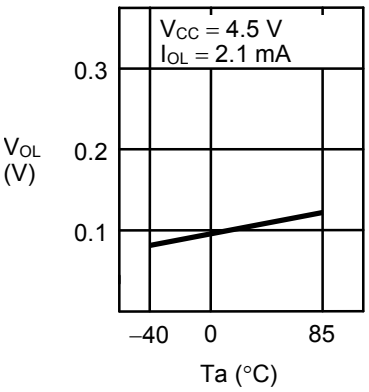
1. 19 High-level output voltage V_{OH} vs. ambient temperature Ta



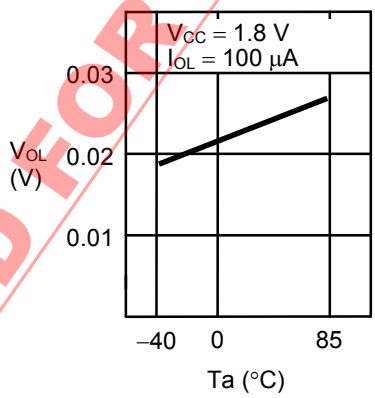
1. 20 High-level output voltage V_{OH} vs. ambient temperature Ta



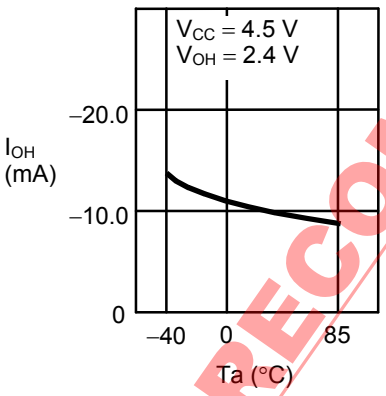
1. 21 Low-level output voltage V_{OL} vs. ambient temperature Ta



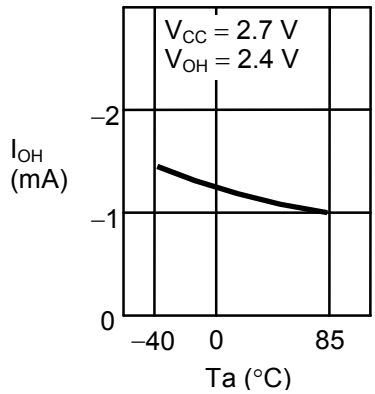
1. 22 Low-level output voltage V_{OL} vs. ambient temperature Ta



1. 23 High-level output current I_{OH} vs. ambient temperature Ta



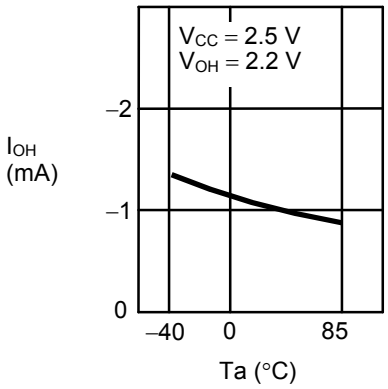
1. 24 High-level output current I_{OH} vs. ambient temperature Ta



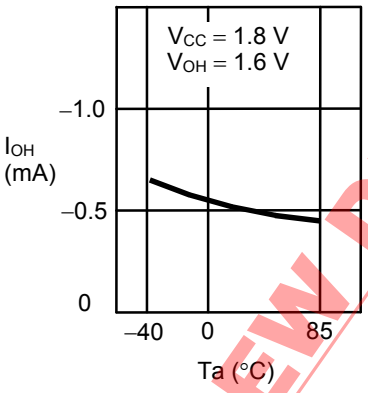
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

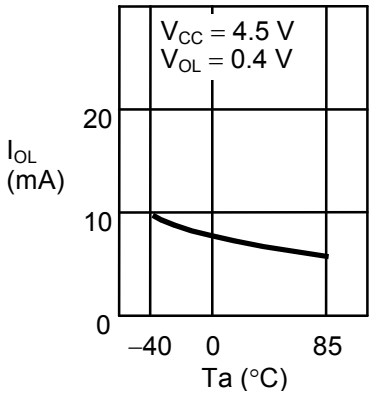
1. 25 High-level output current I_{OH} vs. ambient temperature Ta



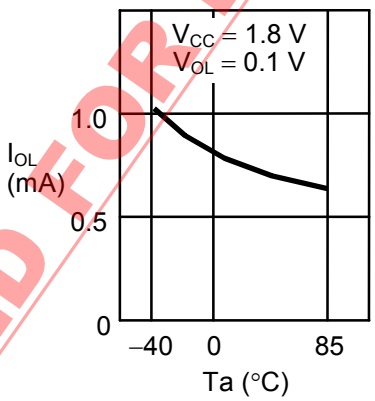
1. 26 High-level output current I_{OH} vs. ambient temperature Ta



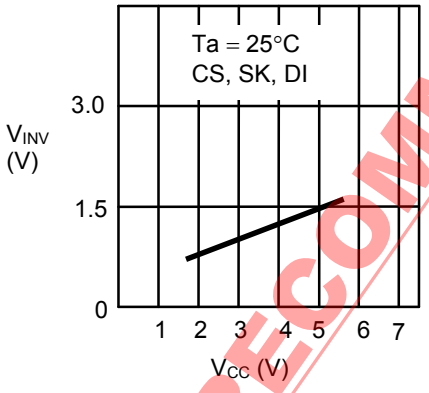
1. 27 Low-level output current I_{OL} vs. ambient temperature Ta



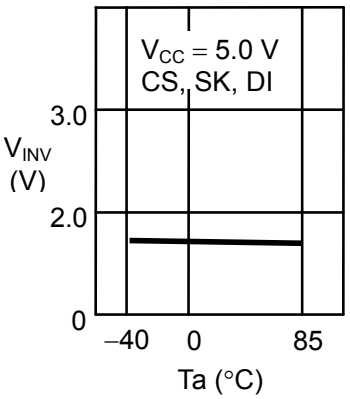
1. 28 Low-level output current I_{OL} vs. ambient temperature Ta



1. 29 Input inverted voltage V_{INV} vs. power supply voltage V_{CC}



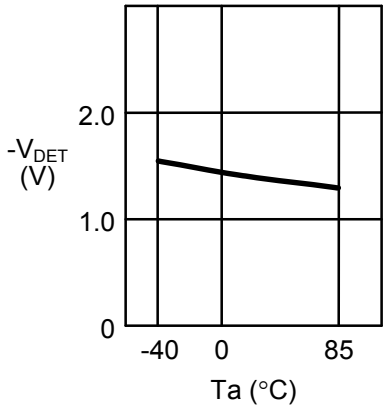
1. 30 Input inverted voltage V_{INV} vs. ambient temperature Ta



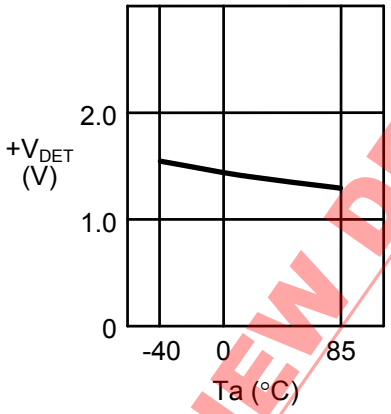
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

1. 31 Low power supply detection voltage $-V_{DET}$ vs. ambient temperature Ta

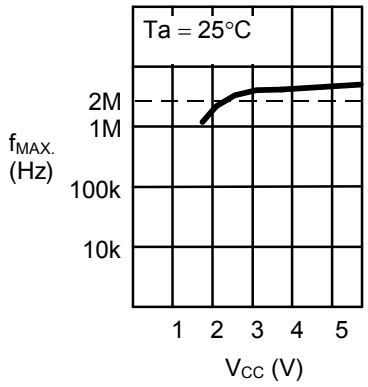


1. 32 Low power supply release voltage $+V_{DET}$ vs. ambient temperature Ta

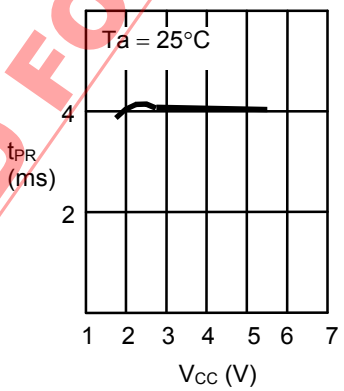


2. AC Characteristics

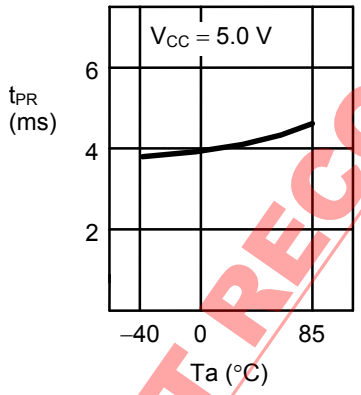
2. 1 Maximum operating frequency $f_{MAX.}$ vs. power supply voltage V_{CC}



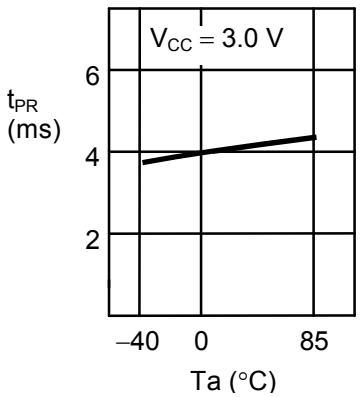
2. 2 Write time t_{PR} vs. power supply voltage V_{CC}



2. 3 Write time t_{PR} vs. ambient temperature Ta



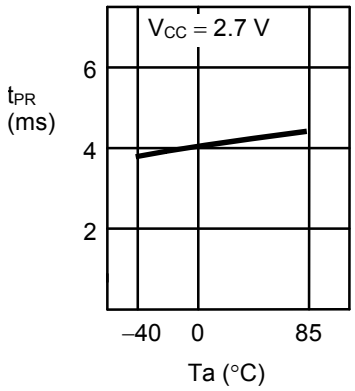
2. 4 Write time t_{PR} vs. ambient temperature Ta



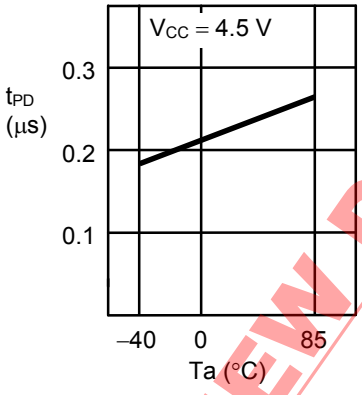
NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

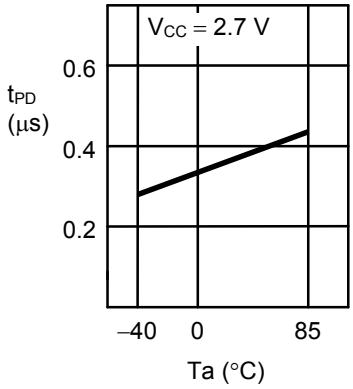
2. 5 Write time t_{PR} vs. ambient temperature Ta



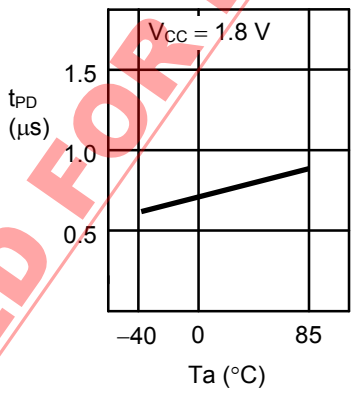
2. 6 Data output delay time t_{PD} vs. ambient temperature Ta



2. 7 Data output delay time t_{PD} vs. ambient temperature Ta



2. 8 Data output delay time t_{PD} vs. ambient temperature Ta



NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

■ Product Name Structure

1. Product name

1. 1 8-Pin SOP (JEDEC), 8-Pin TSSOP

S-93LxxA x 0I - xxxx x

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - G: Lead-free (for details, please contact our sales office)
- Package name (abbreviation) and IC packing specifications
  - J8T1: 8-Pin SOP (JEDEC), Tape
  - T8T1: 8-Pin TSSOP, Tape
- Fixed
- Pin configurations
  - D: 8-Pin SOP (JEDEC)
    8-Pin TSSOP
  - R: 8-Pin SOP (JEDEC) (Rotated)
- Product name
  - S-93L46A: 1 K-bit
  - S-93L56A: 2 K-bit
  - S-93L66A: 4 K-bit

1. 2 TMSOP-8, SNT-8A

S-93LxxA D0I - xxxx U

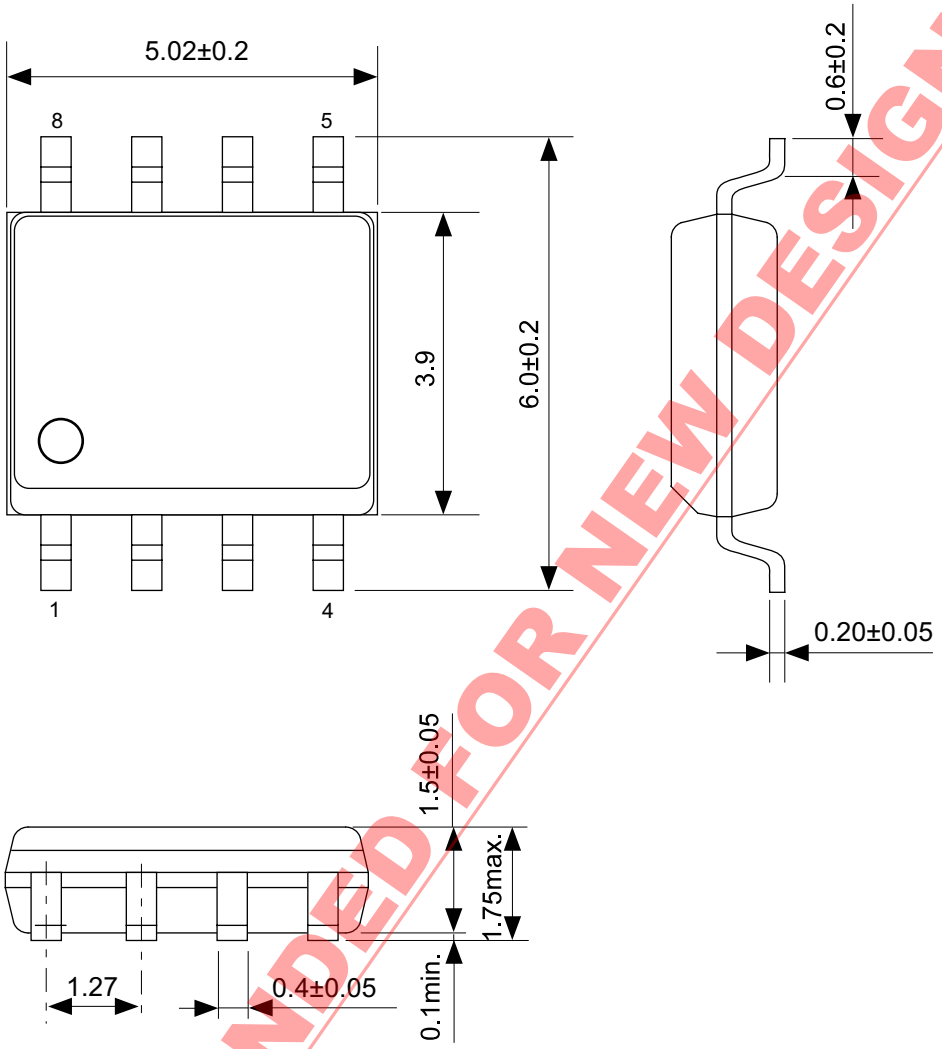
- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package name (abbreviation) and IC packing specifications
  - K8T3: TMSOP-8, Tape
  - I8T1: SNT-8A, Tape
- Fixed
- Product name
  - S-93L46A: 1 K-bit
  - S-93L56A: 2 K-bit
  - S-93L66A: 4 K-bit

2. Packages

Package Name		Drawing Code			
		Package	Tape	Reel	Land
8-Pin SOP (JEDEC)	Environmental code = G	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD	—
	Environmental code = U	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-S1	
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD	—
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1	
TMSOP-8		FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	—
SNT-8A		PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

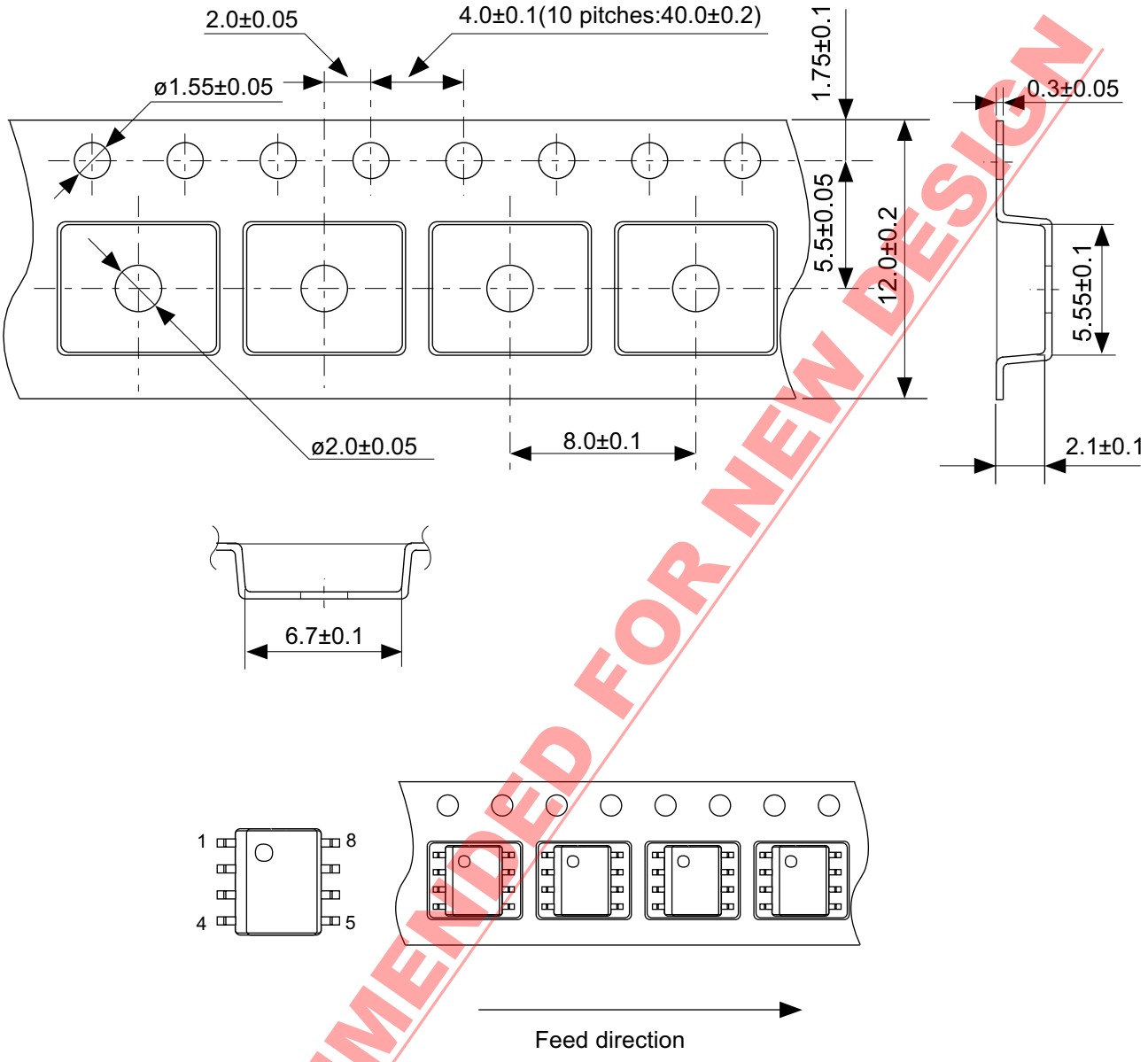


NOT RECOMMENDED FOR NEW DESIGN

No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.2
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.

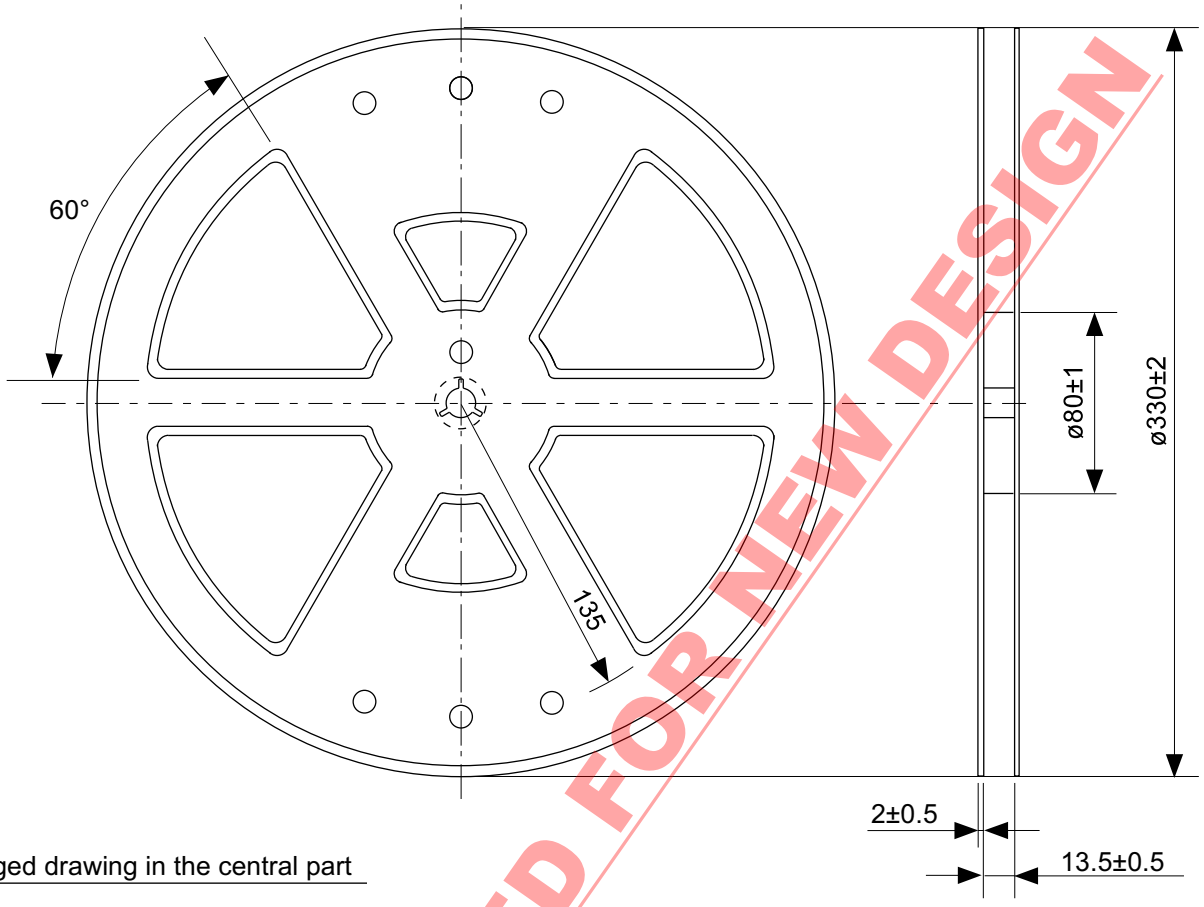


NOT RECOMMENDED FOR NEW DESIGN

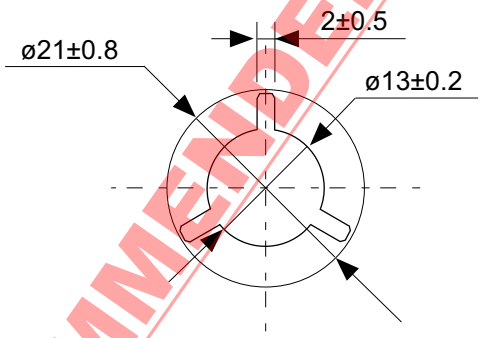
No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Downloaded from Arrow.com.



Enlarged drawing in the central part

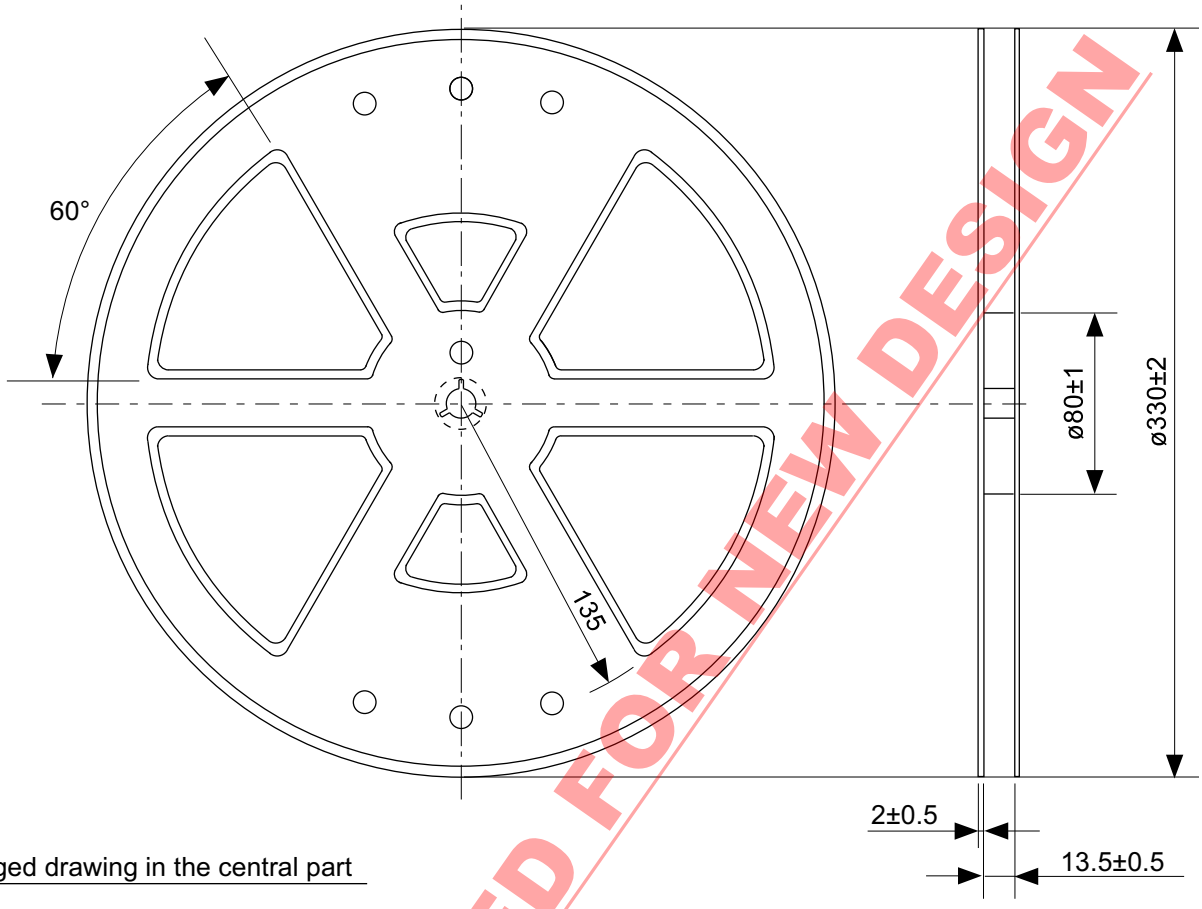


NOT RECOMMENDED FOR NEW DESIGN

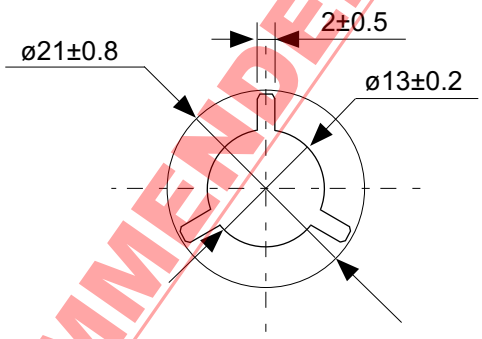
No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
ANGLE		QTY.	2,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



Enlarged drawing in the central part

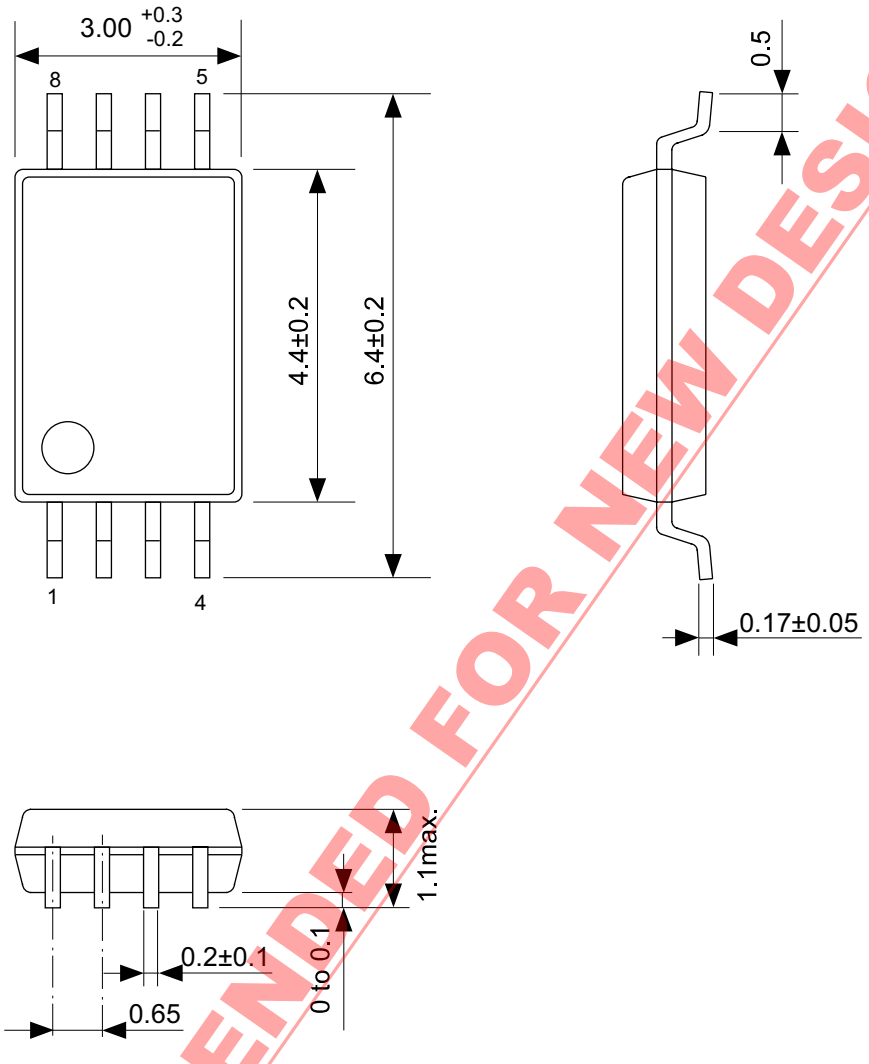


NOT RECOMMENDED FOR NEW DESIGN

No. FJ008-D-R-S1-1.0

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



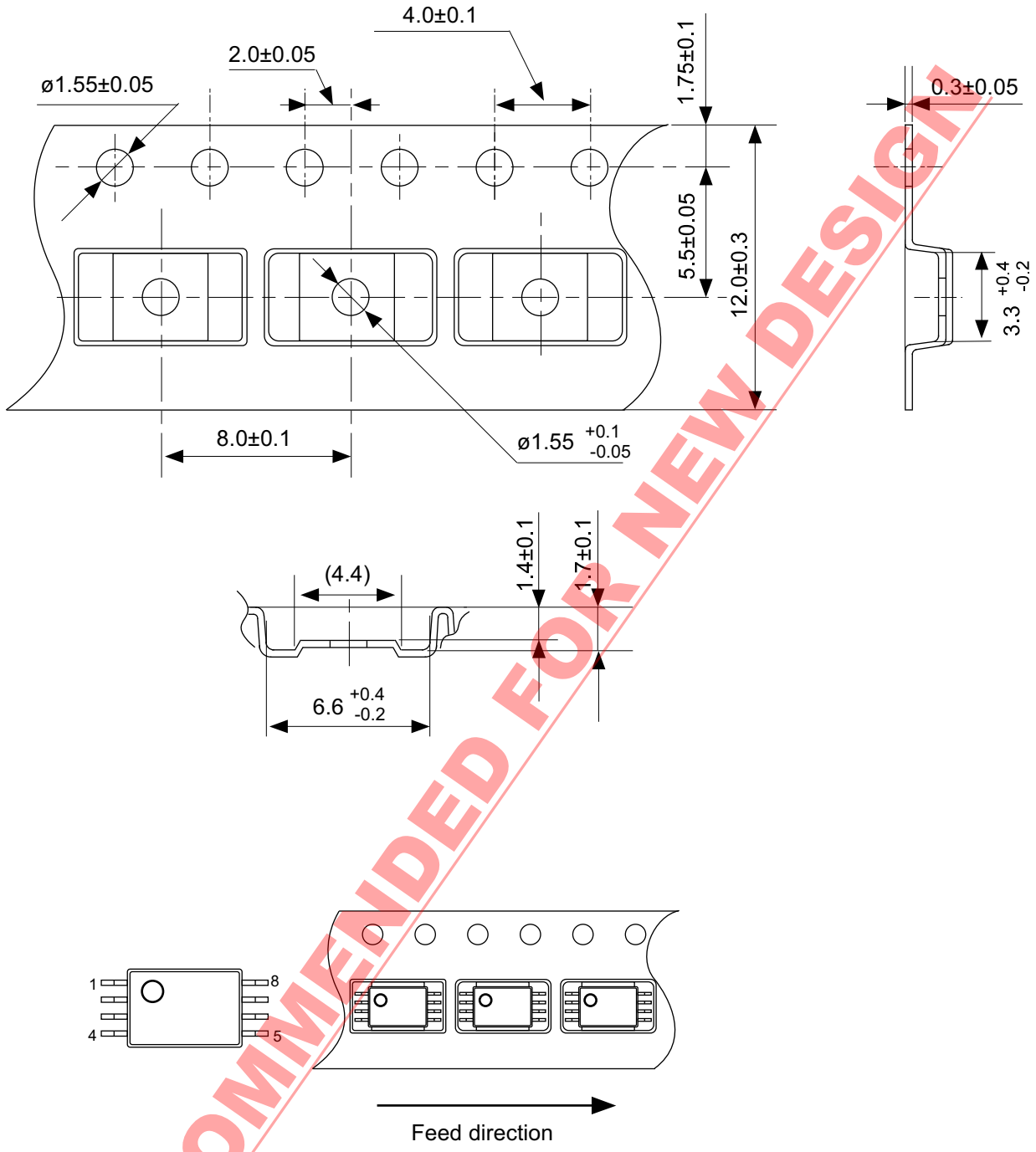
NOT RECOMMENDED FOR NEW DESIGN

No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.

Downloaded from Arrow.com.



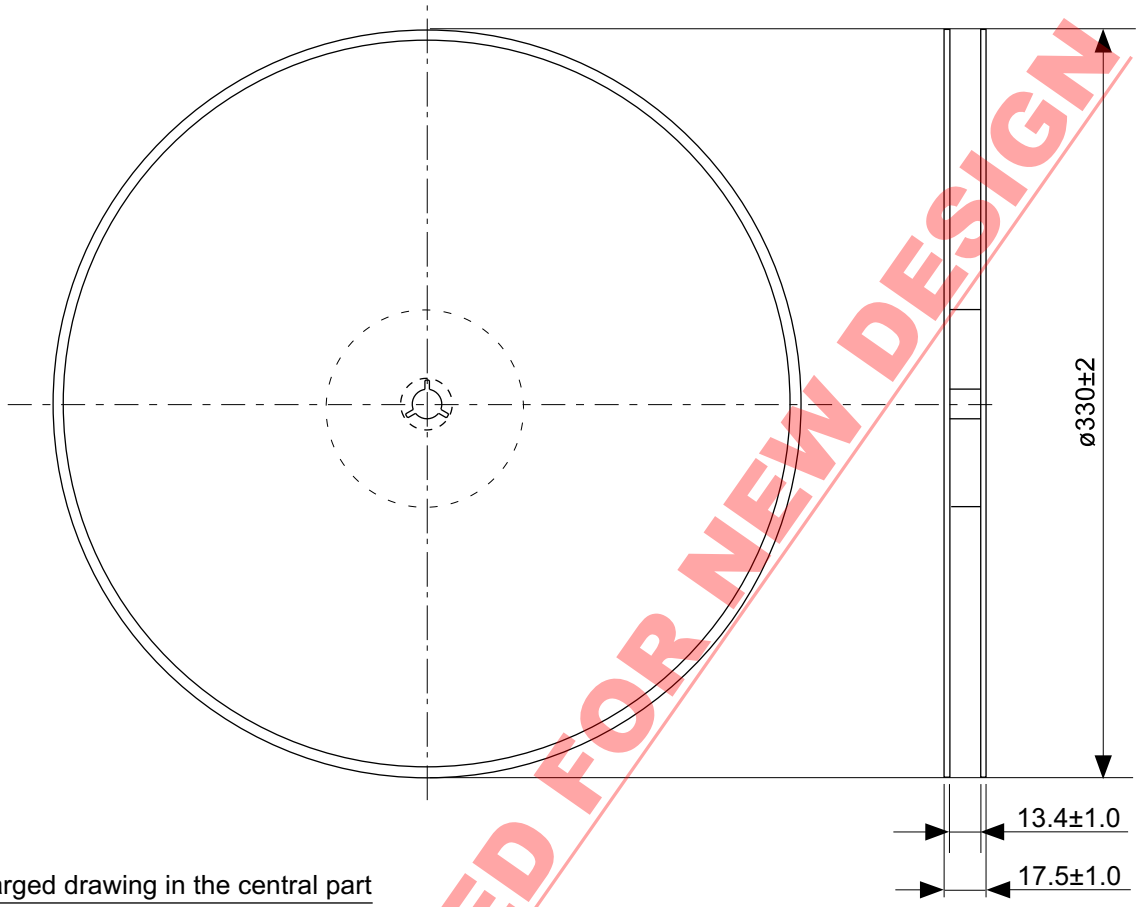
NOT RECOMMENDED FOR NEW DESIGN

No. FT008-E-C-SD-1.0

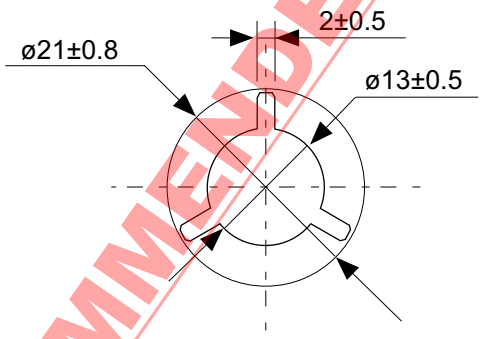
TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

Downloaded from Arrow.com.



Enlarged drawing in the central part

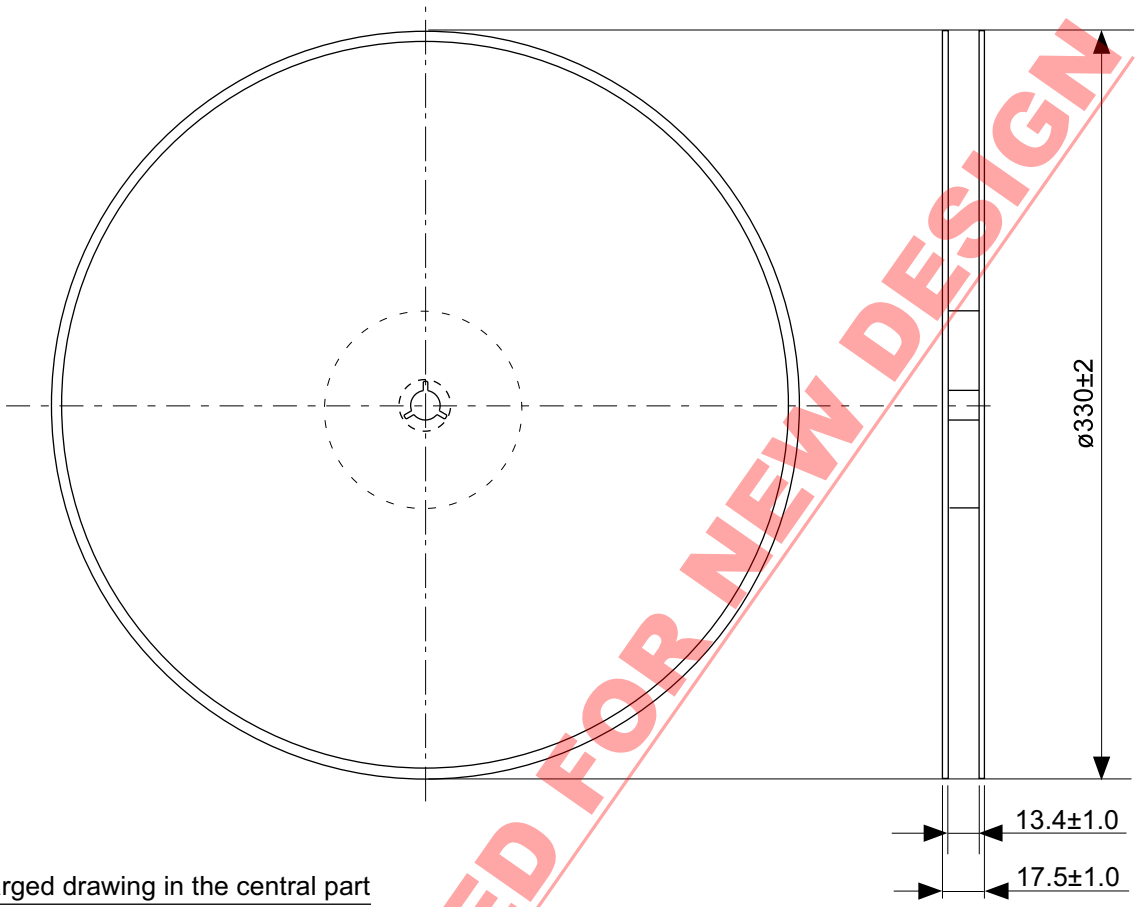


No. FT008-E-R-SD-1.0

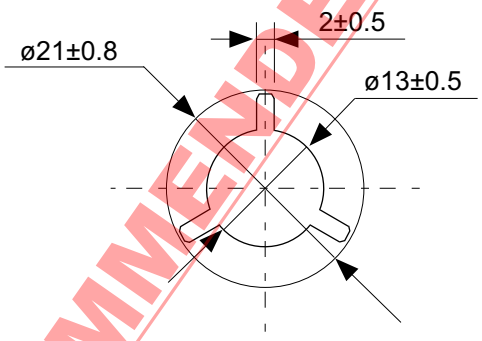
NOT RECOMMENDED FOR NEW DESIGN

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		

Downloaded from Arrow.com.



Enlarged drawing in the central part

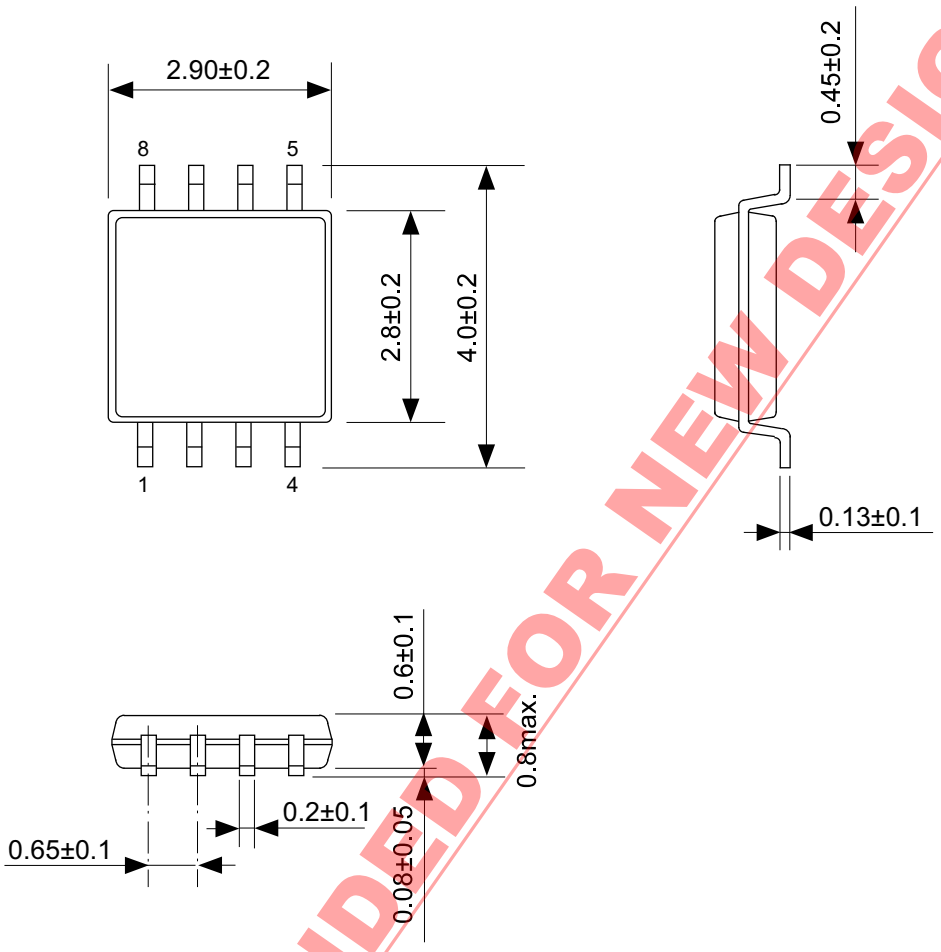


No. FT008-E-R-S1-1.0

NOT RECOMMENDED FOR NEW DESIGN

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.

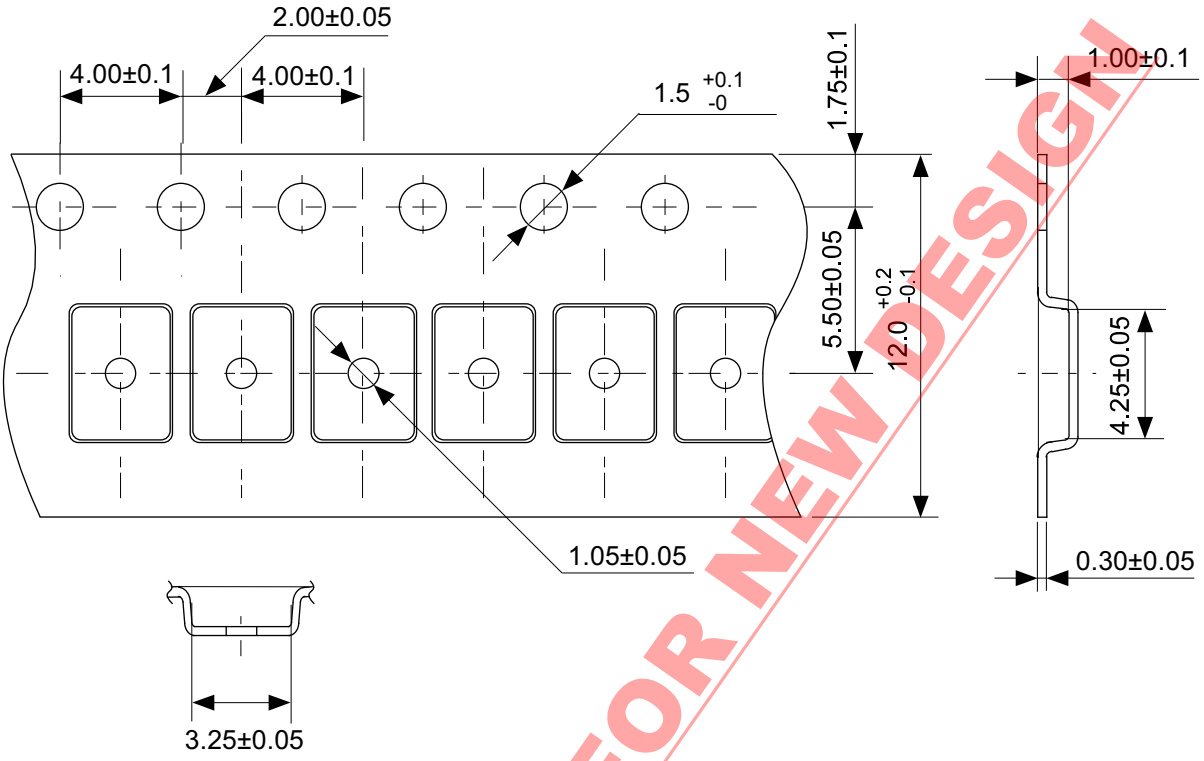


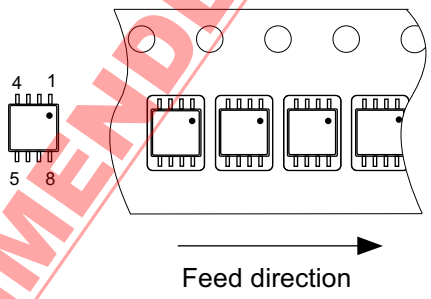
NOT RECOMMENDED FOR NEW DESIGN

No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
	ABLIC Inc.

Downloaded from Arrow.com.





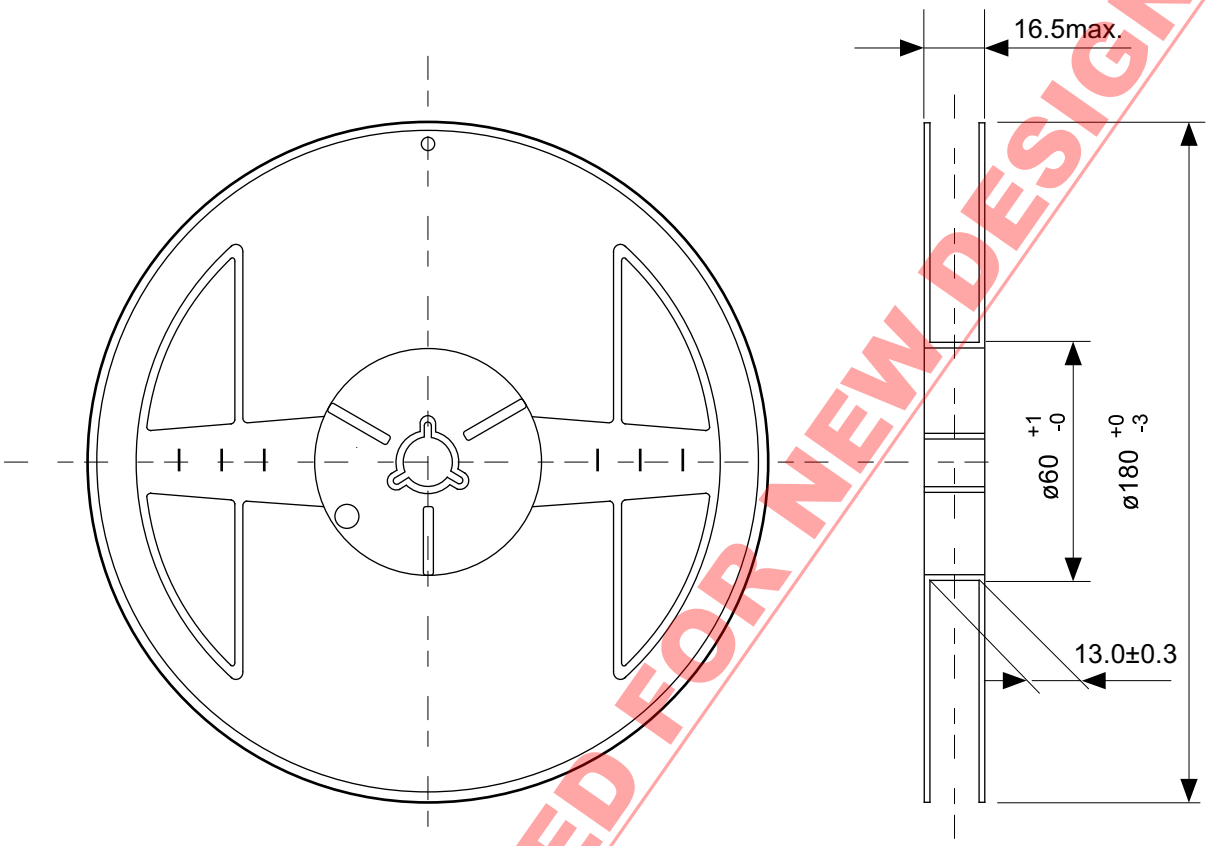
NOT RECOMMENDED FOR NEW DESIGN

No. FM008-A-C-SD-2.0

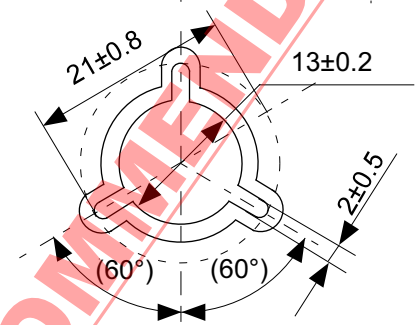
TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

Downloaded from Arrow.com.



Enlarged drawing in the central part

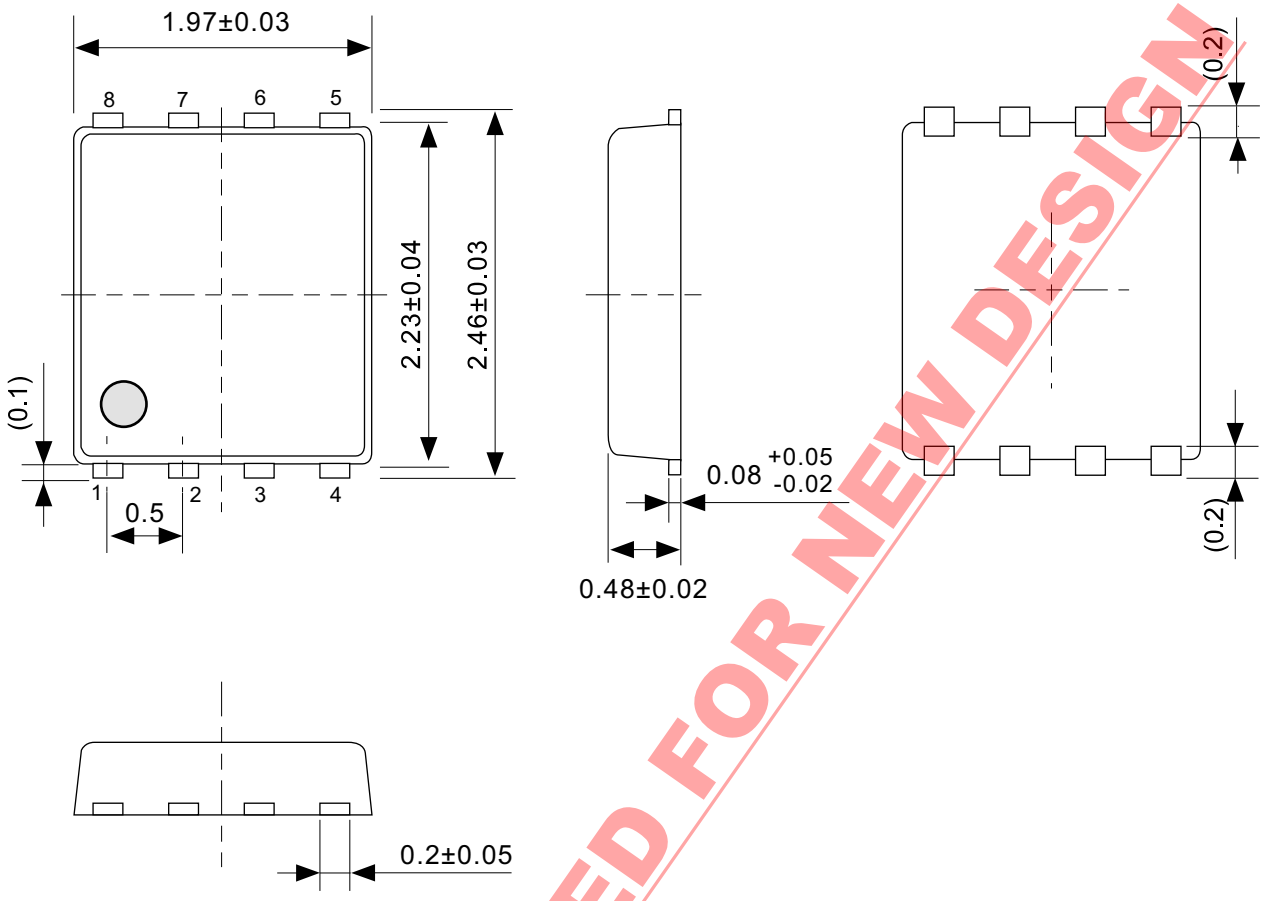


No. FM008-A-R-SD-1.0

NOT RECOMMENDED FOR NEW DESIGN

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



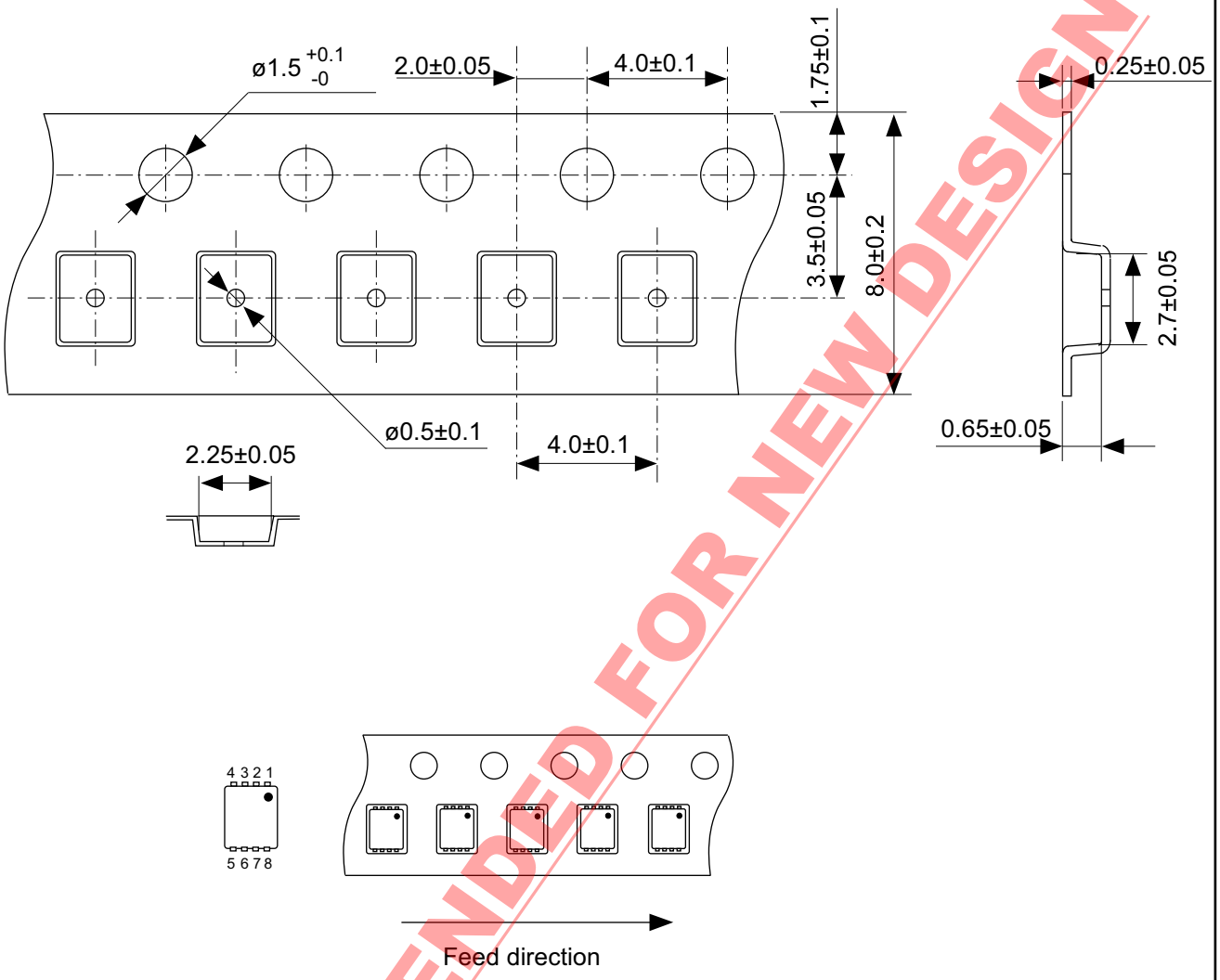
NOT RECOMMENDED FOR NEW DESIGN

No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

Downloaded from Arrow.com.



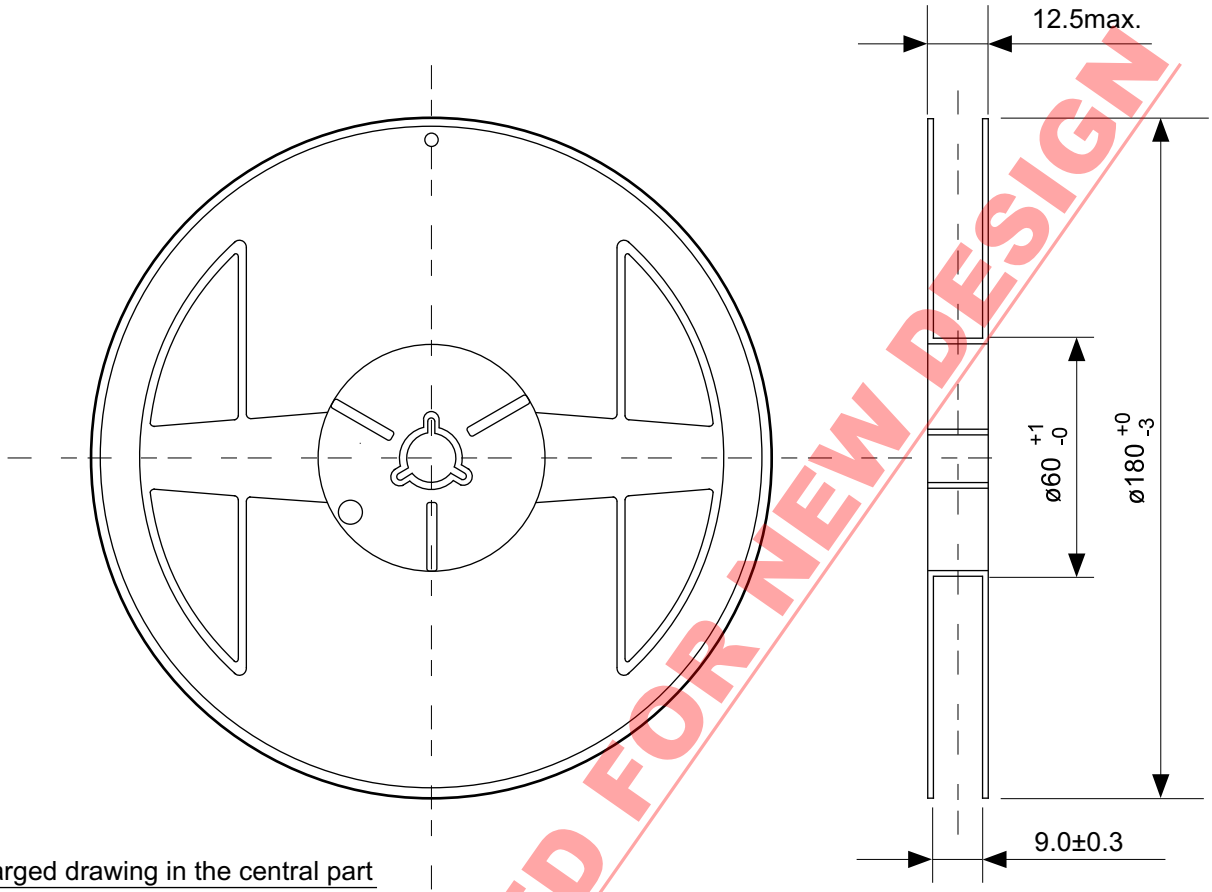
NOT RECOMMENDED FOR NEW DESIGN

No. PH008-A-C-SD-2.0

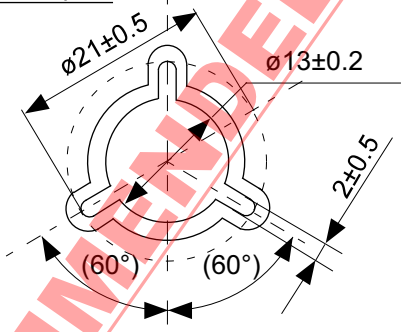
TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

Downloaded from Arrow.com.



Enlarged drawing in the central part

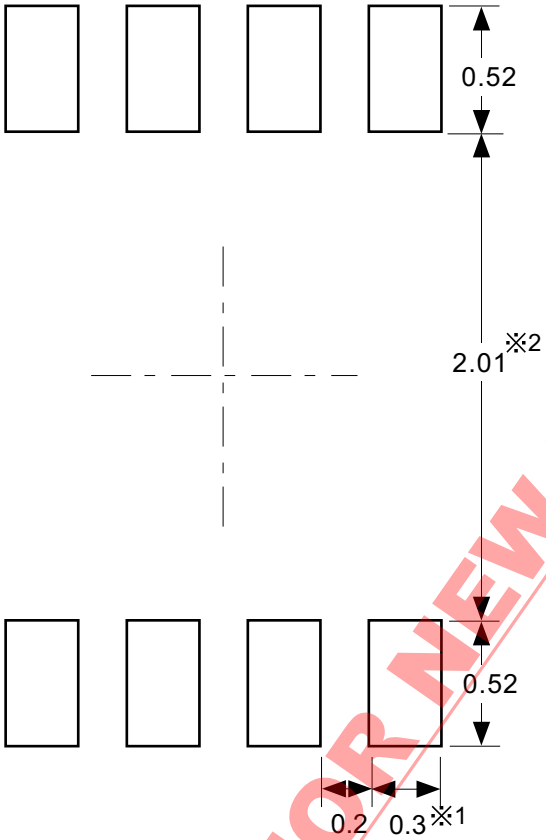


NOT RECOMMENDED FOR NEW DESIGN

No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

Downloaded from Arrow.com.



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution
1. **Do not do silkscreen printing and solder printing under the mold resin of the package.**
2. **The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
3. **Match the mask aperture size and aperture position with the land pattern.**
4. **Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意
1. **请勿在树脂型封装的下面印刷丝网、焊锡。**
2. **在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
3. **钢网的开口尺寸和开口位置请与焊盘模式对齐。**
4. **详细内容请参阅 "SNT 封装的应用指南"。**

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not responsible for damages caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not responsible for damages caused by the incorrect information described herein.
4. Be careful to use the products within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not responsible for damages caused by failures and / or accidents, etc. that occur due to the use of the products outside their specified ranges.
5. When using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not apply the products to the above listed devices and equipments without prior written permission by ABLIC Inc.
   Especially, the products cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
   Prior consultation with our sales office is required when considering the above uses.
   ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
   The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc.
    The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party without the express permission of ABLIC Inc. is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

2.0-2018.01

NOT RECOMMENDED FOR NEW DESIGN

Downloaded from Arrow.com.