Image Recognition Processor

TMPV75 Series

Datasheet

Overview

Revision 2.0.1

Toshiba Electronic Devices & Storage Corporation

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Prologue

The TMPV75 Series are image recognition processors that process input video images in real-time. They detect target objects such as persons, faces, hands, vehicles, traffic lanes, and so on. The series can be used for camera vision systems utilizing various image-recognition technologies such as Advanced Driver Assistance System (ADAS), Intelligent Transport System (ITS), surveillance camera, gaming device, and energy control system for air conditioning and lighting, etc.

This document describes the specification of the Overview of TMPV75 Series.

Who Should Read this Document

This document is intended for the following users.

- Driver software developer
- System designer

Conventions and Notations in this Document

- Numbers are shown in the following formats.
  Hexadecimal number: 0xABC
  Decimal number: 123 or 0d123 (Use only when it needs to be explicitly shown that it is a decimal number.)
  Binary number: 0b111
- "_N" at the end of a signal name indicates that it is a low-active signal.
- The word "assert" means that a signal goes to its active level ("High" level for a high-active signal or "Low" level for a low-active signal). The word "deassert" means that a signal goes to its inactive level.
- A signal which consists of two or more bits of signals can be described as "SIGNAL_NAME[3:0]".
  Example: S[3:0] describes four signal names S3, S2, S1, and S0.
- A word surrounded by "***[]***" shows a register.
  Example: ***[ABCD]***
- "n" substitutes suffix numbers of two or more same kind of registers or bit-fields.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- A bit range of a register is shown as "[m:n]".
  Example: [3:0] expresses the range of bits from 3 to 0.
- A value of a register is expressed by either a hexadecimal number or a binary number.
  Example: ***[ABCD]***.EFG = 0x01 (hexadecimal), ***[XYZn]***.VW = 0b01 (binary)
- The following notations are used for data sizes.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- A property of each bit-field in a register is expressed as follows.
  R: Read only
  W: Write only
  W1C: Write 1 and Clear (The corresponding bit is cleared (=0) when "1" is written to the bit.)
  W1S: Write 1 and Set (The corresponding bit is set (=1) when "1" is written to the bit.)
  R/W: Read and Write
  R/W0C: Read/Write 0 and Clear
  R/W1C: Read/Write 1 and Clear
  R/W1S: Read/Write 1 and Set
  RS/WC: Read Set/Write Clear (Set after a read, and cleared after a write)
- Unless otherwise specified, a register access must be a word access.
- Don't write into a register defined as "reserved", and don't use the value read from the register.
- The value read from a bit-field whose default value is defined as "—" is unknown.
- When writing a register which contains both writable bit-fields and read-only bit-fields, the default values must be written into the read-only bit-fields. When a default value is defined as "—", follow the description of the register.
- Each reserved bit-field of a write-only register should be written with its default value. When a default value is defined as "—", follow the description of the register.

Abbreviation

ADAS	Advanced Driver Assistance System
BCW	Backward Collision Warning
BOP	Back Over Prevention
CAN	Controller Area Network
CoHOG	Co-occurrence Histograms of Oriented Gradients
CPU	Central Processing Unit
CTS	Clear To Send
CVBS	Composite Video Blanking and Sync
DDR2	Double Data Rate 2
DMA	Direct Memory Access
DMAC	DMA Controller
DRAM	Dynamic Random Access Memory
D-Cache	Data Cache
D-RAM	Data RAM
FCW	Forward Collision Warning
FIFO	First In First Out
HOG	Histograms of Oriented Gradients
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
ICE	In-Circuit Emulator
ITS	Intelligent Transport Systems
IVC2	The second generation of Image Recognition VLIW Coprocessor
I-Cache	Instruction Cache
I-RAM	Instruction RAM
JTAG	Joint Test Action Group
LCA	Lane Change Assistance
LCD	Liquid Crystal Display
LDW	Lane Departure Warning
L2-Cache	Level 2 Cache
MeP	Media embedded Processor
MCU	Micro Controller Unit
MMU	Memory Management Unit
MPE	Media Processing Engine
NMI	Non Maskable Interrupt
ODT	On Die Termination
P-BGA	Plastic Ball Grid Array
P-LFBGA	Plastic Low-profile Fine pitch Ball Grid Array
PCM	Pulse Code Modulation
PHY	Physical Layer
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RISC	Reduced Instruction Set Computer
RTS	Request To Send
SIMD	Single Instruction stream, Multiple Data stream
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SXGA	Super eXtended Graphics Array
TLB	Translation Look aside Buffer
TSR	Traffic Sign Recognition
UART	Universal Asynchronous Receiver Transmitter
VENEZIA	Vision ENabling Engine / Zen-Inspired Architecture
VLIW	Very Long Instruction Word
WVGA	Wide Video Graphics Array

1. Overview

The “TMPV75 Series Datasheet” presents TMPV75 Series product specifications and package specifications, and other information required for applied system design. The expression “the product” in this document refers to the TMPV75 Series.

1.1. Overview of TMPV75 Series

The TMPV75 Series is an image recognition processor that performs real-time image processing of input video image data from camera(s), recognizes target objects such as humans, faces, hands, vehicles, traffic lanes, traffic signs, text and so on, or movement of the above objects. The TMPV75 Series is suitable for camera-based vision systems such as advanced driver assistance system (ADAS), intelligent transport systems (ITS), surveillance camera, air-conditioner / light control system and so on.

The TMPV75 Series is Heterogeneous multi-core architecture consists of control CPU(s), multi-core sub-system “VENEZIA (Vision Enabling Engine / Zen-Inspired Architecture)” which has multiple sets of “MPE (Media Processing Engine)” suitable for image processing and multiple image processing accelerators. The TMPV75 Series deliver high image processing performance under low power consumption.

The control CPU consists of a Toshiba original 32-bit RISC core “MeP (Media embedded Processor)” and/or an Arm® 32-bit RISC core “Arm® Cortex®-A9 MPCore(*1)”.

VENEZIA has four sets of MPE that implement a “MeP” core and an “IVC2 (the 2nd generation of Image recognition VLIW Coprocessor)”, enabling parallel execution of up to four image recognition applications.(*2) The IVC2 enables SIMD (Single Instruction stream, Multiple Data stream) technology for simultaneous operations on multiple sets of data with a single instruction required for image processing and VLIW (Very Long Instruction Word) technology to issue multiple instructions.

There are five types of image processing accelerators available for the TMPV75 Series.

(1) Affine Transformation Accelerator
Undistortion of input image data from camera, geometric transformation such as rotation, expansion/dilation, translation, shear and so on of image data by using parameters or table.

(2) Filter Accelerator
Noise reduction, edge/corner detection and other filtering processes, color space conversion and so on.

(3) Histogram Accelerator
Histogram calculation, brightness conversion using lookup table

(4) HOG (Histograms of Oriented Gradients) Accelerator(*3)
Calculation of HOG or Toshiba CoHOG (Co-occurrence Histograms of Oriented Gradients) features and likelihood score output by using LSVM (Linear Support Vector Machine) with templates for human recognition

(5) Matching accelerator
Performs parallax calculation of the left/right image data of a stereo camera, and tracks and detects movement of a template in 2 time images for optical flow

The TMPV75 Series has huge on-chip memory for image data processing. There are four sets of 512KB working RAM, which enables to access simultaneously image data from up to four bus masters (processors, accelerators, video input/output interfaces, etc.).

In addition, video input interfaces, a video output interface, external memory interfaces such as SRAM/NOR memory controller and DDR2 SDRAM controller, a system RAM for control CPU (MeP and/or Arm Cortex-A9 MPCore), a system ROM for boot of MeP, an interrupt controller, general-purpose I/Os, a timer, serial interfaces such as UART, I^2C and SPI, PCM interfaces, CAN interfaces, an external MCU interface(*4), and PCI Express interface(*5) and so on are built in.

(*1) Arm Cortex-A9 MPCore is equipped with only TMPV7528XBG.
(*2) In TMPV7502XBG, VENEZIA has two sets of MPE, enabling parallel execution of up to two image recognition applications.
(*3) HOG Accelerator is not equipped with TMPV7504XBG.
(*4) MCU interface is not equipped with TMPV7502XBG.
(*5) PCI Express interface is equipped with TMPV7528XBG and TMPV7506XBG.

1.2. Highlights

The key points of TMPV75 Series are high image processing performance, low power consumption, and easy software development.

Heterogeneous multi-core architecture

The TMPV75 Series is Heterogeneous multi-core architecture that combines different type of engines such as control CPU(s) designed for easy software development, a multi-core sub-system designed for executing multiple image processing applications and solving various image recognition algorithm by software, and image processing accelerators designed for helping real-time image processing. This architecture delivers high image processing performance under low power consumption, along with easy software development.

- Control CPU
  The TMPV75 Series has Toshiba original 32-bit RISC CPU core “MeP-c5” and/or Arm 32-bit RISC CPU core “Arm Cortex-A9 MPCore(*6)”
- Multi-grain parallellism architecture Multi-core Sub-system
  The TMPV75 Series has Toshiba original multi-core sub-system “VENEZIA”. The VENEZIA is multi-grain parallellism architecture – application level (multi-core), instruction level (VLIW) and data level (SIMD).
  The VENEZIA includes 4 sets of Toshiba original media processing engine “MPE” that enables simultaneous execution of up to four image recognition applications.(*7) Each MPE has a Toshiba original 32-bit RISC CPU core MeP-c5 and an image recognition coprocessor IVC2. The MPE is 3way VLIW machine that can issue up to 3 instructions (one CPU instruction and up to 2 coprocessor instructions). The IVC2 provides SIMD instructions for simultaneous operations on eight sets of 8-bit data, four sets of 16-bit data, and two sets of 32-bit data. The IVC2 can execute simultaneously up to 2 SIMD instructions. Since parallel processing of two instructions is enabled, operations on a maximum of 16 sets of 8-bit data can be processed simultaneously.
- Accelerators to help real-time image processing
  The TMPV75 Series is included with a maximum of five types of image processing accelerators.(*8) Such accelerators help real-time image processing under low power consumption. Toshiba provides the TMPV75 Series Software Development Kit (SDK) including various image processing libraries and drivers to use easily these image processing accelerators.

(*6) Cortex-A9 MPCore is equipped with only TMPV7528XBG.
(*7) The VENEZIA includes 2 sets of “MPE” that enables simultaneous execution of up to two image recognition applications in TMPV7502XBG.
(*8) Depends on type of image processing accelerator and channel number by product.

1.3. Product List

The table below shows the derivatives of the TMPV75 Series.

Table 1-1 Product List

Module Name	Product Name			
	TMPV7528XBG	TMPV7506XBG	TMPV7504XBG	TMPV7502XBG
Control MeP	1 CPU			
VENEZIA	4 MPEs			2 MPEs
Arm Cortex-A9 MPCore	2 CPUs	—		
Affine Transformation Accelerator	1 ch			
Histogram Accelerator	1 ch			
HOG Accelerator	1 ch		—	1 ch
Filter Accelerator	2 ch			1 ch
Matching Accelerator	1 ch			
Video Input Interface	max 4 ch		max 2 ch	1 ch
Video Output Interface	1 ch			
SRAM/NOR Memory Controller	16-bit bus (2 chip select)			
DDR2 SDRAM Controller	32-bit bus × 1 or 16-bit bus × 2			16-bit bus × 1
Working RAM	512 KB × 4			
System RAM	32 KB			
System ROM	64 KB			
DMA Controller	3 ch			
General-Purpose I/O	max 24 bits			max 16 bits
Timer	max 4 ch			
UART Interface	max 5 ch			
I^2C Interface	max 4 ch			
SPI Interface	max 4 ch			1 ch
PCM Interface	Input 2 ch and Output 2 ch			
CAN Interface	max 3 ch			max 2 ch
MCU Interface	8-bit bus			—
PCI Express Interface	1 lane		—	
Operating Frequency	Arm Cortex-A9 MPCore: max 300 MHz MeP, MPE: max 266.7 MHz	max 266.7 MHz		
Operating Temperature Range (Ta)	-40 to 85 °C			
Package	516 pins, P-BGA, 27mm × 27mm, Ball pitch 1.0mm			324 pins, P-LFBGA, 11mm × 11mm, Ball pitch 0.5mm

1.4. Block Diagram

1.4.1. TMPV7528XBG

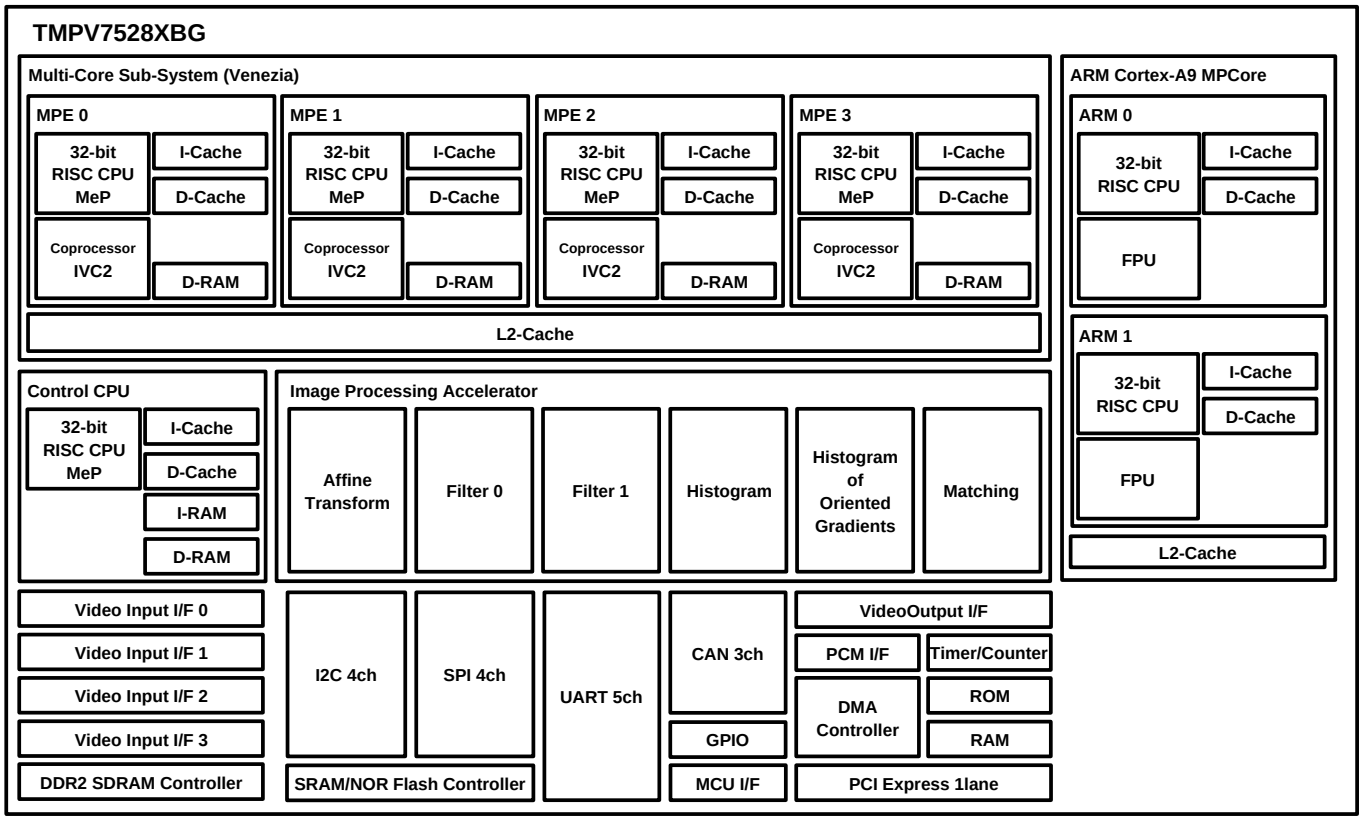


Figure 1-1 TMPV7528XBG Block Diagram

1.4.2. TMPV7506XBG

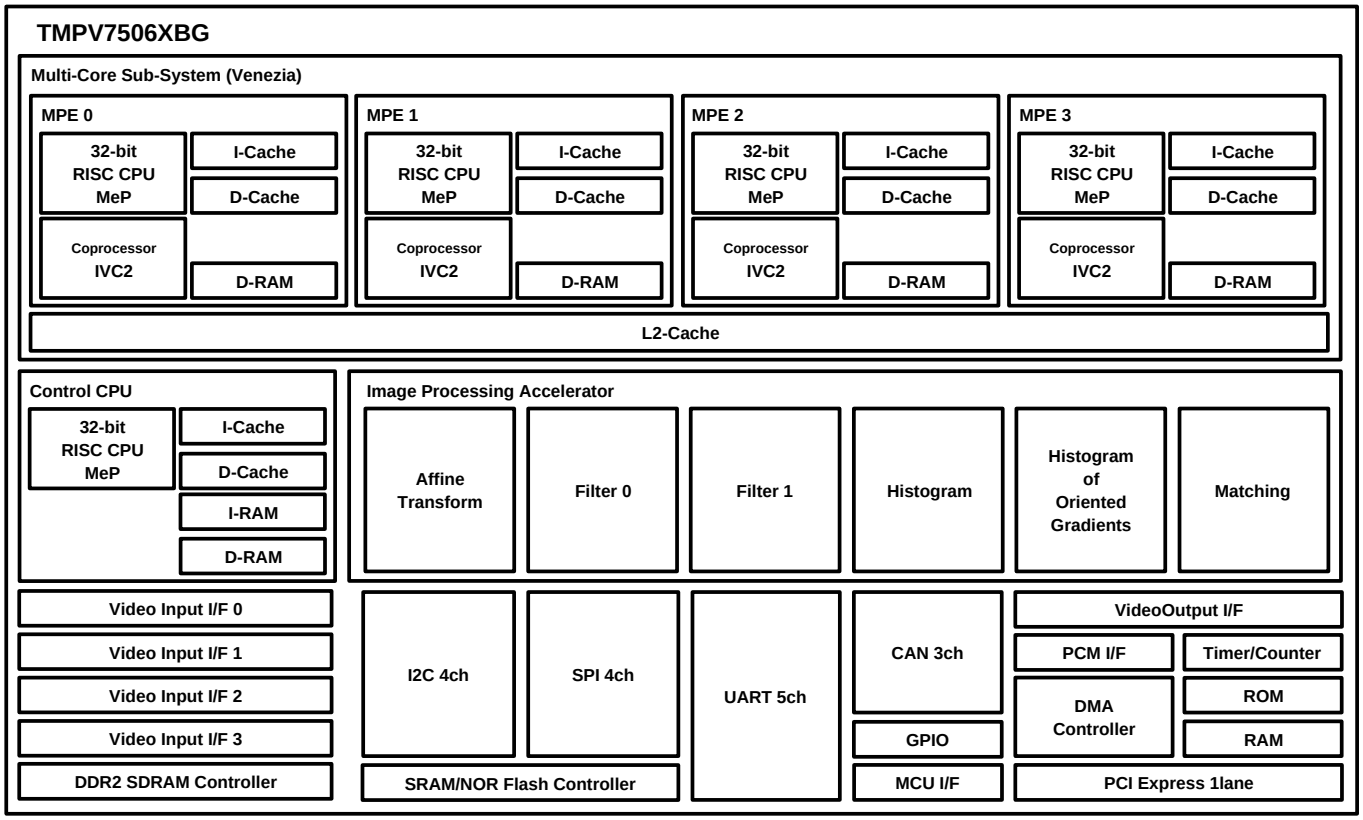


Figure 1-2 TMPV7506XBG Block Diagram

1.4.3. TMPV7504XBG

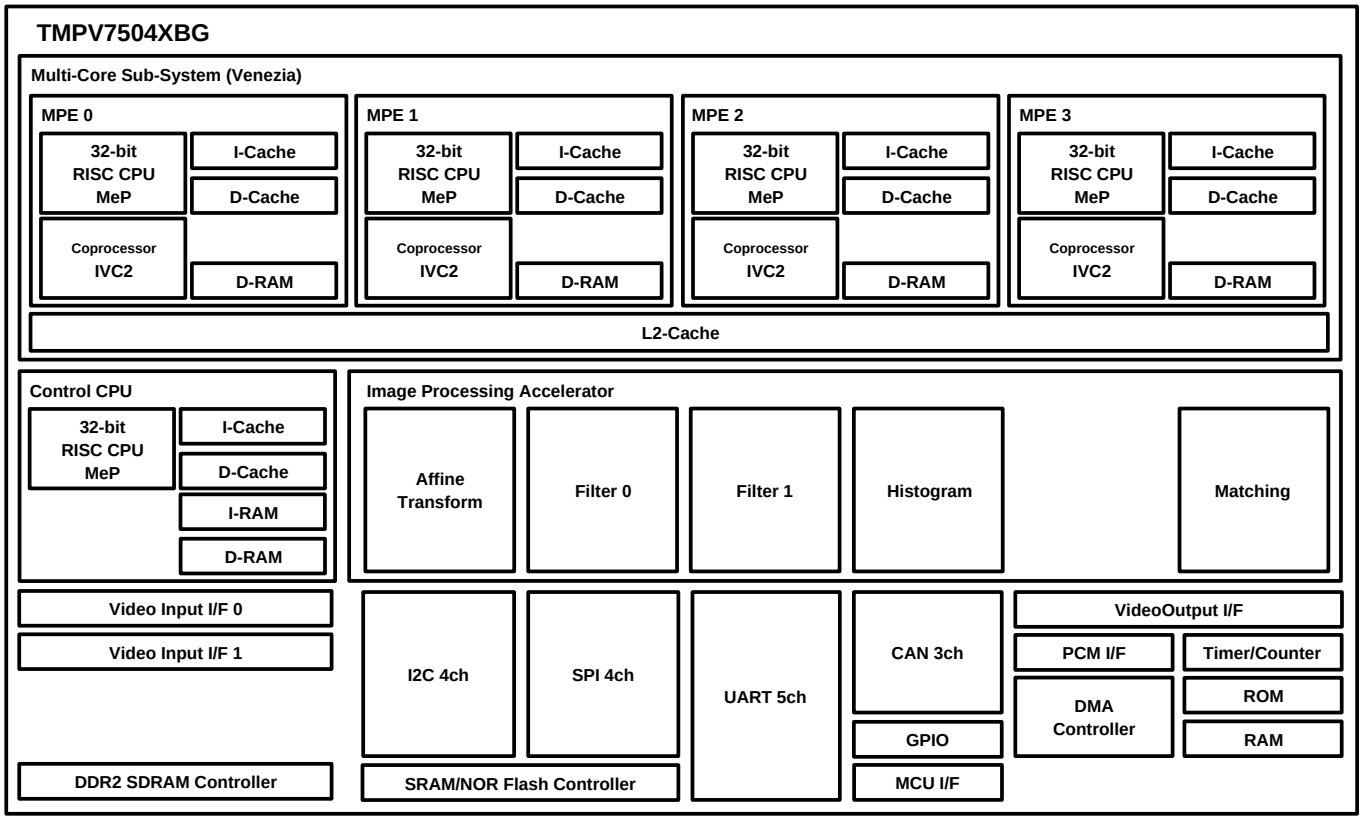


Figure 1-3 TMPV7504XBG Block Diagram

1.4.4. TMPV7502XBG

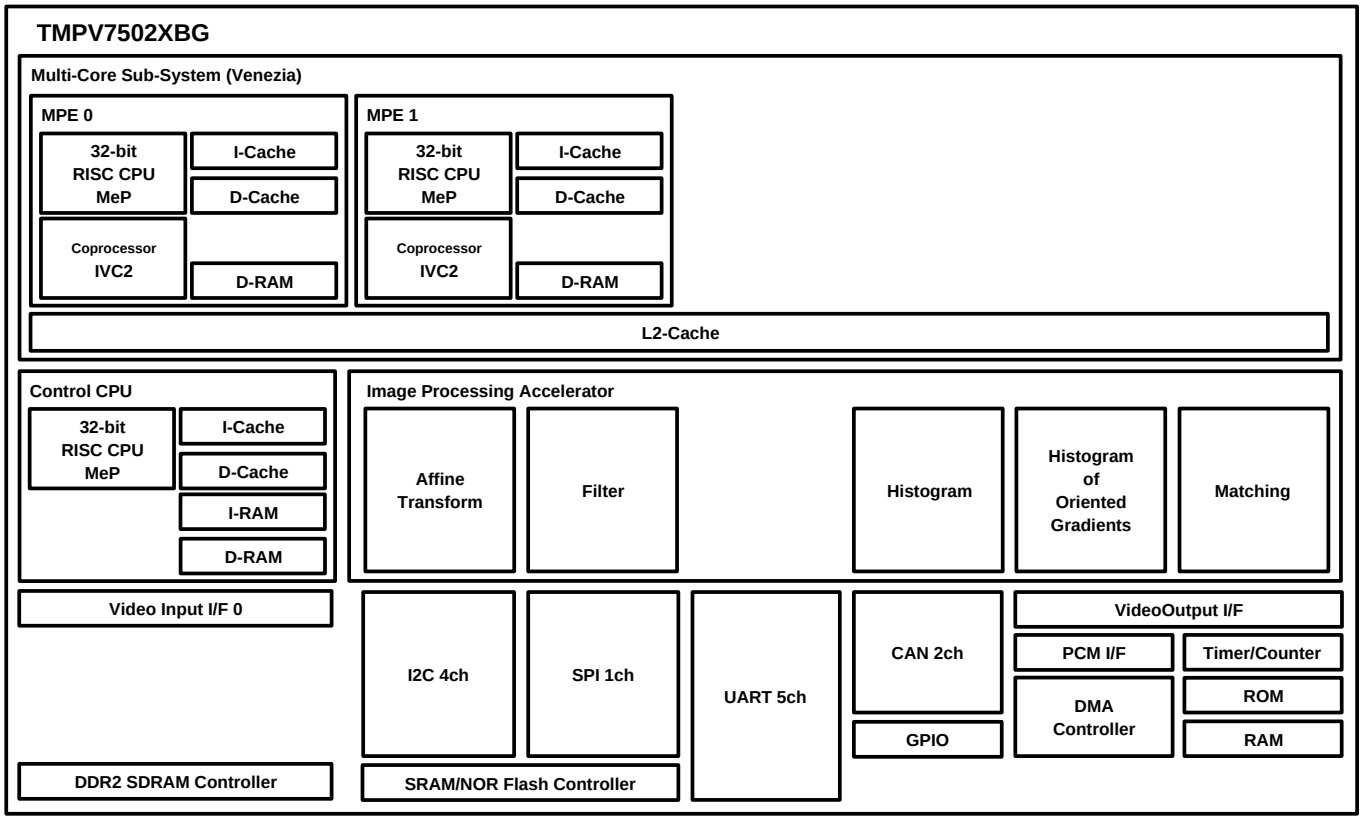


Figure 1-4 TMPV7502XBG Block Diagram

1.5. Applications

The following are the major target applications for the TMPV75 Series.

- Automotive
  - Advanced Driver Assistance System (ADAS)
    - Lane Departure Warning (LDW) system
    - Forward Collision Warning (FCW) system
    - Backward Collision Warning (BCW) system
    - Traffic Sign Recognition (TSR) system
    - Nighttime forward pedestrian detection (Night Vision) system
    - Back Over Prevention (BOP) system
    - Lane Change Assistance (LCA) system
    - Driver authentication system
    - Driver monitoring system
    - Parking assistance (Top View) system
- Industrial
  - Intelligent Transport Systems (ITS)
  - Parking management system
  - Entrance management system
  - Surveillance camera
  - Machine vision
  - Air conditioning/lighting control system
  - Digital signage
- Consumer
  - System used camera-based human detection (Lighting control, etc.)
  - System used camera-based user interface (Games, Toys etc.)
  - Video contents management system
  - Home security system

1.5.1. Example 1: Forward, Backward and Backward-side Monitoring

This is an Advanced Driver Assistance System to monitoring forward, backward, backward-side of vehicle using single or stereo camera system.

There are the following systems and the like in “Forward Monitoring” using forward camera in front of vehicle.

- Lane departure warning (LDW) system
  The detection of traffic lane, and this warns the hazard when a vehicle is departure from traffic lane without the indication of lane changing.
- Forward collision warning (FCW) system
  The detection of forward vehicles, and this warns hazard when there is a possibility of collision.
- Forward pedestrian collision warning system
  The detection of forward around pedestrians, and this warns hazard when there is a possibility of collision.
- Traffic sign recognition (TSR) system
  This warns hazard for driver when the traffic signs are detected and recognized.

There are the following systems and the like in “Backward Monitoring” using backward camera in vehicle.

- Lane departure warning (LDW) system
- Backward collision warning (BCW) system
  This detects backward vehicles and this warns hazard when there is a possibility of collision.
- Back over prevention (BOP) system
  This detects backward near pedestrians using wide angle camera.
- Lane change assistance (LCA) system
  This detects approaching vehicles from backward area, and this assists to change lane.

There are the following system and the like in “Backward-Side Monitoring” using two single cameras in side mirror.

- Lane departure warning (LDW) system
- Lane change assistance (LCA) system
- Roll warning system

When driver turns to right or left, this warns hazard for rolling in pedestrian or bicycle.
TMPV75 Series are capable of working some application at the same time.

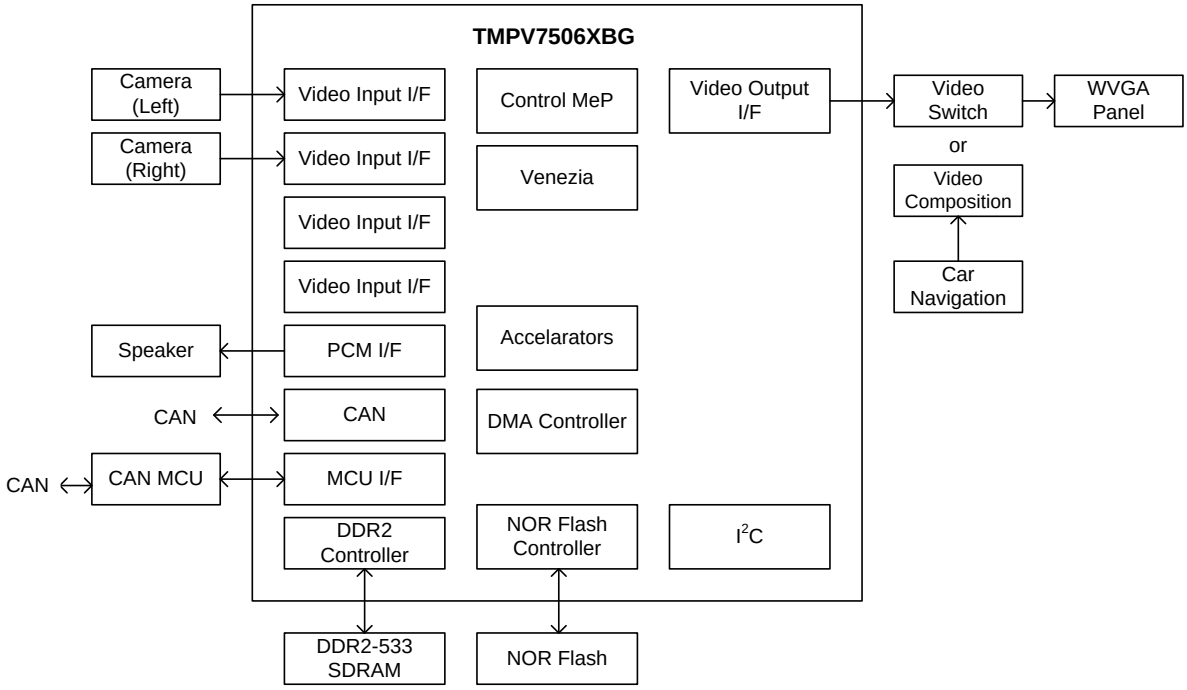


Figure 1-5 Example of Forward, Backward and Backward-Side Monitoring System of TMPV7506XBG

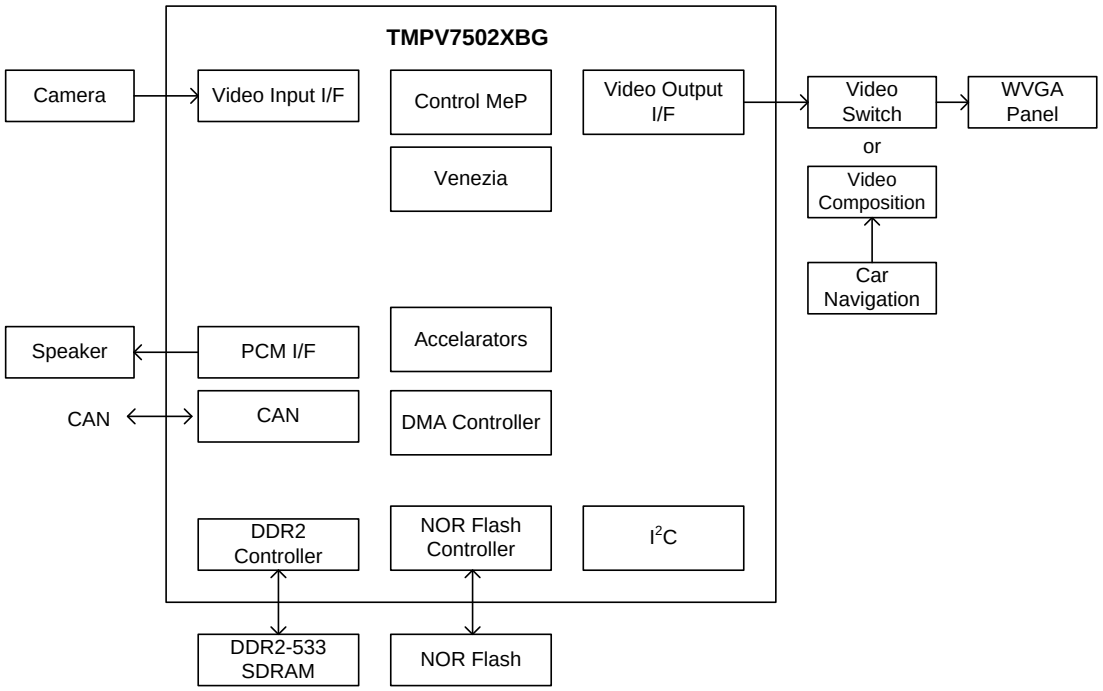


Figure 1-6 Example of Forward, Backward and Backward-Side Monitoring System of TMPV7502XBG

1.5.2. Example 2: Surrounding Monitoring (*9)

Forward, backward, left, and right pictures of vehicle are taken by using four wide angle cameras. These are corrected the distortion of lenses, and these are changed view point. Corrected pictures and top view of vehicle are composed. Monitored pictures from top view point for the vehicle and its surrounding are displayed at LCD panel.

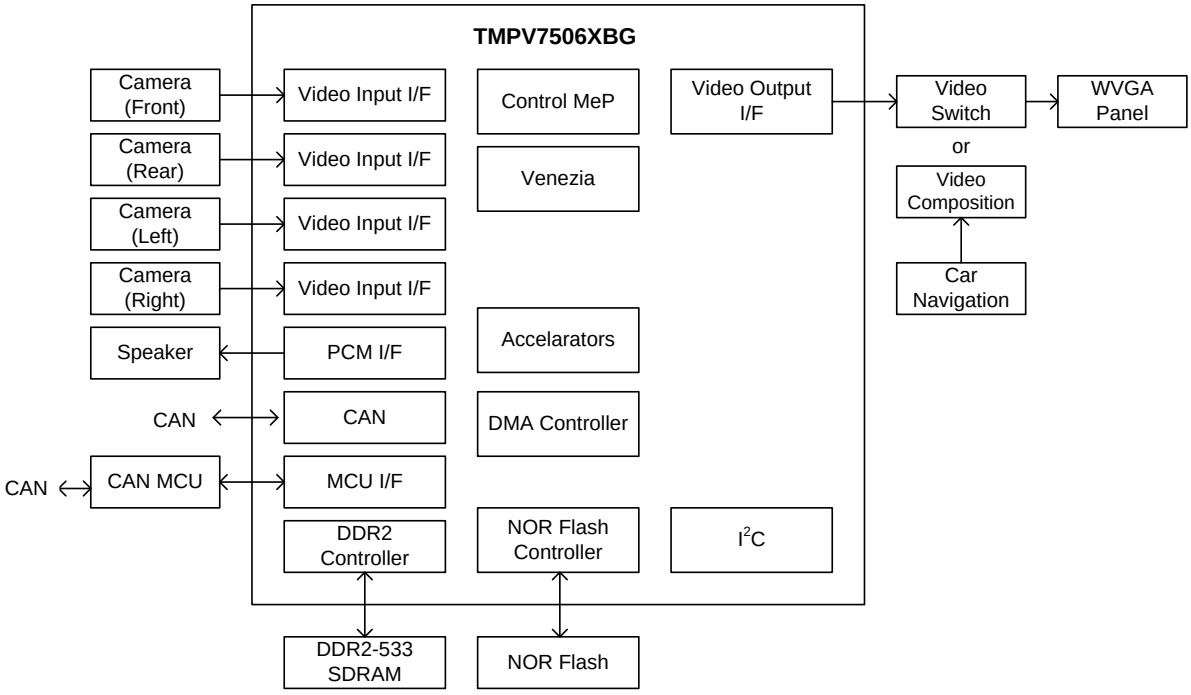


Figure 1-7 Example of Surrounding Monitoring System of TMPV7506XBG

(*9) TMPV7506XBG and TMPV7528XBG equipped 4 channels video input interface, these products correspond this application.

1.5.3. Example 3: Vehicle Inside Monitoring

For Driver Authentication system and Driver Monitoring system and Crew Monitoring system that driver or crews of vehicle are radiated infrared ray, and these pictures are taken by single close infrared camera and these pictures are analyzed and used monitoring system.

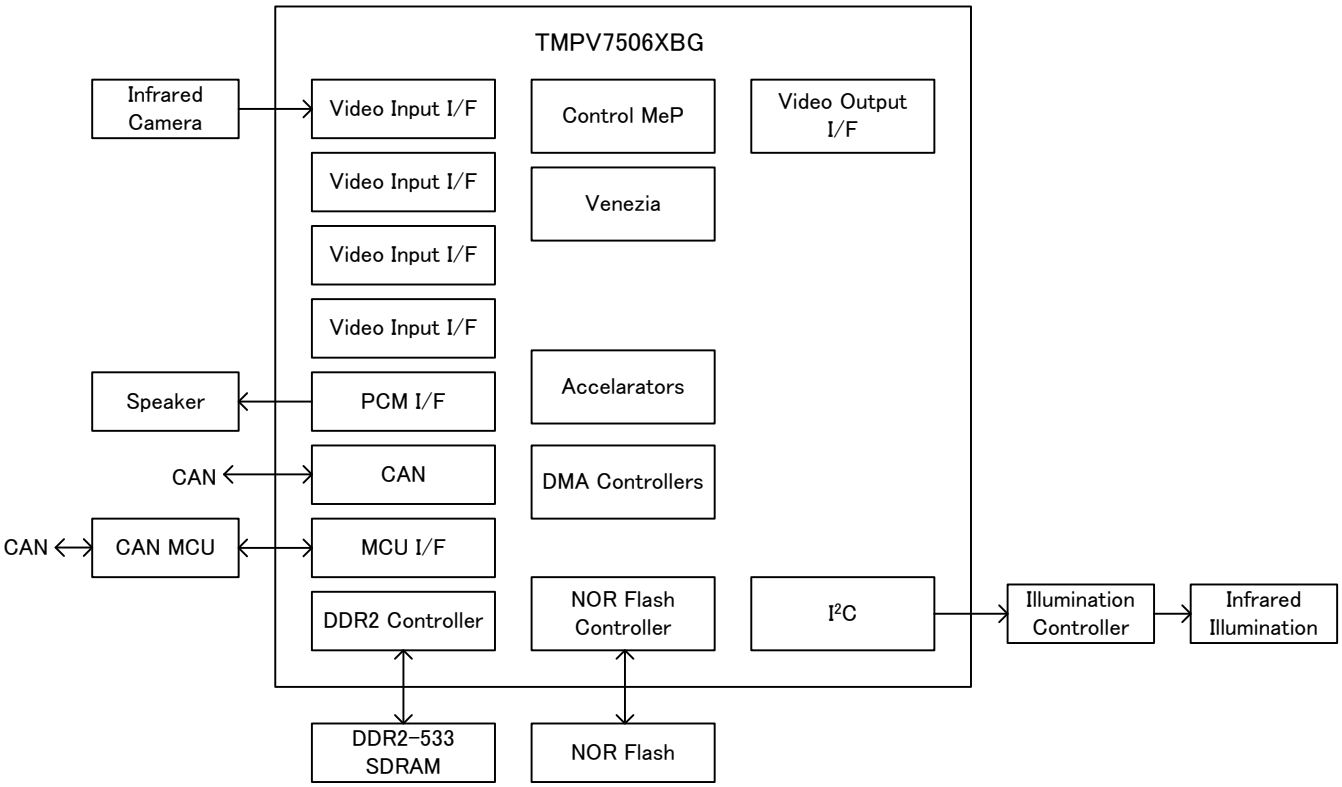


Figure 1-8 Example of Vehicle Inside Monitoring System of TMPV7506XBG

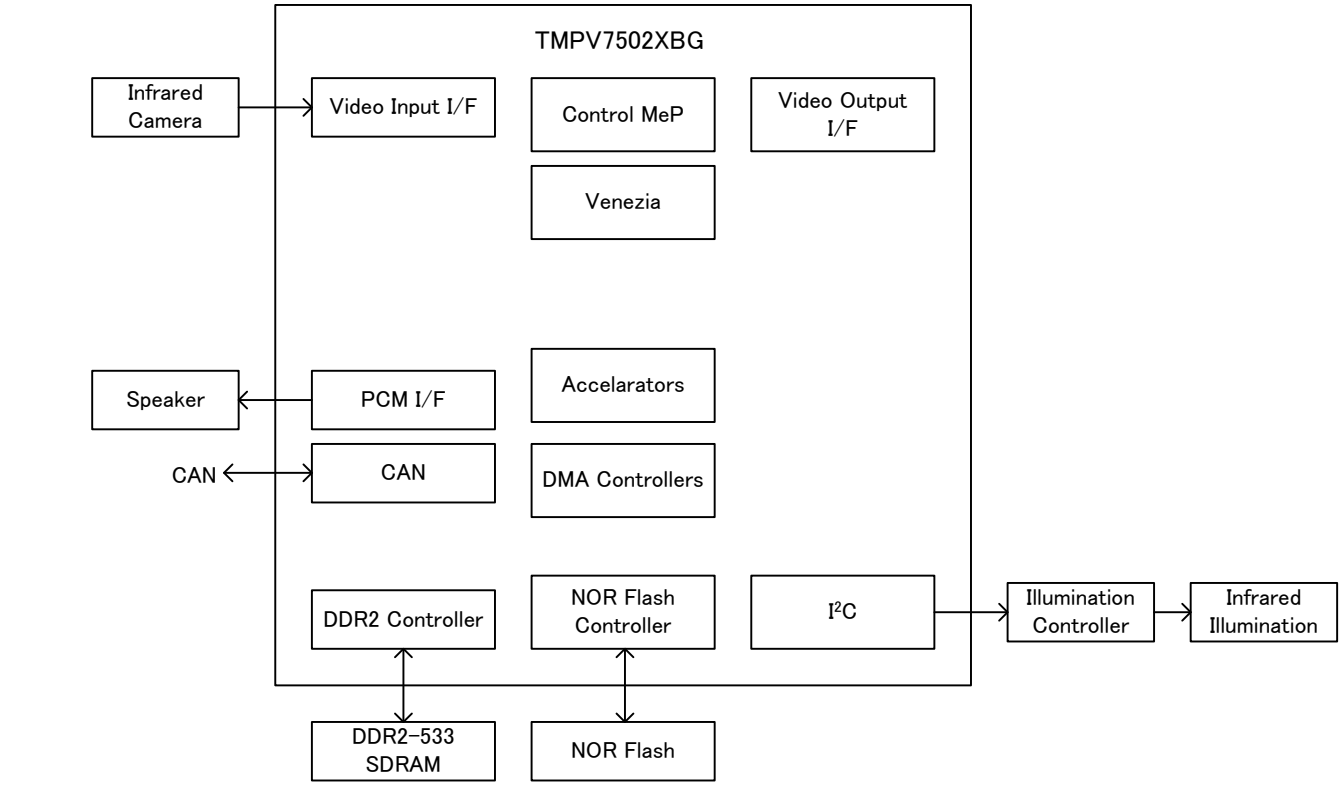


Figure 1-9 Example of Vehicle Inside Monitoring System of TMPV7502XBG

1.6. Module Name Abbreviations

In this document, the following abbreviated expressions are used for the module name.

Table 1-2 Module Name Abbreviations

Module Name	Abbreviated Expression
Control MeP	CMEP
VENEZIA	VENEZIA
Media Processing Engine	MPE (MPE0, MPE1, MPE2, MPE3)
Arm Cortex-A9 MPCore	ARM (ARM0, ARM1)
Affine Transformation Accelerator	AFFINE
Histogram Accelerator	HIST
HOG Accelerator	HOG
Filter Accelerator	FILTER (FILTER_E, FILTER_M)
Matching Accelerator	MATCH
Video Input Interface	VIIF (VIIF0, VIIF1, VIIF2, VIIF3)
Video Output Interface	VOIF
SRAM/NOR Memory Controller	MEMC
DDR2 SDRAM Controller	DDR2C
System ROM	SROM
System RAM	SRAM
Working RAM	WRAM (WRAM0, WRAM1, WRAM2, WRAM3)
Interrupt Controller	INTC
DMA Controller	DMAC (DMAC0, DMAC1, DMAC2)
General-Purpose I/O	GPIO
Timer	TIMER
UART Interface	UART (UART0, UART1, UART2, UART3, UART4)
I^2C Interface	I2C (I2C0, I2C1, I2C2, I2C3)
SPI Interface	SPI (SPI0, SPI1, SPI2, SPI3)
PCM Interface	PCMIF
CAN Interface	CAN (CAN0, CAN1, CAN2)
MCU Interface	MCUIF
PCI Express Interface	PCIE

1.7. Features

1.7.1. Control MeP (CMEP)

- Toshiba original 32-bit RISC core MeP-c5
- 16KB (2-way set-associative) instruction cache and 8KB (2-way set-associative) data cache
- 16KB (8KB × 2 banks) instruction RAM and 32KB (8KB × 4 banks) data RAM
- DMA controller used for reading/writing the instruction RAM and data RAM
- Operating frequency: 266.7 MHz maximum
- 2 channels of timer
- JTAG debug port
  Also connected to VENEZIA, so a single ICE supports the control MeP and VENEZIA debugging

1.7.2. Multi-Core Sub-System VENEZIA (VENEZIA)

- Toshiba original 32-bit RISC multi-core sub-system
- Four media processing engines MPE (MPE0, MPE1, MPE2 and MPE3)(*10)
- Each MPE features
  - 32-bit RISC core MeP-c5
  - 16KB (2-way set-associative) instruction cache and 16KB (2-way set-associative) data cache
  - 64KB (16 KB × 4 banks) data RAM used for efficient image data processing
  - Image recognition VLIW co-processor IVC2
    VLIW (Very Long Instruction Word) technology that issues up to three instructions simultaneously (one MeP instruction and up to two IVC2 instructions can be encoded in a 64-bit VLIW code).
  - SIMD (Single Instruction stream, Multiple Data stream) that perform simultaneous operations on eight sets of 8-bit data, four sets of 16-bit data, and two sets of 32-bit data.
    Each IVC2 can execute simultaneously up to two SIMD instructions.
    Some SIMD instructions can store 256 bits of operation results in accumulators for high speed carry processing (eg. 8-bit data + 8bit data → 32-bit of accumulator).
  - DMA controller used for transferring the data of data RAM
- Operating frequency: 266.7 MHz maximum
- 256KB (4-way set-associative) L2 cache for shared use among the four MPE
- 2 channels of timer
- JTAG debug port
  Also connected to VENEZIA, so a single ICE supports the control MeP and VENEZIA debugging

1.7.3. Arm® Cortex®-A9 MPCore (ARM) (*11)

- Arm 32-bit Out-of-order RISC core Arm Cortex-A9 MPCore (2CPU ARM0 and ARM1)
- Each CPU core features
  - 16KB (4-way associativity) instruction cache and 16KB (4-way associativity) data cache
  - 64-entry TLB MMU
  - Single-precision / Double-precision floating point coprocessor
- Operating frequency: 300 MHz maximum (Frequency can be set by PLL.)
- 128KB (8-way associativity) used as L2 cache for sharing between two CPUs
- In addition to JTAG debug port, an 8-bit trace port is built in
- Built-in 8KB trace buffer

(*10) TMPV7502XBG has two media processing engines MPE (MPE0 and MPE1).
(*11) Arm Cortex-A9 MPCore is equipped with only TMPV7528XBG.

1.7.4. Image Processing Accelerators

1.7.4.1. Affine Transformation Accelerator (AFFINE)

- Three operating modes
  - Geometric transformation such as rotation, expansion/dilation, translation, shear and so on of image data
  - Lens undistortion of input image data from a camera by using distortion model parameters
  - Image transformation by using lookup table for lens undistortion and view point conversion
- Number of channels: 1
- Maximum operating frequency: 266.7 MHz

1.7.4.2. Histogram Accelerator (HIST)

- Three operating modes
  - Histogram
  - Histogram with score
  - Image conversion by using lookup table
- Number of bins and counter sizes selectable from among three types
  - 256 bins 32-bit count
  - 512 bins 16-bit count
  - 1024 bins 8-bit count
- Number of channels: 1
- Maximum operating frequency: 266.7 MHz

1.7.4.3. HOG Accelerator (HOG) (*12)

- Two operating modes
  - HOG (Histograms of Oriented Gradients) feature
  - Toshiba original technology CoHOG (Co-occurrence Histograms of Oriented Gradients) feature
- Number of channels: 1
- Maximum operating frequency: 266.7 MHz

1.7.4.4. Filter Accelerator (FILTER_E, FILTER_M)

- Parallel processing of 64-pixel
- Selection of the following processes by parameters
  - Operation between two image data
  - Operation between an image data and a scalar
  - Smoothing
  - Edge detection
  - Corner detection
  - Gradient matrix calculation
  - Pyramid up/down
  - Color space conversion
  - Morphology operation
  - Template matching

  etc.
- Number of channels: Up to 2 (*13)
- Maximum operating frequency: 180 MHz

1.7.4.5. Matching Accelerator (MATCH)

- Two operating modes
  - Parallax calculation of left/right image data from a stereo camera
  - Specific template search (free search, rectangle search) for tracking and optical flow
- Number of channels: 1
- Maximum operating frequency: 266.7 MHz

(*12) HOG Accelerator is not equipped with TMPV7504XBG.
(*13) TMPV7502XBG is 1channel.

1.7.5. Video Input Interface (VIIF0-3)

- Support for capture of up to four camera images(*14)
- Maximum image size and frame rate
  - Up to SXGA (1280 × 1024 pixels): 30 fps maximum
  - Up to WVGA (800 × 480 pixels): 60 fps maximum
  - Up to QVGA (320 × 240 pixels): 100 fps maximum
- Support for various input video signal formats
  - Grayscale Y8: 4 channels maximum
  - Grayscale Y10: 4 channels maximum
  - Grayscale Y12: 4 channels maximum
  - Color 8-bit Bayer: 4 channels maximum
  - Color 10-bit Bayer: 4 channels maximum
  - Color 12-bit Bayer: 4 channels maximum
  - Color 8-bit ITU-R BT.656: 4 channels maximum
  - Color 8-bit YCbCr422: 4 channels maximum
  - Color 16-bit YCbCr422: 2 channels maximum(*15)
  - Color RGB888: 2 channels maximum(*15) (RGB666, RGB565 are also available.)
  - For NTSC/PAL CVBS input, connection via a Toshiba video decoder “TC90105FG”.
- Color space conversion and writing to memory during video signal capture
  - YCbCr422 → RGB888
  - YCbCr422 → RGB888 + Y8
  - RGB888 → YCbCr422
  - RGB888 → RGB888 + Y8
- Cropping function for cutting out and capturing specific regions
- Independent horizontal/vertical reduction (1/2, 1/4, 1/8) of capture image
- Selection of odd, even, or both fields for interlace

1.7.6. Video Output Interface (VOIF)

- Video output: 1 ch
  - 24-bit RGB888
  - 16-bit RGB565
- Maximum size and frame rate
  - WVGA (800 × 480 pixels): 60 fps
  - SXGA (1280 × 1024): 30 fps for debugging
- Support for various video layer (memory) format
  - Grayscale Y8
  - RGB888 (24-bit color, planar or packed)
  - ARGB8888 (24-bit color with 8-bit alpha value for blending)
  - RGB565 (16-bit color)
  - YCbCr422 (planar or packed)
  - 8-bit indexed color (ARGB8888 lookup table for each index color)
- Video layer
  - Support for synthesis of background color and up to five layers (number of layers depends on memory band width)
  - Layer synthesis can be made transparent using a color key, an 8-bit alpha value (selectable of pixel unit or layer unit) and an escape key.
  - Specification of any one color from RGB888 for background color
  - Each layer display position and display size can be specified in 1 pixel unit
  - Support of 1X, 2X, and 4X scaling source data for each layer

1.7.7. SRAM/NOR Memory Controller (MEMC)

- Memory type: 16-bit data bus width of parallel interface NOR Flash memory, SRAM or ROM
- Access time: Settable as 30.3ns (in case of 266.7MHz system clock) multiple
- Memory capacity: 32 Mbytes × 1 or 2 chip select(s)(*16)

(*14) Depends on the signal format and product.
(*15) TMPV7502XBG is cannot input.
(*16) TMPV7502XBG is 32 Mbytes × 1 chip select.

1.7.8. DDR2 SDRAM Controller (DDR2C)

- Memory type: DDR2-533 (C) SDRAM
- Data bus width: 16 bits × 1 channel or 16 bits × 2 channels(*17)
- Memory capacity: 1Gbits(128MB) or 2Gbits(256MB) × 1 or 2 piece(s)

1.7.9. On-Chip Memory

1.7.9.1. Working RAM (WRAM0-3)

- 512Kbytes × 4 (mapped as 2Mbytes of contiguous address space) of image data working RAMs
- Support for parallel access of image data (128-bit width, 133.3MHz maximum) from up to four masters (Control MeP, MPE in VENEZIA, CPU in Arm Cortex-A9 MPCore, image processing accelerators, DMA controllers, video input interfaces and video output interface)

1.7.9.2. System RAM (SRAM)

- 32Kbytes of scratchpad memory built in for control MeP and Arm Cortex-A9 MPCore

1.7.9.3. System ROM (SROM)

- 64Kbyes of masked ROM built in for booting control MeP and ASCII code font data

1.7.10. Interrupt Controller (INTC)

- Interrupt requests to each processor (Control MeP, Arm Cortex-A9 MPCore and VENEZIA)
- NMI (Non-Maskable Interrupt) input: 1 channel
- External interrupt inputs
  - Up to 24 channels (shared with general-purpose I/O)
  - Edge/level, polarity selectable

1.7.11. DMA Controller (DMAC0-2)

- Three DMA controllers built in
- Two transfer modes
  - Channel transfer mode: Specification of transfer command by register, four channels
  - Thread transfer mode: Consecutive execution of transfer commands stored in memory, eight threads, repeat execution supported
- Fixed source address/destination address steaming also supported
- Transfer of up to 65,535 bytes with a single transfer command

1.7.12. General-Purpose I/O (GPIO)

- 24 bits maximum(*18) (shared pin use between UART, SPI, I^2C, timer and PCM interface)
- One bit unit output set/clear supported

1.7.13. Timer Module (TIMER)

- Four modes
  - Timer mode
    - 32-bit free-run counter
    - Interval interrupt
  - Output compare mode
    - Minimum output unit: 1μs, maximum output: 4294.9s
  - Input capture mode
    - Minimum pulse measurement period: 1μs, measurement up to a maximum of 4294.9s supported
  - PWM(Pulse Width Modulation) output mode
- Up to 4 channels for input/output (shared pin use between UART, SPI, I^2C, PCM interface and general-purpose I/O)

(*17) TMPV7502XBG is 16 bits × 1 channel only.
(*18) TMPV7502XBG is 16 bits maximum.

1.7.14. UART Interface (UART0-4)

- UART4 for debugging
  - 1 channel (exclusive pin)
- UART0-3 for user
  - Up to 4 channels (shared pin use between SPI, I^{2}C, timer, PCM interface and general-purpose I/O)
  - With flow control
- Full-duplex communication protocol (half-duplex communication protocol not supported)
  - Word length: 5 to 8 bits (LSB first)
  - Stop bit: 1 or 1.5 bits (5-bit word length only) / 1 or 2 bits (6 to 8-bit word length only)
  - Parity bit: Odd parity / Even parity / No parity
- 16-bit programmable baud rate generator (300 to 921600 bps)
- 32-byte send FIFO and 32-word(8-bit data + 3-bit flag) receive FIFO

1.7.15. I^{2}C Interface (I2C0-3)

- Up to 4 channels (shared pin use between UART, SPI, timer, PCM interface and general-purpose I/O)
  - Master function and slave function supported (multi-master function not supported)

1.7.16. SPI Interface (SPI0-3)

- Up to 4 channels(*19) (shared pin use between UART, I^{2}C, timer, PCM interface and general-purpose I/O)
- Full-duplex, 4-line (data input, data output, serial clock and chip select) synchronous transfer
- Serial interface enable/disable using chip select supported
- 3-level programmable master bit rate supported
- Programmable clock polarity and clock phase can be selected
- Programmable data sequence (MSB or LSB first) can be configured

1.7.17. PCM Interface (PCMIF)

- Serial audio interface (I^{2}S)
  - Data format: 16, 18, 20 or 24 bits
  - Number of slots: 32, 48 or 64 (slave mode), 64 (master mode)
- Number of channels: 2 channels (L/R) of input and 2channels (L/R) output (shared pin use between UART, SPI, I^{2}C, timer and general-purpose I/O)
- Sub oscillator for audio clock source (master mode)

1.7.18. CAN Interface (CAN0-2)

- Conforming to the CAN protocol specification V2.0 Part B (active)
- Number of channels: 3(*20)
  - Mail box is 32 boxes (31 boxes for transmit/receive, 1 box for receive only) per 1 channel.

1.7.19. MCU Interface (MCUIF) (*21)

- For interfacing with external host MCU
  - 8-bit bidirectional parallel bus
  - Controlled by four signals; read ready, read enable, write ready and write enable
- 32-byte input FIFO and 32-byte output FIFO
- DMA controller for data transfer between FIFO and memory

1.7.20. PCI Express Interface (PCIE) (*22)

- PCI Express Base Specification Revision 1.1
  - Transfer rate: 2.5Gbps/direction
  - Number of lane: 1

(*19) TMPV7502XBG is 1 channel.
(*20) TMPV7502XBG is 2 channels.
(*21) MCU interface is not equipped with TMPV7502XBG.
(*22) PCI Express interface is equipped with TMPV7528XBG and TMPV7506XBG.

- Virtual channel: 1
- Max payload size: 128bytes (Memory read request: up to 4Kbytes)

- Root complex/End point supported

1.7.21. Clock

- PLL: 3 channels
  - SYSPLL: Generates 266.7MHz(max) system clock
  - ARMPLL: Generates 300MHz(max) clock for Arm Cortex-A9 MPCore or Filter accelerators
  - VOIFPLL: Generates 325MHz(max) clock for video output interface
- Oscillator: 2 channels
  - Main: For SYSPLL, ARMPLL or VOIFPLL (12MHz crystal oscillator connection)
  - Sub: For PCM interface or SYSPLL, ARMPLL or VOIFPLL

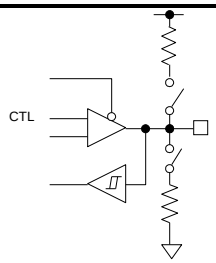
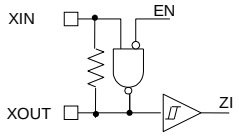
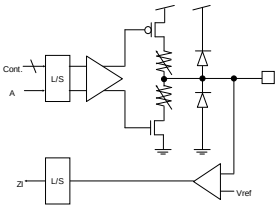
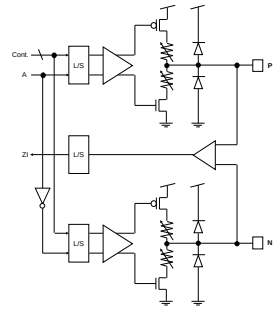
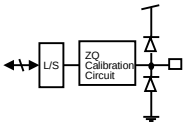
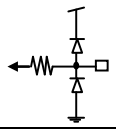
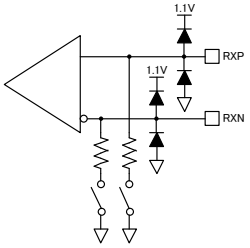
2. Signal Description

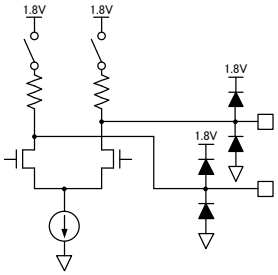
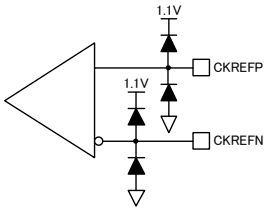
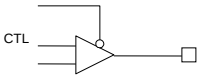
2.1. Signal List

The following paragraphs explain each signal pin. The meaning of each item of each signal pin table is shown below.

- “Pin name”: It shows the name of a pin.
- “Function”: It shows the function of a pin.
- “Structure”: It shows the structure of a pin. The meaning of each value is shown in “Table 2-1 Pin Structure”.
- “I/O enabling control”: It shows the state control at the time of initialization. The meaning of each value is shown below.
  - LE: LatchEnd signal. It is in a Hi-Z state to reset latch taking in.
  - LE-H: LatchEnd signal. H is outputted to reset latch taking in.
  - LE-PD: LatchEnd signal. Up to reset latch taking in -- a Hi-Z state -- and Pull Down.
  - IE: IOSET_EN signal. It is in a Hi-Z state until I/O pin validation is performed.
  - —: I/O enabling control is not performed.
- “The input-and-output direction (DIR)”: (I/O enabling control back) The direction of input and output is shown. The meaning of each value is shown below.
  - I: Input Signal.
  - O: Output signal.
  - B: Bidirectional signal.
  - —: Power supplies etc. are other signals.
- “Pull-Up/Pull-Down”: It shows Pull Up and Pull Down control. The meaning of each value is shown below.
  - PU: Pull Up.
  - PD: Pull Down.
  - —: Neither Pull Up nor Pull Down is carried out.
- “Handling of unused pin”: It shows the processing when not using a pin. The meaning of each value is shown below.
  - OPEN: OPEN (un-connecting) Please carry out.
  - VDD11: Please connect with 1.1V power supply.
  - VDD33: Please connect with 3.3V power supply.
  - VSS: Please connect with VSS Ground.
  - PU: Pull Up.
  - PD: Pull Down.
  - RL: Used as a Reset Latch Setup.
- “Pin position”: It shows the pin position of “2.2. Ball Assignment”. Please follow “Handling of unused pin” with the product which does not have an applicable function. (Refer to “Table 1-1 Product List”)

Table 2-1 Pin Structure

Symbol	Explanation	Structure
BD42	3.3 V I/F bidirectional multi-drive buffer Schmidt Trigger input with pull-up / down (ON/OFF programmable)	
BD84	3.3 V I/F bidirectional multi-drive buffer Schmidt Trigger input with pull-up / down (ON/OFF programmable)	
OSC	The buffer for crystal oscillators with feedback resistance	
DDR-IO	1.8V DDR2 SDRAM input / output buffer (without DQS, CK)	
DDR-DQS	1.8V DDR2 SDRAM input / output buffer	
DDR-CK	1.8V DDR2 SDRAM input / output buffer	
DDR-EXRES	DDR2 SDRAM external resistance connection pin	
DDR-VREF	0.9V DDR2 SDRAM reference voltage pin	
PCIE-RX	1.8V PCI Express differential input buffer (RX)	

Symbol	Explanation	Structure
PCIE-TX	1.8V PCI Express differential output buffer (TX)	
PCIE-REFCLK	1.8V PCI Express differential input buffer (REFCLK)	
PCIE-AMOUT	PCI Express analog monitor output pin	
POWER	Digital power supply pin	—
GND	Digital ground pin	—
A-POWER	Analog power supply pin	—
A-GND	Analog ground pin	—

2.1.1. Video Input Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
VIIF_VSYNC0	VIIF0 Vertical-Synchronizing signal input	BD42	IE	I	PD	VSS	U23	H18
VIIF_HSYNC0	VIIF0 Horizontal-Synchronizing signal input	BD42	IE	I	PD	VSS	U24	G15
VIIF_FIELD0	VIIF0 Field signal input	BD42	IE	I	PD	VSS	U25	G16
VIIF_CK0	VIIF0 Clock Input	BD42	IE	I	PD	VSS	U26	G17
VIIF_VSYNC1	VIIF1 Vertical-Synchronizing signal input	BD42	IE	I	PD	VSS	H23	—
VIIF_HSYNC1	VIIF1 Horizontal-Synchronizing signal input	BD42	IE	I	PD	VSS	H24	—
VIIF_FIELD1	VIIF1 Field signal input	BD42	IE	I	PD	VSS	H25	—
VIIF_CK1	VIIF1 Clock Input	BD42	IE	I	PD	VSS	H26	—
VIIF_VSYNC2	VIIF2 Vertical-Synchronizing signal input	BD42	IE	I	PD	VSS	T23	—
VIIF_HSYNC2	VIIF2 Horizontal-Synchronizing signal input	BD42	IE	I	PD	VSS	T24	—
VIIF_FIELD2	VIIF2 Field signal input	BD42	IE	I	PD	VSS	T25	—
VIIF_CK2	VIIF2 Clock Input	BD42	IE	I	PD	VSS	T26	—
VIIF_VSYNC3	VIIF3 Vertical-Synchronizing signal input	BD42	IE	I	PD	VSS	G23	—
VIIF_HSYNC3	VIIF3 Horizontal-Synchronizing signal input	BD42	IE	I	PD	VSS	G24	—
VIIF_FIELD3	VIIF3 Field signal input	BD42	IE	I	PD	VSS	G25	—
VIIF_CK3	VIIF3 Clock Input	BD42	IE	I	PD	VSS	G26	—
VIIF_D0	VIIF Data Input 0	BD42	IE	I	PD	VSS	Y23	L18
VIIF_D1	VIIF Data Input 1	BD42	IE	I	PD	VSS	Y24	K15
VIIF_D2	VIIF Data Input 2	BD42	IE	I	PD	VSS	Y25	K16
VIIF_D3	VIIF Data Input 3	BD42	IE	I	PD	VSS	Y26	K17
VIIF_D4	VIIF Data Input 4	BD42	IE	I	PD	VSS	W23	K18
VIIF_D5	VIIF Data Input 5	BD42	IE	I	PD	VSS	W24	J15
VIIF_D6	VIIF Data Input 6	BD42	IE	I	PD	VSS	W25	J16
VIIF_D7	VIIF Data Input 7	BD42	IE	I	PD	VSS	W26	J17
VIIF_D8	VIIF Data Input 8	BD42	IE	I	PD	VSS	V23	J18
VIIF_D9	VIIF Data Input 9	BD42	IE	I	PD	VSS	V24	H15
VIIF_D10	VIIF Data Input 10	BD42	IE	I	PD	VSS	V25	H16
VIIF_D11	VIIF Data Input 11	BD42	IE	I	PD	VSS	V26	H17
VIIF_D12	VIIF Data Input 12	BD42	IE	I	PD	VSS	R23	—
VIIF_D13	VIIF Data Input 13	BD42	IE	I	PD	VSS	R24	—
VIIF_D14	VIIF Data Input 14	BD42	IE	I	PD	VSS	R25	—
VIIF_D15	VIIF Data Input 15	BD42	IE	I	PD	VSS	R26	—
VIIF_D16	VIIF Data Input 16	BD42	IE	I	PD	VSS	N23	—
VIIF_D17	VIIF Data Input 17	BD42	IE	I	PD	VSS	N24	—
VIIF_D18	VIIF Data Input 18	BD42	IE	I	PD	VSS	N25	—
VIIF_D19	VIIF Data Input 19	BD42	IE	I	PD	VSS	N26	—
VIIF_D20	VIIF Data Input 20	BD42	IE	I	PD	VSS	M23	—
VIIF_D21	VIIF Data Input 21	BD42	IE	I	PD	VSS	M24	—
VIIF_D22	VIIF Data Input 22	BD42	IE	I	PD	VSS	M25	—

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
VIIF_D23	VIIF Data Input 23	BD42	IE	I	PD	VSS	M26	—
VIIF_D24	VIIF Data Input 24	BD42	IE	I	PD	VSS	L23	—
VIIF_D25	VIIF Data Input 25	BD42	IE	I	PD	VSS	L24	—
VIIF_D26	VIIF Data Input 26	BD42	IE	I	PD	VSS	L25	—
VIIF_D27	VIIF Data Input 27	BD42	IE	I	PD	VSS	L26	—
VIIF_D28	VIIF Data Input 28	BD42	IE	I	PD	VSS	K23	—
VIIF_D29	VIIF Data Input 29	BD42	IE	I	PD	VSS	K24	—
VIIF_D30	VIIF Data Input 30	BD42	IE	I	PD	VSS	K25	—
VIIF_D31	VIIF Data Input 31	BD42	IE	I	PD	VSS	K26	—
VIIF_D32	VIIF Data Input 32	BD42	IE	I	PD	VSS	J23	—
VIIF_D33	VIIF Data Input 33	BD42	IE	I	PD	VSS	J24	—
VIIF_D34	VIIF Data Input 34	BD42	IE	I	PD	VSS	J25	—
VIIF_D35	VIIF Data Input 35	BD42	IE	I	PD	VSS	J26	—
VIIF_D36	VIIF Data Input 36	BD42	IE	I	PD	VSS	F23	—
VIIF_D37	VIIF Data Input 37	BD42	IE	I	PD	VSS	F24	—
VIIF_D38	VIIF Data Input 38	BD42	IE	I	PD	VSS	F25	—
VIIF_D39	VIIF Data Input 39	BD42	IE	I	PD	VSS	F26	—
VIIF_D40	VIIF Data Input 40	BD42	IE	I	PD	VSS	E24	—
VIIF_D41	VIIF Data Input 41	BD42	IE	I	PD	VSS	E25	—
VIIF_D42	VIIF Data Input 42	BD42	IE	I	PD	VSS	E26	—
VIIF_D43	VIIF Data Input 43	BD42	IE	I	PD	VSS	D24	—
VIIF_D44	VIIF Data Input 44	BD42	IE	I	PD	VSS	D25	—
VIIF_D45	VIIF Data Input 45	BD42	IE	I	PD	VSS	D26	—
VIIF_D46	VIIF Data Input 46	BD42	IE	I	PD	VSS	C25	—
VIIF_D47	VIIF Data Input 47	BD42	IE	I	PD	VSS	C26	—

2.1.2. Video Output Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
VOIF_CK	VOIF Clock	BD84	IE	O	PD	OPEN	N3	N1
VOIF_DE	VOIF Data Enable	BD84	IE	O	PD	OPEN	M2	N2
VOIF_VSYNC_N	VOIF Vertical-Synchronizing Output	BD84	IE	O	PU	OPEN	C2	A3
VOIF_HSYNC_N	VOIF Horizontal-Synchronizing Output	BD84	IE	O	PU	OPEN	C1	B3
VOIF_D0	VOIF Data 0 (shared pin with ARM_TRCD0(*23))	BD84	IE	O	PD	OPEN	D3	B2
VOIF_D1	VOIF Data 1 (shared pin with ARM_TRCD1(*23))	BD84	IE	O	PD	OPEN	D2	C3
VOIF_D2	VOIF Data 2 (shared pin with ARM_TRCD2(*23))	BD84	IE	O	PD	OPEN	D1	C2
VOIF_D3	VOIF Data 3	BD84	IE	O	PD	OPEN	E3	C1
VOIF_D4	VOIF Data 4	BD84	IE	O	PD	OPEN	E2	D4
VOIF_D5	VOIF Data 5	BD84	IE	O	PD	OPEN	E1	D3
VOIF_D6	VOIF Data 6	BD84	IE	O	PD	OPEN	F4	D2
VOIF_D7	VOIF Data 7	BD84	IE	O	PD	OPEN	F3	D1
VOIF_D8	VOIF Data 8 (shared pin with ARM_TRCD3(*23))	BD84	IE	O	PD	OPEN	F2	E4
VOIF_D9	VOIF Data 9 (shared pin with ARM_TRCD4(*23))	BD84	IE	O	PD	OPEN	F1	E3
VOIF_D10	VOIF Data 10	BD84	IE	O	PD	OPEN	G4	E2
VOIF_D11	VOIF Data 11	BD84	IE	O	PD	OPEN	G3	E1
VOIF_D12	VOIF Data 12	BD84	IE	O	PD	OPEN	G2	F4
VOIF_D13	VOIF Data 13	BD84	IE	O	PD	OPEN	G1	F3
VOIF_D14	VOIF Data 14	BD84	IE	O	PD	OPEN	H4	G4
VOIF_D15	VOIF Data 15	BD84	IE	O	PD	OPEN	H3	G3
VOIF_D16	VOIF Data 16 (shared pin with ARM_TRCD5(*23))	BD84	IE	O	PD	OPEN	H2	H4
VOIF_D17	VOIF Data 17 (shared pin with ARM_TRCD6(*23))	BD84	IE	O	PD	OPEN	H1	H3
VOIF_D18	VOIF Data 18 (shared pin with ARM_TRCD7(*23))	BD84	IE	O	PD	OPEN	J4	K4
VOIF_D19	VOIF Data 19	BD84	IE	O	PD	OPEN	J3	K3
VOIF_D20	VOIF Data 20	BD84	IE	O	PD	OPEN	J2	L4
VOIF_D21	VOIF Data 21	BD84	IE	O	PD	OPEN	K3	L3
VOIF_D22	VOIF Data 22	BD84	IE	O	PD	OPEN	L3	M4
VOIF_D23	VOIF Data 23	BD84	IE	O	PD	OPEN	M3	M3

(*23) The shared pin with ARM_TRCD[7:0] are applicable only for the TMPV7528XBG. Please refer to “2.3.2. ARM Trace Pins” for pin share.

2.1.3. SRAM/NOR Memory Controller

MEMC_A [23:0] is used for Reset Latch Setting.
Pins set as “H” need to Pull-up by 10kΩ resistors. Pins set as “L” need to Pull-down by 10kΩ resistors.
MEMC_D [15:0] need to Pull-up by 10kΩ resistors.

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
MEMC_CS0_N	MEMC Chip Select 0	BD42	LE-H	O	PU	OPEN	AA23	L15
MEMC_CS1_N	MEMC Chip Select 1	BD42	LE-H	O	PU	OPEN	AA22	L16
MEMC_WE_N	MEMC Write Enable	BD42	LE-H	O	PU	OPEN	AA25	M17
MEMC_OE_N	MEMC Output Enable	BD42	LE-H	O	PU	OPEN	AA24	M18
MEMC_A0	MEMC Address 0	BD42	LE	O	PD	RL	AF20	R14
MEMC_A1	MEMC Address 1	BD42	LE	O	PD	RL	AB21	T14
MEMC_A2	MEMC Address 2	BD42	LE	O	PD	RL	AC21	U14
MEMC_A3	MEMC Address 3	BD42	LE	O	PD	RL	AD21	V14
MEMC_A4	MEMC Address 4	BD42	LE	O	PD	RL	AE21	T15
MEMC_A5	MEMC Address 5	BD42	LE	O	PD	RL	AF21	U15
MEMC_A6	MEMC Address 6	BD42	LE	O	PD	RL	AC22	V15
MEMC_A7	MEMC Address 7	BD42	LE	O	PD	RL	AD22	U16
MEMC_A8	MEMC Address 8	BD42	LE	O	PD	RL	AE22	V16
MEMC_A9	MEMC Address 9	BD42	LE	O	PD	RL	AF22	T17
MEMC_A10	MEMC Address 10	BD42	LE	O	PD	RL	AD23	T18
MEMC_A11	MEMC Address 11	BD42	LE	O	PD	RL	AE23	R16
MEMC_A12	MEMC Address 12	BD42	LE	O	PD	RL	AF23	R17
MEMC_A13	MEMC Address 13	BD42	LE	O	PD	RL	AE24	R18
MEMC_A14	MEMC Address 14	BD42	LE	O	PD	RL	AF24	P15
MEMC_A15	MEMC Address 15	BD42	LE	O	PD	RL	AD25	P16
MEMC_A16	MEMC Address 16	BD42	LE	O	PD	RL	AD26	P17
MEMC_A17	MEMC Address 17	BD42	LE	O	PD	RL	AC24	P18
MEMC_A18	MEMC Address 18	BD42	LE	O	PD	RL	AC25	N15
MEMC_A19	MEMC Address 19	BD42	LE	O	PD	RL	AC26	N16
MEMC_A20	MEMC Address 20	BD42	LE	O	PD	RL	AB23	N17
MEMC_A21	MEMC Address 21	BD42	LE	O	PD	RL	AB24	N18
MEMC_A22	MEMC Address 22	BD42	LE	O	PD	RL	AB25	M15
MEMC_A23	MEMC Address 23	BD42	LE	O	PD	RL	AB26	M16
MEMC_D0	MEMC Data 0	BD42	LE	B	PD	PU	AC17	T9
MEMC_D1	MEMC Data 1	BD42	LE	B	PD	PU	AD17	U9
MEMC_D2	MEMC Data 2	BD42	LE	B	PD	PU	AE17	T10
MEMC_D3	MEMC Data 3	BD42	LE	B	PD	PU	AF17	U10
MEMC_D4	MEMC Data 4	BD42	LE	B	PD	PU	AC18	V10
MEMC_D5	MEMC Data 5	BD42	LE	B	PD	PU	AD18	T11
MEMC_D6	MEMC Data 6	BD42	LE	B	PD	PU	AE18	U11
MEMC_D7	MEMC Data 7	BD42	LE	B	PD	PU	AF18	V11
MEMC_D8	MEMC Data 8	BD42	LE	B	PD	PU	AC19	R12
MEMC_D9	MEMC Data 9	BD42	LE	B	PD	PU	AD19	T12
MEMC_D10	MEMC Data 10	BD42	LE	B	PD	PU	AE19	U12
MEMC_D11	MEMC Data 11	BD42	LE	B	PD	PU	AF19	V12
MEMC_D12	MEMC Data 12	BD42	LE	B	PD	PU	AB20	R13
MEMC_D13	MEMC Data 13	BD42	LE	B	PD	PU	AC20	T13

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
MEMC_D14	MEMC Data 14	BD42	LE	B	PD	PU	AD20	U13
MEMC_D15	MEMC Data 15	BD42	LE	B	PD	PU	AE20	V13

2.1.4. DDR2 SDRAM Controller

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
DDR2C_CKE	DDR2C Clock Enable	DDR-IO	—	O	—	OPEN	A11	E13
DDR2C_CKN	DDR2C Clock	DDR-CK	—	O	—	OPEN	A14	A13
DDR2C_CKP			—	O	—	OPEN	A13	A12
DDR2C_CS_N	DDR2C Chip Select	DDR-IO	—	O	—	OPEN	C11	E15
DDR2C_RAS_N	DDR2C Row Address Strobe	DDR-IO	—	O	—	OPEN	B10	B14
DDR2C_CAS_N	DDR2C Column Address Strobe	DDR-IO	—	O	—	OPEN	C10	E16
DDR2C_WE_N	DDR2C Write Enable	DDR-IO	—	O	—	OPEN	D11	D14
DDR2C_BA0	DDR2C Bank Address 0	DDR-IO	—	O	—	OPEN	B12	B15
DDR2C_BA1	DDR2C Bank Address 1	DDR-IO	—	O	—	OPEN	D12	C14
DDR2C_BA2	DDR2C Bank Address 2	DDR-IO	—	O	—	OPEN	C12	A15
DDR2C_A0	DDR2C Address 0	DDR-IO	—	O	—	OPEN	C14	A16
DDR2C_A1	DDR2C Address 1	DDR-IO	—	O	—	OPEN	B14	D16
DDR2C_A2	DDR2C Address 2	DDR-IO	—	O	—	OPEN	D13	C15
DDR2C_A3	DDR2C Address 3	DDR-IO	—	O	—	OPEN	D15	C16
DDR2C_A4	DDR2C Address 4	DDR-IO	—	O	—	OPEN	B15	A17
DDR2C_A5	DDR2C Address 5	DDR-IO	—	O	—	OPEN	B16	C18
DDR2C_A6	DDR2C Address 6	DDR-IO	—	O	—	OPEN	D16	D17
DDR2C_A7	DDR2C Address 7	DDR-IO	—	O	—	OPEN	D14	B18
DDR2C_A8	DDR2C Address 8	DDR-IO	—	O	—	OPEN	A16	E18
DDR2C_A9	DDR2C Address 9	DDR-IO	—	O	—	OPEN	C17	C17
DDR2C_A10	DDR2C Address 10	DDR-IO	—	O	—	OPEN	C13	B16
DDR2C_A11	DDR2C Address 11	DDR-IO	—	O	—	OPEN	C15	E17
DDR2C_A12	DDR2C Address 12	DDR-IO	—	O	—	OPEN	B17	F18
DDR2C_A13	DDR2C Address 13	DDR-IO	—	O	—	OPEN	C16	B17
DDR2C_DM0	DDR2C Data Mask 0	DDR-IO	—	O	—	VSS	A4	C10
DDR2C_DM1	DDR2C Data Mask 1	DDR-IO	—	O	—	VSS	D5	A5
DDR2C_DM2	DDR2C Data Mask 2	DDR-IO	—	O	—	VSS	E17	—
DDR2C_DM3	DDR2C Data Mask 3	DDR-IO	—	O	—	VSS	A18	—
DDR2C_DQ0	DDR2C Data 0	DDR-IO	—	B	—	VSS	A6	B10
DDR2C_DQ1	DDR2C Data 1	DDR-IO	—	B	—	VSS	B7	D11
DDR2C_DQ2	DDR2C Data 2	DDR-IO	—	B	—	VSS	A8	B11
DDR2C_DQ3	DDR2C Data 3	DDR-IO	—	B	—	VSS	A9	D12
DDR2C_DQ4	DDR2C Data 4	DDR-IO	—	B	—	VSS	B8	C12
DDR2C_DQ5	DDR2C Data 5	DDR-IO	—	B	—	VSS	A7	A10
DDR2C_DQ6	DDR2C Data 6	DDR-IO	—	B	—	VSS	B6	C11
DDR2C_DQ7	DDR2C Data 7	DDR-IO	—	B	—	VSS	A5	A9
DDR2C_DQ8	DDR2C Data 8	DDR-IO	—	B	—	VSS	E7	B7
DDR2C_DQ9	DDR2C Data 9	DDR-IO	—	B	—	VSS	D8	B6
DDR2C_DQ10	DDR2C Data 10	DDR-IO	—	B	—	VSS	E9	B8

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
DDR2C_DQ11	DDR2C Data 11	DDR-IO	—	B	—	VSS	E10	C7
DDR2C_DQ12	DDR2C Data 12	DDR-IO	—	B	—	VSS	D9	D6
DDR2C_DQ13	DDR2C Data 13	DDR-IO	—	B	—	VSS	E8	A7
DDR2C_DQ14	DDR2C Data 14	DDR-IO	—	B	—	VSS	D7	B5
DDR2C_DQ15	DDR2C Data 15	DDR-IO	—	B	—	VSS	D6	A6
DDR2C_DQ16	DDR2C Data 16	DDR-IO	—	B	—	VSS	E20	—
DDR2C_DQ17	DDR2C Data 17	DDR-IO	—	B	—	VSS	D20	—
DDR2C_DQ18	DDR2C Data 18	DDR-IO	—	B	—	VSS	E22	—
DDR2C_DQ19	DDR2C Data 19	DDR-IO	—	B	—	VSS	D22	—
DDR2C_DQ20	DDR2C Data 20	DDR-IO	—	B	—	VSS	D21	—
DDR2C_DQ21	DDR2C Data 21	DDR-IO	—	B	—	VSS	E21	—
DDR2C_DQ22	DDR2C Data 22	DDR-IO	—	B	—	VSS	D19	—
DDR2C_DQ23	DDR2C Data 23	DDR-IO	—	B	—	VSS	D18	—
DDR2C_DQ24	DDR2C Data 24	DDR-IO	—	B	—	VSS	B21	—
DDR2C_DQ25	DDR2C Data 25	DDR-IO	—	B	—	VSS	A21	—
DDR2C_DQ26	DDR2C Data 26	DDR-IO	—	B	—	VSS	A23	—
DDR2C_DQ27	DDR2C Data 27	DDR-IO	—	B	—	VSS	B23	—
DDR2C_DQ28	DDR2C Data 28	DDR-IO	—	B	—	VSS	B22	—
DDR2C_DQ29	DDR2C Data 29	DDR-IO	—	B	—	VSS	A22	—
DDR2C_DQ30	DDR2C Data 30	DDR-IO	—	B	—	VSS	A20	—
DDR2C_DQ31	DDR2C Data 31	DDR-IO	—	B	—	VSS	A19	—
DDR2C_DQSN0	DDR2C Data Strobe 0	DDR-DQS	—	B	—	VDD11	B4	D8
DDR2C_DQSP0			—	B	—	VSS	B5	D9
DDR2C_DQSN1	DDR2C Data Strobe 1	DDR-DQS	—	B	—	VDD11	E5	C5
DDR2C_DQSP1			—	B	—	VSS	E6	C6
DDR2C_DQSN2	DDR2C Data Strobe 2	DDR-DQS	—	B	—	VDD11	E18	—
DDR2C_DQSP2			—	B	—	VSS	E19	—
DDR2C_DQSN3	DDR2C Data Strobe 3	DDR-DQS	—	B	—	VDD11	B19	—
DDR2C_DQSP3			—	B	—	VSS	B20	—
DDR2C_ODT	DDR2C Terminator control	DDR-IO	—	O	—	OPEN	B11	E14
DDR2C_EXRES	DDR2C External resistance connect pin	DDR-EXRES	—	I	—	OPEN	E13	E8
DDR2C_VREF	DDR2C Reference Voltage (0.9V) Input	DDR-VREF	—	I	—	VDD11	E14	E9

2.1.5. General I/O

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
GPIO0	GPIO Data 0 (with pin share(*24))	BD42	IE	B	PD	OPEN	Y3	T5
GPIO1	GPIO Data 1 (with pin share(*24))	BD42	IE	B	PD	OPEN	AA3	U5
GPIO2	GPIO Data 2 (with pin share(*24))	BD42	IE	B	PD	OPEN	AB3	V5
GPIO3	GPIO Data 3 (with pin share(*24))	BD42	IE	B	PD	OPEN	AC1	T6
GPIO4	GPIO Data 4 (with pin share(*24))	BD42	IE	B	PD	OPEN	AC2	U6
GPIO5	GPIO Data 5 (with pin share(*24))	BD42	IE	B	PD	OPEN	AC3	V6
GPIO6	GPIO Data 6 (with pin share(*24))	BD42	IE	B	PD	OPEN	AD1	U7
GPIO7	GPIO Data 7 (with pin share(*24))	BD42	IE	B	PD	OPEN	AD2	V7
GPIO8	GPIO Data 8 (with pin share(*24))	BD42	IE	B	PD	OPEN	R2	N4
GPIO9	GPIO Data 9 (with pin share(*24))	BD42	IE	B	PD	OPEN	R3	N3
GPIO10	GPIO Data 10 (with pin share(*24))	BD42	IE	B	PD	OPEN	T3	P4
GPIO11	GPIO Data 11 (with pin share(*24))	BD42	IE	B	PD	OPEN	U3	P3
GPIO12	GPIO Data 12 (with pin share(*24))	BD42	IE	B	PD	OPEN	U4	P2
GPIO13	GPIO Data 13 (with pin share(*24))	BD42	IE	B	PD	OPEN	V3	P1
GPIO14	GPIO Data 14 (with pin share(*24))	BD42	IE	B	PD	OPEN	V2	R2
GPIO15	GPIO Data 15 (with pin share(*24))	BD42	IE	B	PD	OPEN	W3	R1
GPIO16	GPIO Data 16 (shared pin with ARM_TRCD0(*25))	BD42	IE	B	PD	OPEN	V5	—
GPIO17	GPIO Data 17 (shared pin with ARM_TRCD1(*25))	BD42	IE	B	PD	OPEN	W5	—
GPIO18	GPIO Data 18 (shared pin with ARM_TRCD2(*25))	BD42	IE	B	PD	OPEN	Y5	—
GPIO19	GPIO Data 19 (shared pin with ARM_TRCD3(*25))	BD42	IE	B	PD	OPEN	AA5	—
GPIO20	GPIO Data 20 (shared pin with ARM_TRCD4(*25))	BD42	IE	B	PD	OPEN	AC6	—
GPIO21	GPIO Data 21 (shared pin with ARM_TRCD5(*25))	BD42	IE	B	PD	OPEN	AC7	—
GPIO22	GPIO Data 22 (shared pin with ARM_TRCD6(*25))	BD42	IE	B	PD	OPEN	AC8	—
GPIO23	GPIO Data 23 (shared pin with ARM_TRCD7(*25))	BD42	IE	B	PD	OPEN	AC9	—

(*24) Please refer to “2.3.1.General Purpose I/O Pins” for pin share.
(*25) The shared pin with ARM_TRCD[7:0] are applicable only for the TMPV7528XBG. Please refer to “2.3.2. ARM Trace Pins” for pin share.

2.1.6. PCM Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
PCMIF_CKI	PCMIF Standard clock (for input systems)	BD42	IE	O	PD	OPEN	AC5	R8
PCMIF_CKO	PCMIF Standard clock (for output systems)	BD42	IE	O	PD	OPEN	AD4	T8
PCMIF_BCKO	PCMIF Bit Clock (for output system)	BD42	IE	B	PD	OPEN	AF3	T7
PCMIF_LRCKO	PCMIF channel clock (for output system)	BD42	IE	B	PD	OPEN	AE3	V8
PCMIF_DO	PCMIF Data (for output system)	BD42	IE	O	PD	OPEN	AE4	U8

Note: The signals other than the above (PCMIF_BCKI, PCMIF_LRCKI and PCMIF_DI) share the pin with General Purpose I/O pins. Please refer to “2.3.1. General Purpose I/O Pins” for pin share.

2.1.7. CAN Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
CAN0_RX	CAN0 Receive Data (shared pin with ARM_TRCCK(*26))	BD42	IE	I	PU	OPEN	W2	T2
CAN0_TX	CAN0 Transmit Data (shared pin with ARM_TRCCTL(*26))	BD42	IE	O	PU	OPEN	W1	T1
CAN1_RX	CAN1 Receive Data (shared pin with ARM_TRCCK(*26))	BD42	IE	I	PU	OPEN	Y2	U3
CAN1_TX	CAN1 Transmit Data (shared pin with ARM_TRCCTL(*26))	BD42	IE	O	PU	OPEN	Y1	V3
CAN2_RX	CAN2 Receive Data	BD42	IE	I	PU	OPEN	AA2	—
CAN2_TX	CAN2 Transmit Data	BD42	IE	O	PU	OPEN	AA1	—

(*26) The shared pin with ARM_TRCCK and ARM_TRCCTL are applicable only for the TMPV7528XBG. Please refer to “2.3.2. ARM Trace Pins” for pin share.

2.1.8. MCU Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position	
							7528 7506 7504	7502
MCUIF_RE_N	MCUIF Read Enable	BD42	IE	I	PU	OPEN	AD8	—
MCUIF_RRDY_N	MCUIF Read Ready	BD42	IE	O	PU	OPEN	AE8	—
MCUIF_WE_N	MCUIF Write Enable	BD42	IE	I	PU	OPEN	AF8	—
MCUIF_WRDY_N	MCUIF Write Ready	BD42	IE	O	PU	OPEN	AD7	—
MCUIF_D0	MCUIF Data 0	BD42	IE	B	PD	OPEN	AF6	—
MCUIF_D1	MCUIF Data 1	BD42	IE	B	PD	OPEN	AD5	—
MCUIF_D2	MCUIF Data 2	BD42	IE	B	PD	OPEN	AE5	—
MCUIF_D3	MCUIF Data 3	BD42	IE	B	PD	OPEN	AF5	—
MCUIF_D4	MCUIF Data 4	BD42	IE	B	PD	OPEN	AE7	—
MCUIF_D5	MCUIF Data 5	BD42	IE	B	PD	OPEN	AF7	—
MCUIF_D6	MCUIF Data 6	BD42	IE	B	PD	OPEN	AD6	—
MCUIF_D7	MCUIF Data 7	BD42	IE	B	PD	OPEN	AE6	—

2.1.9. PCI Express Interface

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position(*27)	
							7528 7506	7504 7502
PCIE_CKREFP	PCIE Clock Input	PCIE-REFCLK	—	I	—	VSS	AC11	—
PCIE_CKREFN			—	I	—	VSS	AD11	—
PCIE_RXP	PCIE Receive Data Input	PCIE-RX	—	I	—	OPEN	AE10	—
PCIE_RXN			—	I	—	OPEN	AF10	—
PCIE_TXP	PCIE Transmit Data Output	PCIE-TX	—	O	—	OPEN	AE12	—
PCIE_TXN			—	O	—	OPEN	AF12	—
PCIE_RESET_N	PCIE Reset Input/Output	BD42	IE	B	PD	OPEN	AC13	—
PCIE_AMOUT	PCIE Analog Monitor for test(*28)	PCIE-AMOUT	—	O	—	OPEN	AD13	—

(*27) PCI Express interface pin has only products with PCI Express. Please follow “Handling of unused pin” to corresponding pin of TMPV7504XBG.
(*28) This pin is to be unconnected.

2.1.10. Debugging Support

When develop of debug support tool (ex. ICE) using debug support signal, please contact us.

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position		
							7528	7506 7504	7502
MEP_TMS	CMEP/VENEZIA JTAG Mode Select(*29)	BD42	—	I	—	VDD33	V4	V4	R3
MEP_TRST_N	CMEP/VENEZIA JTAG Reset Input(*29)	BD42	—	I	—	VDD33	W4	W4	T4
MEP_TDI	CMEP/VENEZIA JTAG Data Input(*29)	BD42	—	I	—	VDD33	Y4	Y4	R5
MEP_TDO	CMEP/VENEZIA JTAG Data Output(*30)	BD84	—	B	—	PD	AA4	AA4	R6
MEP_TCK	CMEP/VENEZIA JTAG Clock Input(*31)	BD42	—	I	—	VDD33	AB4	AB4	R7
ARM_TMS	ARM JTAG Mode Select(*32)	BD42	—	I	—	VDD33	K4	—	—
ARM_TDI	ARM JTAG Data Input(*32)	BD42	—	I	—	VDD33	M4	—	—
ARM_TDO	ARM JTAG Data Output(*33)	BD84	—	O	—	OPEN	N4	—	—
ARM_RTCK	ARM JTAG Return Clock(*33)	BD84	—	O	—	OPEN	R4	—	—
ARM_TCK	ARM JTAG Clock Input(*34)	BD42	—	I	—	VDD33	T4	—	—
ARM_SRST_N	ARM Debug Core Reset Input(*32)	BD42	—	I	—	VDD33	L4	—	—
DBGUART_RXD	UART Receive Data for Debugging	BD42	IE	I	PU	OPEN	AB2	AB2	U4
DBGUART_TXD	UART Transmit Data for Debugging	BD42	IE	O	PU	OPEN	AB1	AB1	V4

2.1.11. Others

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position		
							7528	7506 7504	7502
RESET_N	Reset Input	BD42	—	I	—	—	AA26	AA26	L17
NMI_N	NMI Request Input	BD42	—	I	—	VDD33	AF4	AF4	V9
XIN1	OSC1 (main oscillator) Crystal oscillator connect pins	OSC	—	I	—	—	T1	T1	K1
XOUT1			—	O	—	—	U1	U1	L1
XIN2	OSC2 (sub oscillator) Crystal oscillator connect pins	OSC	—	I	—	PD	K1	K1	G1
XOUT2			—	O	—	OPEN	L1	L1	H1
TEST0	Test Control Signal (This pin should be tied to VSS.)	BD42	—	I	—	VSS	AB8	AB8	R11

(*29) When connected to ICE, please pull-up by a resistor of 1kΩ.
(*30) When connected to ICE, please pull-down by a resistor of 470kΩ.
(*31) When connected to ICE, please pull-down by a resistor of 1kΩ.
(*32) When connected to ICE, please pull-up. Please follow by resistor value of specifications of ICE.
(*33) When connected to ICE, please do not pull-up and pull-down.
(*34) When connected to ICE, please pull-down. Please follow by resistor value of specifications of ICE.

Symbol	Function	Structure	I/O Enable Control	DIR	Pull-Up/ Pull-Down	Handling of unused pin	Pin Position		
							7528	7506 7504	7502
TEST1	Test Control Signal (This pin should be tied to VSS.)	BD42	—	I	—	VSS	AB7	AB7	R10
TEST2	Test Control Signal (This pin should be tied to VSS.)	BD42	—	I	—	VSS	AB6	AB6	R9
TESTV	Test Power Supply (This pin should be tied to VSS.)	—	—	I	—	VSS	J5	J5	—
TESTA0	Test Control Signal (This pin should be tied to VDD33.)	BD42	—	I	—	VDD33	—	K4	—
TESTA1	Test Control Signal (This pin should be tied to VDD33.)	BD42	—	I	—	VDD33	—	M4	—
TESTA2	Test Control Signal (This pin should be tied to VDD33.)	BD42	—	I	—	VDD33	—	T4	—
TESTA3	Test Control Signal (This pin should be tied to VDD33.)	BD42	—	I	—	VDD33	—	L4	—
TESTA4	Test Control Signal (Please do not connect anything to the user board.)	BD84	—	O	—	OPEN	—	N4	—
TESTA5	Test Control Signal (Please do not connect anything to the user board.)	BD84	—	O	—	OPEN	—	R4	—
TESTS0	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	B	PD	OPEN	AF16	AF16	—
TESTS1	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	B	PD	OPEN	AE16	AE16	—
TESTS2	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	B	PD	OPEN	AD16	AD16	—
TESTS3	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	B	PD	OPEN	AC16	AC16	—
TESTS4	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	O	—	OPEN	AC15	AC15	—
TESTS5	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	I	PD	OPEN	AD15	AD15	—
TESTS6	Test Control Signal (Please pull-down.)	BD84	LE-PD	B	—	PD	AE15	AE15	—
TESTS7	Test Control Signal (Please do not connect anything to the user board.)	BD84	LE-PD	I	PD	OPEN	AF15	AF15	—

2.1.12. Power Supply and Ground

Symbol	Function	Structure	Pin Position	
			7528 7506 7504	7502
DDR2C_PLL_AVDD11	DDRPHY Power Supply (1.1V)	A-POWER	F13	F8
DDR2C_PLL_AVSS	DDRPHY Ground	A-GND	F14	F9
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F6	E6
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F7	F6
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F8	F11
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F10	F12
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F11	F14
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F16	F15
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F17	F16
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F19	—
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F20	—
DDR2C_AVDD18	DDR2C Power Supply (1.8V)	A-POWER	F21	—
DDR2C_AVDD11	DDR2C Power Supply (1.1V)	A-POWER	E12	—
DDR2C_AVDD11	DDR2C Power Supply (1.1V)	A-POWER	F12	—
DDR2C_AVDD11	DDR2C Power Supply (1.1V)	A-POWER	E15	—
DDR2C_AVDD11	DDR2C Power Supply (1.1V)	A-POWER	F15	—
PCIE_AVDD11	PCIE Analog Power Supply (1.1V)	A-POWER	AA12	—
PCIE_AVDD11	PCIE Analog Power Supply (1.1V)	A-POWER	AB12	—
PCIE_AVDD11	PCIE Analog Power Supply (1.1V)	A-POWER	AC12	—
PCIE_AVDD11	PCIE Analog Power Supply (1.1V)	A-POWER	AD12	—
PCIE_AVDD18	PCIE Analog Power Supply (1.8V)	A-POWER	AA13	—
PCIE_AVDD18	PCIE Analog Power Supply (1.8V)	A-POWER	AB13	—
PCIE_AVSS	PCIE Ground	A-GND	AA11	—
PCIE_AVSS	PCIE Ground	A-GND	AB10	—
PCIE_AVSS	PCIE Ground	A-GND	AB11	—
PCIE_AVSS	PCIE Ground	A-GND	AC10	—
PCIE_AVSS	PCIE Ground	A-GND	AD9	—
PCIE_AVSS	PCIE Ground	A-GND	AD10	—
PCIE_AVSS	PCIE Ground	A-GND	AE9	—
PCIE_AVSS	PCIE Ground	A-GND	AE11	—
PCIE_AVSS	PCIE Ground	A-GND	AE13	—
PCIE_AVSS	PCIE Ground	A-GND	AF9	—
PCIE_AVSS	PCIE Ground	A-GND	AF11	—
PCIE_AVSS	PCIE Ground	A-GND	AF13	—
PLL1_AVDD11	PLL1 Power Supply (1.1V)	A-POWER	T2	L2
PLL2_AVDD11	PLL2 Power Supply (1.1V)	A-POWER	K2	H2
PLL3_AVDD11	PLL3 Power Supply (1.1V)	A-POWER	N2	F2
PLL1_AVSS	PLL1 Ground	A-GND	U2	M2
PLL2_AVSS	PLL2 Ground	A-GND	L2	K2
PLL3_AVSS	PLL3 Ground	A-GND	N1	G2
VDD11	System Power Supply (1.1V)	POWER	K5	E7
VDD11	System Power Supply (1.1V)	POWER	K6	E10
VDD11	System Power Supply (1.1V)	POWER	K21	F7
VDD11	System Power Supply (1.1V)	POWER	K22	F10
VDD11	System Power Supply (1.1V)	POWER	N5	G10

Symbol	Function	Structure	Pin Position	
			7528 7506 7504	7502
VDD11	System Power Supply (1.1V)	POWER	N6	J5
VDD11	System Power Supply (1.1V)	POWER	N21	J6
VDD11	System Power Supply (1.1V)	POWER	N22	J7
VDD11	System Power Supply (1.1V)	POWER	R5	J12
VDD11	System Power Supply (1.1V)	POWER	R6	J13
VDD11	System Power Supply (1.1V)	POWER	R21	J14
VDD11	System Power Supply (1.1V)	POWER	R22	L5
VDD11	System Power Supply (1.1V)	POWER	V6	L6
VDD11	System Power Supply (1.1V)	POWER	V21	L7
VDD11	System Power Supply (1.1V)	POWER	V22	L12
VDD11	System Power Supply (1.1V)	POWER	AA10	L13
VDD11	System Power Supply (1.1V)	POWER	AA15	L14
VDD11	System Power Supply (1.1V)	POWER	AA18	N10
VDD11	System Power Supply (1.1V)	POWER	AB15	P10
VDD11	System Power Supply (1.1V)	POWER	AB18	—
VDD11	System Power Supply (1.1V)	POWER	M5	—
VDD11	System Power Supply (1.1V)	POWER	M6	—
VDD11	System Power Supply (1.1V)	POWER	M21	—
VDD11	System Power Supply (1.1V)	POWER	M22	—
VDD33	System Power Supply (3.3V)	POWER	G5	H5
VDD33	System Power Supply (3.3V)	POWER	G22	H6
VDD33	System Power Supply (3.3V)	POWER	H5	H7
VDD33	System Power Supply (3.3V)	POWER	H6	H12
VDD33	System Power Supply (3.3V)	POWER	H21	H13
VDD33	System Power Supply (3.3V)	POWER	H22	H14
VDD33	System Power Supply (3.3V)	POWER	T5	N5
VDD33	System Power Supply (3.3V)	POWER	T6	N6
VDD33	System Power Supply (3.3V)	POWER	T21	N7
VDD33	System Power Supply (3.3V)	POWER	T22	N8
VDD33	System Power Supply (3.3V)	POWER	W6	N11
VDD33	System Power Supply (3.3V)	POWER	W21	N12
VDD33	System Power Supply (3.3V)	POWER	W22	N13
VDD33	System Power Supply (3.3V)	POWER	AA8	N14
VDD33	System Power Supply (3.3V)	POWER	AA16	P8
VDD33	System Power Supply (3.3V)	POWER	AA19	P11
VDD33	System Power Supply (3.3V)	POWER	AB16	—
VDD33	System Power Supply (3.3V)	POWER	AB19	—
VSS	System Ground	GND	A1	A1
VSS	System Ground	GND	A2	A2
VSS	System Ground	GND	A3	A4
VSS	System Ground	GND	A10	A8
VSS	System Ground	GND	A12	A11
VSS	System Ground	GND	A15	A14
VSS	System Ground	GND	A17	A18
VSS	System Ground	GND	A24	B1
VSS	System Ground	GND	A25	B4
VSS	System Ground	GND	A26	B9

Symbol	Function	Structure	Pin Position	
			7528 7506 7504	7502
VSS	System Ground	GND	B1	B12
VSS	System Ground	GND	B2	B13
VSS	System Ground	GND	B3	C4
VSS	System Ground	GND	B9	C8
VSS	System Ground	GND	B13	C9
VSS	System Ground	GND	B18	C13
VSS	System Ground	GND	B24	D5
VSS	System Ground	GND	B25	D7
VSS	System Ground	GND	B26	D10
VSS	System Ground	GND	C3	D13
VSS	System Ground	GND	C4	D15
VSS	System Ground	GND	C5	D18
VSS	System Ground	GND	C6	E5
VSS	System Ground	GND	C7	E11
VSS	System Ground	GND	C8	E12
VSS	System Ground	GND	C9	F1
VSS	System Ground	GND	C18	F5
VSS	System Ground	GND	C19	F13
VSS	System Ground	GND	C20	F17
VSS	System Ground	GND	C21	G5
VSS	System Ground	GND	C22	G6
VSS	System Ground	GND	C23	G7
VSS	System Ground	GND	C24	G8
VSS	System Ground	GND	D4	G9
VSS	System Ground	GND	D10	G11
VSS	System Ground	GND	D17	G12
VSS	System Ground	GND	D23	G13
VSS	System Ground	GND	E4	G14
VSS	System Ground	GND	E11	G18
VSS	System Ground	GND	E16	H8
VSS	System Ground	GND	E23	H9
VSS	System Ground	GND	F5	H10
VSS	System Ground	GND	F9	H11
VSS	System Ground	GND	F18	J1
VSS	System Ground	GND	F22	J2
VSS	System Ground	GND	G6	J3
VSS	System Ground	GND	G21	J4
VSS	System Ground	GND	J1	J8
VSS	System Ground	GND	J6	J9
VSS	System Ground	GND	J21	J10
VSS	System Ground	GND	J22	J11
VSS	System Ground	GND	L5	K5
VSS	System Ground	GND	L6	K6
VSS	System Ground	GND	L11	K7
VSS	System Ground	GND	L12	K8
VSS	System Ground	GND	L13	K9
VSS	System Ground	GND	L14	K10

Symbol	Function	Structure	Pin Position	
			7528 7506 7504	7502
VSS	System Ground	GND	L15	K11
VSS	System Ground	GND	L16	K12
VSS	System Ground	GND	L21	K13
VSS	System Ground	GND	L22	K14
VSS	System Ground	GND	M1	L8
VSS	System Ground	GND	M11	L9
VSS	System Ground	GND	M12	L10
VSS	System Ground	GND	M13	L11
VSS	System Ground	GND	M14	M1
VSS	System Ground	GND	M15	M5
VSS	System Ground	GND	M16	M6
VSS	System Ground	GND	N11	M7
VSS	System Ground	GND	N12	M8
VSS	System Ground	GND	N13	M9
VSS	System Ground	GND	N14	M10
VSS	System Ground	GND	N15	M11
VSS	System Ground	GND	N16	M12
VSS	System Ground	GND	P1	M13
VSS	System Ground	GND	P2	M14
VSS	System Ground	GND	P3	N9
VSS	System Ground	GND	P4	P5
VSS	System Ground	GND	P5	P6
VSS	System Ground	GND	P6	P7
VSS	System Ground	GND	P11	P9
VSS	System Ground	GND	P12	P12
VSS	System Ground	GND	P13	P13
VSS	System Ground	GND	P14	P14
VSS	System Ground	GND	P15	R4
VSS	System Ground	GND	P16	R15
VSS	System Ground	GND	P21	T3
VSS	System Ground	GND	P22	T16
VSS	System Ground	GND	P23	U1
VSS	System Ground	GND	P24	U2
VSS	System Ground	GND	P25	U17
VSS	System Ground	GND	P26	U18
VSS	System Ground	GND	R1	V1
VSS	System Ground	GND	R11	V2
VSS	System Ground	GND	R12	V17
VSS	System Ground	GND	R13	V18
VSS	System Ground	GND	R14	—
VSS	System Ground	GND	R15	—
VSS	System Ground	GND	R16	—
VSS	System Ground	GND	T11	—
VSS	System Ground	GND	T12	—
VSS	System Ground	GND	T13	—
VSS	System Ground	GND	T14	—
VSS	System Ground	GND	T15	—

Symbol	Function	Structure	Pin Position	
			7528 7506 7504	7502
VSS	System Ground	GND	T16	—
VSS	System Ground	GND	U5	—
VSS	System Ground	GND	U6	—
VSS	System Ground	GND	U21	—
VSS	System Ground	GND	U22	—
VSS	System Ground	GND	V1	—
VSS	System Ground	GND	Y6	—
VSS	System Ground	GND	Y21	—
VSS	System Ground	GND	Y22	—
VSS	System Ground	GND	AA6	—
VSS	System Ground	GND	AA7	—
VSS	System Ground	GND	AA9	—
VSS	System Ground	GND	AA14	—
VSS	System Ground	GND	AA17	—
VSS	System Ground	GND	AA20	—
VSS	System Ground	GND	AA21	—
VSS	System Ground	GND	AB5	—
VSS	System Ground	GND	AB9	—
VSS	System Ground	GND	AB14	—
VSS	System Ground	GND	AB17	—
VSS	System Ground	GND	AB22	—
VSS	System Ground	GND	AC4	—
VSS	System Ground	GND	AC14	—
VSS	System Ground	GND	AC23	—
VSS	System Ground	GND	AD3	—
VSS	System Ground	GND	AD14	—
VSS	System Ground	GND	AD24	—
VSS	System Ground	GND	AE1	—
VSS	System Ground	GND	AE2	—
VSS	System Ground	GND	AE14	—
VSS	System Ground	GND	AE25	—
VSS	System Ground	GND	AE26	—
VSS	System Ground	GND	AF1	—
VSS	System Ground	GND	AF2	—
VSS	System Ground	GND	AF14	—
VSS	System Ground	GND	AF25	—
VSS	System Ground	GND	AF26	—

2.2. Ball Assignment

2.2.1. TMPV7528XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VSS	VSS	DDR2C_DM0	DDR2C_DQ7	DDR2C_DQ0	DDR2C_DQ5	DDR2C_DQ2	DDR2C_DQ3	VSS	DDR2C_CKE	VSS	DDR2C_CKP	DDR2C_CKN	VSS	DDR2C_A8	VSS	DDR2C_DM3	DDR2C_DQ31	DDR2C_DQ30	DDR2C_DQ25	DDR2C_DQ29	DDR2C_DQ26	VSS	VSS	VSS	A
B	VSS	VSS	VSS	DDR2C_DQSN0	DDR2C_DQSP0	DDR2C_DQ6	DDR2C_DQ1	DDR2C_DQ4	VSS	DDR2C_RAS_N	DDR2C_ODT	DDR2C_BA0	VSS	DDR2C_A1	DDR2C_A4	DDR2C_A5	DDR2C_A12	VSS	DDR2C_DQSN3	DDR2C_DQSP3	DDR2C_DQ24	DDR2C_DQ28	DDR2C_DQ27	VSS	VSS	VSS	B
C	VOIF_HSYNC_N	VOIF_VSYNC_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR2C_CAS_N	DDR2C_CS_N	DDR2C_BA2	DDR2C_A10	DDR2C_A0	DDR2C_A11	DDR2C_A13	DDR2C_A9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VIIF_D46	VIIF_D47	C
D	VOIF_D2	VOIF_D1	VOIF_D0	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ12	VSS	DDR2C_WE_N	DDR2C_BA1	DDR2C_A2	DDR2C_A7	DDR2C_A3	DDR2C_A6	VSS	DDR2C_DQ23	DDR2C_DQ22	DDR2C_DQ17	DDR2C_DQ20	DDR2C_DQ19	VSS	VIIF_D43	VIIF_D44	VIIF_D45	D
E	VOIF_D5	VOIF_D4	VOIF_D3	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ8	DDR2C_DQ13	DDR2C_DQ10	DDR2C_DQ11	VSS	DDR2C_AVDD11	DDR2C_EXRES	DDR2C_VREF	DDR2C_AVDD11	VSS	DDR2C_DM2	DDR2C_DQSN2	DDR2C_DQSP2	DDR2C_DQ16	DDR2C_DQ21	DDR2C_DQ18	VSS	VIIF_D40	VIIF_D41	VIIF_D42	E
F	VOIF_D9	VOIF_D8	VOIF_D7	VOIF_D6	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD11	DDR2C_PLL_AVDD11	DDR2C_PLL_AVSS	DDR2C_AVDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	VIIF_D36	VIIF_D37	VIIF_D38	VIIF_D39	F
G	VOIF_D13	VOIF_D12	VOIF_D11	VOIF_D10	VDD33	VSS															VSS	VDD33	VIIF_VSYNC3	VIIF_HSYNC3	VIIF_FIELD3	VIIF_CK3	G
H	VOIF_D17	VOIF_D16	VOIF_D15	VOIF_D14	VDD33	VDD33															VDD33	VDD33	VIIF_VSYNC1	VIIF_HSYNC1	VIIF_FIELD1	VIIF_CK1	H
J	VSS	VOIF_D20	VOIF_D19	VOIF_D18	TESTV	VSS															VSS	VSS	VIIF_D32	VIIF_D33	VIIF_D34	VIIF_D35	J
K	XIN2	PLL2_AVDD11	VOIF_D21	ARM_TMS	VDD11	VDD11															VDD11	VDD11	VIIF_D28	VIIF_D29	VIIF_D30	VIIF_D31	K
L	XOUT2	PLL2_AVSS	VOIF_D22	ARM_SRST_N	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VIIF_D24	VIIF_D25	VIIF_D26	VIIF_D27	L
M	VSS	VOIF_DE	VOIF_D23	ARM_TDI	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D20	VIIF_D21	VIIF_D22	VIIF_D23	M
N	PLL3_AVSS	PLL3_AVDD11	VOIF_CK	ARM_TDO	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D16	VIIF_D17	VIIF_D18	VIIF_D19	N
P	VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS	P
R	VSS	GPIO8	GPIO9	ARM_RTCK	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D12	VIIF_D13	VIIF_D14	VIIF_D15	R
T	XIN1	PLL1_AVDD11	GPIO10	ARM_TCK	VDD33	VDD33					VSS	VSS	VSS	VSS	VSS	VSS					VDD33	VDD33	VIIF_VSYNC2	VIIF_HSYNC2	VIIF_FIELD2	VIIF_CK2	T
U	XOUT1	PLL1_AVSS	GPIO11	GPIO12	VSS	VSS															VSS	VSS	VIIF_VSYNC0	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	U
V	VSS	GPIO14	GPIO13	MEP_TMS	GPIO16	VDD11															VDD11	VDD11	VIIF_D8	VIIF_D9	VIIF_D10	VIIF_D11	V
W	CAN0_TX	CAN0_RX	GPIO15	MEP_TRST_N	GPIO17	VDD33															VDD33	VDD33	VIIF_D4	VIIF_D5	VIIF_D6	VIIF_D7	W
Y	CAN1_TX	CAN1_RX	GPIO0	MEP_TDI	GPIO18	VSS															VSS	VSS	VIIF_D0	VIIF_D1	VIIF_D2	VIIF_D3	Y
AA	CAN2_TX	CAN2_RX	GPIO1	MEP_TDO	GPIO19	VSS	VSS	VDD33	VSS	VDD11	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18	VSS	VDD11	VDD33	VSS	VDD11	VDD33	VSS	VSS	MEMC_CS1_N	MEMC_CS0_N	MEMC_OE_N	MEMC_WE_N	RESET_N	AA
AB	DBGUART_TXD	DBGUART_RXD	GPIO2	MEP_TCK	VSS	TEST2	TEST1	TEST0	VSS	PCIE_AVSS	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18	VSS	VDD11	VDD33	VSS	VDD11	VDD33	MEMC_D12	MEMC_A1	VSS	MEMC_A20	MEMC_A21	MEMC_A22	MEMC_A23	AB
AC	GPIO3	GPIO4	GPIO5	VSS	PCMIF_CKI	GPIO20	GPIO21	GPIO22	GPIO23	PCIE_AVSS	PCIE_CKREFP	PCIE_AVDD11	PCIE_RESET_N	VSS	TESTS4	TESTS3	MEMC_D0	MEMC_D4	MEMC_D8	MEMC_D13	MEMC_A2	MEMC_A6	VSS	MEMC_A17	MEMC_A18	MEMC_A19	AC
AD	GPIO6	GPIO7	VSS	PCMIF_CKO	MCUIF_D1	MCUIF_D6	MCUIF_WRDY_N	MCUIF_RE_N	PCIE_AVSS	PCIE_AVSS	PCIE_CKREFN	PCIE_AVDD11	PCIE_AMOUT	VSS	TESTS5	TESTS2	MEMC_D1	MEMC_D5	MEMC_D9	MEMC_D14	MEMC_A3	MEMC_A7	MEMC_A10	VSS	MEMC_A15	MEMC_A16	AD
AE	VSS	VSS	PCMIF_LRCKO	PCMIF_DO	MCUIF_D2	MCUIF_D7	MCUIF_D4	MCUIF_RRDY_N	PCIE_AVSS	PCIE_RXP	PCIE_AVSS	PCIE_TXP	PCIE_AVSS	VSS	TESTS6	TESTS1	MEMC_D2	MEMC_D6	MEMC_D10	MEMC_D15	MEMC_A4	MEMC_A8	MEMC_A11	MEMC_A13	VSS	VSS	AE
AF	VSS	VSS	PCMIF_BCKO	NMI_N	MCUIF_D3	MCUIF_D0	MCUIF_D5	MCUIF_WE_N	PCIE_AVSS	PCIE_RXN	PCIE_AVSS	PCIE_TXN	PCIE_AVSS	VSS	TESTS7	TESTS0	MEMC_D3	MEMC_D7	MEMC_D11	MEMC_A0	MEMC_A5	MEMC_A9	MEMC_A12	MEMC_A14	VSS	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-1 Ball Assignment of TMPV7528XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	VSS	VSS	DDR2C_DM0	DDR2C_DQ7	DDR2C_DQ0	DDR2C_DQ5	DDR2C_DQ2	DDR2C_DQ3	VSS	DDR2C_CKE	VSS	DDR2C_CKP
B	VSS	VSS	VSS	DDR2C_DQSN0	DDR2C_DQSP0	DDR2C_DQ6	DDR2C_DQ1	DDR2C_DQ4	VSS	DDR2C_RAS_N	DDR2C_ODT	DDR2C_BA0	VSS
C	VOIF_HSYNC_N	VOIF_VSYNC_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR2C_CAS_N	DDR2C_CS_N	DDR2C_BA2	DDR2C_A10
D	VOIF_D2	VOIF_D1	VOIF_D0	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ12	VSS	DDR2C_WE_N	DDR2C_BA1	DDR2C_A2
E	VOIF_D5	VOIF_D4	VOIF_D3	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ8	DDR2C_DQ13	DDR2C_DQ10	DDR2C_DQ11	VSS	DDR2C_AVDD11	DDR2C_EXRES
F	VOIF_D9	VOIF_D8	VOIF_D7	VOIF_D6	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD11	DDR2C_PLL_AVDD11
G	VOIF_D13	VOIF_D12	VOIF_D11	VOIF_D10	VDD33	VSS							
H	VOIF_D17	VOIF_D16	VOIF_D15	VOIF_D14	VDD33	VDD33							
J	VSS	VOIF_D20	VOIF_D19	VOIF_D18	TESTV	VSS							
K	XIN2	PLL2_AVDD11	VOIF_D21	ARM_TMS	VDD11	VDD11							
L	XOUT2	PLL2_AVSS	VOIF_D22	ARM_SRST_N	VSS	VSS					VSS	VSS	VSS
M	VSS	VOIF_DE	VOIF_D23	ARM_TDI	VDD11	VDD11					VSS	VSS	VSS
N	PLL3_AVSS	PLL3_AVDD11	VOIF_CK	ARM_TDO	VDD11	VDD11					VSS	VSS	VSS
P	VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS
R	VSS	GPIO8	GPIO9	ARM_RTCK	VDD11	VDD11					VSS	VSS	VSS
T	XIN1	PLL1_AVDD11	GPIO10	ARM_TCK	VDD33	VDD33					VSS	VSS	VSS
U	XOUT1	PLL1_AVSS	GPIO11	GPIO12	VSS	VSS							
V	VSS	GPIO14	GPIO13	MEP_TMS	GPIO16	VDD11							
W	CAN0_TX	CAN0_RX	GPIO15	MEP_TRST_N	GPIO17	VDD33							
Y	CAN1_TX	CAN1_RX	GPIO0	MEP_TDI	GPIO18	VSS							
AA	CAN2_TX	CAN2_RX	GPIO1	MEP_TDO	GPIO19	VSS	VSS	VDD33	VSS	VDD11	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18
AB	DBGUART_TXD	DBGUART_RXD	GPIO2	MEP_TCK	VSS	TEST2	TEST1	TEST0	VSS	PCIE_AVSS	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18
AC	GPIO3	GPIO4	GPIO5	VSS	PCMIF_CKI	GPIO20	GPIO21	GPIO22	GPIO23	PCIE_AVSS	PCIE_CKREFP	PCIE_AVDD11	PCIE_RESET_N
AD	GPIO6	GPIO7	VSS	PCMIF_CKO	MCUIF_D1	MCUIF_D6	MCUIF_WRDY_N	MCUIF_RE_N	PCIE_AVSS	PCIE_AVSS	PCIE_CKREFN	PCIE_AVDD11	PCIE_AMOUT
AE	VSS	VSS	PCMIF_LRCKO	PCMIF_DO	MCUIF_D2	MCUIF_D7	MCUIF_D4	MCUIF_RRDY_N	PCIE_AVSS	PCIE_RXP	PCIE_AVSS	PCIE_TXP	PCIE_AVSS
AF	VSS	VSS	PCMIF_BCKO	NMI_N	MCUIF_D3	MCUIF_D0	MCUIF_D5	MCUIF_WE_N	PCIE_AVSS	PCIE_RXN	PCIE_AVSS	PCIE_TXN	PCIE_AVSS

Figure 2-2 Ball Assignment of TMPV7528XBG (Column 1 to 13)

TOP VIEW

14	15	16	17	18	19	20	21	22	23	24	25	26	
DDR2C_CKN	VSS	DDR2C_A8	VSS	DDR2C_DM3	DDR2C_DQ31	DDR2C_DQ30	DDR2C_DQ25	DDR2C_DQ29	DDR2C_DQ26	VSS	VSS	VSS	A
DDR2C_A1	DDR2C_A4	DDR2C_A5	DDR2C_A12	VSS	DDR2C_DQSN3	DDR2C_DQSP3	DDR2C_DQ24	DDR2C_DQ28	DDR2C_DQ27	VSS	VSS	VSS	B
DDR2C_A0	DDR2C_A11	DDR2C_A13	DDR2C_A9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VIIF_D46	VIIF_D47	C
DDR2C_A7	DDR2C_A3	DDR2C_A6	VSS	DDR2C_DQ23	DDR2C_DQ22	DDR2C_DQ17	DDR2C_DQ20	DDR2C_DQ19	VSS	VIIF_D43	VIIF_D44	VIIF_D45	D
DDR2C_VREF	DDR2C_AVDD11	VSS	DDR2C_DM2	DDR2C_DQSN2	DDR2C_DQSP2	DDR2C_DQ16	DDR2C_DQ21	DDR2C_DQ18	VSS	VIIF_D40	VIIF_D41	VIIF_D42	E
DDR2C_PLL_AVSS	DDR2C_AVDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	VIIF_D36	VIIF_D37	VIIF_D38	VIIF_D39	F
							VSS	VDD33	VIIF_VSYNC3	VIIF_HSYNC3	VIIF_FIELD3	VIIF_CK3	G
							VDD33	VDD33	VIIF_VSYNC1	VIIF_HSYNC1	VIIF_FIELD1	VIIF_CK1	H
							VSS	VSS	VIIF_D32	VIIF_D33	VIIF_D34	VIIF_D35	J
							VDD11	VDD11	VIIF_D28	VIIF_D29	VIIF_D30	VIIF_D31	K
VSS	VSS	VSS					VSS	VSS	VIIF_D24	VIIF_D25	VIIF_D26	VIIF_D27	L
VSS	VSS	VSS					VDD11	VDD11	VIIF_D20	VIIF_D21	VIIF_D22	VIIF_D23	M
VSS	VSS	VSS					VDD11	VDD11	VIIF_D16	VIIF_D17	VIIF_D18	VIIF_D19	N
VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS	P
VSS	VSS	VSS					VDD11	VDD11	VIIF_D12	VIIF_D13	VIIF_D14	VIIF_D15	R
VSS	VSS	VSS					VDD33	VDD33	VIIF_VSYNC2	VIIF_HSYNC2	VIIF_FIELD2	VIIF_CK2	T
							VSS	VSS	VIIF_VSYNC0	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	U
							VDD11	VDD11	VIIF_D8	VIIF_D9	VIIF_D10	VIIF_D11	V
							VDD33	VDD33	VIIF_D4	VIIF_D5	VIIF_D6	VIIF_D7	W
							VSS	VSS	VIIF_D0	VIIF_D1	VIIF_D2	VIIF_D3	Y
VSS	VDD11	VDD33	VSS	VDD11	VDD33	VSS	VSS	MEMC_CS1_N	MEMC_CS0_N	MEMC_OE_N	MEMC_WE_N	RESET_N	AA
VSS	VDD11	VDD33	VSS	VDD11	VDD33	MEMC_D12	MEMC_A1	VSS	MEMC_A20	MEMC_A21	MEMC_A22	MEMC_A23	AB
VSS	TESTS4	TESTS3	MEMC_D0	MEMC_D4	MEMC_D8	MEMC_D13	MEMC_A2	MEMC_A6	VSS	MEMC_A17	MEMC_A18	MEMC_A19	AC
VSS	TESTS5	TESTS2	MEMC_D1	MEMC_D5	MEMC_D9	MEMC_D14	MEMC_A3	MEMC_A7	MEMC_A10	VSS	MEMC_A15	MEMC_A16	AD
VSS	TESTS6	TESTS1	MEMC_D2	MEMC_D6	MEMC_D10	MEMC_D15	MEMC_A4	MEMC_A8	MEMC_A11	MEMC_A13	VSS	VSS	AE
VSS	TESTS7	TESTS0	MEMC_D3	MEMC_D7	MEMC_D11	MEMC_A0	MEMC_A5	MEMC_A9	MEMC_A12	MEMC_A14	VSS	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-3 Ball Assignment of TMPV7528XBG (Column 14 to 26)

2.2.2. TMPV7506XBG and TMPV7504XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VSS	VSS	DDR2C_DM0	DDR2C_DQ7	DDR2C_DQ0	DDR2C_DQ5	DDR2C_DQ2	DDR2C_DQ3	VSS	DDR2C_CKE	VSS	DDR2C_CKP	DDR2C_CKN	VSS	DDR2C_A8	VSS	DDR2C_DM3	DDR2C_DQ31	DDR2C_DQ30	DDR2C_DQ25	DDR2C_DQ29	DDR2C_DQ26	VSS	VSS	VSS	A
B	VSS	VSS	VSS	DDR2C_DQSN0	DDR2C_DQSP0	DDR2C_DQ6	DDR2C_DQ1	DDR2C_DQ4	VSS	DDR2C_RAS_N	DDR2C_ODT	DDR2C_BA0	VSS	DDR2C_A1	DDR2C_A4	DDR2C_A5	DDR2C_A12	VSS	DDR2C_DQSN3	DDR2C_DQSP3	DDR2C_DQ24	DDR2C_DQ28	DDR2C_DQ27	VSS	VSS	VSS	B
C	VOIF_HSYNC_N	VOIF_VSYNC_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR2C_CAS_N	DDR2C_CS_N	DDR2C_BA2	DDR2C_A10	DDR2C_A0	DDR2C_A11	DDR2C_A13	DDR2C_A9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VIIF_D46	VIIF_D47	C
D	VOIF_D2	VOIF_D1	VOIF_D0	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ12	VSS	DDR2C_WE_N	DDR2C_BA1	DDR2C_A2	DDR2C_A7	DDR2C_A3	DDR2C_A6	VSS	DDR2C_DQ23	DDR2C_DQ22	DDR2C_DQ17	DDR2C_DQ20	DDR2C_DQ19	VSS	VIIF_D43	VIIF_D44	VIIF_D45	D
E	VOIF_D5	VOIF_D4	VOIF_D3	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ8	DDR2C_DQ13	DDR2C_DQ10	DDR2C_DQ11	VSS	DDR2C_AVDD11	DDR2C_EXRES	DDR2C_VREF	DDR2C_AVDD11	VSS	DDR2C_DM2	DDR2C_DQSN2	DDR2C_DQSP2	DDR2C_DQ16	DDR2C_DQ21	DDR2C_DQ18	VSS	VIIF_D40	VIIF_D41	VIIF_D42	E
F	VOIF_D9	VOIF_D8	VOIF_D7	VOIF_D6	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD11	DDR2C_PLL_AVDD11	DDR2C_PLL_AVSS	DDR2C_AVDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	VIIF_D36	VIIF_D37	VIIF_D38	VIIF_D39	F
G	VOIF_D13	VOIF_D12	VOIF_D11	VOIF_D10	VDD33	VSS															VSS	VDD33	VIIF_VSYNC3	VIIF_HSYNC3	VIIF_FIELD3	VIIF_CK3	G
H	VOIF_D17	VOIF_D16	VOIF_D15	VOIF_D14	VDD33	VDD33															VDD33	VDD33	VIIF_VSYNC1	VIIF_HSYNC1	VIIF_FIELD1	VIIF_CK1	H
J	VSS	VOIF_D20	VOIF_D19	VOIF_D18	TESTV	VSS															VSS	VSS	VIIF_D32	VIIF_D33	VIIF_D34	VIIF_D35	J
K	XIN2	PLL2_AVDD11	VOIF_D21	TESTA0	VDD11	VDD11															VDD11	VDD11	VIIF_D28	VIIF_D29	VIIF_D30	VIIF_D31	K
L	XOUT2	PLL2_AVSS	VOIF_D22	TESTA3	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VIIF_D24	VIIF_D25	VIIF_D26	VIIF_D27	L
M	VSS	VOIF_DE	VOIF_D23	TESTA1	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D20	VIIF_D21	VIIF_D22	VIIF_D23	M
N	PLL3_AVSS	PLL3_AVDD11	VOIF_CK	TESTA4	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D16	VIIF_D17	VIIF_D18	VIIF_D19	N
P	VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS	P
R	VSS	GPIO8	GPIO9	TESTA5	VDD11	VDD11					VSS	VSS	VSS	VSS	VSS	VSS					VDD11	VDD11	VIIF_D12	VIIF_D13	VIIF_D14	VIIF_D15	R
T	XIN1	PLL1_AVDD11	GPIO10	TESTA2	VDD33	VDD33					VSS	VSS	VSS	VSS	VSS	VSS					VDD33	VDD33	VIIF_VSYNC2	VIIF_HSYNC2	VIIF_FIELD2	VIIF_CK2	T
U	XOUT1	PLL1_AVSS	GPIO11	GPIO12	VSS	VSS															VSS	VSS	VIIF_VSYNC0	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	U
V	VSS	GPIO14	GPIO13	MEP_TMS	GPIO16	VDD11															VDD11	VDD11	VIIF_D8	VIIF_D9	VIIF_D10	VIIF_D11	V
W	CAN0_TX	CAN0_RX	GPIO15	MEP_TRST_N	GPIO17	VDD33															VDD33	VDD33	VIIF_D4	VIIF_D5	VIIF_D6	VIIF_D7	W
Y	CAN1_TX	CAN1_RX	GPIO0	MEP_TDI	GPIO18	VSS															VSS	VSS	VIIF_D0	VIIF_D1	VIIF_D2	VIIF_D3	Y
AA	CAN2_TX	CAN2_RX	GPIO1	MEP_TDO	GPIO19	VSS	VSS	VDD33	VSS	VDD11	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18	VSS	VDD11	VDD33	VSS	VDD11	VDD33	VSS	VSS	MEMC_CS1_N	MEMC_CS0_N	MEMC_OE_N	MEMC_WE_N	RESET_N	AA
AB	DBGUART_TXD	DBGUART_RXD	GPIO2	MEP_TCK	VSS	TEST2	TEST1	TEST0	VSS	PCIE_AVSS	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18	VSS	VDD11	VDD33	VSS	VDD11	VDD33	MEMC_D12	MEMC_A1	VSS	MEMC_A20	MEMC_A21	MEMC_A22	MEMC_A23	AB
AC	GPIO3	GPIO4	GPIO5	VSS	PCMIF_CKI	GPIO20	GPIO21	GPIO22	GPIO23	PCIE_AVSS	PCIE_CKREFP	PCIE_AVDD11	PCIE_RESET_N	VSS	TESTS4	TESTS3	MEMC_D0	MEMC_D4	MEMC_D8	MEMC_D13	MEMC_A2	MEMC_A6	VSS	MEMC_A17	MEMC_A18	MEMC_A19	AC
AD	GPIO6	GPIO7	VSS	PCMIF_CKO	MCUIF_D1	MCUIF_D6	MCUIF_WRDY_N	MCUIF_RE_N	PCIE_AVSS	PCIE_AVSS	PCIE_CKREFN	PCIE_AVDD11	PCIE_AMOUT	VSS	TESTS5	TESTS2	MEMC_D1	MEMC_D5	MEMC_D9	MEMC_D14	MEMC_A3	MEMC_A7	MEMC_A10	VSS	MEMC_A15	MEMC_A16	AD
AE	VSS	VSS	PCMIF_LRCKO	PCMIF_DO	MCUIF_D2	MCUIF_D7	MCUIF_D4	MCUIF_RRDY_N	PCIE_AVSS	PCIE_RXP	PCIE_AVSS	PCIE_TXP	PCIE_AVSS	VSS	TESTS6	TESTS1	MEMC_D2	MEMC_D6	MEMC_D10	MEMC_D15	MEMC_A4	MEMC_A8	MEMC_A11	MEMC_A13	VSS	VSS	AE
AF	VSS	VSS	PCMIF_BCKO	NMI_N	MCUIF_D3	MCUIF_D0	MCUIF_D5	MCUIF_WE_N	PCIE_AVSS	PCIE_RXN	PCIE_AVSS	PCIE_TXN	PCIE_AVSS	VSS	TESTS7	TESTS0	MEMC_D3	MEMC_D7	MEMC_D11	MEMC_A0	MEMC_A5	MEMC_A9	MEMC_A12	MEMC_A14	VSS	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-4 Ball Assignment of TMPV7506XBG and TMPV7504XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	VSS	VSS	DDR2C_DM0	DDR2C_DQ7	DDR2C_DQ0	DDR2C_DQ5	DDR2C_DQ2	DDR2C_DQ3	VSS	DDR2C_CKE	VSS	DDR2C_CKP
B	VSS	VSS	VSS	DDR2C_DQSN0	DDR2C_DQSP0	DDR2C_DQ6	DDR2C_DQ1	DDR2C_DQ4	VSS	DDR2C_RAS_N	DDR2C_ODT	DDR2C_BA0	VSS
C	VOIF_HSYNC_N	VOIF_VSYNC_N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDR2C_CAS_N	DDR2C_CS_N	DDR2C_BA2	DDR2C_A10
D	VOIF_D2	VOIF_D1	VOIF_D0	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ12	VSS	DDR2C_WE_N	DDR2C_BA1	DDR2C_A2
E	VOIF_D5	VOIF_D4	VOIF_D3	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ8	DDR2C_DQ13	DDR2C_DQ10	DDR2C_DQ11	VSS	DDR2C_AVDD11	DDR2C_EXRES
F	VOIF_D9	VOIF_D8	VOIF_D7	VOIF_D6	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD11	DDR2C_PLL_AVDD11
G	VOIF_D13	VOIF_D12	VOIF_D11	VOIF_D10	VDD33	VSS							
H	VOIF_D17	VOIF_D16	VOIF_D15	VOIF_D14	VDD33	VDD33							
J	VSS	VOIF_D20	VOIF_D19	VOIF_D18	TESTV	VSS							
K	XIN2	PLL2_AVDD11	VOIF_D21	TESTA0	VDD11	VDD11							
L	XOUT2	PLL2_AVSS	VOIF_D22	TESTA3	VSS	VSS					VSS	VSS	VSS
M	VSS	VOIF_DE	VOIF_D23	TESTA1	VDD11	VDD11					VSS	VSS	VSS
N	PLL3_AVSS	PLL3_AVDD11	VOIF_CK	TESTA4	VDD11	VDD11					VSS	VSS	VSS
P	VSS	VSS	VSS	VSS	VSS	VSS					VSS	VSS	VSS
R	VSS	GPIO8	GPIO9	TESTA5	VDD11	VDD11					VSS	VSS	VSS
T	XIN1	PLL1_AVDD11	GPIO10	TESTA2	VDD33	VDD33					VSS	VSS	VSS
U	XOUT1	PLL1_AVSS	GPIO11	GPIO12	VSS	VSS							
V	VSS	GPIO14	GPIO13	MEP_TMS	GPIO16	VDD11							
W	CAN0_TX	CAN0_RX	GPIO15	MEP_TRST_N	GPIO17	VDD33							
Y	CAN1_TX	CAN1_RX	GPIO0	MEP_TDI	GPIO18	VSS							
AA	CAN2_TX	CAN2_RX	GPIO1	MEP_TDO	GPIO19	VSS	VSS	VDD33	VSS	VDD11	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18
AB	DBGUART_TXD	DBGUART_RXD	GPIO2	MEP_TCK	VSS	TEST2	TEST1	TEST0	VSS	PCIE_AVSS	PCIE_AVSS	PCIE_AVDD11	PCIE_AVDD18
AC	GPIO3	GPIO4	GPIO5	VSS	PCMIF_CKI	GPIO20	GPIO21	GPIO22	GPIO23	PCIE_AVSS	PCIE_CKREFP	PCIE_AVDD11	PCIE_RESET_N
AD	GPIO6	GPIO7	VSS	PCMIF_CKO	MCUIF_D1	MCUIF_D6	MCUIF_WRDY_N	MCUIF_RE_N	PCIE_AVSS	PCIE_AVSS	PCIE_CKREFN	PCIE_AVDD11	PCIE_AMOUT
AE	VSS	VSS	PCMIF_LRCKO	PCMIF_DO	MCUIF_D2	MCUIF_D7	MCUIF_D4	MCUIF_RRDY_N	PCIE_AVSS	PCIE_RXP	PCIE_AVSS	PCIE_TXP	PCIE_AVSS
AF	VSS	VSS	PCMIF_BCKO	NMI_N	MCUIF_D3	MCUIF_D0	MCUIF_D5	MCUIF_WE_N	PCIE_AVSS	PCIE_RXN	PCIE_AVSS	PCIE_TXN	PCIE_AVSS
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 2-5 Ball Assignment of TMPV7506XBG and TMPV7504XBG (Column 1 to 13)

TOP VIEW

14	15	16	17	18	19	20	21	22	23	24	25	26	
DDR2C_CKN	VSS	DDR2C_A8	VSS	DDR2C_DM3	DDR2C_DQ31	DDR2C_DQ30	DDR2C_DQ25	DDR2C_DQ29	DDR2C_DQ26	VSS	VSS	VSS	A
DDR2C_A1	DDR2C_A4	DDR2C_A5	DDR2C_A12	VSS	DDR2C_DQSN3	DDR2C_DQSP3	DDR2C_DQ24	DDR2C_DQ28	DDR2C_DQ27	VSS	VSS	VSS	B
DDR2C_A0	DDR2C_A11	DDR2C_A13	DDR2C_A9	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VIIF_D46	VIIF_D47	C
DDR2C_A7	DDR2C_A3	DDR2C_A6	VSS	DDR2C_DQ23	DDR2C_DQ22	DDR2C_DQ17	DDR2C_DQ20	DDR2C_DQ19	VSS	VIIF_D43	VIIF_D44	VIIF_D45	D
DDR2C_VREF	DDR2C_AVDD11	VSS	DDR2C_DM2	DDR2C_DQSN2	DDR2C_DQSP2	DDR2C_DQ16	DDR2C_DQ21	DDR2C_DQ18	VSS	VIIF_D40	VIIF_D41	VIIF_D42	E
DDR2C_PLL_AVSS	DDR2C_AVDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	VIIF_D36	VIIF_D37	VIIF_D38	VIIF_D39	F
							VSS	VDD33	VIIF_VSYNC3	VIIF_HSYNC3	VIIF_FIELD3	VIIF_CK3	G
							VDD33	VDD33	VIIF_VSYNC1	VIIF_HSYNC1	VIIF_FIELD1	VIIF_CK1	H
							VSS	VSS	VIIF_D32	VIIF_D33	VIIF_D34	VIIF_D35	J
							VDD11	VDD11	VIIF_D28	VIIF_D29	VIIF_D30	VIIF_D31	K
VSS	VSS	VSS					VSS	VSS	VIIF_D24	VIIF_D25	VIIF_D26	VIIF_D27	L
VSS	VSS	VSS					VDD11	VDD11	VIIF_D20	VIIF_D21	VIIF_D22	VIIF_D23	M
VSS	VSS	VSS					VDD11	VDD11	VIIF_D16	VIIF_D17	VIIF_D18	VIIF_D19	N
VSS	VSS	VSS					VSS	VSS	VSS	VSS	VSS	VSS	P
VSS	VSS	VSS					VDD11	VDD11	VIIF_D12	VIIF_D13	VIIF_D14	VIIF_D15	R
VSS	VSS	VSS					VDD33	VDD33	VIIF_VSYNC2	VIIF_HSYNC2	VIIF_FIELD2	VIIF_CK2	T
							VSS	VSS	VIIF_VSYNC0	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	U
							VDD11	VDD11	VIIF_D8	VIIF_D9	VIIF_D10	VIIF_D11	V
							VDD33	VDD33	VIIF_D4	VIIF_D5	VIIF_D6	VIIF_D7	W
							VSS	VSS	VIIF_D0	VIIF_D1	VIIF_D2	VIIF_D3	Y
VSS	VDD11	VDD33	VSS	VDD11	VDD33	VSS	VSS	MEMC_CS1_N	MEMC_CS0_N	MEMC_OE_N	MEMC_WE_N	RESET_N	AA
VSS	VDD11	VDD33	VSS	VDD11	VDD33	MEMC_D12	MEMC_A1	VSS	MEMC_A20	MEMC_A21	MEMC_A22	MEMC_A23	AB
VSS	TESTS4	TESTS3	MEMC_D0	MEMC_D4	MEMC_D8	MEMC_D13	MEMC_A2	MEMC_A6	VSS	MEMC_A17	MEMC_A18	MEMC_A19	AC
VSS	TESTS5	TESTS2	MEMC_D1	MEMC_D5	MEMC_D9	MEMC_D14	MEMC_A3	MEMC_A7	MEMC_A10	VSS	MEMC_A15	MEMC_A16	AD
VSS	TESTS6	TESTS1	MEMC_D2	MEMC_D6	MEMC_D10	MEMC_D15	MEMC_A4	MEMC_A8	MEMC_A11	MEMC_A13	VSS	VSS	AE
VSS	TESTS7	TESTS0	MEMC_D3	MEMC_D7	MEMC_D11	MEMC_A0	MEMC_A5	MEMC_A9	MEMC_A12	MEMC_A14	VSS	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-6 Ball Assignment of TMPV7506XBG and TMPV7504XBG (Column 14 to 26)

2.2.3. TMPV7502XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	VSS	VSS	VOIF_VSYNC_N	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ13	VSS	DDR2C_DQ7	DDR2C_DQ5	VSS	DDR2C_CKP	DDR2C_CKN	VSS	DDR2C_BA2	DDR2C_A0	DDR2C_A4	VSS	A
B	VSS	VOIF_D0	VOIF_HSYNC_N	VSS	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ8	DDR2C_DQ10	VSS	DDR2C_DQ0	DDR2C_DQ2	VSS	VSS	DDR2C_RAS_N	DDR2C_BA0	DDR2C_A10	DDR2C_A13	DDR2C_A7	B
C	VOIF_D3	VOIF_D2	VOIF_D1	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ11	VSS	VSS	DDR2C_DM0	DDR2C_DQ6	DDR2C_DQ4	VSS	DDR2C_BA1	DDR2C_A2	DDR2C_A3	DDR2C_A9	DDR2C_A5	C
D	VOIF_D7	VOIF_D6	VOIF_D5	VOIF_D4	VSS	DDR2C_DQ12	VSS	DDR2C_DQSN0	DDR2C_DQSP0	VSS	DDR2C_DQ1	DDR2C_DQ3	VSS	DDR2C_WE_N	VSS	DDR2C_A1	DDR2C_A6	VSS	D
E	VOIF_D11	VOIF_D10	VOIF_D9	VOIF_D8	VSS	DDR2C_AVDD18	VDD11	DDR2C_EXRES	DDR2C_VREF	VDD11	VSS	VSS	DDR2C_CKE	DDR2C_ODT	DDR2C_CS_N	DDR2C_CAS_N	DDR2C_A11	DDR2C_A8	E
F	VSS	PLL3_AVDD11	VOIF_D13	VOIF_D12	VSS	DDR2C_AVDD18	VDD11	DDR2C_PLL_AVDD11	DDR2C_PLL_AVSS	VDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_A12	F
G	XIN2	PLL3_AVSS	VOIF_D15	VOIF_D14	VSS	VSS	VSS	VSS	VSS	VDD11	VSS	VSS	VSS	VSS	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	VSS	G
H	XOUT2	PLL2_AVDD11	VOIF_D17	VOIF_D16	VDD33	VDD33	VDD33	VSS	VSS	VSS	VSS	VDD33	VDD33	VDD33	VIIF_D9	VIIF_D10	VIIF_D11	VIIF_VSYNC0	H
J	VSS	VSS	VSS	VSS	VDD11	VDD11	VDD11	VSS	VSS	VSS	VSS	VDD11	VDD11	VDD11	VIIF_D5	VIIF_D6	VIIF_D7	VIIF_D8	J
K	XIN1	PLL2_AVSS	VOIF_D19	VOIF_D18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VIIF_D1	VIIF_D2	VIIF_D3	VIIF_D4	K
L	XOUT1	PLL1_AVDD11	VOIF_D21	VOIF_D20	VDD11	VDD11	VDD11	VSS	VSS	VSS	VSS	VDD11	VDD11	VDD11	MEMC_CS0_N	MEMC_CS1_N	RESET_N	VIIF_D0	L
M	VSS	PLL1_AVSS	VOIF_D23	VOIF_D22	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MEMC_A22	MEMC_A23	MEMC_WE_N	MEMC_OE_N	M
N	VOIF_CK	VOIF_DE	GPIO9	GPIO8	VDD33	VDD33	VDD33	VDD33	VSS	VDD11	VDD33	VDD33	VDD33	VDD33	MEMC_A18	MEMC_A19	MEMC_A20	MEMC_A21	N
P	GPIO13	GPIO12	GPIO11	GPIO10	VSS	VSS	VSS	VDD33	VSS	VDD11	VDD33	VSS	VSS	VSS	MEMC_A14	MEMC_A15	MEMC_A16	MEMC_A17	P
R	GPIO15	GPIO14	MEP_TMS	VSS	MEP_TDI	MEP_TDO	MEP_TCK	PCMIF_CK1	TEST2	TEST1	TEST0	MEMC_D8	MEMC_D12	MEMC_A0	VSS	MEMC_A11	MEMC_A12	MEMC_A13	R
T	CAN0_TX	CAN0_RX	VSS	MEP_TRST_N	GPIO0	GPIO3	PCMIF_BCKO	PCMIF_CK0	MEMC_D0	MEMC_D2	MEMC_D5	MEMC_D9	MEMC_D13	MEMC_A1	MEMC_A4	VSS	MEMC_A9	MEMC_A10	T
U	VSS	VSS	CAN1_RX	DBGUART_RXD	GPIO1	GPIO4	GPIO6	PCMIF_DO	MEMC_D1	MEMC_D3	MEMC_D6	MEMC_D10	MEMC_D14	MEMC_A2	MEMC_A5	MEMC_A7	VSS	VSS	U
V	VSS	VSS	CAN1_TX	DBGUART_TXD	GPIO2	GPIO5	GPIO7	PCMIF_LRCKO	NMI_N	MEMC_D4	MEMC_D7	MEMC_D11	MEMC_D15	MEMC_A3	MEMC_A6	MEMC_A8	VSS	VSS	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 2-7 Ball Assignment of TMPV7502XBG

TOP VIEW

	1	2	3	4	5	6	7	8	9
A	VSS	VSS	VOIF_VSYNC_N	VSS	DDR2C_DM1	DDR2C_DQ15	DDR2C_DQ13	VSS	DDR2C_DQ7
B	VSS	VOIF_D0	VOIF_HSYNC_N	VSS	DDR2C_DQ14	DDR2C_DQ9	DDR2C_DQ8	DDR2C_DQ10	VSS
C	VOIF_D3	VOIF_D2	VOIF_D1	VSS	DDR2C_DQSN1	DDR2C_DQSP1	DDR2C_DQ11	VSS	VSS
D	VOIF_D7	VOIF_D6	VOIF_D5	VOIF_D4	VSS	DDR2C_DQ12	VSS	DDR2C_DQSN0	DDR2C_DQSP0
E	VOIF_D11	VOIF_D10	VOIF_D9	VOIF_D8	VSS	DDR2C_AVDD18	VDD11	DDR2C_EXRES	DDR2C_VREF
F	VSS	PLL3_AVDD11	VOIF_D13	VOIF_D12	VSS	DDR2C_AVDD18	VDD11	DDR2C_PLL_AVDD11	DDR2C_PLL_AVSS
G	XIN2	PLL3_AVSS	VOIF_D15	VOIF_D14	VSS	VSS	VSS	VSS	VSS
H	XOUT2	PLL2_AVDD11	VOIF_D17	VOIF_D16	VDD33	VDD33	VDD33	VSS	VSS
J	VSS	VSS	VSS	VSS	VDD11	VDD11	VDD11	VSS	VSS
K	XIN1	PLL2_AVSS	VOIF_D19	VOIF_D18	VSS	VSS	VSS	VSS	VSS
L	XOUT1	PLL1_AVDD11	VOIF_D21	VOIF_D20	VDD11	VDD11	VDD11	VSS	VSS
M	VSS	PLL1_AVSS	VOIF_D23	VOIF_D22	VSS	VSS	VSS	VSS	VSS
N	VOIF_CK	VOIF_DE	GPIO9	GPIO8	VDD33	VDD33	VDD33	VDD33	VSS
P	GPIO13	GPIO12	GPIO11	GPIO10	VSS	VSS	VSS	VDD33	VSS
R	GPIO15	GPIO14	MEP_TMS	VSS	MEP_TDI	MEP_TDO	MEP_TCK	PCMIF_CK1	TEST2
T	CAN0_TX	CAN0_RX	VSS	MEP_TRST_N	GPIO0	GPIO3	PCMIF_BCKO	PCMIF_CK0	MEMC_D0
U	VSS	VSS	CAN1_RX	DBGUART_RXD	GPIO1	GPIO4	GPIO6	PCMIF_DO	MEMC_D1
V	VSS	VSS	CAN1_TX	DBGUART_TXD	GPIO2	GPIO5	GPIO7	PCMIF_LRCKO	NMI_N

Figure 2-8 Ball Assignment of TMPV7502XBG (Column 1 to 9)

TOP VIEW

10	11	12	13	14	15	16	17	18	
DDR2C_DQ5	VSS	DDR2C_CKP	DDR2C_CKN	VSS	DDR2C_BA2	DDR2C_A0	DDR2C_A4	VSS	A
DDR2C_DQ0	DDR2C_DQ2	VSS	VSS	DDR2C_RAS_N	DDR2C_BA0	DDR2C_A10	DDR2C_A13	DDR2C_A7	B
DDR2C_DM0	DDR2C_DQ6	DDR2C_DQ4	VSS	DDR2C_BA1	DDR2C_A2	DDR2C_A3	DDR2C_A9	DDR2C_A5	C
VSS	DDR2C_DQ1	DDR2C_DQ3	VSS	DDR2C_WE_N	VSS	DDR2C_A1	DDR2C_A6	VSS	D
VDD11	VSS	VSS	DDR2C_CKE	DDR2C_ODT	DDR2C_CS_N	DDR2C_CAS_N	DDR2C_A11	DDR2C_A8	E
VDD11	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_AVDD18	DDR2C_AVDD18	DDR2C_AVDD18	VSS	DDR2C_A12	F
VDD11	VSS	VSS	VSS	VSS	VIIF_HSYNC0	VIIF_FIELD0	VIIF_CK0	VSS	G
VSS	VSS	VDD33	VDD33	VDD33	VIIF_D9	VIIF_D10	VIIF_D11	VIIF_VSYNC0	H
VSS	VSS	VDD11	VDD11	VDD11	VIIF_D5	VIIF_D6	VIIF_D7	VIIF_D8	J
VSS	VSS	VSS	VSS	VSS	VIIF_D1	VIIF_D2	VIIF_D3	VIIF_D4	K
VSS	VSS	VDD11	VDD11	VDD11	MEMC_CS0_N	MEMC_CS1_N	RESET_N	VIIF_D0	L
VSS	VSS	VSS	VSS	VSS	MEMC_A22	MEMC_A23	MEMC_WE_N	MEMC_OE_N	M
VDD11	VDD33	VDD33	VDD33	VDD33	MEMC_A18	MEMC_A19	MEMC_A20	MEMC_A21	N
VDD11	VDD33	VSS	VSS	VSS	MEMC_A14	MEMC_A15	MEMC_A16	MEMC_A17	P
TEST1	TEST0	MEMC_D8	MEMC_D12	MEMC_A0	VSS	MEMC_A11	MEMC_A12	MEMC_A13	R
MEMC_D2	MEMC_D5	MEMC_D9	MEMC_D13	MEMC_A1	MEMC_A4	VSS	MEMC_A9	MEMC_A10	T
MEMC_D3	MEMC_D6	MEMC_D10	MEMC_D14	MEMC_A2	MEMC_A5	MEMC_A7	VSS	VSS	U
MEMC_D4	MEMC_D7	MEMC_D11	MEMC_D15	MEMC_A3	MEMC_A6	MEMC_A8	VSS	VSS	V
10	11	12	13	14	15	16	17	18	

Figure 2-9 Ball Assignment of TMPV7502XBG (Column 10 to 18)

2.3. Shared Pins

2.3.1. General Purpose I/O Pins

General purpose I/O pins (GPIO[23:0]) share pins with the following functions. In addition, GPIO[23:16] are also shared ARM trace pin (refer to “2.3.2. ARM Trace Pins”).

- PCM Interface (PCMIF)
  - PCMIF_LRCKI
  - PCMIF_BCKI
  - PCMIF_DI
- SPI Interface (SPI0-3)
  - SPI0_SCK, SPI1_SCK, SPI2_SCK, SPI3_SCK
  - SPI0_SDI, SPI1_SDI, SPI2_SDI, SPI3_SDI
  - SPI0_SDO, SPI1_SDO, SPI2_SDO, SPI3_SDO
  - SPI0_SCS_N, SPI1_SCS_N, SPI2_SCS_N, SPI3_SCS_N
- I2C Interface (I2C0-3)
  - I2C0_SCL, I2C1_SCL, I2C2_SCL, I2C3_SCL
  - I2C0_SDA, I2C1_SDA, I2C2_SDA, I2C3_SDA
- UART Interface (UART0-3)
  - Without flow control
    - UART0_RXD, UART1_RXD, UART2_RXD, UART3_RXD
    - UART0_TXD, UART1_TXD, UART2_TXD, UART3_TXD
  - With flow control
    - UART0_RXD, UART1_RXD, UART2_RXD, UART3_RXD
    - UART0_TXD, UART1_TXD, UART2_TXD, UART3_TXD
    - UART0_CTS, UART1_CTS, UART2_CTS, UART3_CTS
    - UART0_RTS, UART1_RTS, UART2_RTS, UART3_RTS
- Timer module (TIMER)
  - TIMER_GTI0, TIMER_GTI1, TIMER_GTI2, TIMER_GTI3
  - TIMER_GTO0, TIMER_GTO1, TIMER_GTO2, TIMER_GTO3
  - TIMER_PWM0_N, TIMER_PWM1_N, TIMER_PWM2_N, TIMER_PWM3_N

2.3.2. ARM Trace Pins

In TMPV7528XBG, supports trace function as a debugging supporting. The trace function shares pins (ARM_TRCCLK, ARM_TRCCTL and ARM_TRCD[7:0]) with the following functions.

- CAN0/1 RX/TX Signal
  - CAN0_RX, CAN1_RX
  - CAN0_TX, CAN1_TX
- General purpose I/O
  - GPIO[23:16]
- Video Output Interface
  - VOIF_D[18:16], VOIF_D[9:8] and VOIF_D[2:0]

3. Package Information

3.1. TMPV7528XBG, TMPV7506XBG, TMPV7504XBG Package Drawing

Package name: P-BGA516-2727-1.00-002

Unit: mm

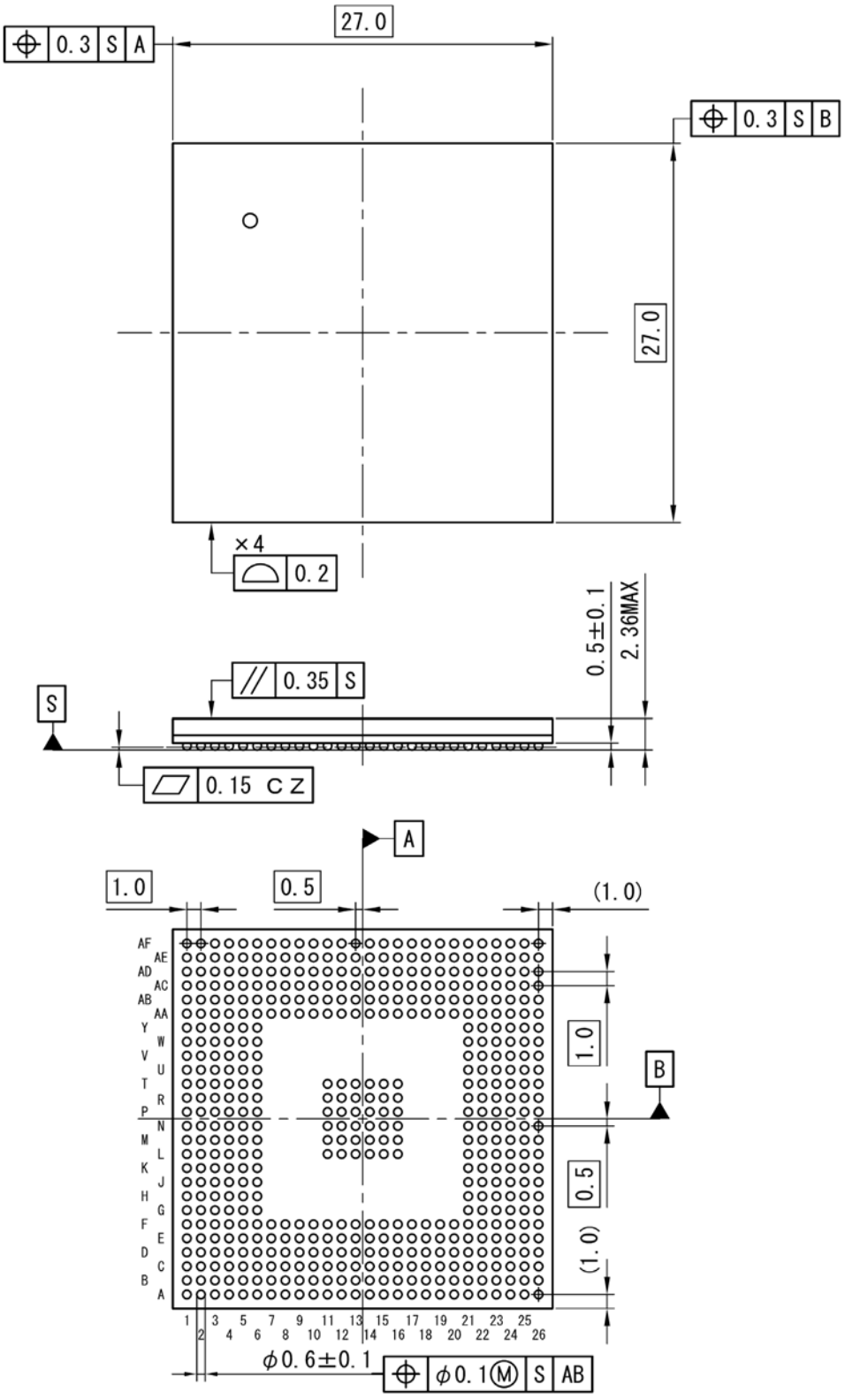


Figure 3-1 TMPV7528XBG, TMPV7506XBG, TMPV7504XBG Package Drawing

3.2. TMPV7502XBG Package Drawing

Package name: P-LFBGA324-1111-0.50-001

Unit: mm

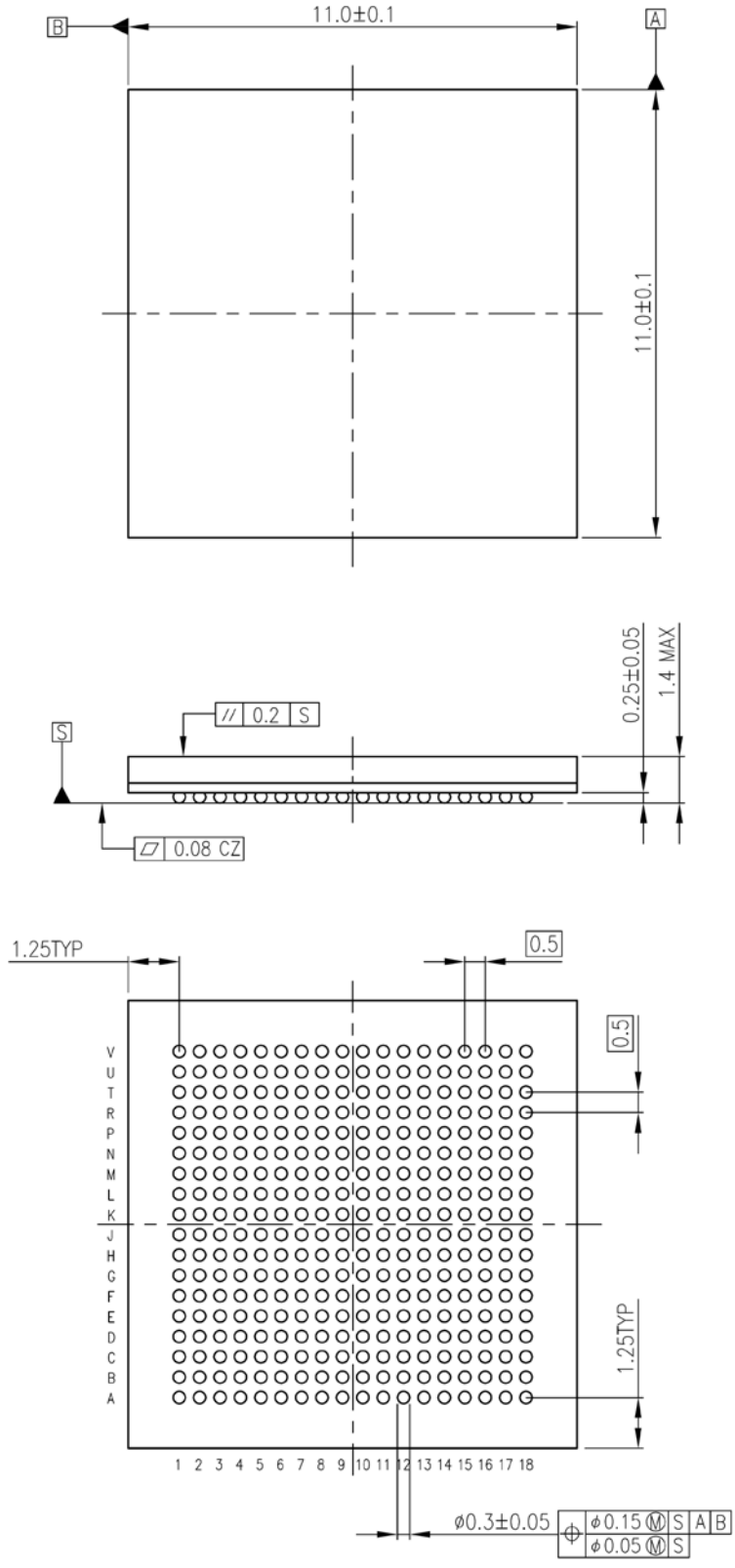


Figure 3-2 TMPV7502XBG Package Drawing

Revision History

Rev.	Date of Issue	Changes
1.0.0	2013/12/10	1st Release
2.0.0	2014/10/31	Contents Revised
2.0.1	2019/1/15	Contents Revised

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