5 GHz–20 GHz GaAs pHEMT MMIC Wideband LNA

MMA044AA

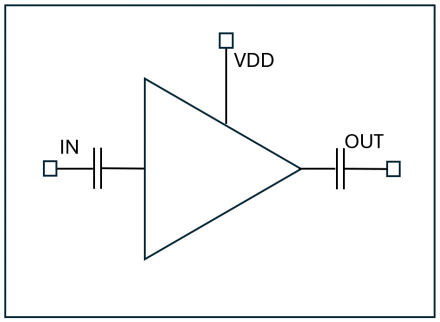
Product Overview

The MMA044AA is a Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) pseudomorphic High-Electron Mobility Transistor (pHEMT) amplifier. Nominally biased at 4V and 100 mA, the amplifier offers a flat gain of 21 dB, noise figure of 1.5 dB, and OIP3 of 32 dBm. It is ideal for test instrumentation, wide-band A&D, and space applications requiring low noise, flat gain, and linearity. The amplifier MMIC operates with a single positive supply voltage provided via on-chip bias inductors and requires minimum off-chip components. Both the input and output are AC coupled via on-chip blocking caps and are nominally matched to 50Ω.

Key Features

- Frequency range: 5 GHz–20 GHz
- High gain: 21 dB
- Low noise figure: 1.5 dB
- High output IP3: 32 dBm
- Single positive supply: 4V at 100 mA
- Integrated bias inductors
- Capable of operating from 3.5V to 5V
- Nominally matched 50Ω at input/output
- Die size: 1.38 mm × 1.15 mm × 0.1 mm

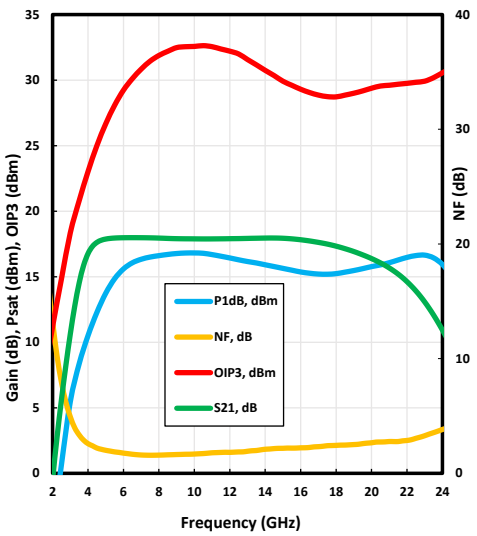
Amplifier Functional Diagram



Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter–wave communications systems

Performance Curves



Performance Overview

Parameter	Typ.	Units
Operational frequency range	5 – 20	GHz
Gain	21	dB
Noise figure	1.5	dB
P1dB at 10 GHz	16	dBm
P_{sat} at 10 GHz	17	dBm
OIP3 at 10 GHz	32	dBm
Current at +4V supply	100	mA

Export Classification: EAR99

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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, V_{DD} = 5V, I_{DD} = 110 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		5		20	GHz
Gain	5 GHz–20 GHz	17	21		dB
Gain flatness	5 GHz–20 GHz		±0.25		dB
Noise figure	5 GHz–15 GHz		1.5	2	dB
	15 GHz–20 GHz		2	2.5	
Input return loss	5 GHz–20 GHz	8	12		dB
Output return loss	5 GHz–20 GHz	9	12		dB
P1dB	5 GHz–20 GHz	13	16		dBm
P_{sat}	5 GHz–15 GHz	14	17		dBm
OIP3	5 GHz–20 GHz	28	32		dBm
OIP2	5 GHz–20 GHz		65		dBm
V_{DD}(drain supply voltage)			4		V
I_{DD}(drain supply current)			100		mA

1.2 Absolute Maximum Ratings

Table 1–2 shows the absolute maximum ratings of the MMA044AA device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings potentially could cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	5V
RF input power (P_{IN})	+24 dBm
Channel temperature	+175 °C
Thermal resistance	62 °C/W
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The graphs shown in Figures 1–1 through 1–36 represent the Typical Performance versus Temperature curves of the MMA044AA device under specific bias conditions. All measurements were taken using the test circuit shown Figure 3-2.

Figure 1-1. Gain vs. Temperature at 3.5V

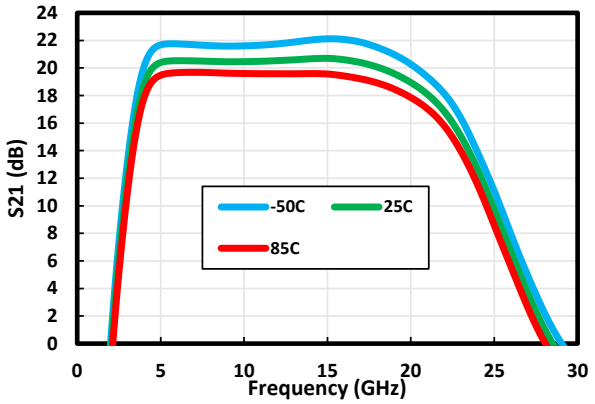


Figure 1-2. Gain vs. Temperature at 4V

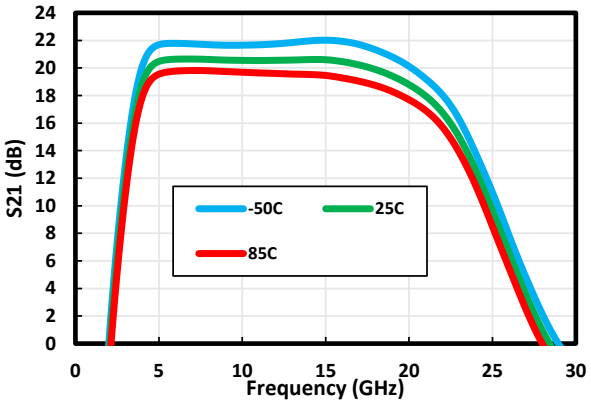


Figure 1-3. Gain vs. Temperature at 4.5V

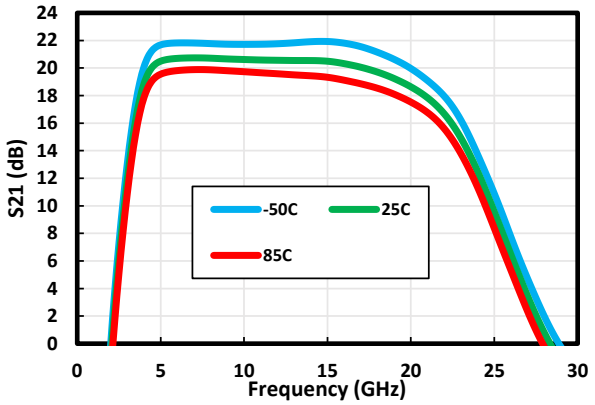


Figure 1-4. Gain vs. Temperature at 5V

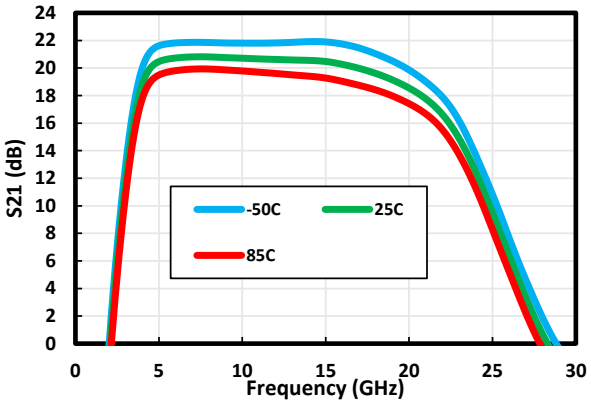


Figure 1-5. S11 vs. Temperature at 3.5V

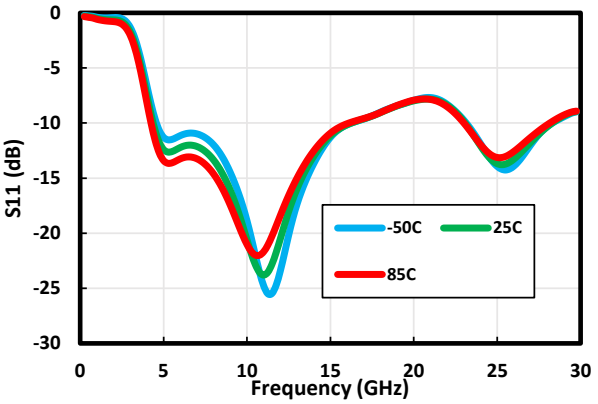


Figure 1-6. S11 vs. Temperature at 4V

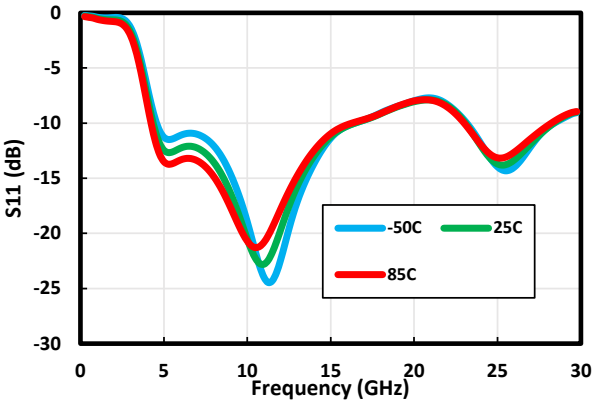


Figure 1-7. S11 vs. Temperature at 4.5V

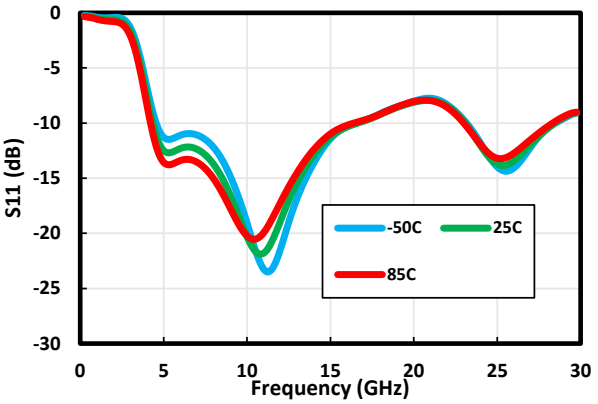


Figure 1-8. S11 vs. Temperature at 5V

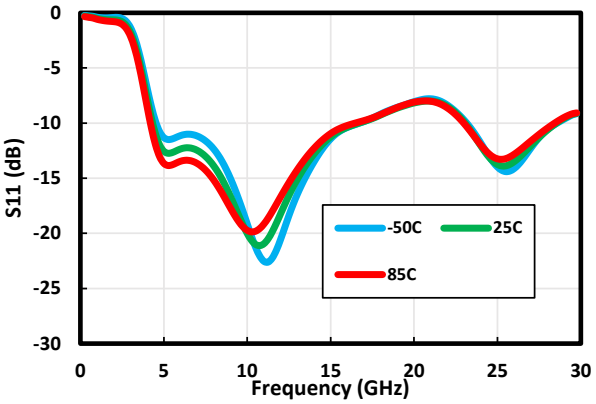


Figure 1-9. S22 vs. Temperature at 3.5V

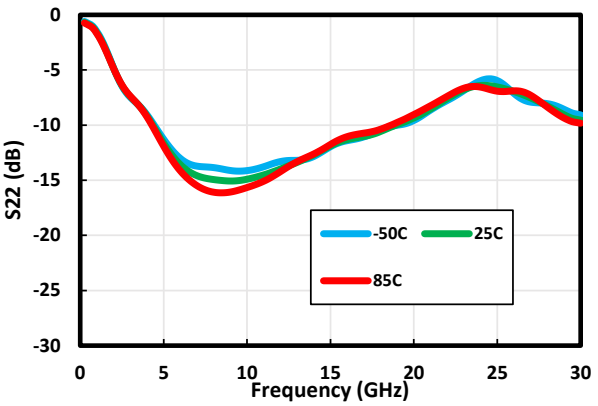


Figure 1-10. S22 vs. Temperature at 4V

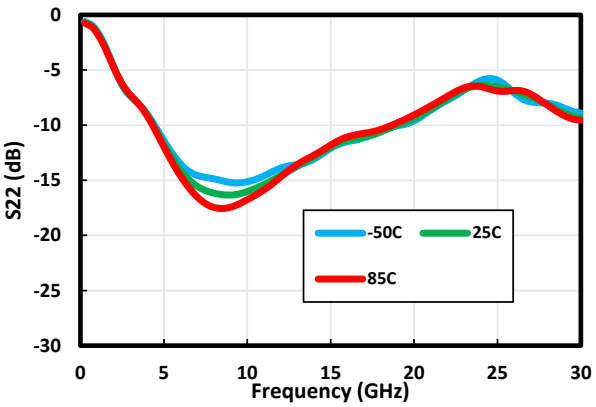


Figure 1-11. S22 vs. Temperature at 4.5V

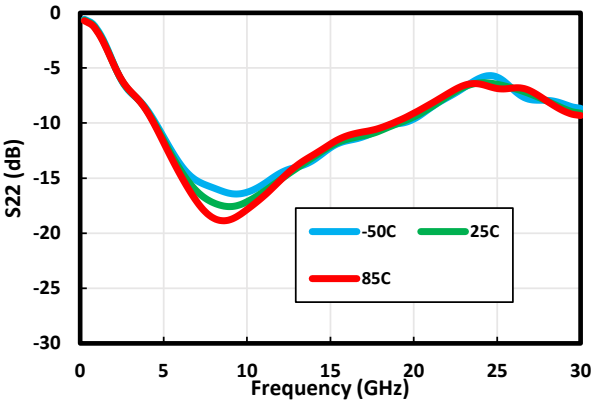


Figure 1-12. S22 vs. Temperature at 5V

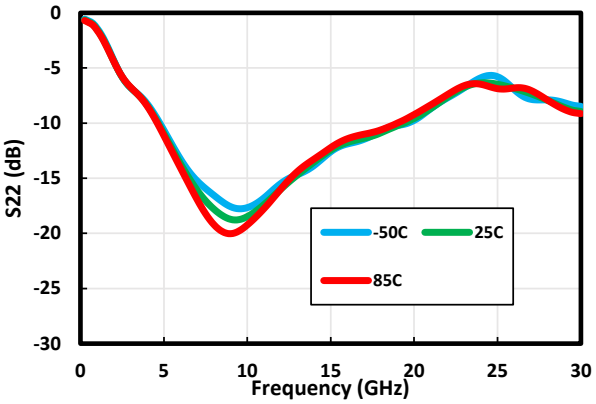


Figure 1-13. NF vs. Temperature at 3.5V

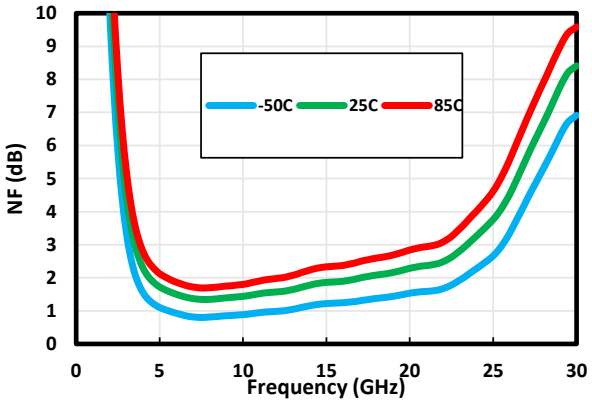


Figure 1-14. NF vs. Temperature at 4V

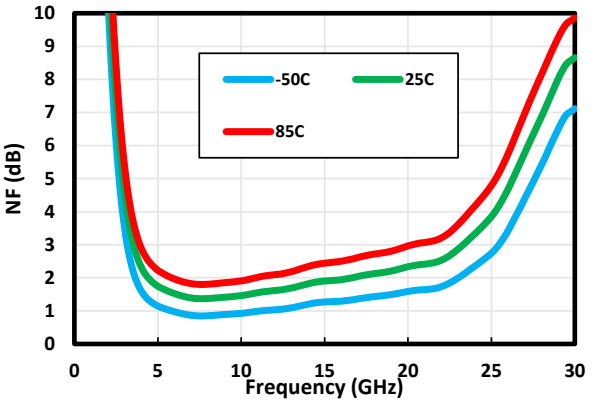


Figure 1-15. NF vs. Temperature at 4.5V

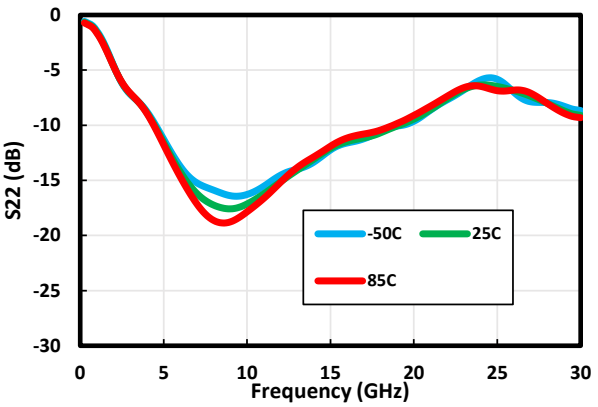


Figure 1-16. NF vs. Temperature at 5V

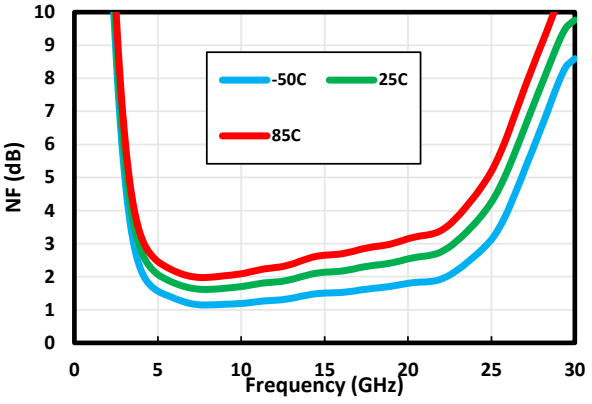


Figure 1-17. P1dB vs. Temperature at 3.5V

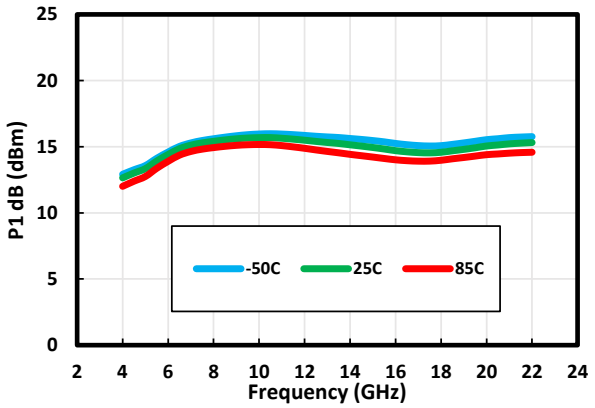


Figure 1-18. P1dB vs. Temperature at 4V

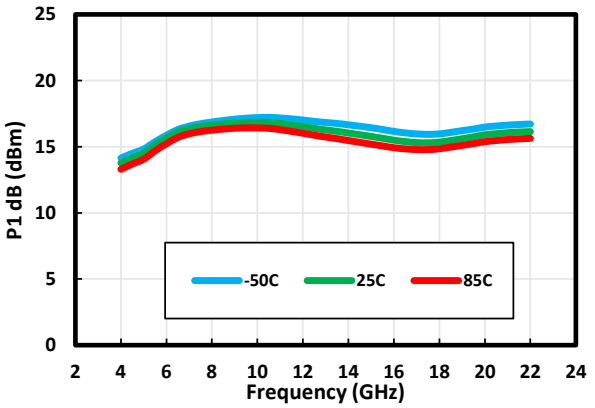


Figure 1-19. P1dB vs. Temperature at 4.5V

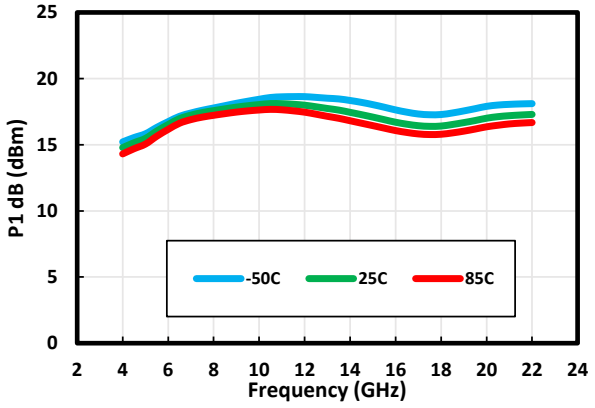


Figure 1-20. P1dB vs. Temperature at 5V

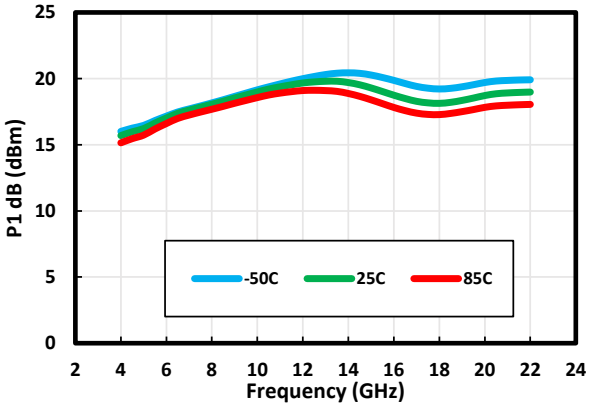


Figure 1-21. P_{sat} vs. Temperature at 3.5V

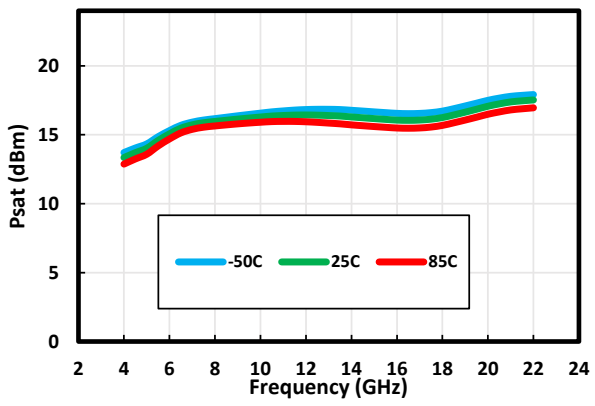


Figure 1-22. P_{sat} vs. Temperature at 4V

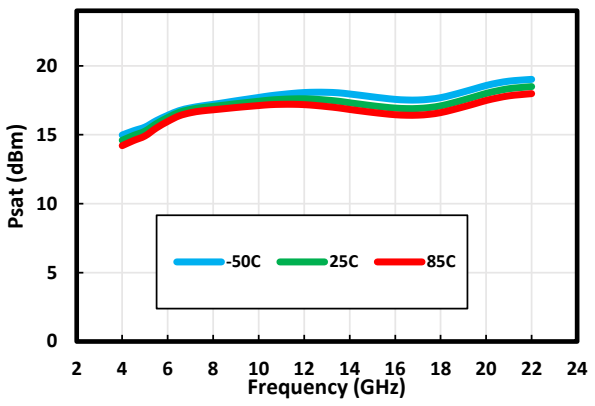


Figure 1-23. P_{sat} vs. Temperature at 4.5V

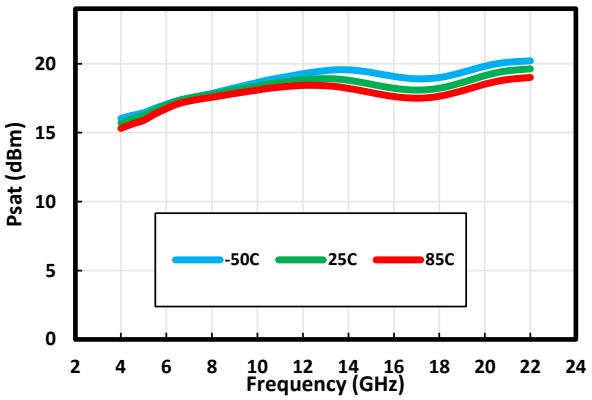


Figure 1-24. P_{sat} vs. Temperature at 5V

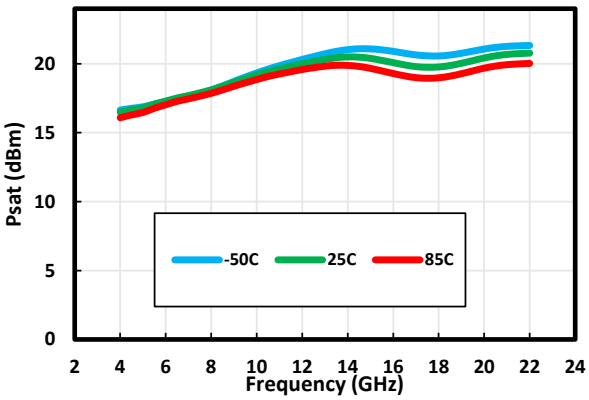


Figure 1-25. OIP2 (low) vs. Temperature at 3.5V

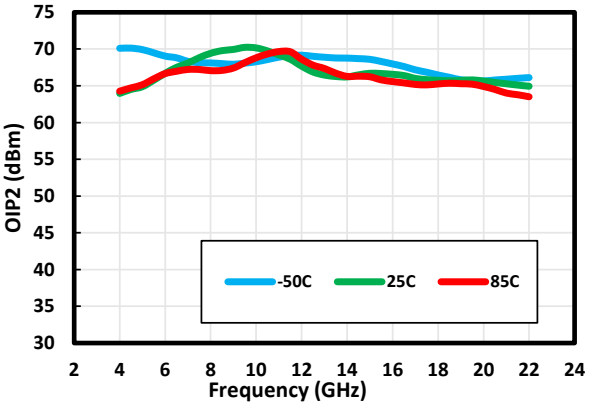


Figure 1-26. OIP2 (low) vs. Temperature at 4V

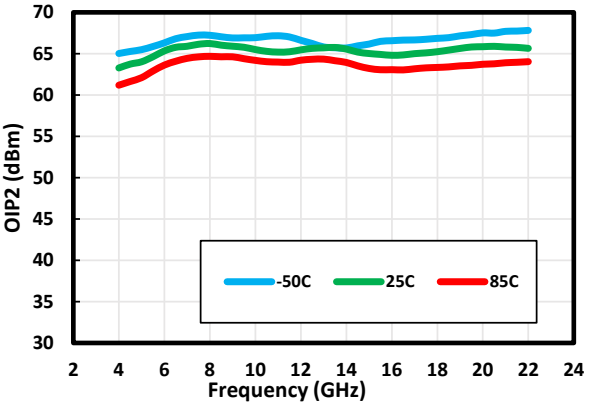


Figure 1-27. OIP2 (low) vs. Temperature at 4.5V

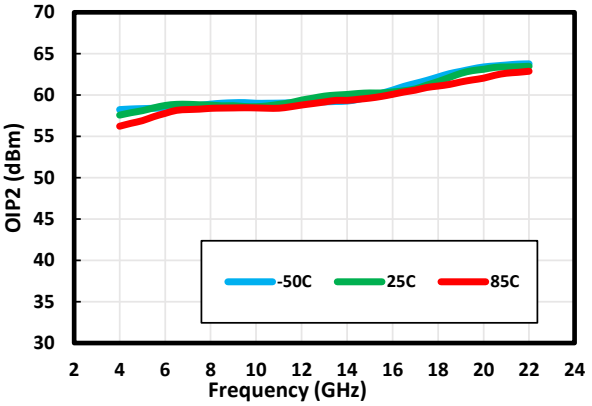


Figure 1-28. OIP2 (low) vs. Temperature at 5V

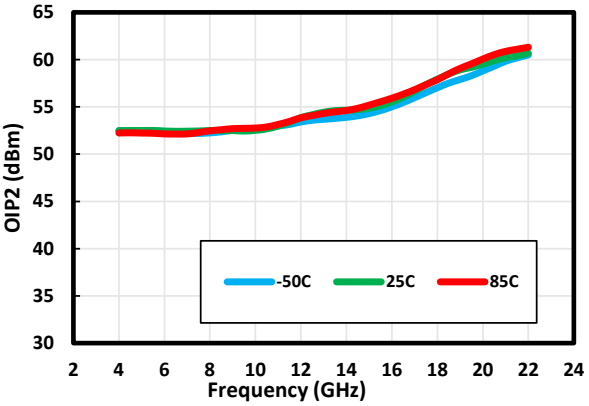


Figure 1-29. OIP3 vs. Temperature at 3.5V

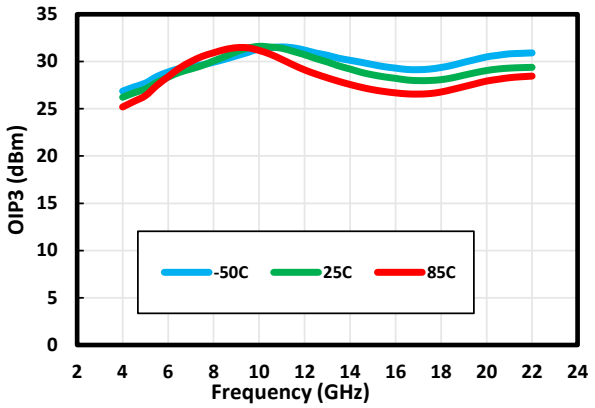


Figure 1-30. OIP3 vs. Temperature at 4V

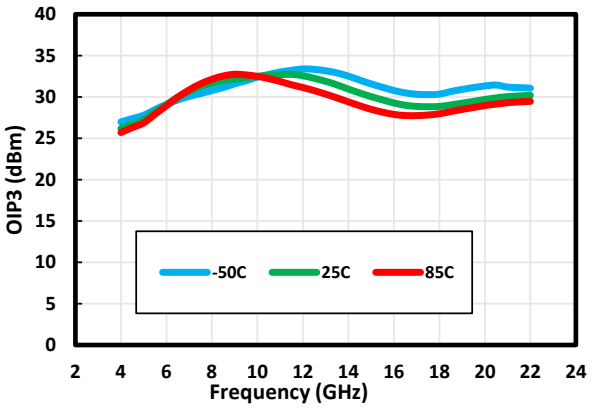


Figure 1-31. OIP3 vs. Temperature at 4.5V

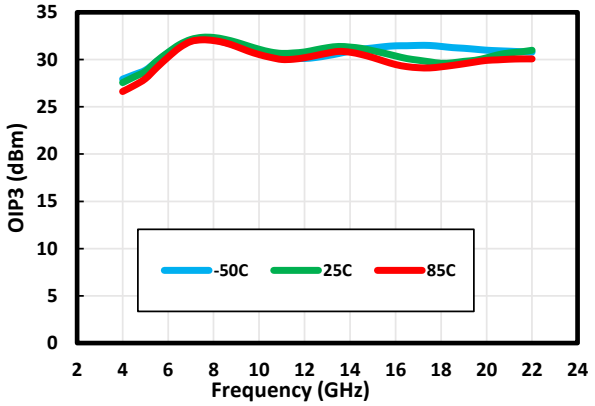


Figure 1-32. OIP3 vs. Temperature at 5V

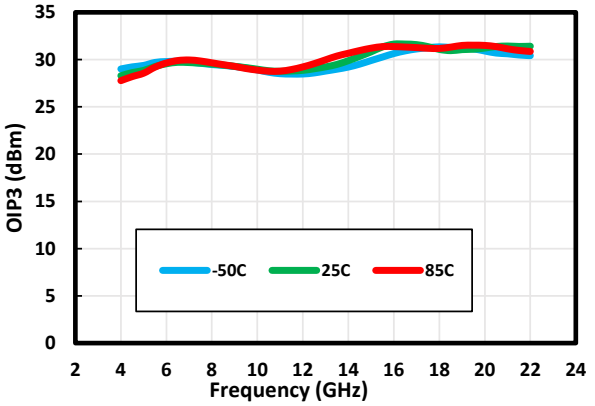


Figure 1-33. IM3 vs. Temperature at 3.5V

0 dBm Per Tone Output Power

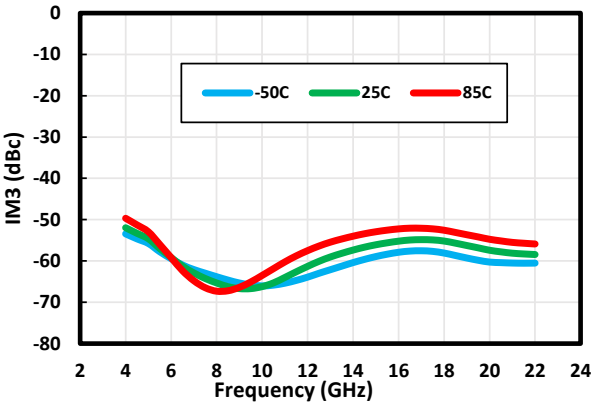


Figure 1-34. IM3 vs. Temperature at 4V

0 dBm Per Tone Output Power

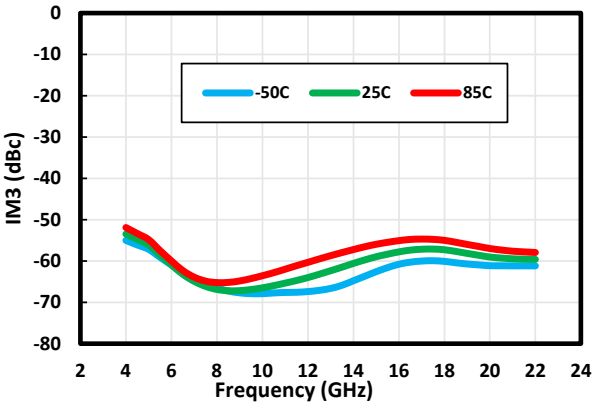


Figure 1-35. IM3 vs. Temperature at 4.5V

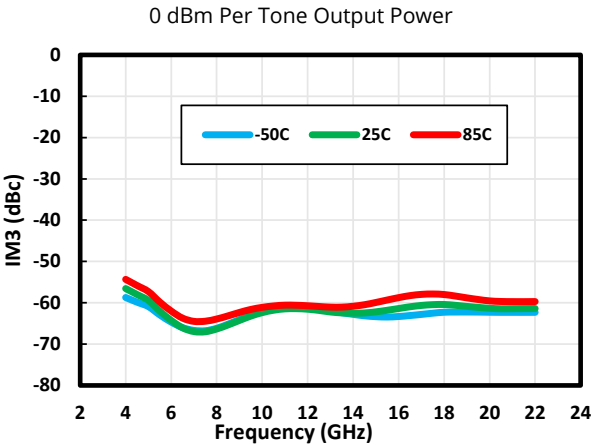
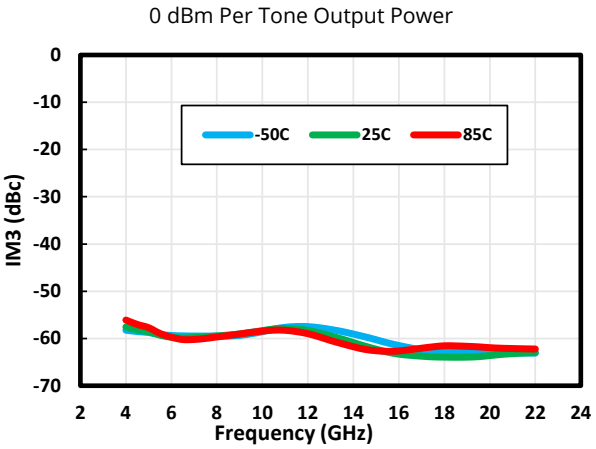


Figure 1-36. IM3 vs. Temperature at 5V



1.3.2 Typical Performances vs. Bias

The graphs shown in Figures 1–37 through 1–48 represent the Typical Performance versus Bias curves of the MMA044AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-37. Gain vs. V_{DD}

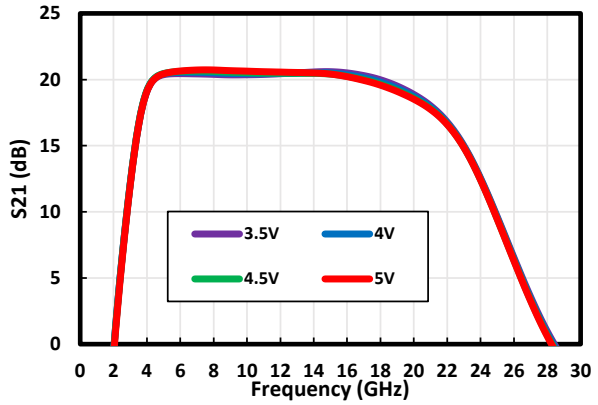


Figure 1-38. S11 vs. V_{DD}

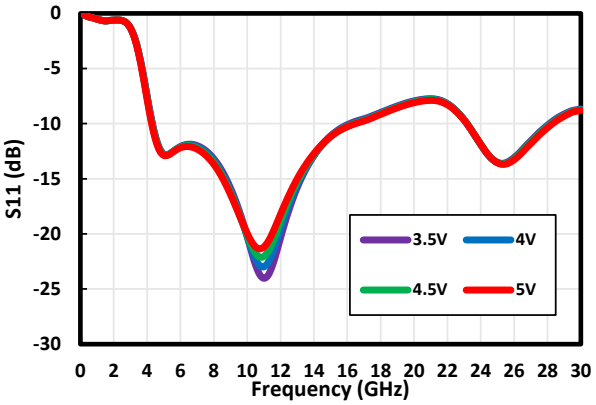


Figure 1-39. S22 vs. V_{DD}

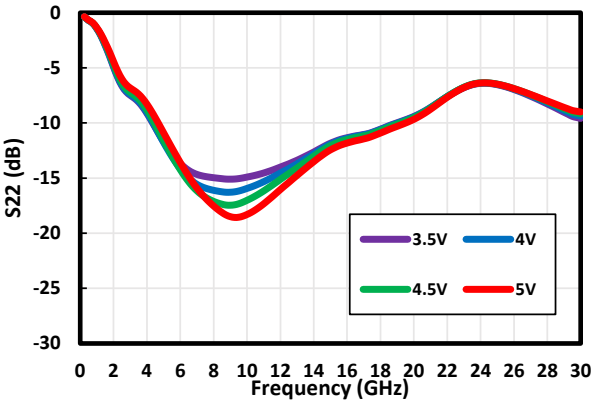


Figure 1-40. S12 vs. V_{DD}

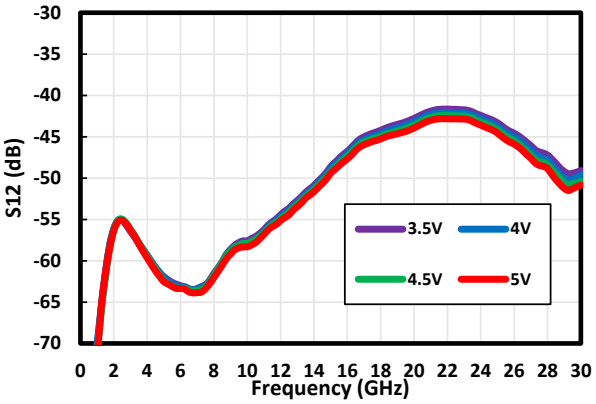


Figure 1-41. NF vs. V_{DD}

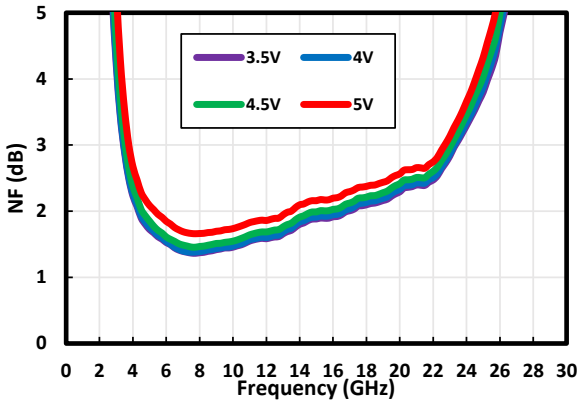


Figure 1-42. P1dB vs. V_{DD}

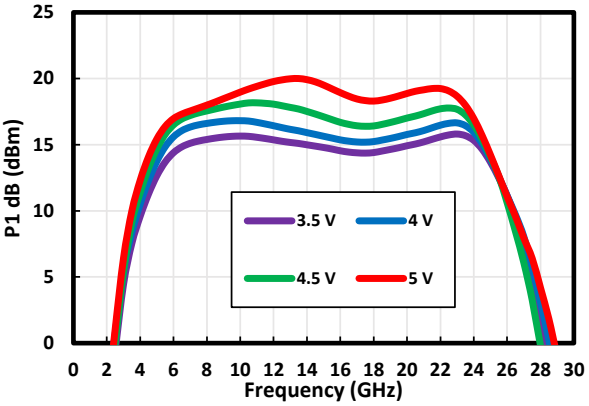


Figure 1-43. P_{sat} vs. V_{DD}

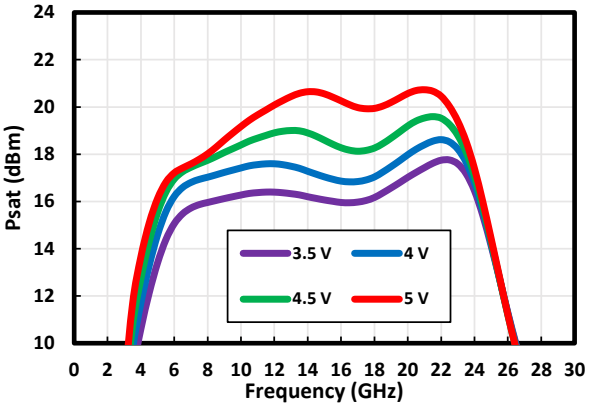


Figure 1-44. OIP3 vs. V_{DD}

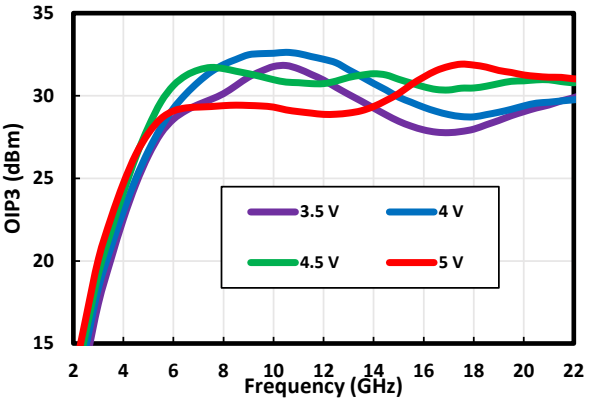


Figure 1-45. $OIP2_{LOW}$ vs. V_{DD}

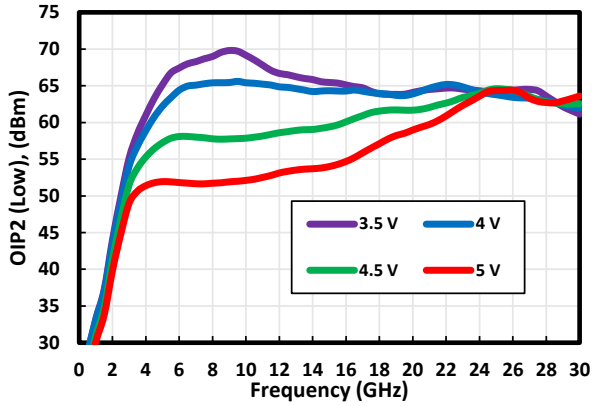


Figure 1-46. IM3 vs. V_{DD} at 0 dBm per tone

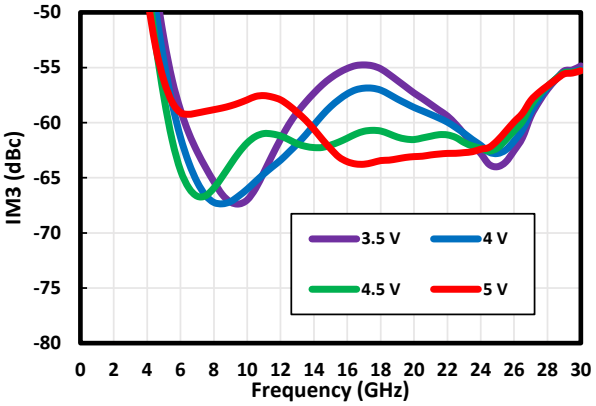


Figure 1-47. 2^{nd} Harmonic vs. V_{DD} at 6 dBm

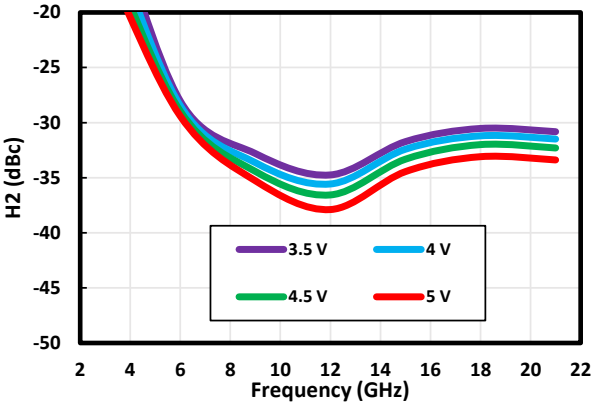
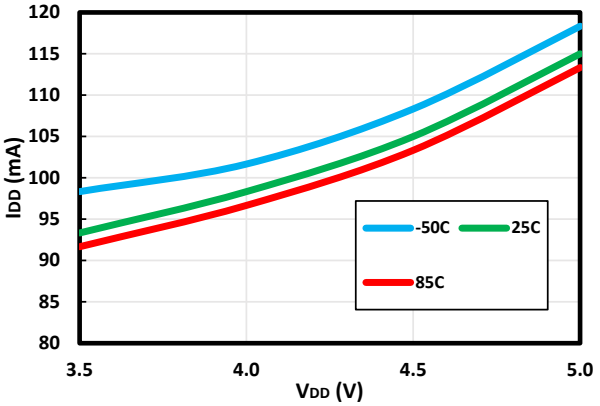


Figure 1-48. I_{DD} vs. V_{DD}, Temperature



1.3.3 Typical Performances vs. Output Power

The graphs shown in Figures 1–49 through 1–57 represent the Typical Performance versus Output power curves of the MMA044AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-49. IM2 vs. Power at 3.5V

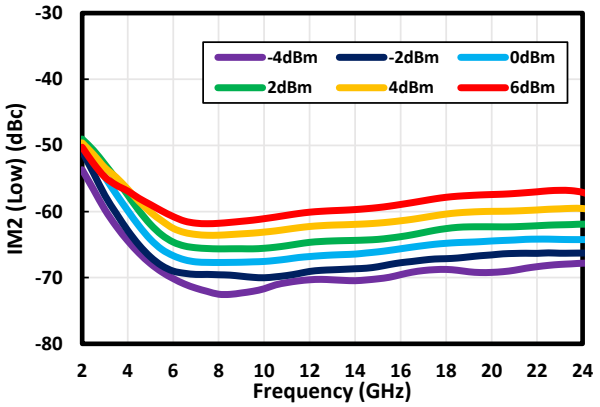


Figure 1-50. IM2 vs. Power at 4V

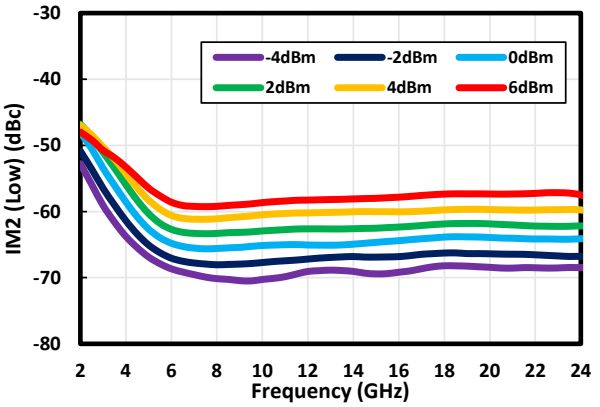


Figure 1-51. IM2 vs. Power at 4.5V

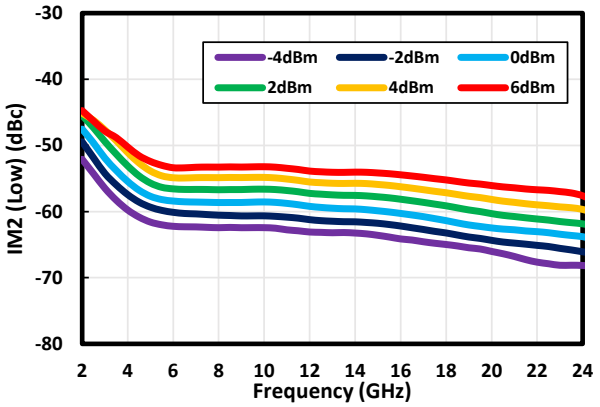


Figure 1-52. IM2 vs. Power at 5V

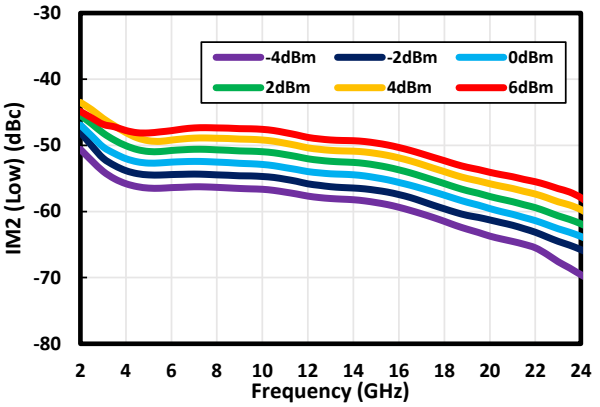


Figure 1-53. IM3 vs. Power at 3.5V

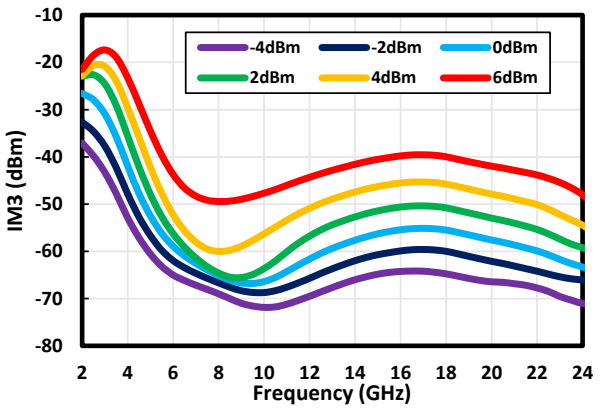


Figure 1-54. IM3 vs. Power at 4V

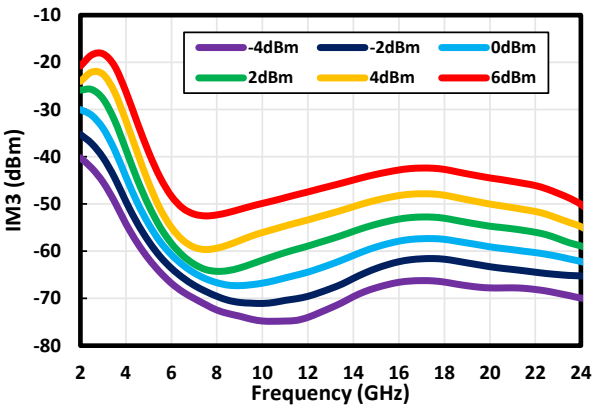


Figure 1-55. IM3 vs. Power at 4.5V

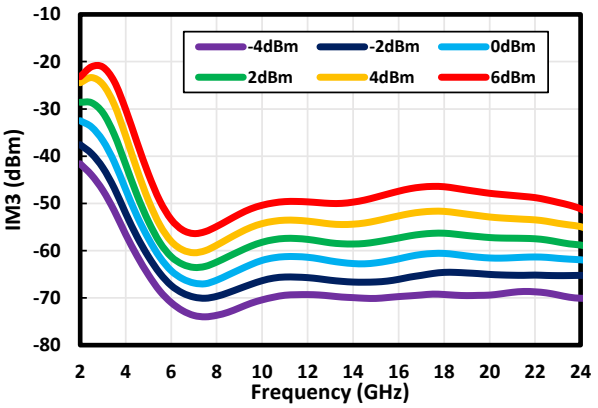


Figure 1-56. IM3 vs. Power at 5V

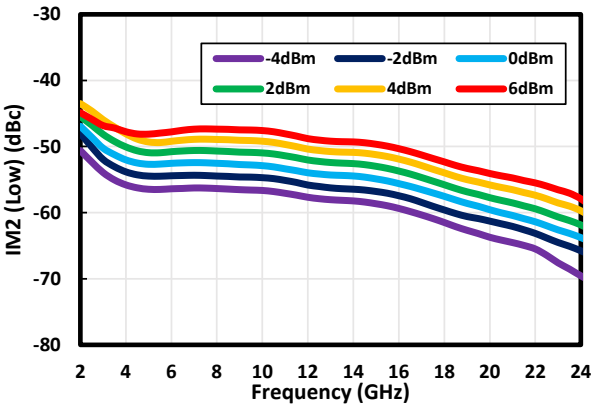
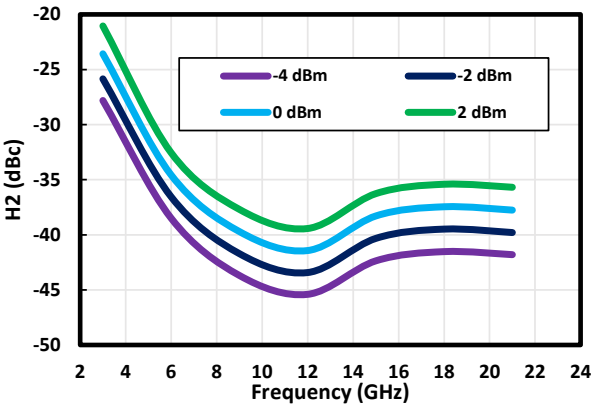


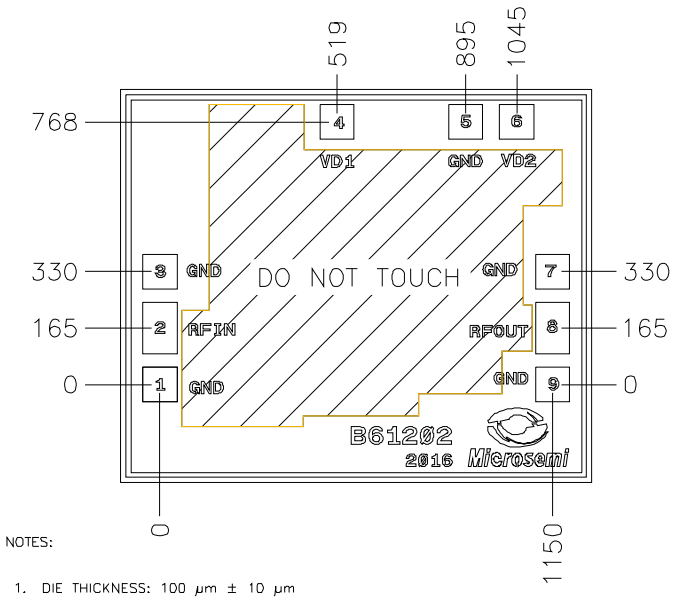
Figure 1-57. 2nd Harmonic vs. Power at 4V



2. Die Specifications

Figure 2-1 illustrates the chip outline of the MMA044AA device. Dimensions are in millimeters and are relative to the zero datum locations shown in the drawing. Nominal die dimensions are 1.38 mm × 1.15 mm × 0.1 mm. The minimum bond pad size is 0.1 mm × 0.1 mm. Both the bond pad surface and the backside metal are 3 µm thick gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The air-bridge keep-out region is shown inside.

Figure 2-1. Die Outline Drawing (mm)



NOTES:

1. DIE THICKNESS: 100 µm ± 10 µm
2. DIE OVERALLL: 1380µm X 1150µm
3. ALL DIMENSIONS SHOWN ARE µm WITH A TOLERANCE OF ± 5 µm UNLESS OTHERWISE SPECIFIED
4. DIE SIZE REFLECTS UN-CUT DIMENSIONS. LASER KERF REDUCES DIE SIZE BY ~25 µm EACH DIMENSION.
5. MARKING INFO:
   2016 = DESIGN DATE (DOES NOT CHANGE)
   B61202 = DIE NAME

PAD NO.	DESCRIPTION	µm PAD SIZE
1	GND	100X100
2	RFIN	100X150
3	GND	100X100
4	VD1	
5	GND	
6	VD2	
7	GND	
8	RFOUT	100X150
9	GND	100X100

Table 2-1. I/O Pad Description

Pad Number	Pad Name	Pad Description
2	RFIN	This pad AC decoupled from FET gates and nominally matched to 50Ω.
8	RFOUT	This pad AC decoupled from FET drains and nominally matched to 50Ω.
4,6	VD1, VD2	These pads used to supply +VDD voltage bias to the MMIC.
1, 3, 5, 7, 9	GND	Ground connections used for die test purposes; DC/RF ground is using die backside metal.

3. Application Circuit

Figure 3-1. Application Circuit: Schematic

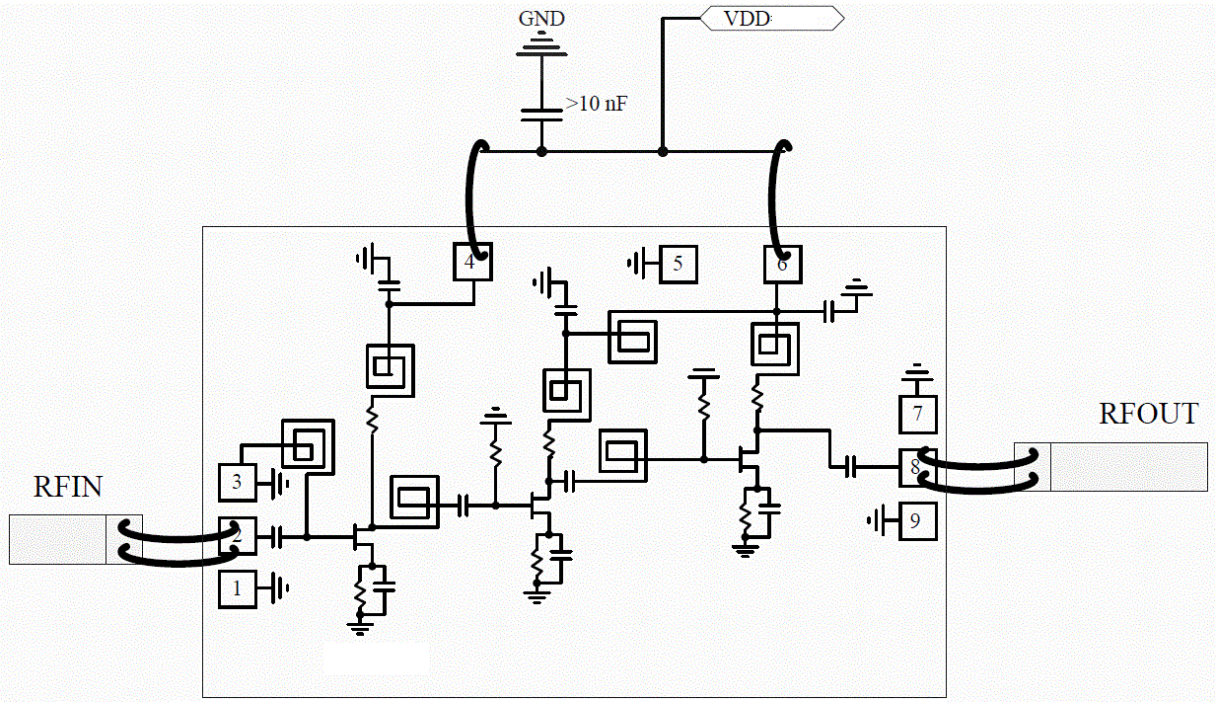


Figure 3-2. Die Test Circuit: Assembly Drawing

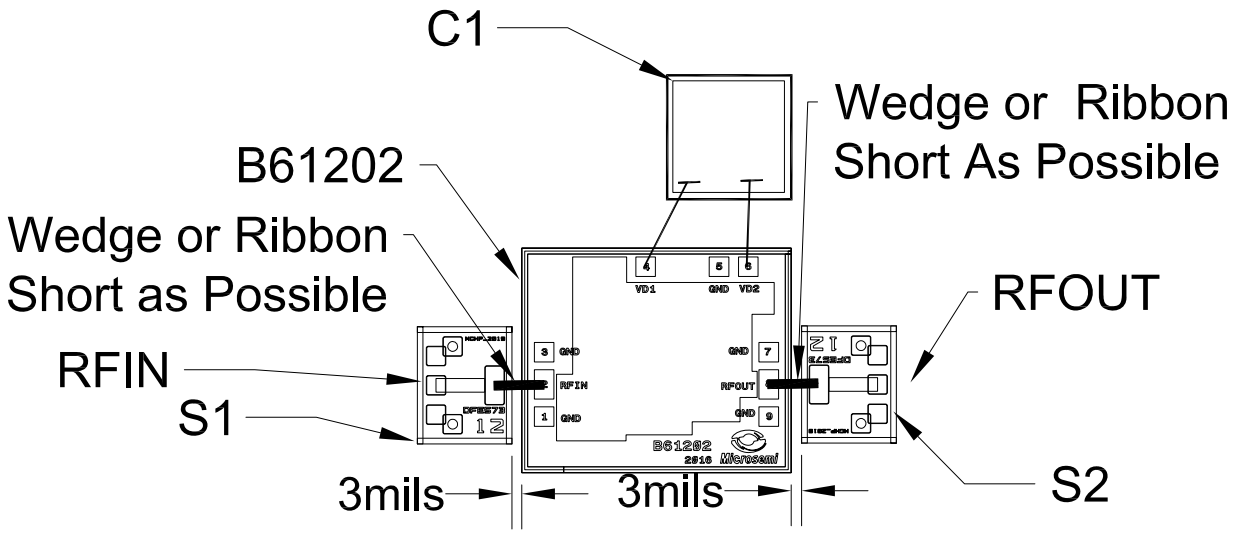


Table 3-1. List of Material for Test Circuit

Reference	Part Number	Description
B61202	MMA044AA	MMA044AA amplifier die
C1	160U02A102MT4W	Johanson Dielectric, Cer.Cap 1 nF
S1, S2	E57312	Probe launchers
Epoxy	EpoTech H20E	Conductive epoxy for die and cap mount

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microchip application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA044AA	Die
MMA044PP3	QFN 3 mm × 3 mm packaged device

4.3 Packing Information

Standard Format
Gel pack
50 pieces per pack

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
B	02/2025	Updated with new data throughout, updated plots.
A	05/2022	Document created.

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