

MC14514B, MC14515B

4-Bit Transparent Latch / 4-to-16 Line Decoder

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical “1” at the selected output, whereas the MC14515B (output active low option) presents a logical “0” at the selected output. The latches are R–S type flip–flops which hold the last input data presented prior to the strobe transition from “1” to “0”. These high and low options of a 4–bit latch / 4 to 16 line decoder are constructed with N–channel and P–channel enhancement mode devices in a single monolithic structure. The latches are R–S type flip–flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load the Rated Temperature Range
- These Devices are Pb–Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Parameter | Symbol | Value | Unit |
|---|-------------------|-----------------------|------|
| DC Supply Voltage Range | V_{DD} | –0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | V_{in}, V_{out} | –0.5 to V_{DD} +0.5 | V |
| Input or Output Current (DC or Transient) per Pin | I_{in}, I_{out} | ±10 | mA |
| Power Dissipation per Package (Note 1) | P_D | 500 | mW |
| Ambient Temperature Range | T_A | –55 to +125 | °C |
| Storage Temperature Range | T_{stg} | –65 to +150 | °C |
| Lead Temperature (8–Second Soldering) | T_L | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW”

Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



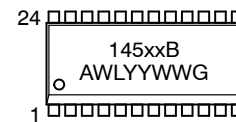
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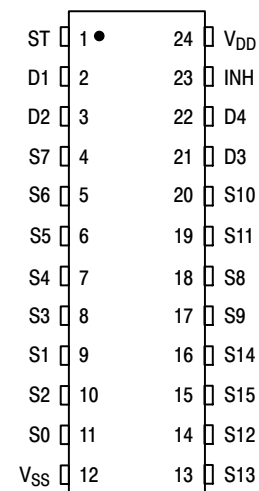
SOIC–24
DW SUFFIX
CASE 751E

MARKING DIAGRAM



xx = 14 or 15
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

PIN ASSIGNMENT

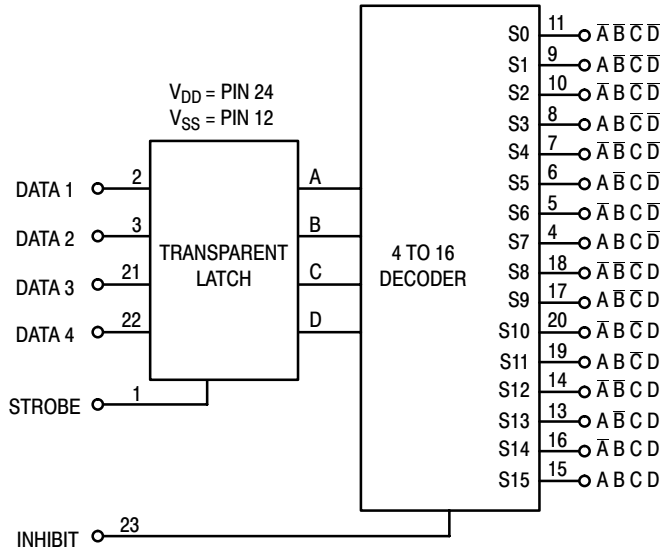


ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14514B, MC14515B

BLOCK DIAGRAM



DECODE TRUTH TABLE (Strobe = 1)*

| Inhibit | Data Inputs | | | | Selected Output MC14514 = Logic "1" MC14515 = Logic "0" |
|---------|-------------|---|---|---|---|
| | D | C | B | A | |
| 0 | 0 | 0 | 0 | 0 | S0 |
| 0 | 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 0 | 1 | 0 | S2 |
| 0 | 0 | 0 | 1 | 1 | S3 |
| 0 | 0 | 1 | 0 | 0 | S4 |
| 0 | 0 | 1 | 0 | 1 | S5 |
| 0 | 0 | 1 | 1 | 0 | S6 |
| 0 | 0 | 1 | 1 | 1 | S7 |
| 0 | 1 | 0 | 0 | 0 | S8 |
| 0 | 1 | 0 | 0 | 1 | S9 |
| 0 | 1 | 0 | 1 | 0 | S10 |
| 0 | 1 | 0 | 1 | 1 | S11 |
| 0 | 1 | 1 | 0 | 0 | S12 |
| 0 | 1 | 1 | 0 | 1 | S13 |
| 0 | 1 | 1 | 1 | 0 | S14 |
| 0 | 1 | 1 | 1 | 1 | S15 |
| 1 | X | X | X | X | All Outputs = 0, MC14514 All Outputs = 1, MC14515 |

X = Don't Care

*Strobe = 0, Data is latched

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|----------------------|--------------------|
| MC14514BDWR2G | SOIC-24 (Pb-Free) | 1000 / Tape & Reel |
| NLV14514BDWR2G* | | |
| MC14515BDWR2G | SOIC-24 (Pb-Free) | 1000 / Tape & Reel |
| NLV14515BDWR2G* | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14514B, MC14515B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|---|------------------------------|------------------------|--|------|-------|-----------------|------|--------|------|------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | |
| Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD} | “0” Level V _{OL} | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | “1” Level V _{OH} | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage “0” Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) “1” Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IL} | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| | V _{IH} | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | Source I _{OH} | 5.0 | – 1.2 | – | – 1.0 | – 1.7 | – | – 0.7 | – | mAdc |
| | | 5.0 | – 0.25 | – | – 0.2 | – 0.36 | – | – 0.14 | – | |
| | | 10 | – 0.62 | – | – 0.5 | – 0.9 | – | – 0.35 | – | |
| | | 15 | – 1.8 | – | – 1.5 | – 3.5 | – | – 1.1 | – | |
| | Sink I _{OL} | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | I _{in} | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance (V _{in} = 0) | C _{in} | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | μAdc |
| | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | |
| | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | |
| Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _{TL} | 5.0 10 15 | I _T = (1.35 μA/kHz) f + I _{DD} I _T = (2.70 μA/kHz) f + I _{DD} I _T = (4.05 μA/kHz) f + I _{DD} | | | | | | | μAdc |

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L – 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14514B, MC14515B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} | All Types | | | Unit |
|---|-------------------------|-----------------|------------------|--------------------|--------------------|------|
| | | | Min | Typ (Note 6) | Max | |
| Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$ | t_{TLH} | 5.0 10 15 | – – – | 180 90 65 | 360 180 130 | ns |
| Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time; Data, Strobe to S $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.86 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 10 15 | – – – | 550 225 150 | 1100 450 300 | ns |
| Inhibit Propagation Delay Times $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 10 15 | – – – | 400 150 100 | 800 300 200 | ns |
| Setup Time Data to Strobe | t_{su} | 5.0 10 15 | 250 100 75 | 125 50 38 | – – – | ns |
| Hold Time Strobe to Data | t_h | 5.0 10 15 | –20 0 10 | –100 –40 –30 | – – – | ns |
| Strobe Pulse Width | t_{WH} | 5.0 10 15 | 350 100 75 | 175 50 38 | – – – | ns |

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

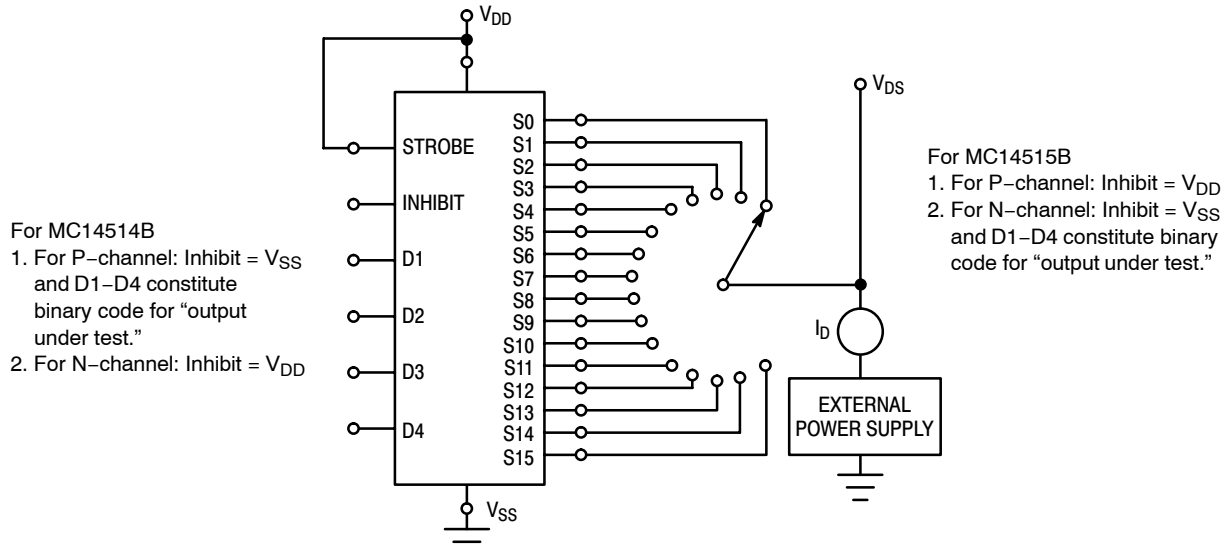


Figure 1. Drain Characteristics Test Circuit

MC14514B, MC14515B

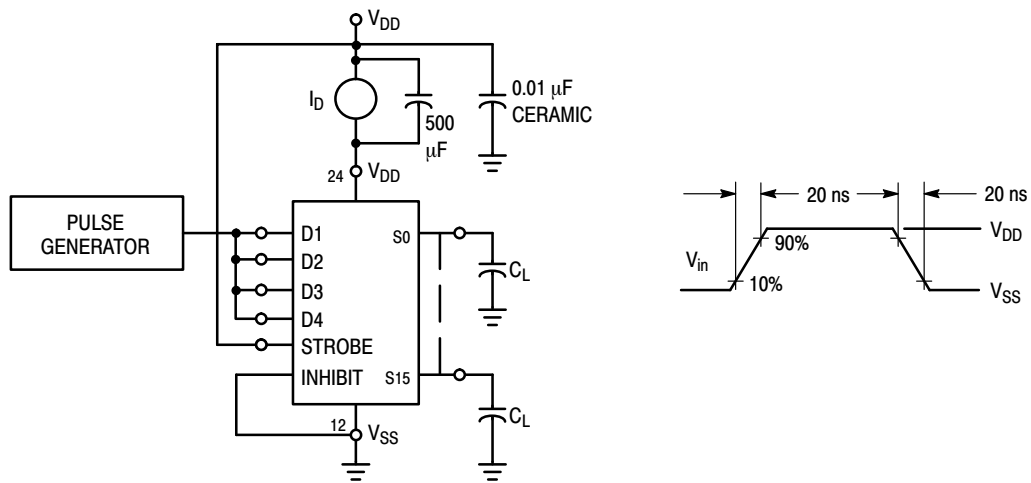


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

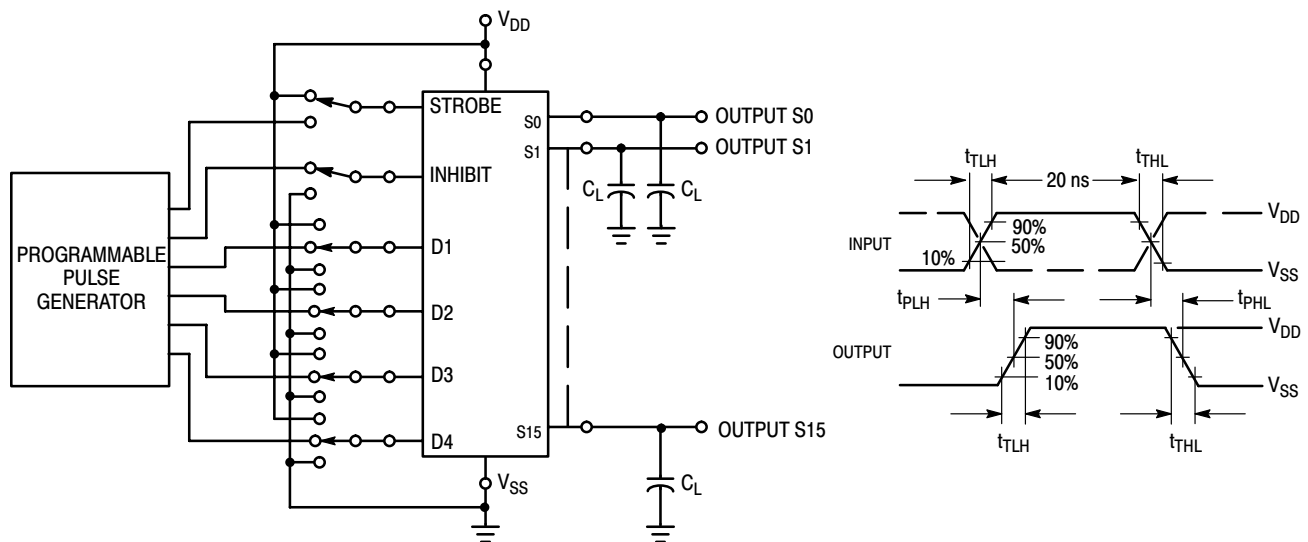
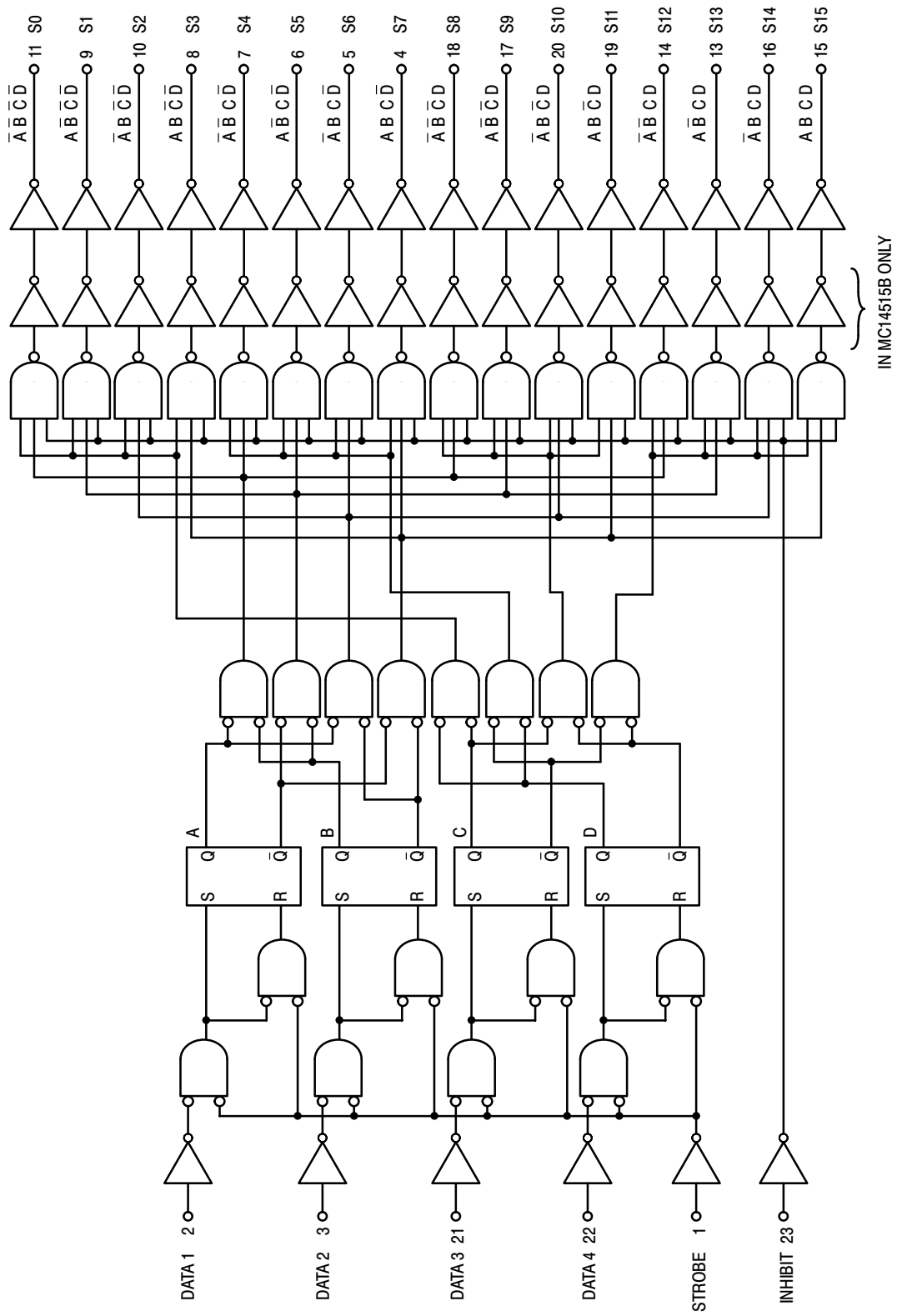


Figure 3. Switching Time Test Circuit and Waveforms

MC14514B, MC14515B

LOGIC DIAGRAM



MC14514B, MC14515B

COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

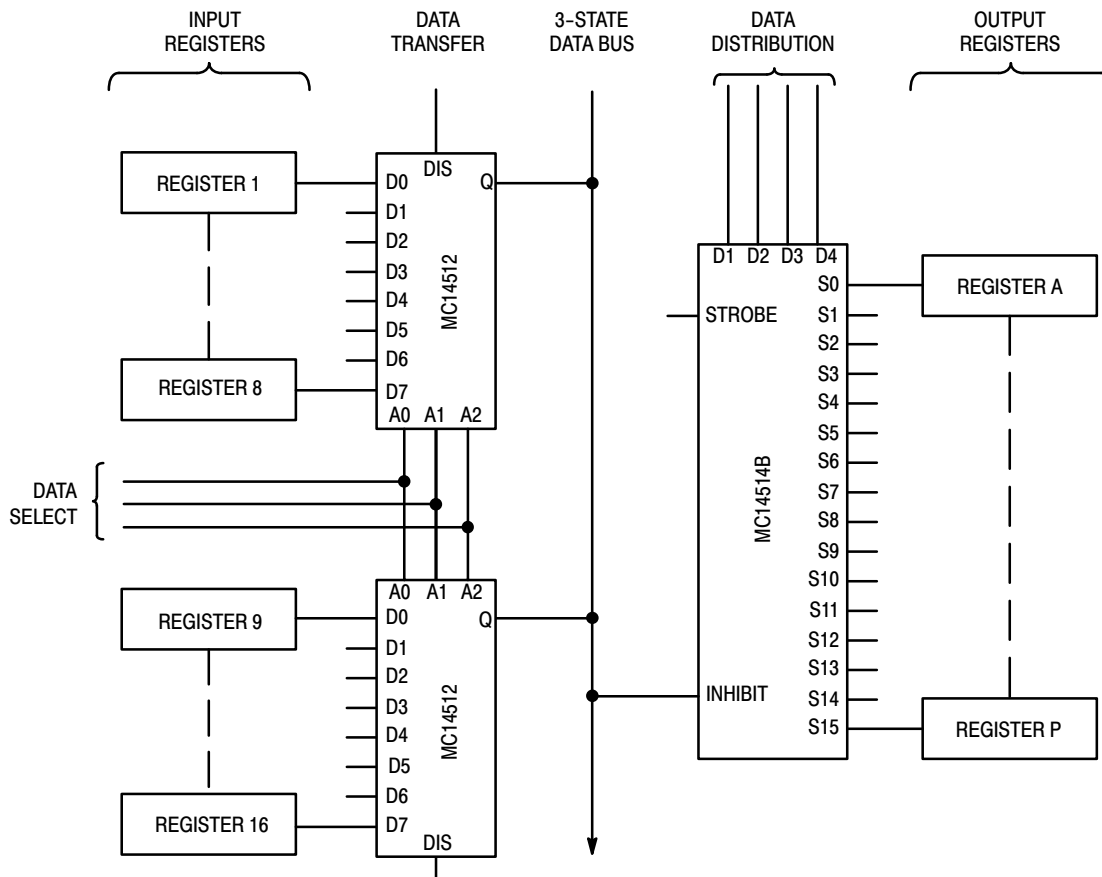
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight

times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

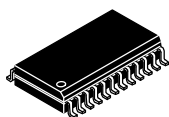
DATA ROUTING SYSTEM



MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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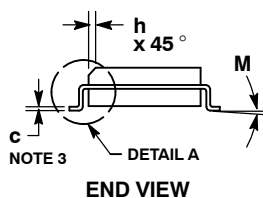
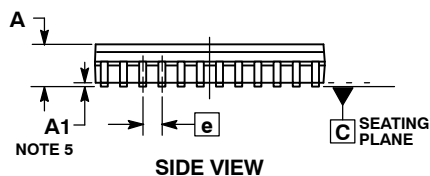
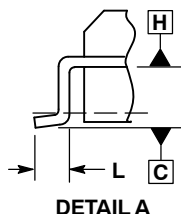
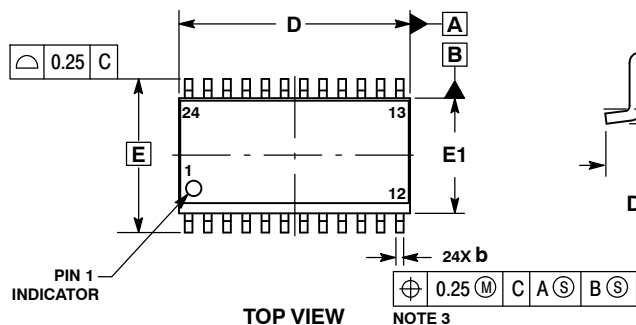
ON



SCALE 1:1

SOIC-24 WB
CASE 751E-04
ISSUE F

DATE 03 JUL 2012

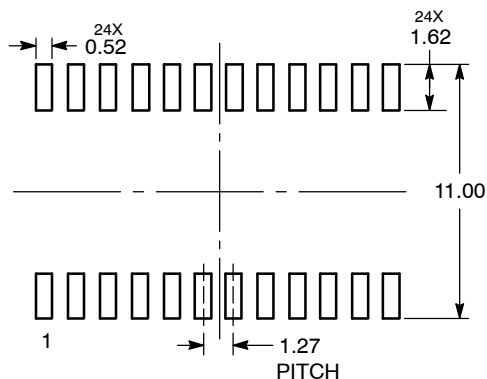


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| MILLIMETERS | | |
|-------------|-----------|-------|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.13 | 0.29 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 15.25 | 15.54 |
| E | 10.30 BSC | |
| E1 | 7.40 | 7.60 |
| e | 1.27 BSC | |
| h | 0.25 | 0.75 |
| L | 0.41 | 0.90 |
| M | 0° | 8° |

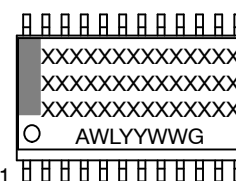
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

| | | |
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| DESCRIPTION: | SOIC-24 WB | PAGE 1 OF 2 |

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