SPDT, 3 Ω R_{ON} Switch

The NLASB3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and RDS $_{
m ON}$ resistances while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power–supply range (from $V_{
m CC}$ to GND). This device is a drop in replacement for the NC7SB3157.

The select pin has overvoltage protection that allows voltages above V_{CC} , up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

Features

- High Speed: $t_{PD} = 1.0 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2.0 \mu A$ (Max) at $T_A = 25^{\circ}C$
- Standard CMOS Logic Levels
- High Bandwidth, Improved Linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- May be used for Clock Switching, Data Multiplexing, etc.
- R_{ON} Typical = 3 Ω @ V_{CC} = 4.5 V
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- 2 Devices can Switch Balanced Signal Pairs, e.g. LVDS > 200 Mb/s
- Latchup Performance Exceeds 300 mA
- Pin for Pin Drop in for NC7SB3157
- Tiny SC88 and WDFN6 Packages
- ESD Performance:
 - ♦ Human Body Model; > 2000 V;
 - Machine Model; > 200 V
- NLVASB3157 Features Extended Automotive Temperature Range;
 -55°C to +125°C (See Appendix A)
- Pb-Free Packages are Available



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MARKING DIAGRAMS



SC-88 DF SUFFIX CASE 419B





WDFN6 MT SUFFIX CASE 506AS



AF, F = Specific Device Code
M = Date Code*
= Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

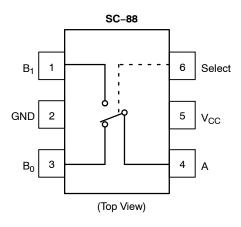
FUNCTION TABLE

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

ORDERING INFORMATION

Device	Package	Shipping [†]
NLASB3157DFT2	SC-88	3000 / Tape & Reel
NLASB3157DFT2G	SC-88 (Pb-Free)	3000 / Tape & Reel
NLVASB3157DFT2	SC-88	3000 / Tape & Reel
NLVASB3157DFT2G	SC-88 (Pb-Free)	3000 / Tape & Reel
NLASB3157MTR2G	WDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



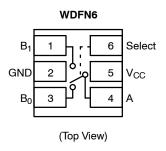


Figure 1. Pin Assignment & Logic Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	-0.5 to +7.0	V
DC Switch Voltage (Note 1)	V _{IS}	-0.5 to V _{CC} + 0.5	V
DC Input Voltage (Note 1)	V _{IN}	-0.5 to + 7.0	V
DC Input Diode Current @ V _{IN} < 0 V	lık	-50	mA
DC Output Current	I _{OUT}	128	mA
DC V _{CC} or Ground Current	I _{CC} /I _{GND}	+100	mA
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature Under Bias	T _J	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	T _L	260	°C
Power Dissipation @ +85°C	P _D	180	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	V _{CC}	1.65	5.5	V
Select Input Voltage	V _{IN}	0	5.5	V
Switch Input Voltage	V _{IS}	0	V _{CC}	V
Output Voltage	V _{OUT}	0	V _{CC}	V
Operating Temperature	T _A	-55	+125	°C
Input Rise and Fall Time Control Input V_{CC} = 2.3 V-3.6 V Control Input V_{CC} = 4.5 V-5.5 V	t _r , t _f	0	10 5.0	ns/V
Thermal Resistance	$\theta_{\sf JA}$	-	350	°C/W

^{2.} Select input must be held HIGH or LOW, it must not float.

^{1.} The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

DC ELECTRICAL CHARACTERISTICS - NLASB3157

			V _{CC}		T _A = +25°C	;	T _A = -40°		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage		1.65-1.95 2.3-5.5				0.75 V _{CC} 0.7 V _{CC}		٧
V _{IL}	LOW Level Input Voltage		1.65-1.95 2.3-5.5					0.25 V _{CC} 0.3 V _{CC}	٧
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0–5.5		±0.05	± 0.1		±1	μΑ
I _{OFF}	OFF State Leakage Current	$0 \le A, B \le V_{CC}$	1.65–5.5		±0.05	±0.1		±1	μΑ
R _{ON}	Switch On Resistance (Note 3)	$V_{IN} = 0$ V, $I_O = 30$ mA $V_{IN} = 2.4$ V, $I_O = -30$ mA $V_{IN} = 4.5$ V, $I_O = -30$ mA	4.5		3.0 5.0 7.0			7.0 12 15	Ω
		V _{IN} = 0 V, I _O = 24 mA V _{IN} = 3 V, I _O = -24 mA	3.0		4.0 10			9.0 20	Ω
		$V_{IN} = 0 \text{ V}, I_O = 8 \text{ mA}$ $V_{IN} = 2.3 \text{ V}, I_O = -8 \text{ mA}$	2.3		5.0 13			12 30	Ω
		V _{IN} = 0 V, I _O = 4 mA V _{IN} = 1.65 V, I _O = -4 mA	1.65		6.5 17			20 50	Ω
I _{CC}	Quiescent Supply Current All Channels ON or OFF	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$	5.5			1.0		10	μΑ
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range (Note 3) (Note 7)	$\begin{split} I_A &= -30 \text{ mA}, \ 0 \le V_{Bn} \\ &\le V_{CC} \\ I_A &= -24 \text{ mA}, \ 0 \le V_{Bn} \end{split}$	4.5 3.0					25 50	Ω
		\leq V _{CC} I _A = -8 mA, 0 \leq V _{Bn} \leq V _{CC}	2.3					100	
		$I_A = -4 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	1.65					300	
ΔR_{ON}	On Resistance Match Between Channels (Note 3) (Note 4) (Note 5)	$\begin{split} I_A &= -30 \text{ mA}, V_{Bn} = 3.15 \\ I_A &= -24 \text{ mA}, V_{Bn} = 2.1 \\ I_A &= -8 \text{ mA}, V_{Bn} = 1.6 \\ I_A &= -4 \text{ mA}, V_{Bn} = 1.15 \end{split}$	4.5 3.0 2.3 1.65		0.15 0.2 0.5 0.5				Ω
R _{flat}	On Resistance Flatness (Note 3)	$I_A = -30 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	5.0		6.0				Ω
	(Note 4) (Note 6)	$I_A = -24 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	3.3		12				
		$I_A = -8 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	2.5		28				
		$I_A = -4 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	1.8		125				

Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
 Parameter is characterized but not tested in production.

ΔR_{ON} = R_{ON} max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
 Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

^{7.} Guaranteed by Design.

AC ELECTRICAL CHARACTERISTICS - NLASB3157

			V _{CC}	T,	գ = +25°	$T_A = -40^{\circ}C$ to		C to +85°C		Figure
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Unit	Number
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus (Note 9)	V _I = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					1.2 0.8 0.3	ns	Figures 2, 3
t _{PZL} t _{PZH}	Output Enable Time Turn On Time (A to B _n)	$V_I = 2 \times V_{CC}$ for t_{PZL} $V_I = 0$ V for t_{PZH}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 7.6 5.7	ns	Figures 2, 3
t _{PLZ} t _{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	$V_I = 2 \times V_{CC}$ for t_{PLZ} $V_I = 0$ V for t_{PHZ}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 5.3 3.8	ns	Figures 2, 3
t _{B-M}	Break Before Make Time (Note 8)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4
Q	Charge Injection (Note 8)	C_L = 0.1 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	5.0 3.3		7.0 3.0				pC	Figure 5
OIRR	Off Isolation (Note 10)	$R_L = 50 \Omega$ f = 10 MHz	1.65-5.5		-57				dB	Figure 6
Xtalk	Crosstalk	$R_L = 50 \Omega$ f = 10 MHz	1.65-5.5		-54				dB	Figure 7
BW	-3 dB Bandwidth	R _L = 50 Ω	1.65-5.5		250				MHz	Figure 10
THD	Total Harmonic Distortion (Note 8)	$R_L = 600 \Omega$ 0.5 V_{P-P} f = 600 Hz to 20 kHz	5.0		0.011				%	

CAPACITANCE - NLASB3157 (Note 11)

Symbol	Parameter	Test Conditions	Тур	Max	Unit	Figure Number
C _{IN}	Select Pin Input Capacitance	V _{CC} = 0 V	2.3		pF	
C _{IO-B}	B Port Off Capacitance	V _{CC} = 5.0 V	6.5		pF	Figure 8
C _{IOA-ON}	A Port Capacitance when Switch is Enabled	V _{CC} = 5.0 V	18.5		pF	Figure 9

^{8.} Guaranteed by Design.

^{9.} This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

^{10.} Off Isolation = $20 \log_{10} [V_A/V_{Bn}]$. 11. $T_A = +25^{\circ}C$, f = 1 MHz, Capacitance is characterized but not tested in production.

APPENDIX A

DC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

			V _{CC}	7	$T_A = +25^{\circ}C$		T _A = -55°C to +125°C		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V _{CC} 0.7 V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V _{CC} 0.3 V _{CC}	V
I _{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	0–5.5		±0.05	±0.1		±1	μΑ
l _{OFF}	OFF State Leakage Current	$0 \le A, B \le V_{CC}$	1.65–5.5		±0.05	±0.1		±1	μΑ
R _{ON}	Switch On Resistance (Note 12)	$V_{IN} = 0 \text{ V, } I_O = 30 \text{ mA}$ $V_{IN} = 2.4 \text{ V, } I_O = -30 \text{ mA}$ $V_{IN} = 4.5 \text{ V, } I_O = -30 \text{ mA}$	4.5		3.0 5.0 7.0			8.5 13.0 15.0	Ω
		V _{IN} = 0 V, I _O = 24 mA V _{IN} = 3 V, I _O = -24 mA	3.0		4.0 10			11 20	
		$V_{IN} = 0 \text{ V, } I_O = 8 \text{ mA}$ $V_{IN} = 2.3 \text{ V, } I_O = -8 \text{ mA}$	2.3		5.0 13			12 30	
		V _{IN} = 0 V, I _O = 4 mA V _{IN} = 1.65 V, I _O = -4 mA	1.65		6.5 17			20 50	
I _{CC}	Quiescent Supply Current All Channels ON or OFF	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$	5.5			1.0		10	μΑ
	Analog Signal Range		V _{CC}	0		V _{CC}	0	V _{CC}	V
R _{RANGE}	On Resistance Over Signal Range	$\begin{split} I_A &= -30 \text{ mA, } 0 \leq V_{Bn} \leq V_{CC} \\ I_A &= -24 \text{ mA, } 0 \leq V_{Bn} \leq V_{CC} \end{split}$	4.5					25	Ω
	(Note 12) (Note 14)	$I_A = -8 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	3.0					50	
		$I_A = -4 \text{ mA}, 0 \le V_{Bn}$ $\le V_{CC}$	2.3					100	
			1.65					300	

^{12.} Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

^{13.} Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

^{14.} Guaranteed by Design.

^{*} For $\Delta R_{ON},\,R_{FLAT},\,Q,\,OIRR,\,Xtalk,\,BW,\,THD,\,and\,CIN\,\,see\,\,-40^{\circ}C$ to 85°C section.

APPENDIX A AC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS - NLVASB3157

			V _{CC}	T,	$T_A = +25^{\circ}C$ $T_A = -55^{\circ}C \text{ to } +125^{\circ}$		to +125°C		Figure	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Unit	Number
t _{PHL} t _{PLH}	Propagation Delay Bus to Bus (Note 16)	V _I = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					1.2 0.8 0.3	ns	Figures 2, 3
[†] PZL [†] PZH	Output Enable Time Turn On Time (A to B _n)	$V_I = 2 \times V_{CC}$ for t_{PZL} $V_I = 0$ V for t_{PZH}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 9.0 7.0	ns	Figures 2, 3
[†] PLZ [†] PHZ	Output Disable Time Turn Off Time (A Port to B Port)	$V_I = 2 \times V_{CC}$ for t_{PLZ} $V_I = 0$ V for t_{PHZ}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 6.5 5.0	ns	Figures 2, 3
t _{B-M}	Break Before Make Time (Note 15)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4

^{15.} Guaranteed by Design.16. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

^{*} For ΔR_{ON} , R_{FLAT} , Q, OIRR, Xtalk, BW, THD, and CIN see -40°C to 85°C section.

AC LOADING AND WAVEFORMS

NOTE: Input driven by 50 Ω source terminated in 50 Ω

NOTE: C_L includes load and stray capacitance

NOTE: Input PRR = 1.0 MHz; t_W = 500 ns

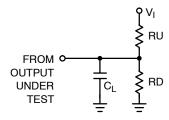
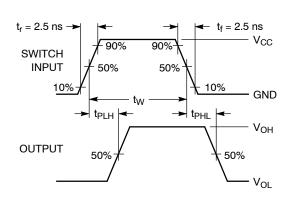


Figure 2. AC Test Circuit



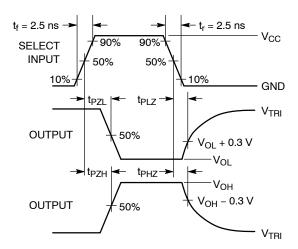
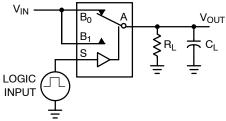


Figure 3. AC Waveforms



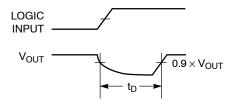


Figure 4. Break Before Make Interval Timing

AC LOADING AND WAVEFORMS

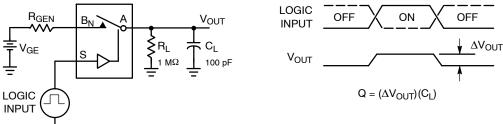


Figure 5. Charge Injection Test

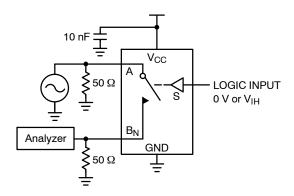


Figure 6. Off Isolation

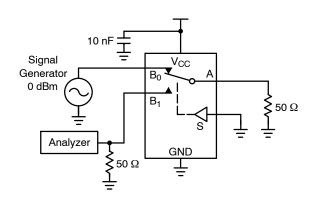


Figure 7. Crosstalk

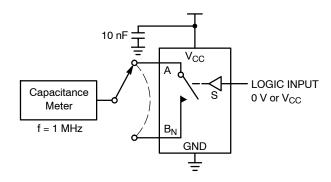


Figure 8. Channel Off Capacitance

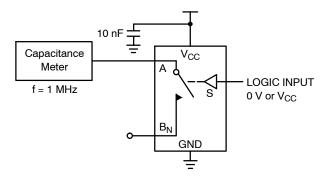


Figure 9. Channel On Capacitance

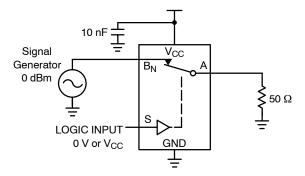
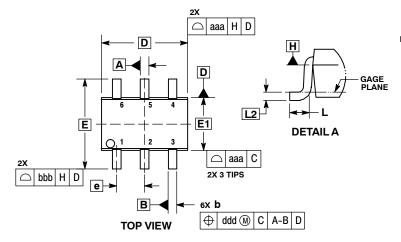


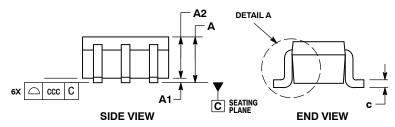
Figure 10. Bandwidth

PACKAGE DIMENSIONS

SC-88/SOT-363/SC-70 **DF SUFFIX**

CASE 419B-02 **ISSUE Y**



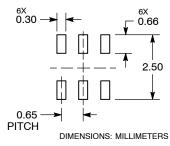


- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS D AND C APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION D AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. RADIUS OF THE FOOT.

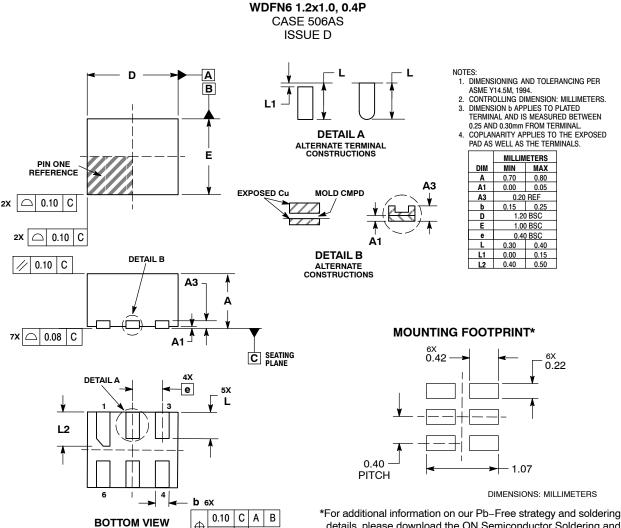
	MIL	LIMETE	ERS	INCHES				
DIM	MIN	NOM	MAX	MIN	NOM	MAX		
Α			1.10			0.043		
A1	0.00		0.10	0.000		0.004		
A2	0.70	0.90	1.00	0.027	0.035	0.039		
b	0.15	0.20	0.25	0.006	0.008	0.010		
С	0.08	0.15	0.22	0.003	0.006	0.009		
D	1.80	2.00	2.20	0.070	0.078	0.086		
Е	2.00	2.10	2.20	0.078	0.082	0.086		
E1	1.15	1.25	1.35	0.045	0.049	0.053		
е	(0.65 BS	С	0	.026 BS	С		
L	0.26	0.36	0.46	0.010	0.014	0.018		
L2	0.15 BSC			0.006 BSC				
aaa		0.15			0.006			
bbb		0.30		0.012				
ccc		0.10		0.004				
ddd		0.10			0.004			

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS



details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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