MOTIX™ TLE9868QXB20

Arm® Cortex®-M3 microcontroller with LIN and H-bridge MOSFET driver for automotive applications
BF, UH, and UI step

AEC Qualified RoHS

Features

- 32-bit Arm®* Cortex®-M3 core
- 128 KB flash
- 4 KB RAM
- On-chip OSC and PLL for clock generation
- MOSFET driver including charge pump for H-Bridge motor application
- 1 LIN 2.2 transceiver
- Two differential 14-bit sigma-delta ADCs
- Single power supply from 5.5 V to 28 V
- Temperature range T_j = -40°C to +150°C



VQFN-48-31



VQFN-48-37



VQFN-48-79

Potential applications

- Wiper
- Auxiliary pumps
- Fans
- Window lift
- Sunroof
- Tailgate

Product validation

Qualified for automotive applications.
Product validation according to AEC-Q100/101.

Description

Type	Orderable part number (OPN)	Design step	Package	Marking
TLE9868QXB20	TLE9868QXB20XUMA2	BF	VQFN-48-31	
TLE9868QXB20	TLE9868QXB20XUMA4	UH	VQFN-48-37, VQFN-48-79	
TLE9868QXB20	TLE9868QXB20XUMA5	UI	VQFN-48-37, VQFN-48-79	

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1 Overview

Summary of Features

- 32-bit Arm® Cortex®-M3 core
  - Up to 20 MHz clock frequency
  - One clock per machine cycle architecture
- On-chip memory
  - 128 KB flash including
  - 4 KB EEPROM (emulated in flash)
  - 512 byte 100-time programmable memory (100TP)
  - 4 KB RAM
  - Boot ROM for startup firmware and flash routines
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- MOSFET driver including charge pump for H-Bridge Motor Application
- 10 general-purpose I/O Ports (GPIO)
- 5 analog inputs, 10-bit A/D Converter (ADC1)
- 2 differential Sigma Delta 14-bit ADC (ADC3/4)
- 16-bit timers - GPT12, Timer2, Timer21, and Timer3
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full-duplex serial interfaces (UART) with LIN support (for UART1 only)
- 2 synchronous serial channels (SSC)
- On-chip debug support via 2-wire SWD
- 1 LIN 2.2 transceiver
- 1 high-voltage monitoring input
- Single power supply from 5.5 V to 27 V
- Extended power supply voltage range from 3 V to 28 V
- Low-dropout voltage regulators (LDO)
- 5 V voltage supply for external loads (e.g., Hall sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power-saving modes
  - MCU slow-down mode
  - Sleep mode
  - Cyclic wake-up sleep mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Short-circuit protection
- Loss of clock detection with fail-safe mode entry for low system power consumption
- Temperature range T_j = -40°C to +150°C
- Package VQFN-48 with LTI feature

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Overview

- Green package (RoHS compliant)
- AEC-qualified

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1.1 Abbreviations

The following acronyms and terms are used within this document. List see in **Table 1**.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture compare unit 6
CGU	Clock generation unit
CMU	Cyclic management unit
CP	Charge pump for MOSFET driver
DPP	Data post-processing
ECC	Error correction code
EEPROM	Electrically erasable programmable read only memory
EIM	Exceptional interrupt measurement
FSM	Finite state machine
GPIO	General-purpose input/output
H-Bridge	Half-bridge
ICU	Interrupt control unit
IEN	Interrupt enable
IIR	Infinite impulse response
LDM	Load instruction
LDO	Low-dropout voltage regulator
LIN	Local interconnect network
LSB	Least significant bit
LTI	Lead tip inspection
MCU	Microcontroller unit
MF	Measurement functions
MPU	Memory protection unit
MRST	Master receive, slave transmit
MSB	Most significant bit
MTSR	Master transmit, slave receive
MU	Measurement unit
NMI	Non-maskable interrupt
NVIC	Nested vector interrupt controller
NVM	Non-volatile memory
OPN	Orderable part number
OSC	Oscillator
OTP	One-time programmable
PBA	Peripheral bridge

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Table 1 Acronyms (cont'd)

Acronyms	Name
PCU	Power control unit
PD	Pull-down
PGU	Power supply generation unit
PLL	Phase-locked loop
PU	Pull-up
PWM	Pulse-width modulation
RAM	Random-access memory
RCU	Reset control unit
rfu	Reserved for future use
RMU	Reset management unit
ROM	Read-only memory
SCU-DM	System control unit – digital modules
SCU-PM	System control unit – power modules
SFR	Special function register
SOW	Short open window (for WDT)
SPI	Serial Peripheral Interface
SSC	Synchronous serial channel
STM	Store instruction
SWD	Arm® Serial Wire Debug
TCCR	Temperature compensation control register
TMS	Test mode select
TSD	Thermal shut-down
UART	Universal asynchronous receiver-transmitter
VBG	Voltage reference bandgap
VCO	Voltage-controlled oscillator
VPRE	Preregulator
WDT	Watchdog timer in SCU-DM
WDT1	Watchdog timer in SCU-PM
WMU	Wake-up management unit
100TP	100-time programmable

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2 Block diagram

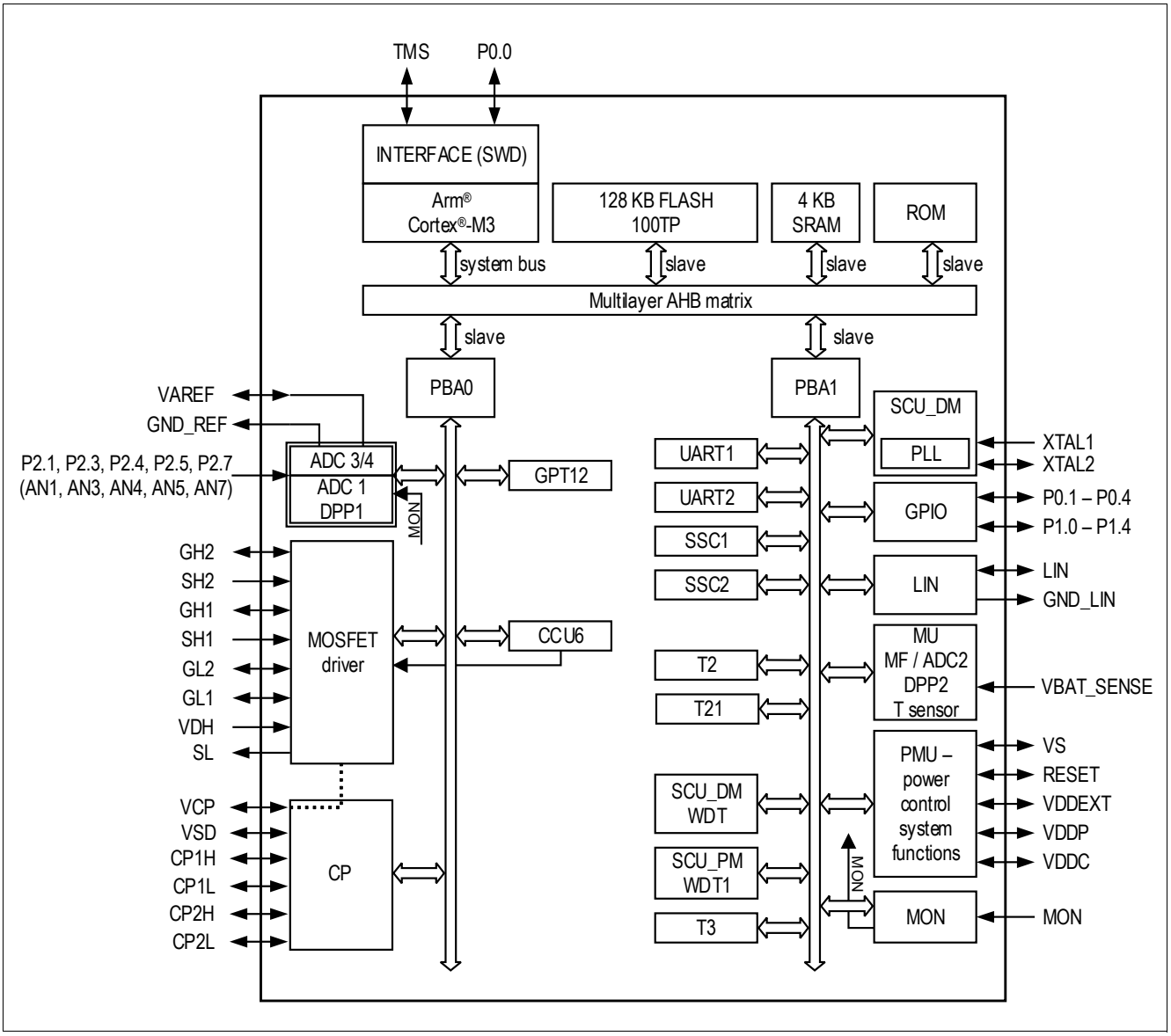


Figure 1 Block diagram

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3 Device pinout and pin configuration

3.1 Device pinout

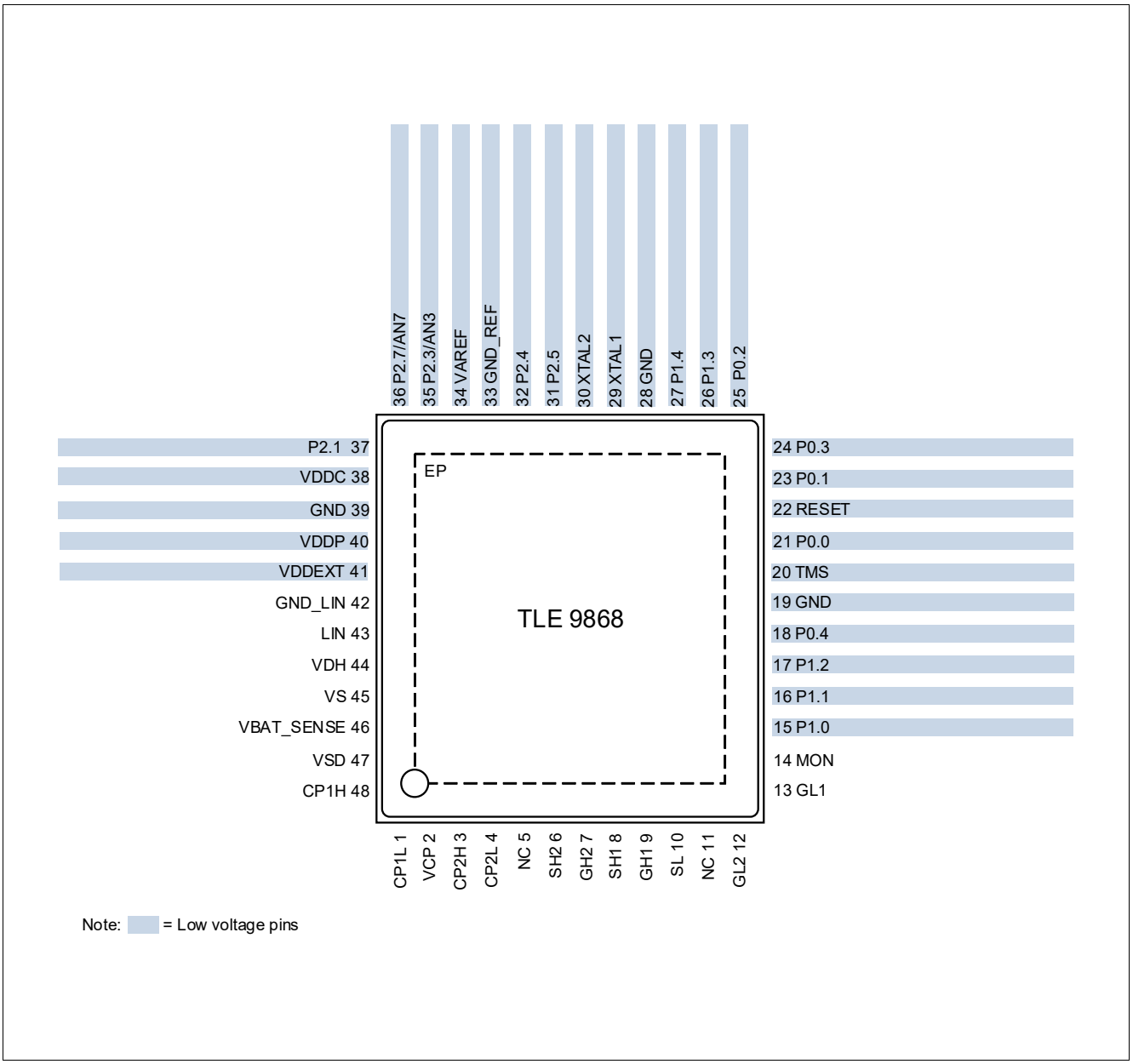


Figure 2 Device pinout

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3.2 Pin configuration

After a reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high-impedance state (Hi-Z)

The functions and default states of the TLE9868QXB20 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions are listed.

Table 2 Pin definitions and functions

Symbol	Pin number	Type	Reset state[1)]	Function	
P0				**Port 0** Port 0 is a 5-bit bidirectional general-purpose I/O port. Alternate functions can be assigned and are listed in the port description. The main functions are listed below.	
P0.0	21	I/O	I/PU	SWD	Serial wire debug clock
P0.1	23	I/O	I/PU	GPIO TxD_1	General-purpose I/O UART_1
P0.2	25	I/O	I/PD	GPIO MTSR_1	General-purpose I/O SSC_1 Master Transmit Slave Receive *Note: For a functional SWD connection, this GPIO must be tied to zero.*
P0.3	24	I/O	I/PU	GPIO SCLK_1	General-purpose I/O SSC_1 clock signal
P0.4	18	I/O	I/PD	GPIO GPIO	LIN_2 enable signal SSC_2 CS signal
P1				**Port 1** Port 1 is a 5-bit bidirectional general-purpose I/O port. Alternate functions can be assigned and are listed in the port description. The main functions are listed below.	
P1.0	15	I/O	I	GPIO SCLK_2	General-purpose I/O SSC_2 clock signal
P1.1	16	I/O	I	MTSR_2 TxD_2	SSC_2 master transmit slave receive UART_2 TxD
P1.2	17	I/O	I	MRST_2 RxD_2	SSC_2 master receive slave transmit UART_2 RxD

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Table 2 Pin definitions and functions (cont'd)

Symbol	Pin number	Type	Reset state[1)]	Function	
P1.3	26	I/O	I	GPIO GPIO	General-purpose I/O, used for inrush transistor SSC_1 chip select
P1.4	27	I/O	I	GPIO RxD_1	General-purpose I/O UART_1
P2				**Port 2** Port 2 is a 5-bit general-purpose input-only port. Alternate functions can be assigned and are listed in the port description. The main functions are listed below.	
P2.1	37	I	I	AN1 Pull-up	ADC analog input 1 (temperature) Strong Pull-Up for Inrush control
P2.3	35	I	I	AN3	ADC analog input 3 (sensor), ADC3+
P2.4	32	I	I	AN4 MRST_1	ADC analog input 4 (sensor), ADC4+ SSC_1 master receive slave transmit
P2.5	31	I	I	AN5 MRST_2 RxD_2	ADC analog input 5 (Sensor), ADC4- SSC_2 master receive slave transmit UART_2 RxD
P2.7	36	I	I	AN7	ADC analog input 7 (sensor or temperature), ADC3-
Power supply					
VS	45	P	–	Battery supply input	
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.	
VDDC	38	P	–	[3)]Core supply (1.5 V in Active mode). Do not connect external loads, but connect an external buffer capacitor.	
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)	
GND	5	P	–	GND analog	
GND	11	P	–	GND analog	
GND	19	P	–	GND digital	
GND	28	P	–	GND digital	
GND	39	P	–	GND analog	
Monitor input					
MON	14	I	–	High voltage monitor input	
LIN interface					
LIN	43	I/O	–	LIN bus interface input/output	
GND_LIN	42	P	–	LIN ground	
Charge pump					
CP1H	48	P	–	Charge pump capacity 1 high, connect external C	
CP1L	1	P	–	Charge pump capacity 1 low, connect external C	
CP2H	3	P	–	Charge pump capacity 2 high, connect external C	

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Table 2 Pin definitions and functions (cont'd)

Symbol	Pin number	Type	Reset state[1)]	Function
CP2L	4	P	–	Charge pump capacity 2 low, connect external C
VCP	2	P	–	Charge pump capacity
VSD	47	P	–	Battery supply input for charge pump
MOSFET driver				
VDH	44	P	–	Voltage drain high-side MOSFET driver
SH2	6	P	–	Source high-side FET 2
GH2	7	P	–	Gate high-side FET 2
SH1	8	P	–	Source high-side FET 1
GH1	9	P	–	Gate high-side FET 1
SL	10	P	–	Source low-side FET
GL2	12	P	–	Gate low-side FET 2
GL1	13	P	–	Gate low-side FET 1
Others				
GND_REF	33	P	–	GND for VAREF
VAREF	34	I/O	–	5V ADC1 reference voltage, optional buffer or input
XTAL1	29	I	–	External oscillator input
XTAL2	30	O	–	External oscillator output
TMS	20	I I/O	I/PD	TMS Test mode select input SWD Serial Wire Debug input/output
RESET	22	I/O	PU	Reset input, not available during Sleep mode
VBAT_SENSE	46	I	–	Battery supply voltage sense input
EP	–	–	–	Exposed pad, connect to GND

1) Only valid for digital IO.
2) Also named VDD5V.
3) Also named VDD1V5.

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4 Modes of operation

The TLE9868QXB20 highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost-effective clock that is particularly well suited for LIN communications. A LIN transceiver is available as a communication interface. Driver stages for an H-bridge with external MOSFET are integrated, featuring PWM capability, protection features, and a charge pump for operation at low supply voltage. A 10-bit SAR ADC and two differential 14-bit Sigma Delta ADCs are implemented for high-precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The microcontroller unit supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a LIN bus message, via the monitoring input, or using a programmable time period (cyclic wake-up).

The TLE9868QXB20 has several operation modes mainly to support low power consumption requirements.

Reset mode

The Reset mode is a transition mode used, e.g., during power-up of the device after a power-on reset, or after wake-up from Sleep mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep mode.

Active mode

In Active mode, all modules are activated and the TLE9868QXB20 is fully operational.

Sleep mode

The Sleep mode is a low-power mode. The transition to the low-power mode is performed by setting the corresponding bits in the MCU mode control register or in case of failure (see below). In Sleep mode the embedded microcontroller power supply is deactivated, allowing for the lowest system power consumption. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pin, or through cyclic wake-up.

Sleep mode in case of failure

Sleep mode is activated after 5 watchdog failures or in case of supply failure (5 times). In this case, MON is enabled as the wake source and cyclic wake-up is activated with 1 s of wait time.

Sleep mode with cyclic wake-up

The Cyclic Wake-Up mode is a special operating mode of the Sleep mode. The transition to Cyclic Wake-Up mode is performed by first setting the corresponding bits in the mode control register followed by the Sleep mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Sleep mode.

When using Sleep mode with cyclic wake-up, the voltage regulator is switched off and started again with the wake. A limited number of registers is buffered during sleep, and can be used by software, e.g., for counting sleep/wake cycles.

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Modes of operation

MCU Slow Down mode

In MCU Slow Down mode the MCU frequency is reduced to save power during operation. LIN communication is still possible. LS MOSFET can be activated.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 3 Power Mode Configurations

Module/function	Active mode	Slow Down mode	Sleep mode	Comment
VDDEXT	ON/OFF	ON/OFF	OFF	–
VDDP	ON	ON	OFF	–
VDDC	ON	ON	OFF	–
Bridge Driver	ON/OFF	LS FET ON/OFF	OFF	–
LIN TRx	ON/OFF	ON/OFF	Wake-up only/ OFF	–
VS sense	ON/OFF brownout detection	ON/OFF brownout detection	POR on VS	Brownout det. done in PCU
VBAT_SENSE	ON/OFF	ON/OFF	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	ON	OFF	–
CYCLIC WAKE	n.a.	n.a.	Cyclic wake-up/ OFF	–
Measurement	ON[1)]	ON[1)]	OFF	–
MCU	ON	Slow-down	OFF	–
Peripherals	ON	Slow-down	OFF	–
CLOCK GEN (MC)	ON	Scaled down	OFF	–
LP_CLK (18 MHz)	ON	ON	OFF	WDT1
LP_CLK2 (100 kHz)	ON	ON	ON/OFF	For cyclic wake-up

1) May not be switched off due to safety reasons.

Wake-up source prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless, all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. This is to ensure that no wake-up event is lost.

As the default wake-up source, the MON input is activated after power-on reset only. Additionally, the device is in Cyclic Wake-Up mode with the configurable dead time setting.

Wake-up levels and transitions

The wake-up can be triggered by rising, falling, or both signal edges for the monitor input, GPIOs, by LIN, or by cyclic wake-up.

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5 Power management unit (PMU)

5.1 Features

- System mode control (startup, sleep and active)
- Power management (cyclic wake-up)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail-safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). The power management unit is designed to ensure fail-safe behavior of the system IC by controlling all system modes, including the corresponding transitions. Additionally, the PMU provides well-defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functions, especially the reset behavior of the embedded MCU. All these functions are controlled by a state machine. The system master function of the PMU uses an independent logic supply and system clock. For this reason, the PMU has an "Internal logic supply and system clock" module which works independently of the MCU clock.

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5.2.1 Block diagram

The following figure shows the structure of the power management unit. **Table 4** describes the submodules in more detail.

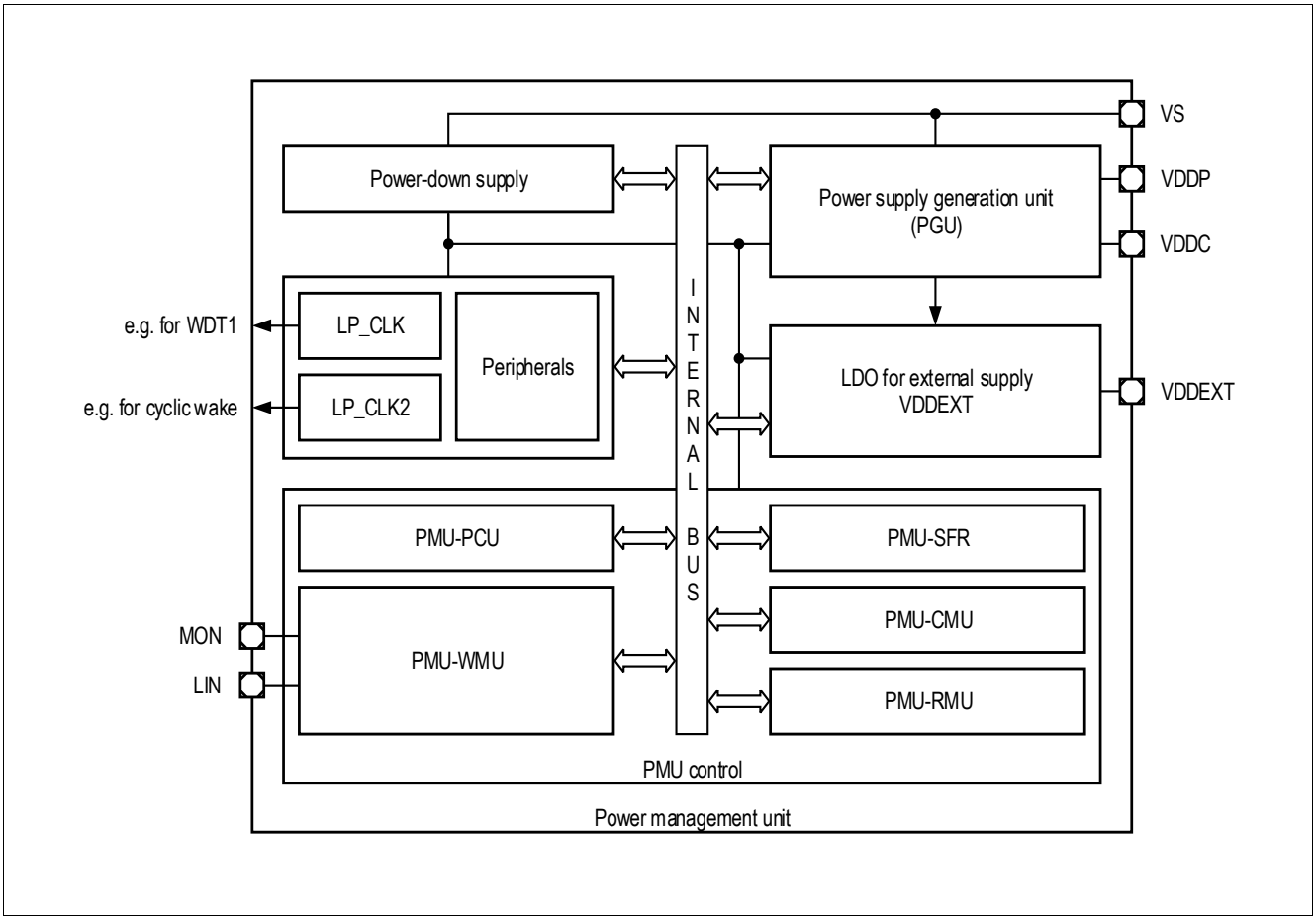


Figure 3 Power management unit block diagram

Table 4 Description of PMU submodules

Module name	Modules	Functions
Power-down supply	Independent supply voltage generation for PMU.	This supply is dedicated to the PMU to ensure an operation independently of generated power supplies (VDDP, VDDC).
LP_CLK (18 MHz)	• Clock source for all PMU submodules. • Backup clock source for the system. • Clock source for WDT1.	This ultra-low-power oscillator generates the clock for the PMU. This clock is also used as the backup clock for the system in case of PLL clock failures and as an independent clock source for WDT1.
LP_CLK2 (100 kHz)	Clock source for PMU.	This ultra-low-power oscillator generates the clock for the PMU in the cyclic modes.
Peripherals	Peripheral blocks of PMU.	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

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Table 4 Description of PMU submodules (cont'd)

Module name	Modules	Functions
Power supply generation unit (PGU)	Voltage regulators for VDDP and VDDC.	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g., sensors).	This voltage regulator is a dedicated supply for external modules.
PMU-SFR	All extended special function registers that are relevant to the PMU.	This module contains all registers needed to control and monitor the PMU.
PMU-PCU	Power control unit of the PMU.	This block is responsible for controlling all power-related actions within the PGU module. It also contains all regulator-related diagnostics such as undervoltage and overvoltage detection as well as overcurrent and short-circuit diagnostics.
PMU-WMU	Wake-up management unit of the PMU.	This block is responsible for controlling all actions related to wake-up within the PMU module.
PMU-CMU	Cyclic management unit of the PMU.	This block is responsible for controlling all actions in cyclic mode.
PMU-RMU	Reset management unit of the PMU.	This block generates resets triggered by the PMU, such as undervoltage or short-circuit reset, and passes all resets to the relevant modules and their registers.

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5.2.2 PMU modes overview

The following state diagram shows the available modes of the device.

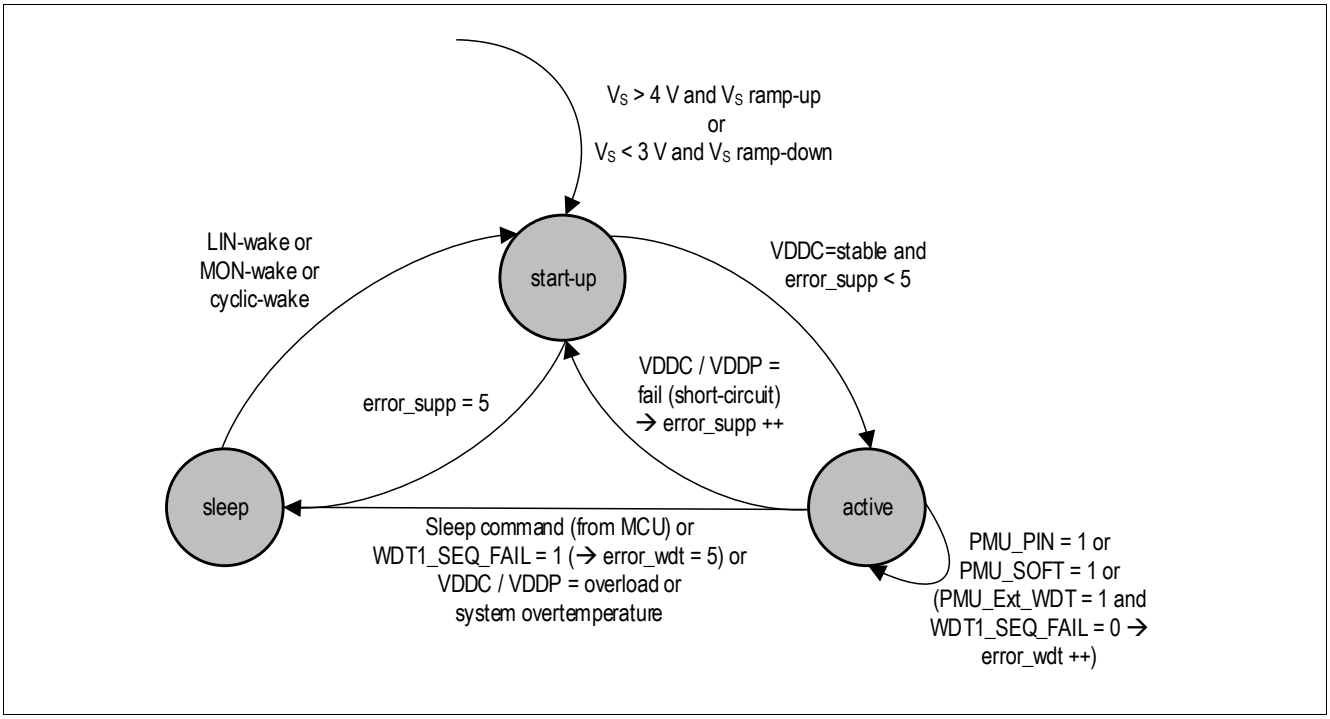


Figure 4 Power management unit system modes

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5.3 Power supply generation unit (PGU)

5.3.1 Voltage regulator 5.0 V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. LIN transceiver).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (undervoltage reset, V_{DDPUV})
- Preregulator for the VDDC regulator
- GPIO supply
- Pull-down current source at the output for Sleep mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

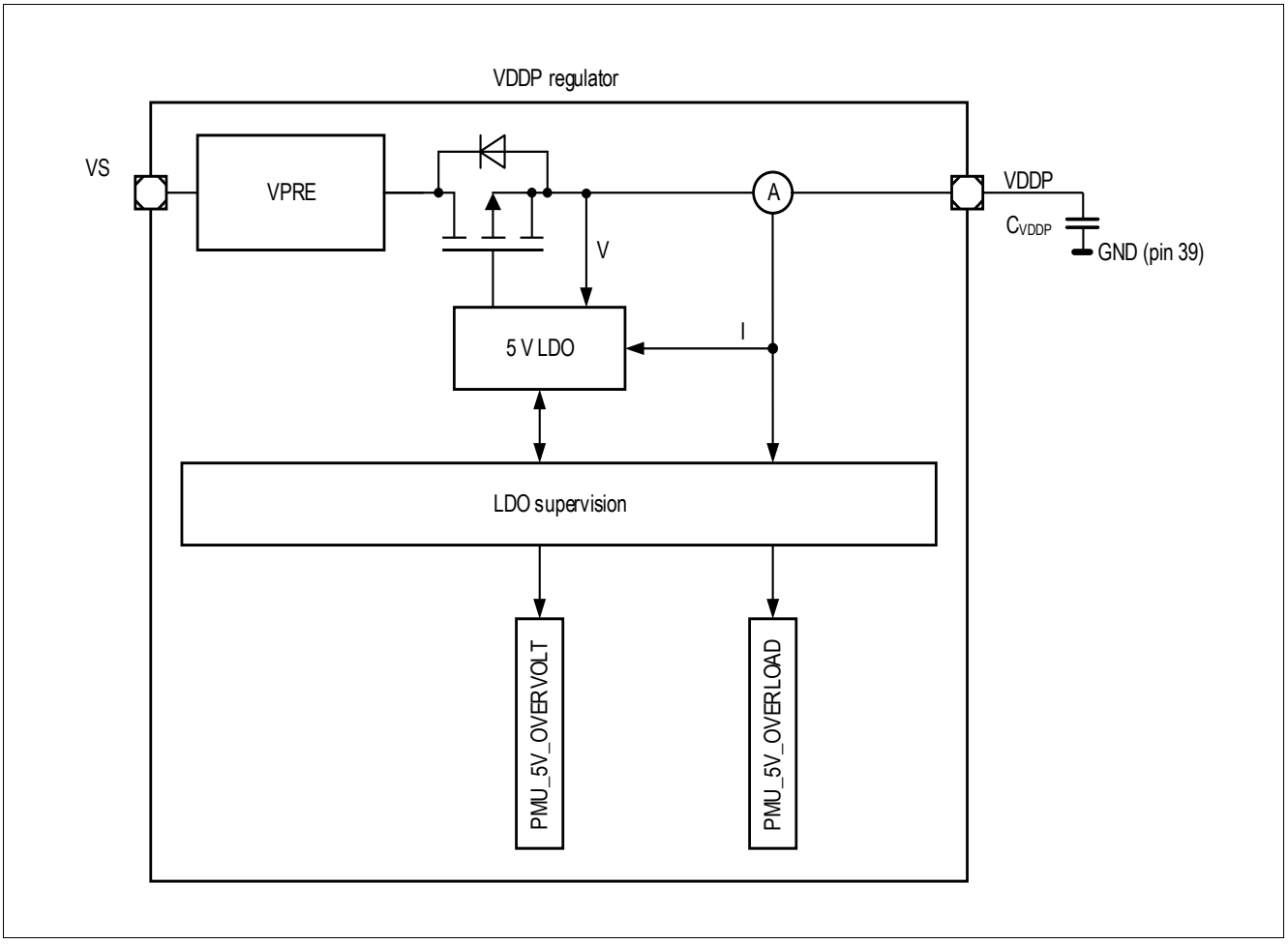


Figure 5 Module block diagram of the VDDP voltage regulator

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5.3.2 Voltage regulator 1.5 V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, the digital peripherals, and other internal analog 1.5 V functions (e.g., ADC2) of the chip.

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset
- Pull-down current source at the output for Sleep mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

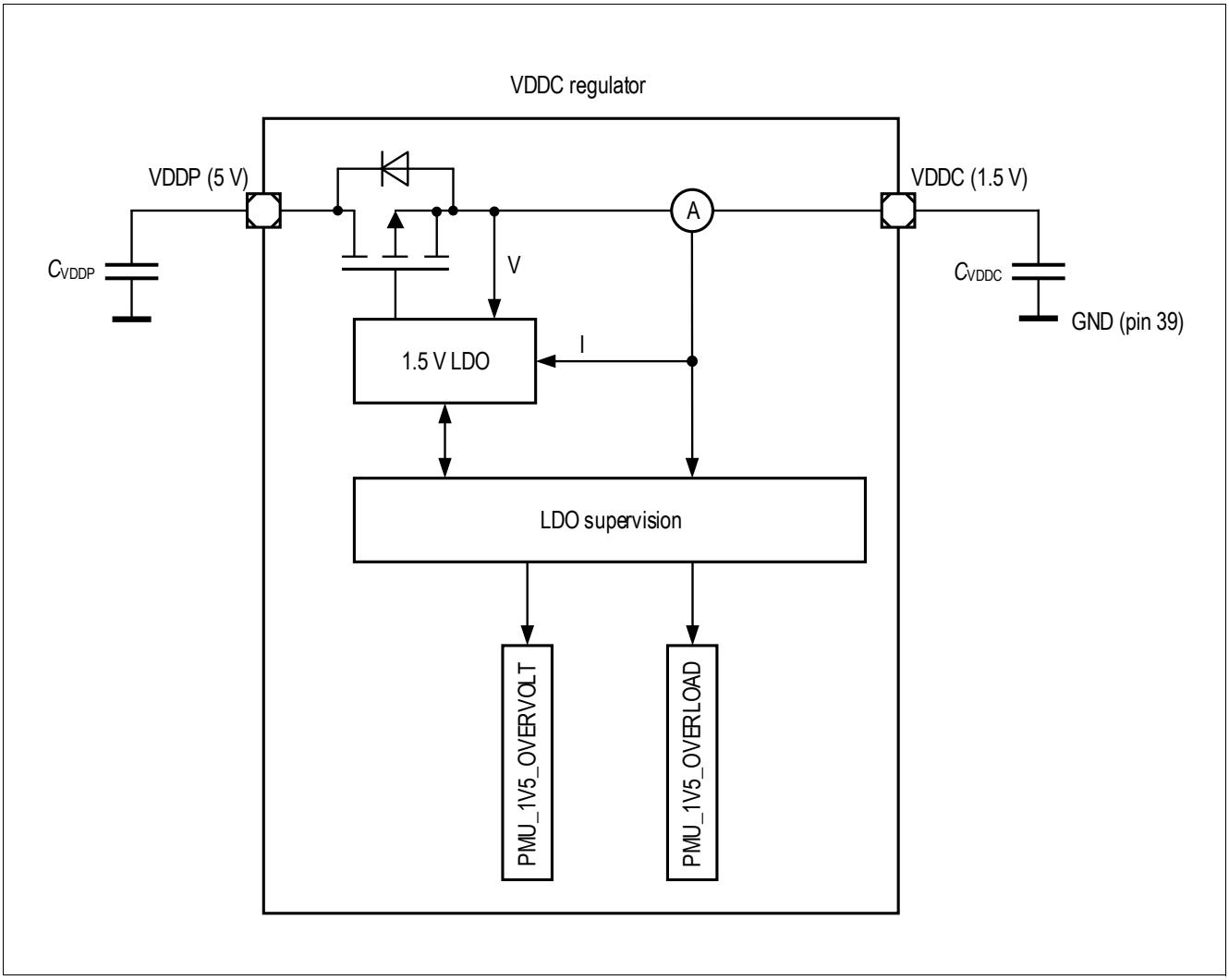


Figure 6 Module block diagram of the VDDC voltage regulator

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5.3.3 External voltage regulator 5.0 V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used, e.g., to supply an external sensor, LEDs, or potentiometers. VDDEXT can be used as reference for ADC3/4.

Features

- Switchable +5 V, low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Pull-down current source at the output for Sleep mode only (typ. 100 µA)

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

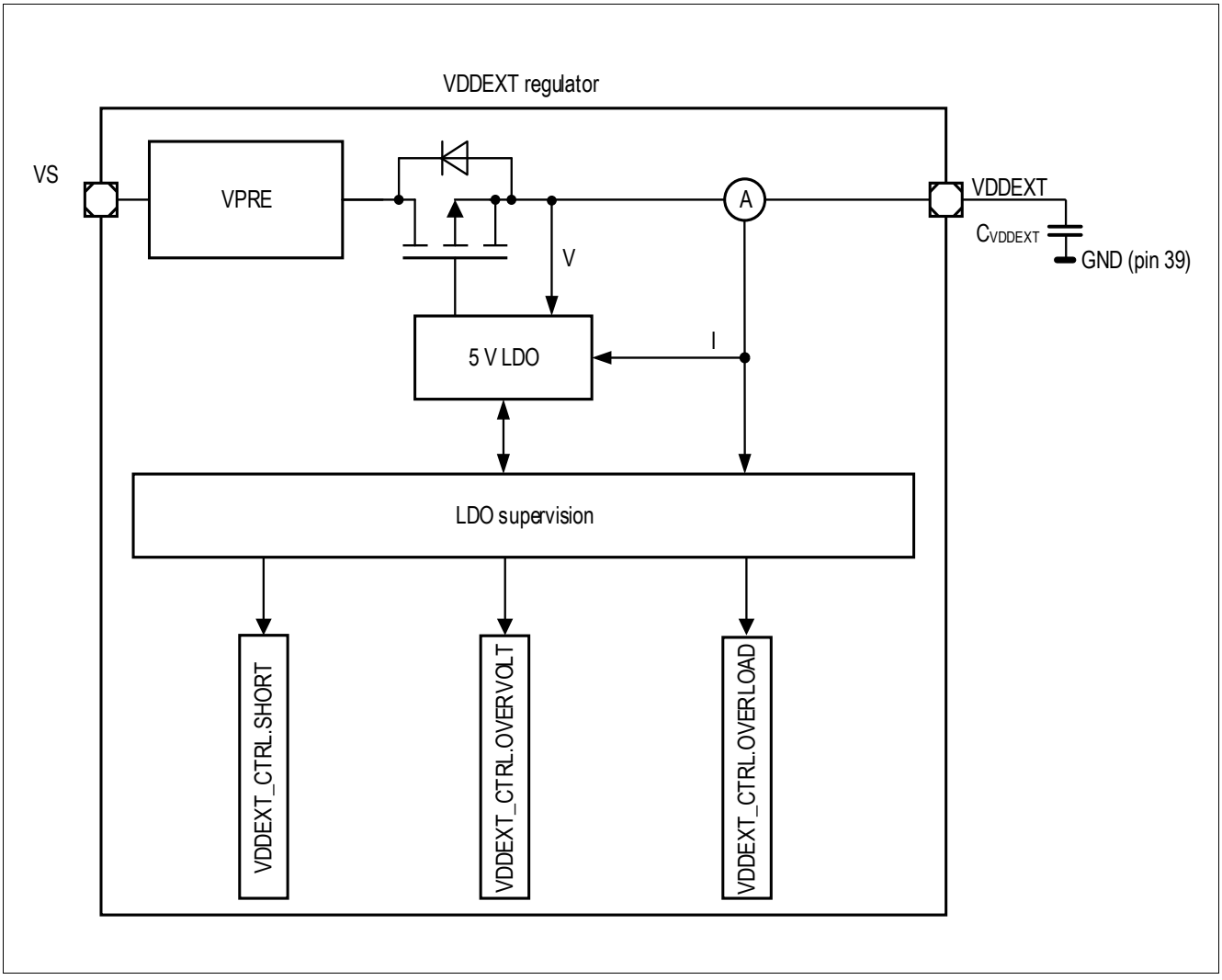


Figure 7 Module block diagram of the external voltage regulator

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6 System control unit – digital modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (Active mode, Sleep mode)
- Enabling interrupts for many system peripherals
- General-purpose input/output control
- Debug mode control of system peripherals

6.2 Introduction

The system control unit (SCU) supports all central control tasks in the TLE9868QXB20. The SCU is made up of the following submodules:

- Clock system and control
- Reset control
- Power management
- Interrupt management
- General port control
- Flexible peripheral management
- Module suspension control
- Watchdog timer
- Error detection and correction in data memory
- Miscellaneous control

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6.2.1 Block diagram

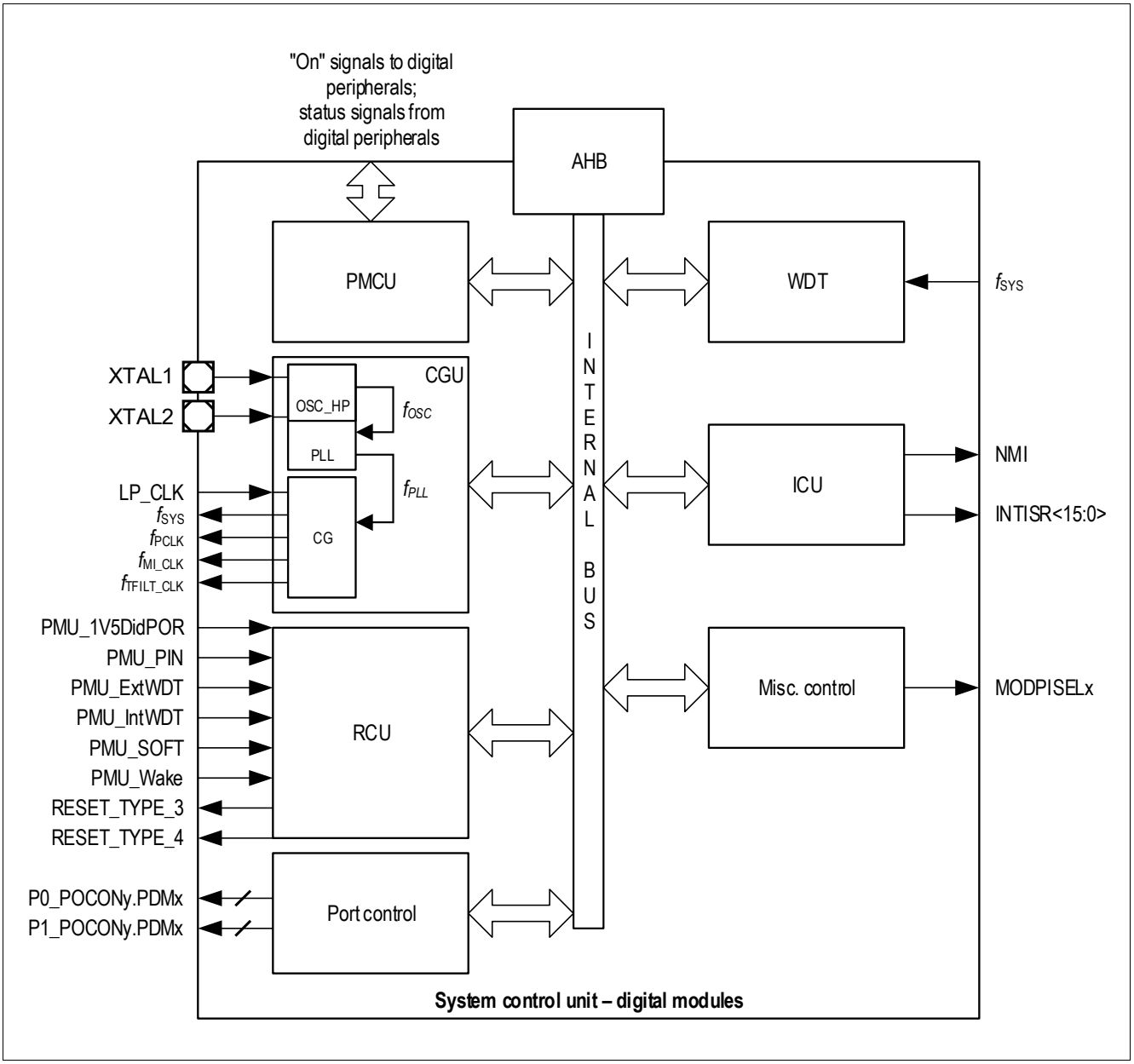


Figure 8 System control unit – digital modules block diagram

AHB (Advanced High-Performance Bus)

PMCU (power module control unit)

WDT (watchdog timer in SCU-DM)

- f_{SYS}: System clock

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System control unit – digital modules (SCU-DM)

CGU (clock generation unit)

- f_{SYS}: System clock
- f_{PCLK}: Peripheral clock
- f_{MI_CLK}: Measurement interface clock
- f_{TFILT_CLK}: Analog module filter clock
- LP_CLK Clock source for all PMU submodules and WDT1

ICU (interrupt control unit)

- NMI (non-maskable interrupt)
- INTISR<15,13:4,1,0> External interrupt signals

RCU (reset control unit)

- PMU_1V5DidPOR Undervoltage reset of power-down supply
- PMU_PIN Reset generated by reset pin
- PMU_ExtWDT WDT1 reset
- PMU_IntWDT WDT (SCU) reset
- PMU_SOFT Software reset
- PMU_Wake Sleep mode exit with reset
- RESET_TYPE_3 Peripheral reset (contains all resets)
- RESET_TYPE_4 Peripheral reset (without SOFT and WDT reset)

Port control

- P0_POCONy.PDMx Driver strength control
- P1_POCONy.PDMx Driver strength control

Miscellaneous control

- MODPISELx mode selection registers for UART (source section) and timer (trigger or count selection)

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6.3 Clock generation unit

The clock generation unit (CGU) enables a flexible clock generation for the TLE9868QXB20. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9868QXB20 consists of one oscillator circuit (OSC_HP), a phase-locked loop (PLL) module with an internal oscillator (OSC_PLL), and a clock control unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from one of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low-precision clock f_{LP_CLK} (hardware-enabled for startup after reset and during power-down wake-up sequence)

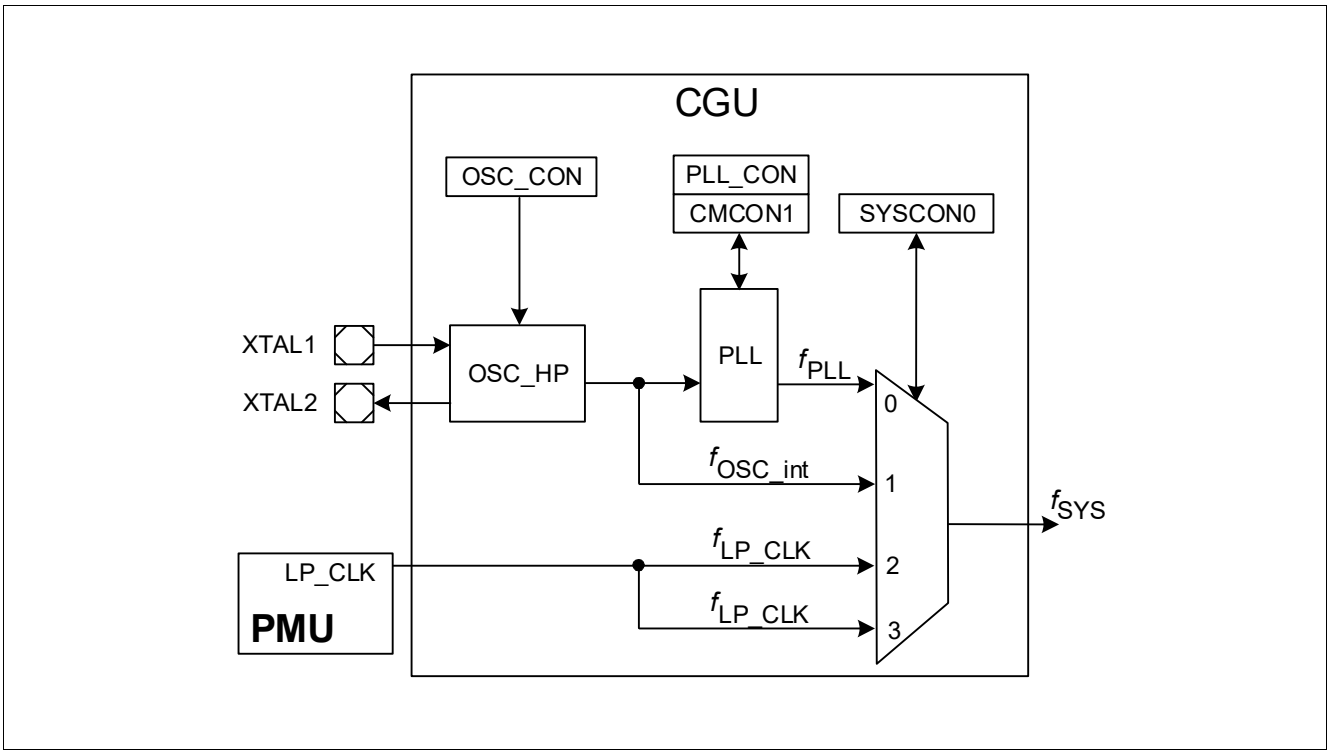


Figure 9 Clock generation unit block diagram

The following sections describe the different parts of the CGU.

6.3.1 Low-precision clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9868QXB20 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user-configurable.

6.3.2 High-precision oscillator circuit (OSC_HP)

The high-precision oscillator circuit, designed to work with either an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input and XTAL2 as the output.

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6.3.2.1 External Input Clock mode

When the clock signal is supplied directly – that is, not using an external crystal and bypassing the oscillator – the input frequency needs to be equal to or greater than 4 MHz if the PLL VCO part is used.

When an external clock signal is used, it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to the XTAL1 and XTAL2 pins. It normally consists of two load capacitances, C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative-resistance method. The load cap values listed in **Table 5** can be used as starting points for the evaluation:

Table 5 External CAP capacitors

Fundamental mode crystal frequency (approx., MHz)	Load caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

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7 System control unit – power modules (SCU-PM)

7.1 Features

- Clock watchdog unit (CWU): Supervises all clocks with NMI signaling relevant to power modules.
- Interrupt control unit (ICU): All interrupt flags and status flags with system relevance.
- Power control unit (PCU): Takes over control when device enters and exits Sleep mode.
- External watchdog (WDT1): Independent system watchdog for monitoring system activity.

7.2 Introduction

7.2.1 Block diagram

The system control unit of the power modules consists of the submodules in the figure shown below:

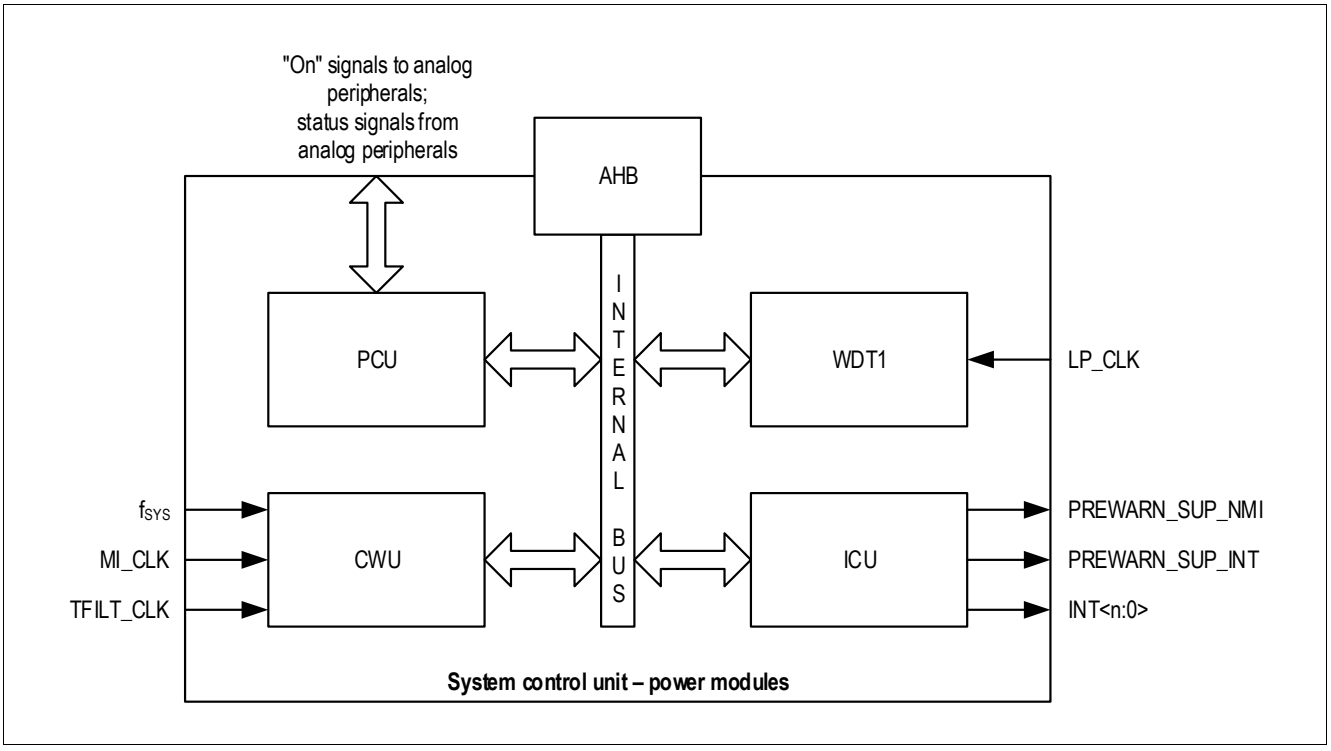


Figure 10 Block diagram of system control unit – power modules

AHB (Advanced High-performance Bus)

CWU (clock watchdog unit)

- f_{sys}: System frequency
- MI_CLK: Measurement interface clock (analog clock), derived from f_{sys} using division factors 1/2/3/4
- TFILT_CLK: Clock used for digital filters, derived from f_{sys} using configurable division factors

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WDT1 (system watchdog)

- LP_CLK Clock source for all PMU submodules and WDT1

ICU (interrupt control unit)

- PREWARN_SUP_NMI Supply prewarning NMI request
- PREWARN_SUP_INT Supply prewarning interrupt
- Grouping of peripheral interrupts for external interupt nodes:
  - Grouping single peripheral interrupts for interrupt node INT<2> (measurement unit (MU))
  - Grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - Grouping single peripheral interrupts for interrupt node INT<10> (UART1-LIN transceiver)
  - Grouping single peripheral interrupts for interrupt node INT<14> (bridge driver)

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8 Arm® Cortex®-M3 core

8.1 Features

The key features of the Arm® Cortex®-M3 implemented are listed below.

Processor core: a low-gate-count core, with low-latency interrupt processing

- A subset of the Thumb®-2 instruction set
- Banked stack pointer (SP) only
- 32-bit hardware divide instructions, SDIV and UDIV (Thumb-2 instructions)
- Handler and thread modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, push/pop for low interrupt latency
- Automatic processor state saving and restoration for low-latency interrupt service routine (ISR) entry and exit
- Arm® architecture v7-M Style BE8/LE support
- Arm®v6 unaligned accesses

Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing

- Interrupts, configurable from 1 to 16
- Bits of priority (4)
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of preemptive interrupt levels and non-preemptive interrupt levels.
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state-saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, DCode, and system bus interface
- Memory access alignment
- Write buffer for buffering of write data

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8.2 Introduction

The Arm® Cortex®-M3 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Arm® Cortex® family processors, the Arm® Cortex®-M3 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Arm® Cortex®-M3 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block diagram

Figure 11 shows the functional blocks of the Arm® Cortex®-M3.

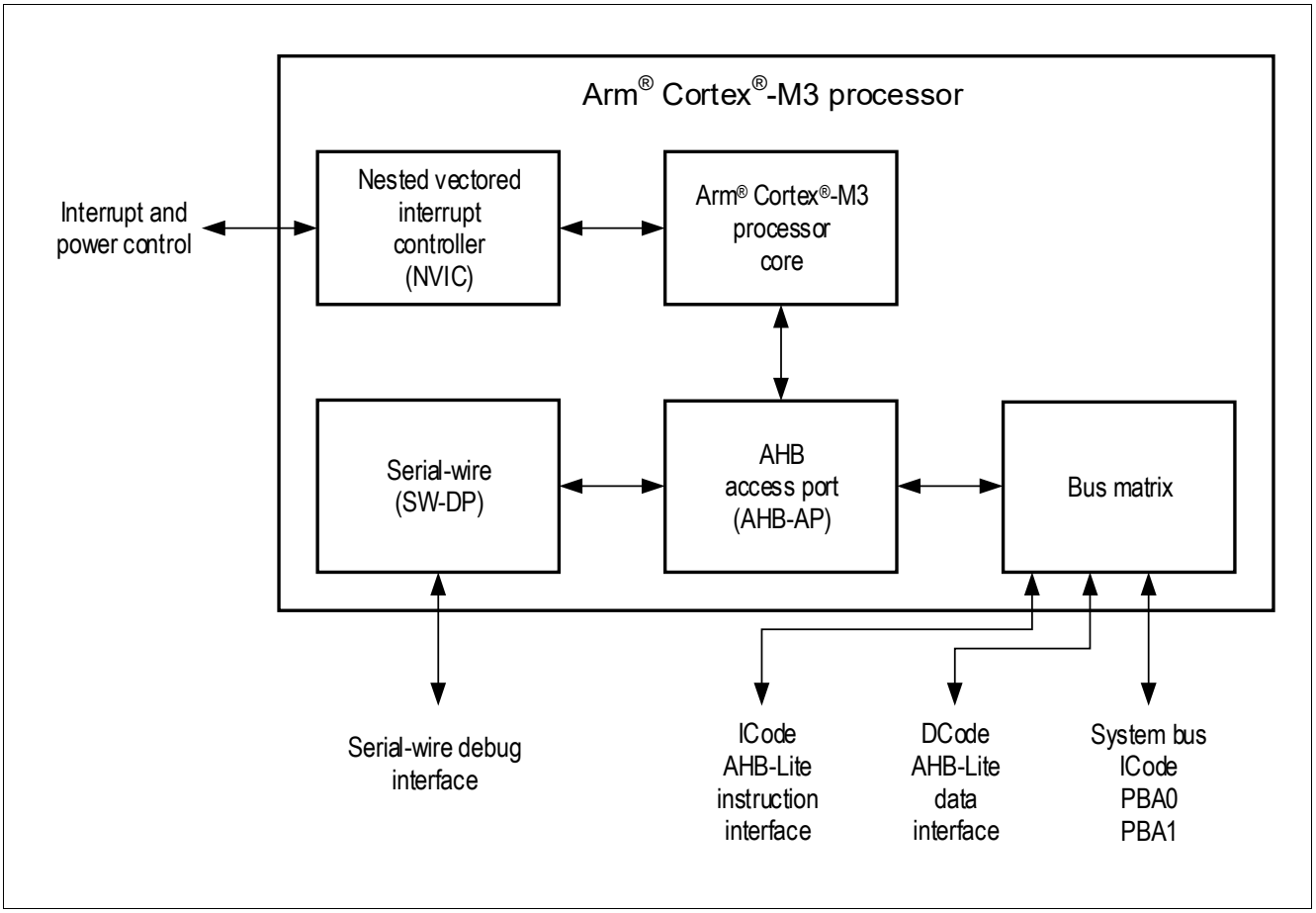


Figure 11 Arm® Cortex®-M3 block diagram

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9 Address space organization

The TLE9868QXB20 manipulates operands in the following memory spaces:

- 128 KB (incl. 4 KB emulated EEPROM) of flash memory in code space
- 32 KB boot ROM memory in code space (used for boot code and IP storage)
- 4 KB RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral space

The figure below shows the detailed address alignment of the TLE9868QXB20:

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Address space organization

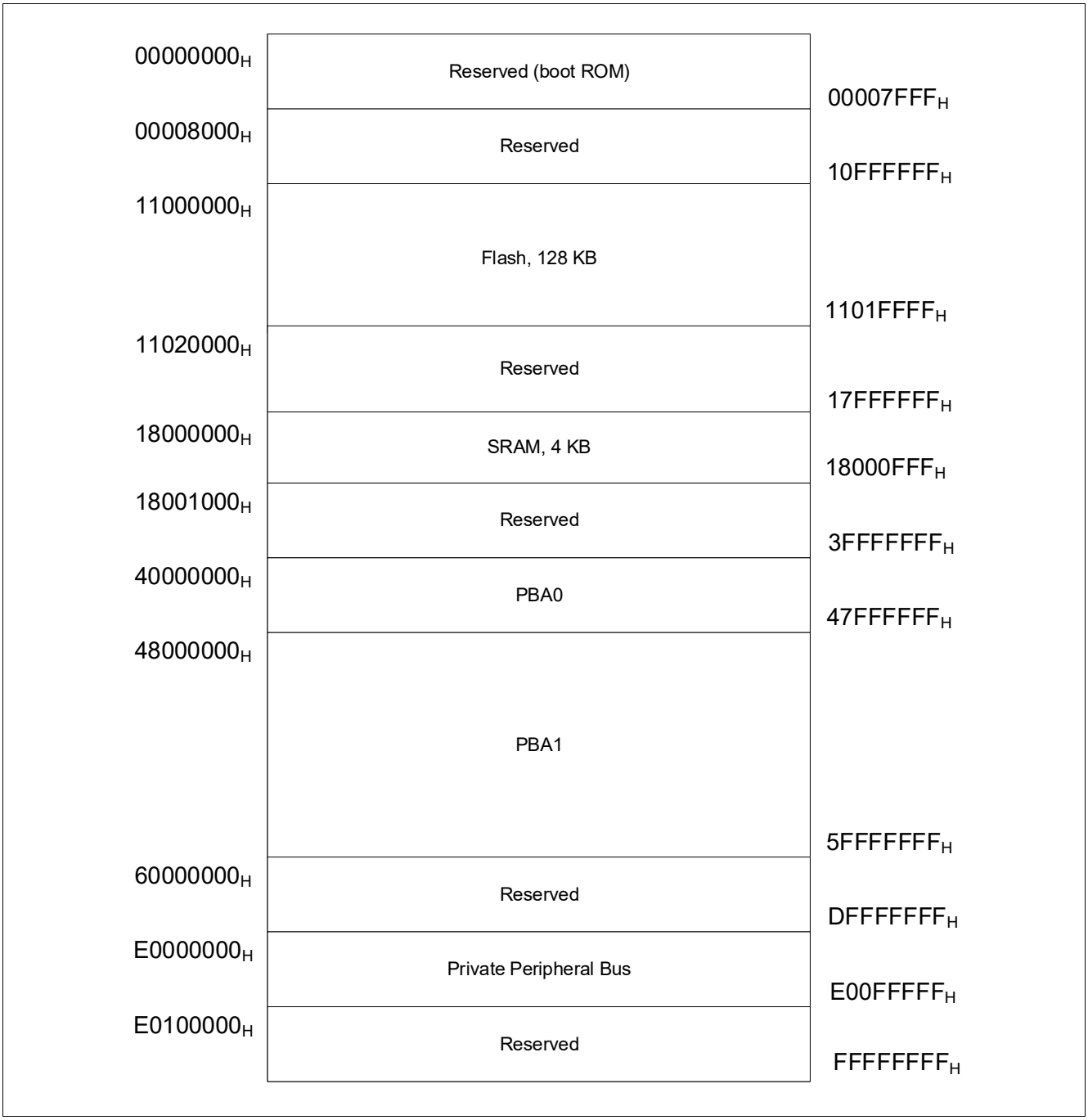


Figure 12 TLE9868QXB20 memory map

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10 Memory control unit

10.1 Features

- Handles all system memory types and their interaction with the CPU
- Memory protection for D-flash and P-flash system memory
- Address management with access violation detection including reporting
- Linear address range for all memory types (no paging)

10.2 Introduction

10.2.1 Block diagram

The memory control unit is divided into the following submodules:

- NVM memory module (embedded flash memory)
- RAM memory module
- BootROM memory module
- Memory protection unit (MPU) module
- Peripheral bridge PBA0

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Memory control unit

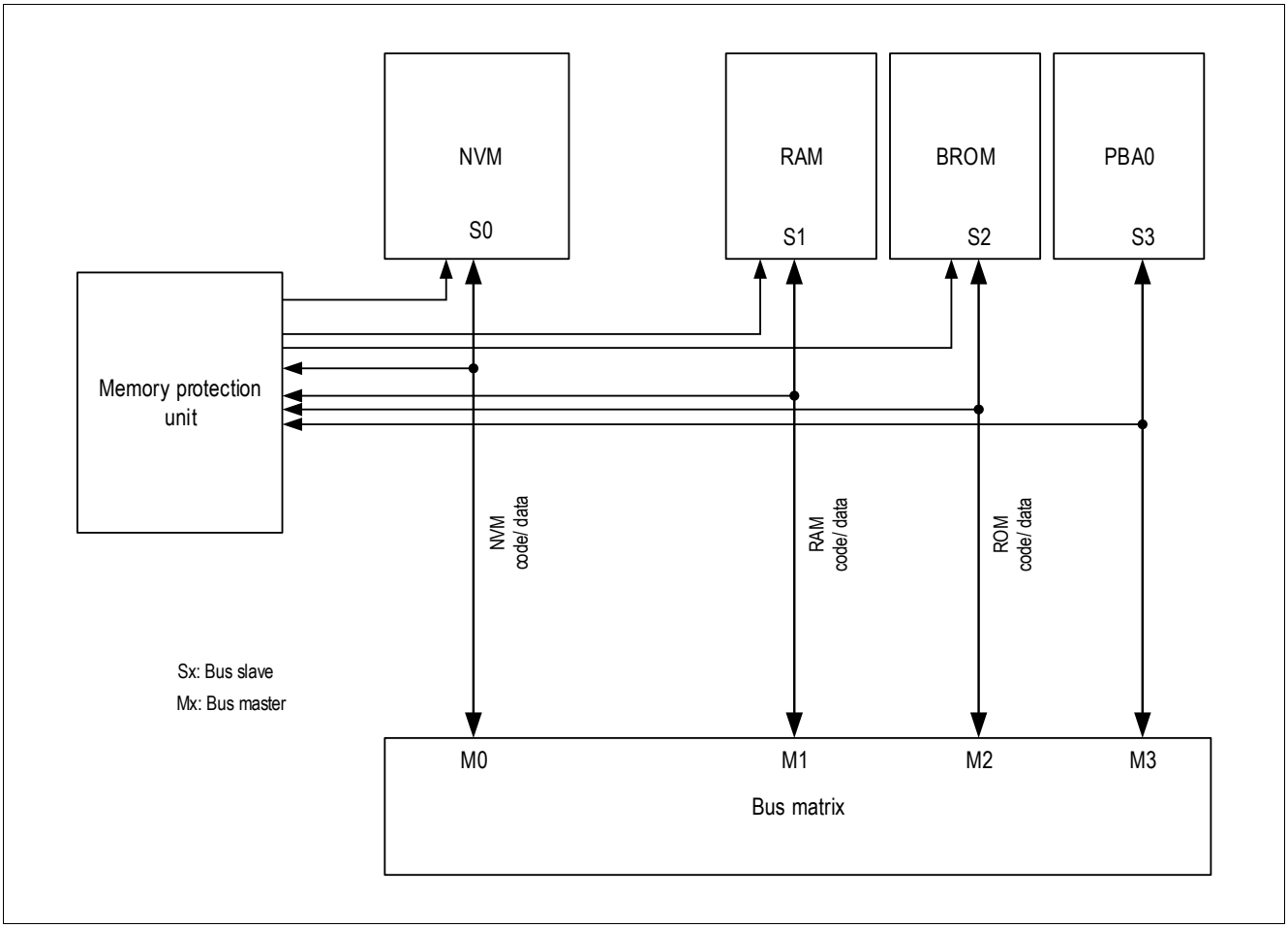


Figure 13 Block diagram of the memory control unit

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10.3 NVM module (flash memory)

The flash memory provides embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via LIN (flash mode) and SWD.
- Error correction code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single-bit errors.
- Interrupts and signals double-bit errors by the NMI.
- Possibility of checking single bit error occurrence by ROM routines.
- Program width of 128 byte (page).
- Minimum erase width of 128 bytes (page).
- Integrated hardware support for EEPROM emulation.
- 8-byte read access.
- Physical read access time: 75 ns.
- Code-read access acceleration integrated; read buffer and automatic pre-fetch.
- Page-program time: t_{PR} .
- Page-erase (128 bytes) and sector-erase (4 KB) time: t_{ER}.
- Erased bit (cell) is read as ‘1’, for code flash and 100TP.
- Erased bit (cell) is read as ‘0’ plus NMIMAP request, for data flash.

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency f_{sys}. Integrated firmware routines for erasing NVM, EEPROM emulation, and other operations are provided.

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11 Interrupt system

11.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

11.2 Introduction

Before enabling an interrupt, all corresponding interrupt status flags must be cleared.

11.2.1 Overview

The TLE9868QXB20 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, bridge driver and A/D converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2, as well as UART2, external interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for external interrupt 0 and 1.

Table 6 Interrupt vector table

Service request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU-ADC2/T3	2	Measurement unit, VBG, SDADC, Timer3
ADC1	3	ADC1 interrupt / VREF5V overload / VREF5V OV/UV
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 (ASC-LIN) interrupt (receive, transmit), Timer2, linsync1, LIN
UART2	11	UART2 interrupt (receive, transmit), Timer21, external interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge driver / charge pump
n.u.	15	Not used

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Table 7 NMI interrupt table

Service request	Node	Description
Watchdog timer NMI	NMI	Watchdog timer overflow
PLL NMI	NMI	PLL loss-of-lock
NVM operation complete NMI	NMI	NVM operation complete
Overtemperature NMI	NMI	System overtemperature
Oscillator watchdog NMI	NMI	Oscillator watchdog / MI_CLK watchdog timer overflow
NVM map error NMI	NMI	NVM map error
ECC error NMI	NMI	RAM/NVM uncorrectable ECC error
Supply prewarning NMI	NMI	Supply prewarning

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12 Watchdog timer (WDT1)

12.1 Features

There are two watchdog timers in the system. The watchdog timer (WDT) within the system control unit – digital modules (see **System control unit – digital modules (SCU-DM)**) and the Watchdog Timer (WDT1) located within the system control unit – power modules (see **System control unit – power modules (SCU-PM)**). The watchdog timer WDT1 is described in this section.

In Active mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active mode. In Sleep mode and SWD mode (Debug mode), the WDT1 is automatically disabled.

Functional Features

- Windowed watchdog timer with programmable timing in Active mode.
- Long-open window (typ. 80 ms) after power-up, reset, wake-up.
- Short-open window (typ. 30 ms) to facilitate flash programming.
- Disabled during debugging.
- Safety shutdown to Sleep mode after 5 missed WDT1 services.

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12.2 Introduction

The behavior of the watchdog timer in Active mode is illustrated in **Figure 14**.

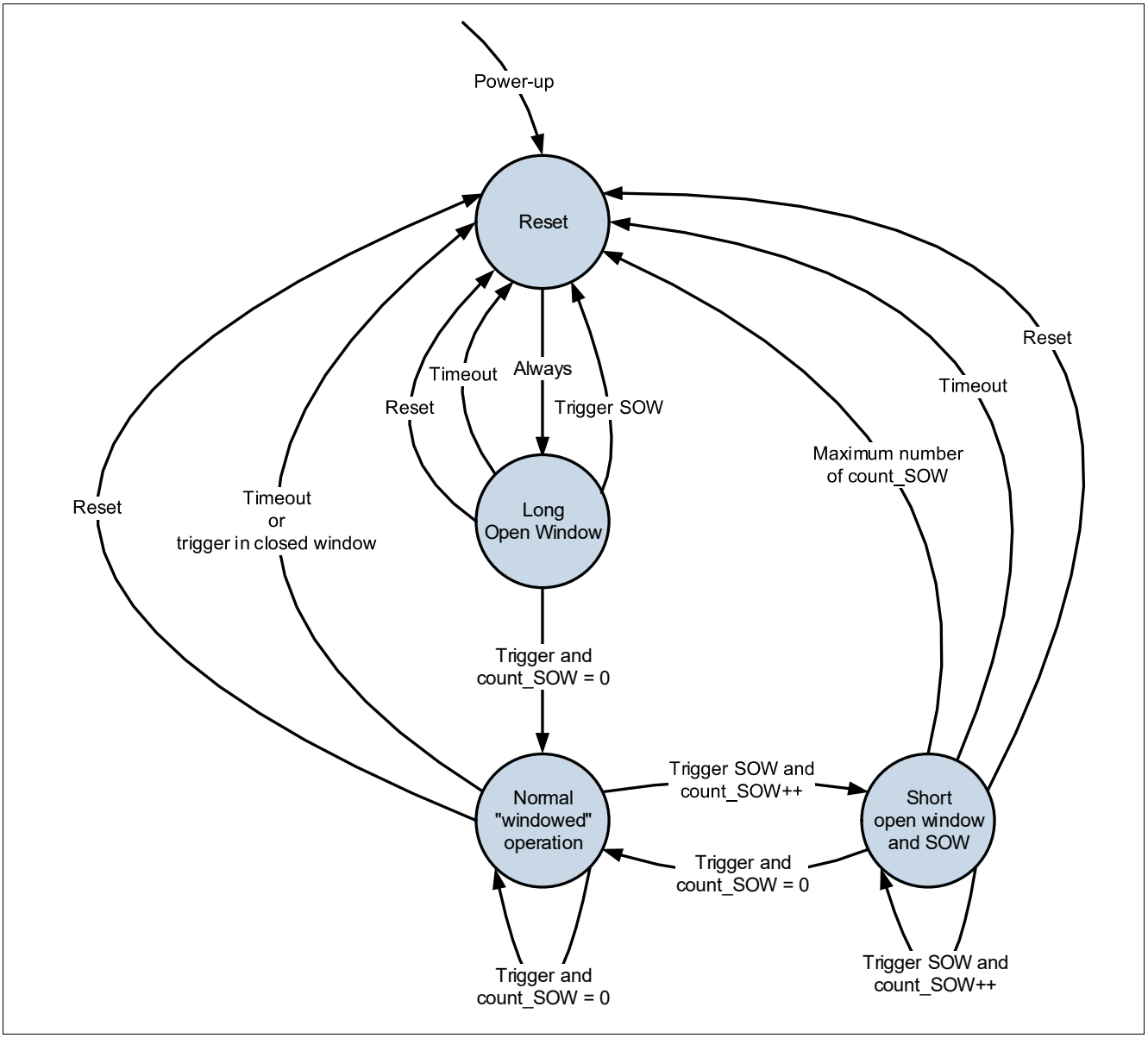


Figure 14 Watchdog timer behavior

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13 GPIO ports and peripheral I/O

The TLE9868QXB20 has 15 port pins organized into three parallel ports: Port 0 (P0), port 1 (P1) and port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general-purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. For ports configured as an output, the open drain mode can be selected. On port 2 (P2), analog inputs are shared with general-purpose inputs.

13.1 Features

Features of bidirectional ports (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open-drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general-purpose I/O)
- Alternate input/output for on-chip peripherals

Features of the analog port (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals
- Strong pull-up on P2.1

13.2 Introduction

13.2.1 Port 0 and port 1

Figure 15 shows the block diagram of a TLE9868QXB20 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open-drain pin with or without an internal pull-up/pull-down.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The voltage level present at the port pin is translated into a logical 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open-drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general-purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined

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in registers Px_ALTSEL0 and Px_ALTSEL1. When a port pin is used in an alternate function, its direction must be set accordingly in the register Px_DIR.

Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register Px_PUDSEL selects whether a pull-up or pull-down device is activated, while register Px_PUDEN enables or disables the pull device.

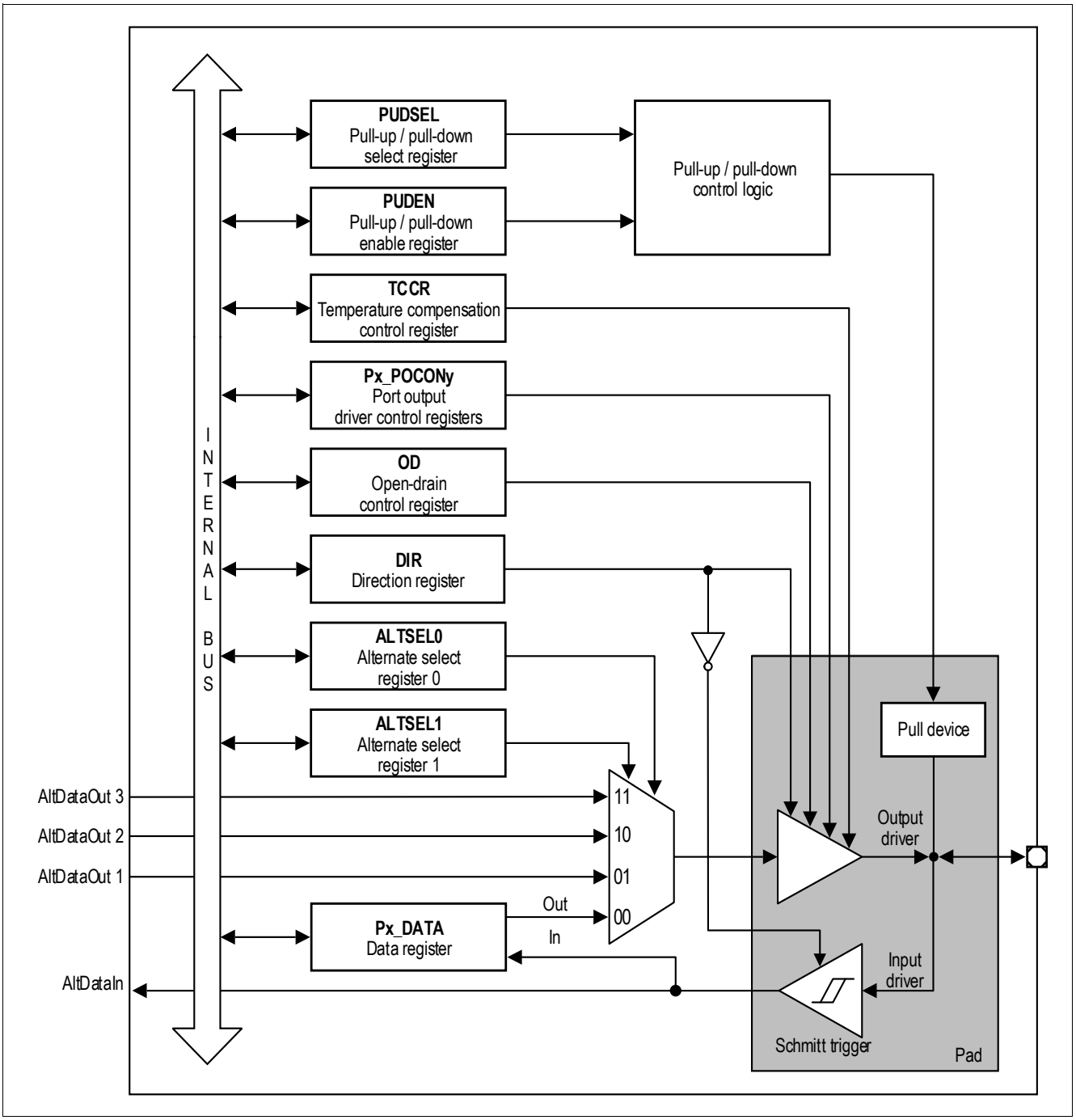


Figure 15 General structure of a bidirectional port (P0, P1)

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13.2.2 Port 2

Figure 16 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated, while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

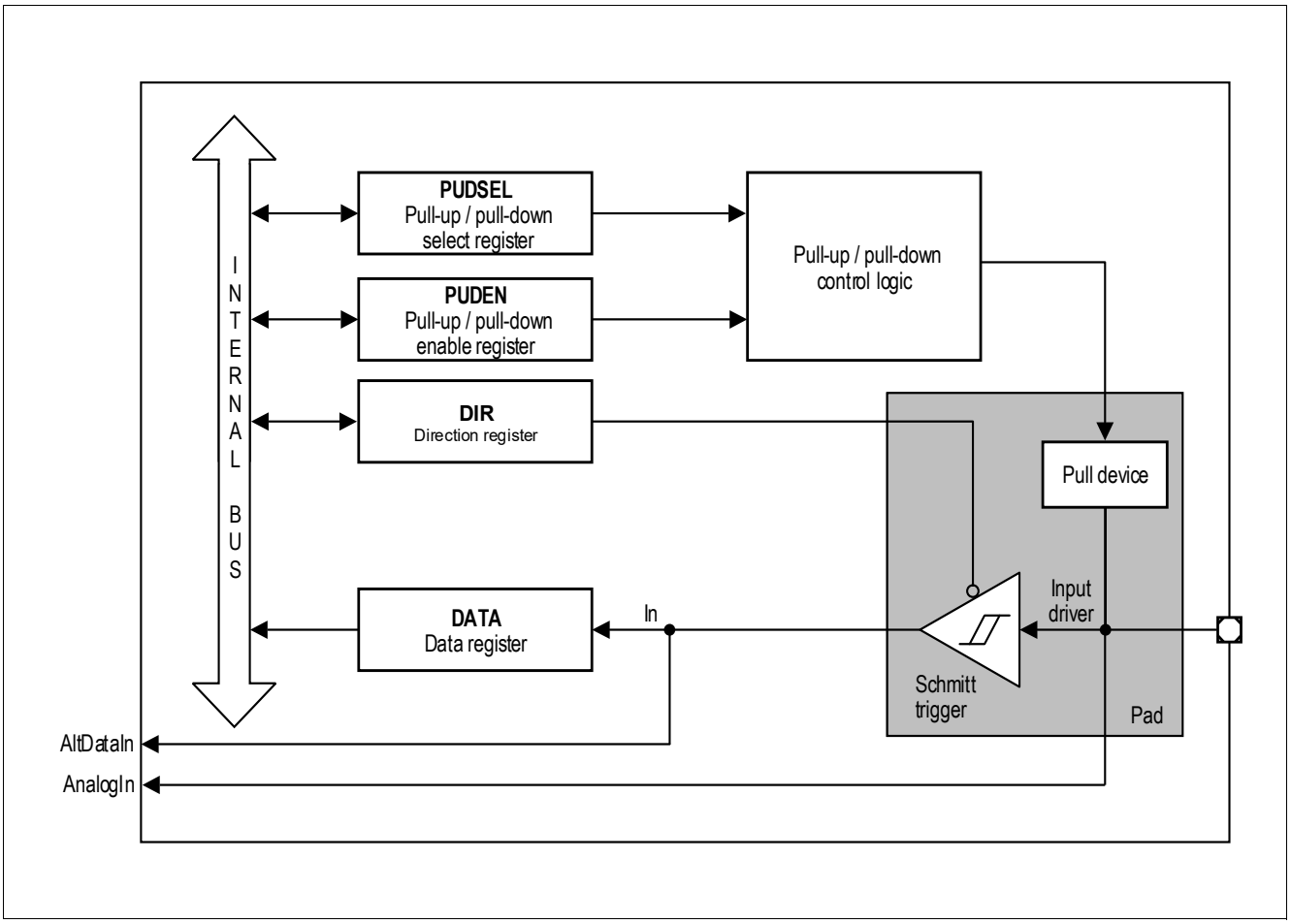


Figure 16 General structure of input port (P2)

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13.3 TLE9868QXB20 port module

13.3.1 Port 0

13.3.1.1 Port 0 functions

Table 8 Port 0 input/output functions

Port pin	Input/output	Select	Connected signals	From/to module
P0.0	Input	GPI	P0_DATA.P0	–
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	–
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	–
		INP1	T13HR_0	CCU6
		INP2	TxD1	LIN_TxD
		INP3	CAPINA	GPT12CAP
		INP4	T21_0	Timer21
		INP5	T4INC	GPT12T4
		INP6	MRST_1_2	SSC1
		INP7	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	–
		ALT1	TxD1	UART1 / LIN_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

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Table 8 Port 0 input/output functions (cont'd)

Port pin	Input/output	Select	Connected signals	From/to module
P0.2	Input	GPI	P0_DATA.P2	–
		INP1	CCPOS2_1	CCU6
		INP2	T2EUDA	GPT12T2
		INP3	MTSR_1	SSC1
		INP4	T21EX_0	Timer21
		INP5	T6INA	GPT12T6
	Output	GPO	P0_DATA.P2	–
		ALT1	COUT60_0	CCU6
		ALT2	MTSR_1	SSC1
		ALT3	EXF2_0	Timer2
P0.3	Input	GPI	P0_DATA.P3	–
		INP1	SCK_1	SSC1
		INP2	CAPINB	GPT12
		INP3	T5INA	GPT12T5
		INP4	T4EUDA	GPT12T4
		INP5	CCPOS0_1	CCU6
	Output	GPO	P0_DATA.P3	–
		ALT1	SCK_1	SSC1
		ALT2	EXF21_2	Timer21
		ALT3	T6OUT	GPT12T6
P0.4	Input	GPI	P0_DATA.P4	–
		INP1	MRST_1_0	SSC1
		INP2	CC60_0	CCU6
		INP3	T21_2	Timer21
		INP4	EXINT2_2	SCU
		INP5	T3EUDA	GPT12T3
		INP6	CCPOS1_1	CCU6
	Output	GPO	P0_DATA.P4	–
		ALT1	MRST_1_0	SSC1
		ALT2	CC60_0	CCU6
		ALT3	CLKOUT_0	SCU

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13.3.2 Port 1

13.3.2.1 Port 1 functions

Table 9 Port 1 input/output functions

Port pin	Input/output	Select	Connected signals	From/to module
P1.0	Input	GPI	P1_DATA.P0	–
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	–
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer21
P1.1	Input	GPI	P1_DATA.P1	–
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	–
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2	UART2
P1.2	Input	GPI	P1_DATA.P2	–
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer2
		INP3	T21EX_3	Timer21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	–
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

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Table 9 Port 1 input/output functions (cont'd)

Port pin	Input/output	Select	Connected signals	From/to module
P1.3	Input	GPI	P1_DATA.P3	–
		INP1	T6INB	GPT12T6
		INP2	–	–
		INP3	CC62_0	CCU6
		INP4	T6EUDB	GPT12T6
		INP5	–	–
		INP6	CCPOS0_2	CCU6
		INP7	EXINT1_1	SCU
	Output	GPO	P1_DATA.P3	–
		ALT1	EXF21_1	Timer21
		ALT2	CC62_0	CCU6
		ALT3	TXD2	UART2
P1.4	Input	GPI	P1_DATA.P4	–
		INP1	EXINT2_1	SCU
		INP2	T21EX_1	Timer21
		INP3	T5EUDA	GPT12T5
		INP4	RxD1	UART1
		INP5	T2INB	GPT12T2
		INP6	CCPOS1_2	CCU6
		INP7	MRST_1_3	SSC1
	Output	GPO	P1_DATA.P4	–
		ALT1	CLKOUT_1	SCU
		ALT2	COUT62_0	CCU6
		ALT3	RxD1	UART1 / LIN_RxD

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13.3.3 Port 2

13.3.3.1 Port 2 functions

Table 10 Port 2 input functions

Port pin	Input/output	Select	Connected signals	From/to module
P2.1	Input	GPI	P2_DATA.P1	–
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC1
P2.3	Input	GPI	P2_DATA.P3	–
		INP1	CCPOS1_0	CCU6
		INP2	$\overline{\text{CTRAP\#_1}}$	CCU6
		INP3	T21EX_2	Timer21
		INP4	CC60_1	CCU6
		INP5	EXINT0_3	SCU
		ANALOG	AN3	ADC1
P2.4	Input	GPI	P2_DATA.P4	–
		INP1	$\overline{\text{CTRAP\#_0}}$	CCU6
		INP2	T2EUDB	GPT12T2
		INP3	MRST_1_1	SSC1
		INP4	EXINT1_3	SCU
		ANALOG	AN4	ADC1
P2.5	Input	GPI	P2_DATA.P5	–
		INP1	RXD2_1	UART2
		INP2	T3EUDB	GPT12T3
		INP3	MRST_2_1	SSC2
		INP4	T2_1	Timer2
		ANALOG	AN5	ADC1
P2.7	Input	GPI	P2_DATA.P7	–
		INP1	CCPOS2_0	CCU6
		INP2	EXINT2_0	SCU
		INP3	T13HR_1	CCU6
		INP4	–	–
		INP5	CC62_1	CCU6
		ANALOG	AN7	ADC1

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14 General-purpose timer units (GPT12)

14.1 Features

14.1.1 Features of block GPT1

The following list summarizes the supported features:

- f_{GPT} is derived from PCLK
- f_{GPT}/4 maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 Operating modes:
  - Timer mode
  - Gated Timer mode
  - Counter mode
  - Incremental Interface mode
- Reload and capture functionality
- Shared interrupt: node 0

14.1.2 Features of block GPT2

The following list summarizes the supported features:

- f_{GPT} is derived from PCLK
- f_{GPT}/2 maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 Operating modes:
  - Timer mode
  - Gated Timer mode
  - Counter mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: node 1

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14.2 Introduction

The general-purpose timer unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse-width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated Timer or Counter mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources through the PISEL register.

The GPT module is clocked with clock f_{GPT}. f_{GPT} is a clock derived from PCLK.

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14.2.1 Block diagram of GPT1

The GPT1 block contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

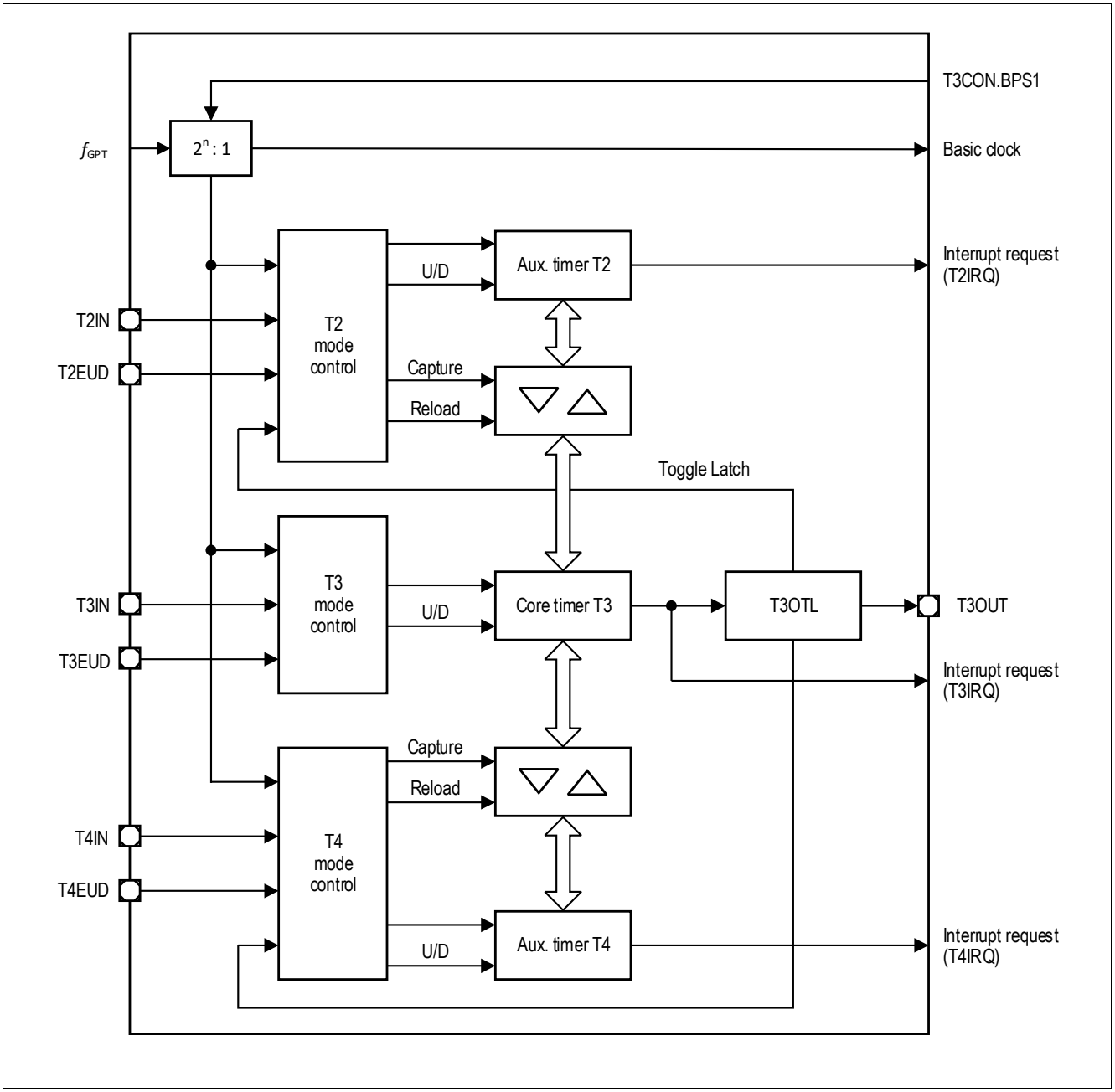


Figure 17 GPT1 block diagram (n = 2 … 5)

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14.2.2 Block diagram of GPT2

The GPT2 block contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional capture/reload register (CAPREL) supports capture and reload operation with extended functionality.

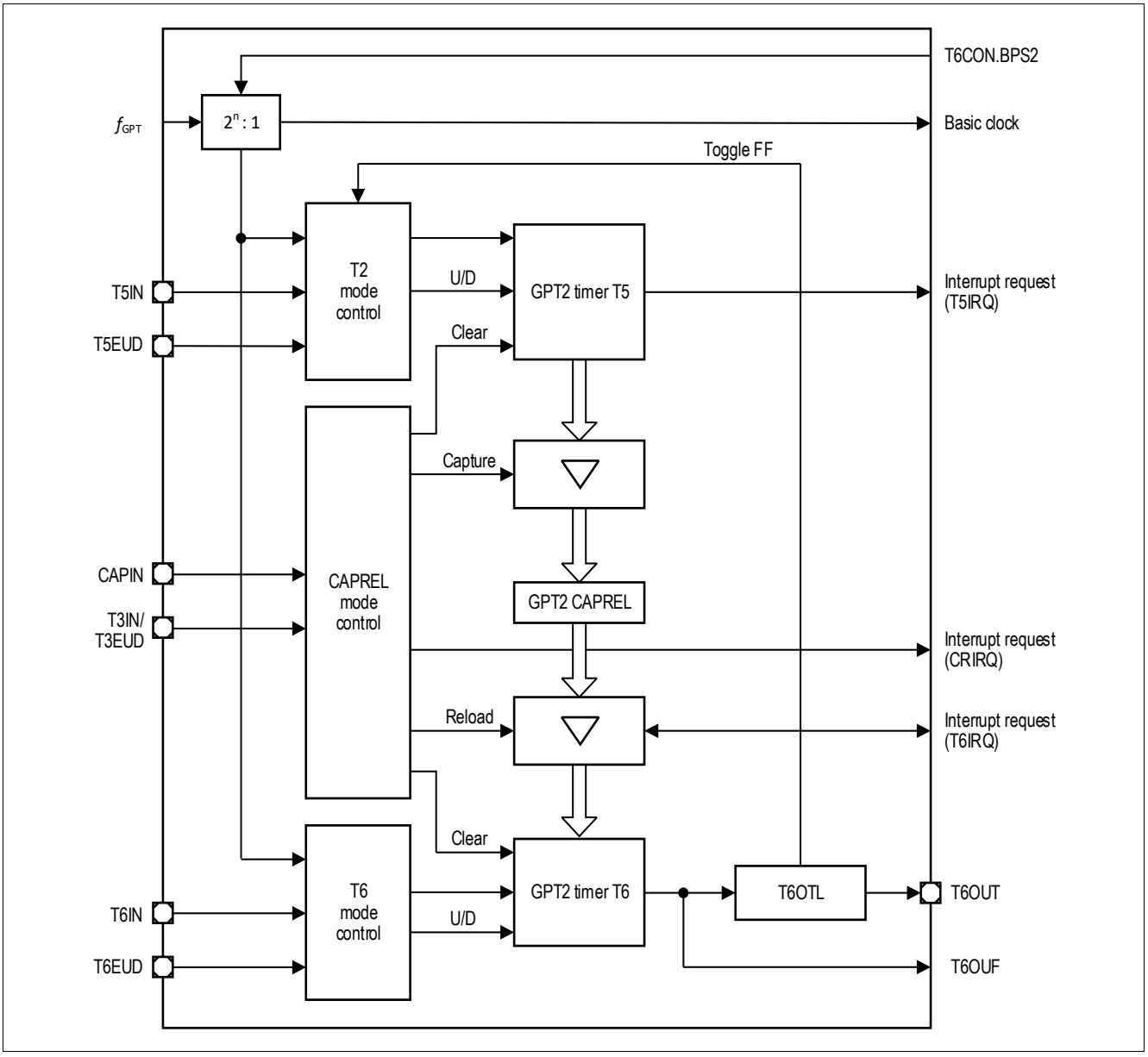


Figure 18 GPT2 block diagram (n = 1 … 4)

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15 Timer2 and Timer21

15.1 Features

- 16-bit auto-reload mode
  - Selectable up- or down-counting
- One-channel 16-bit capture mode

15.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer2 and Timer21 can function as timers or counters in each of their modes. As timers, they count with an input clock of $f_{PCLK}/12$ (if the prescaler is disabled). As a counter, Timer2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for counting is $f_{PCLK}/24$ (if the prescaler is disabled).

15.2.1 Timer2 and Timer21 mode overview

Table 11 Timer2 and Timer21 modes

Mode	Description
Auto-reload	**Up/down-count-disabled** • Counting up only. • Counting starts from the 16-bit reload value, overflow at $FFFF_H$. • The reload event can be configured to be triggered only by the overflow condition or by a negative or positive edge at the input pin T2EX as well. • Programmable reload value in register RC2. • Interrupt is generated with reload events.

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Table 11 Timer2 and Timer21 modes (cont'd)

Mode	Description
Auto-reload	**Up/down-count-enabled** • Counting up or down, direction determined by level at input pin T2EX. • No interrupt is generated. • Counting up – Counting starts from the 16-bit reload value, overflow at $FFFF_H$. – Reload event triggered by overflow condition. – Programmable reload value in register RC2. • Counting down – Counting starts from $FFFF_H$, underflow at value defined in register RC2. – Reload event triggered by underflow condition. – Reload value fixed at $FFFF_H$.
Channel capture	• Counting up only. • Counting starts from 0000_H, overflow at $FFFF_H$. • Reload event triggered by overflow condition. • Reload value fixed at 0000_H. • Capture event triggered by falling/rising edge at pin T2EX. • Captured timer value stored in register RC2. • Reload or capture events generate interrupts.

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16 Timer3

16.1 Features

- 16-bit incremental timer/counter (counting up)
- Counting frequency up to f_{sys}
- Selectable clock prescaler
- Six operating modes
- Interrupt on overflow
- Interrupt on compare

16.2 Introduction

The possible applications for this timer include measuring the time interval between events, counting events, and generating a signal at regular intervals.

Timer3 can function as a timer or a counter. When functioning as a timer, Timer3 is incremented in periods based on the MI_CLK or LP_CLK clocks. When functioning as a counter, Timer3 is incremented in response to a 1-to-0 transition (falling edge) at its configured input. Timer3 can be configured in four different operating modes for a variety of applications (see **Table 12**).

The different operating modes allow the timer to be used for tasks such as:

- Simple measurements of the times between two events.
- Triggering the measuring unit upon PWM/CCU6 unit
- Measurement of the 100 kHz LP_CLK2

16.3 Functional description

Six modes of operation are provided to enable using this timer for various tasks. In every mode, the clocking source can be selected from MI_CLK and LP_CLK. In addition, a prescaler provides the capability to divide the selected clock source by 2, 4, or 8. The timer counts upwards, starting with the value in the timer count registers, up to the maximum count value, which depends on the selected mode of operation. Timer3 provides two individual interrupts on counter overflow, one for the low-byte and one for the high-byte counter register.

16.3.1 Timer3 mode overview

Table 12 provides an overview of the timer modes together with the reasonable configuration options.

Table 12 Timer3 modes

Mode	Submode	Operation
0	**No submode**	**13-bit timer** The timer essentially operates an 8-bit counter with a divide-by-32 prescaler.
1	**a**	**16-bit timer** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter.

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Table 12 Timer3 modes (cont'd)

Mode	Submode	Operation
1	**b**	**16-bit timer triggered by an event** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter, which is triggered by an event to enable a single-shot measurement on a preset channel with the measurement unit.
2	**No submode**	**8-bit timer with autoreloading** The timer register TL3 is reloaded with a user-defined 8-bit value in TH3 on overflow.
3	**a**	**Timer3 operating as two 8-bit timers** The timer registers TL3 and TH3, operate as two separate 8-bit counters.
3	**b**	**Timer3 operating as two 8-bit timers for clock measurement** The timer registers, TL3 and TH3, operate as two separate 8-bit counters. In this mode, the LP_CLK2 low power clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 measures the interval between the edges.

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17 Capture/compare unit 6 (CCU6)

17.1 Feature set overview

This section gives an overview over the different building blocks and their main features.

Timer12 block features

- Three capture/compare channels. Each channel can be used either as capture or as compare channel.
- Supports three-phase PWM (six outputs with separate signals for high-side and low-side switches).
- 16-bit resolution, maximum count frequency = peripheral clock.
- Dead-time control for each channel to avoid short-circuits in the power stage.
- Concurrent update of the T12 registers.
- Center-aligned and edge-aligned PWM can be generated.
- Single-shot mode is supported.
- Start can be controlled by external events.
- External events can be counted.
- Multiple interrupt request sources.
- Hysteresis-like control mode.

Timer13 block features

- One independent compare channel with one output.
- 16-bit resolution, maximum count frequency = peripheral clock.
- Concurrent update of T13 registers.
- Can be synchronized to T12.
- Interrupt generation at period-match and compare-match.
- Single-shot mode is supported.
- Start can be controlled by external events.
- Capability of counting external events.

Additional specific functions

- Block commutation for brushless DC-drives implemented.
- Position detection via hall-sensor pattern.
- Noise filter for position input signals supported.
- Automatic rotational speed measurement and commutation control for block commutation.
- Integrated error handling.
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$).
- Control modes for multi-channel AC drives.
- Output levels can be selected and adapted to the power stage.

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17.2 Introduction

The CCU6 unit is made up of the T12 timer block with three capture/compare channels and the T13 timer block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive DC motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide efficient software control.

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g., a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work only in compare mode. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for modulating signals.

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17.2.1 Block diagram

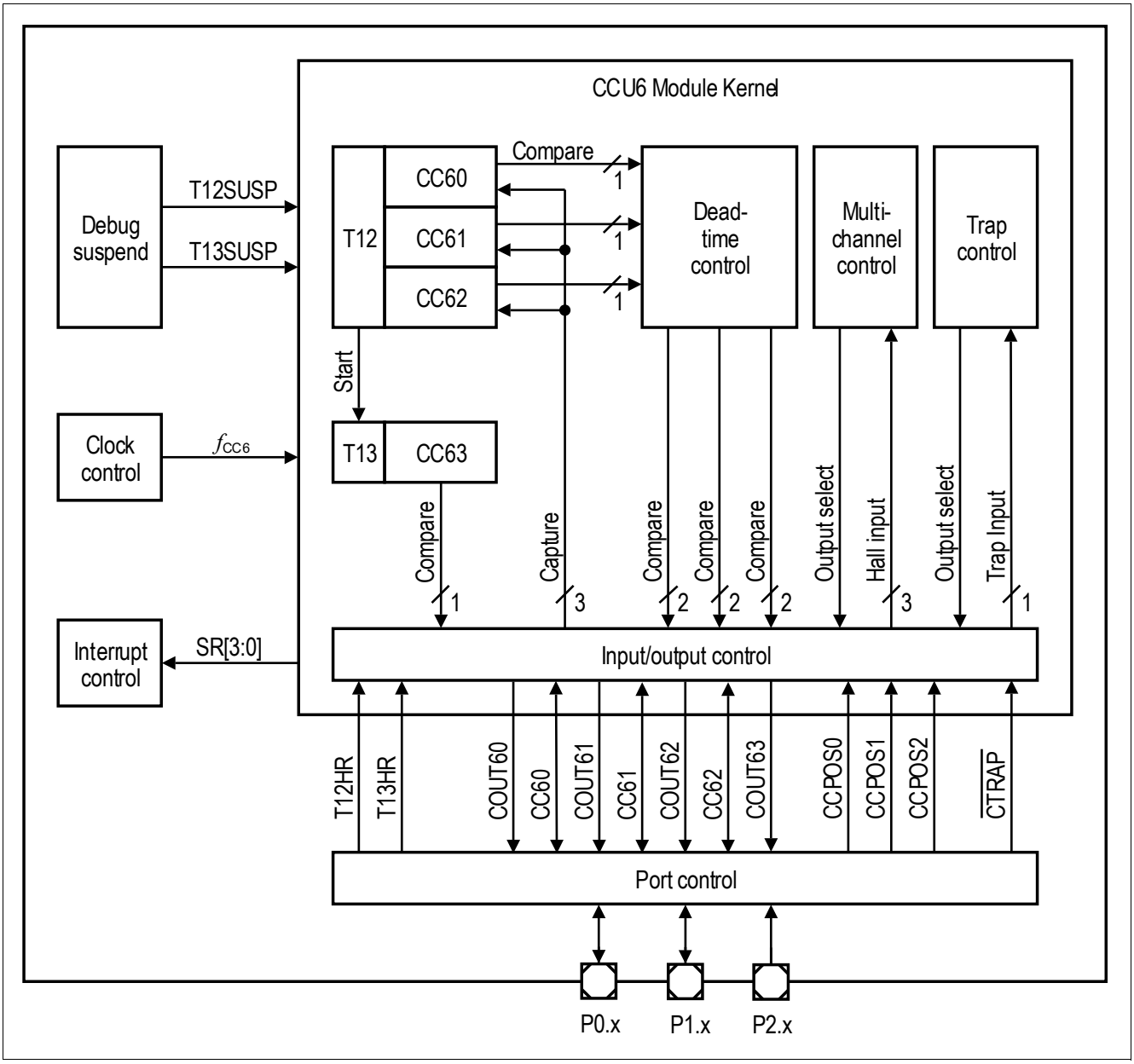


Figure 19 CCU6 block diagram

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18 UART1/UART2

The description in this chapter applies to both UART1 and UART2.

18.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first.
  - Fixed or variable baud rate.
- Receive-buffered.
- Multiprocessor communication.
- Interrupt are generated when data transmission or receptions are complete.
- Baud-rate generator with fractional divider for generating a wide range of baud rates.
- Hardware logic for break and synch byte detection.

18.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time when the reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed through the special function register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

18.2.1 Block diagram

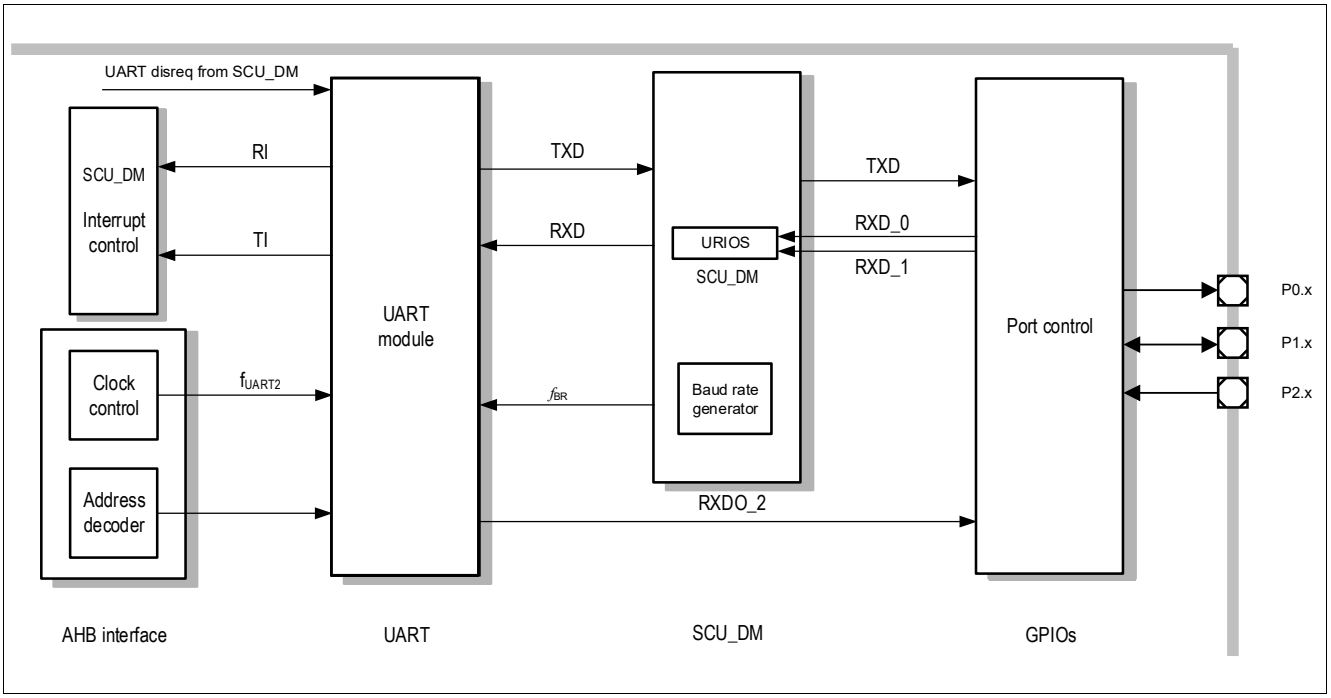


Figure 20 UART block diagram

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18.3 UART modes

The UART can be used in four different modes. In mode 0, it operates as an 8-bit shift register. In mode 1, it operates as an 8-bit serial port. In modes 2 and 3, it operates as a 9-bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to the appropriate values, as shown in **Table 13**.

Table 13 UART modes

SM0	SM1	Operating mode	Baud rate
0	0	Mode 0: 8-bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-bit shift UART	Variable
1	0	Mode 2: 9-bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-bit shift UART	Variable

UART1 is connected to the integrated LIN transceiver, and to GPIO for test purposes. UART2 is connected to GPIO only.

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19 LIN transceiver

19.1 Features

General functional features

- Compliant with the LIN2.2 standard, backward-compatible with LIN1.3, LIN2.0, and LIN 2.1
- Compliant with SAE J2602 (slew rate, receiver hysteresis)

Special features

- Measurement of the LIN master baudrate via Timer2
- LIN can be used as input/output with SFR bits
- TxD timeout feature (optional, on by default)

Operation mode features

- LIN Sleep mode (LSLM)
- LIN Receive-Only mode (LROM)
- LIN Normal mode (LNM)
- High voltage input/output mode (LHVIO)

Supported baud rates

- Mode for transmission with up to 10.4 kilobaud
- Mode for transmission with up to 20 kilobaud
- Mode for transmission with up to 40 kilobaud
- Mode for transmission with up to 115.2 kilobaud

Slope mode features

- Normal Slope mode (20 kbit/s)
- Low Slope mode (10.4 kbit/s)
- Fast Slope mode (62.5 kbit/s)
- Flash mode (115.2 kbit/s, 250 kbit/s)

Wake-up features

- LIN bus wake-up

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19.2 Introduction

The LIN module is a transceiver for the Local Interconnect Network (LIN), compliant with the LIN2.2 standard and backward-compatible with LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single-wire, bidirectional bus typically used for in-vehicle networks, using baud rates between 2.4 kilobaud and 20 kilobaud. Additionally, baud rates up to 115.2 kilobaud are implemented.

The LIN module offers several different operation modes, including a LIN Sleep mode and the LIN Normal mode. The integrated slope control allows using several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash mode up to 115.2 kilobaud is implemented. In specific conditions, this Flash mode supports data rates of up to 250 kbit/s. (In production environments, in point-to-point communications with reduced wire lengths and limited supply voltages.).

19.2.1 Block diagram

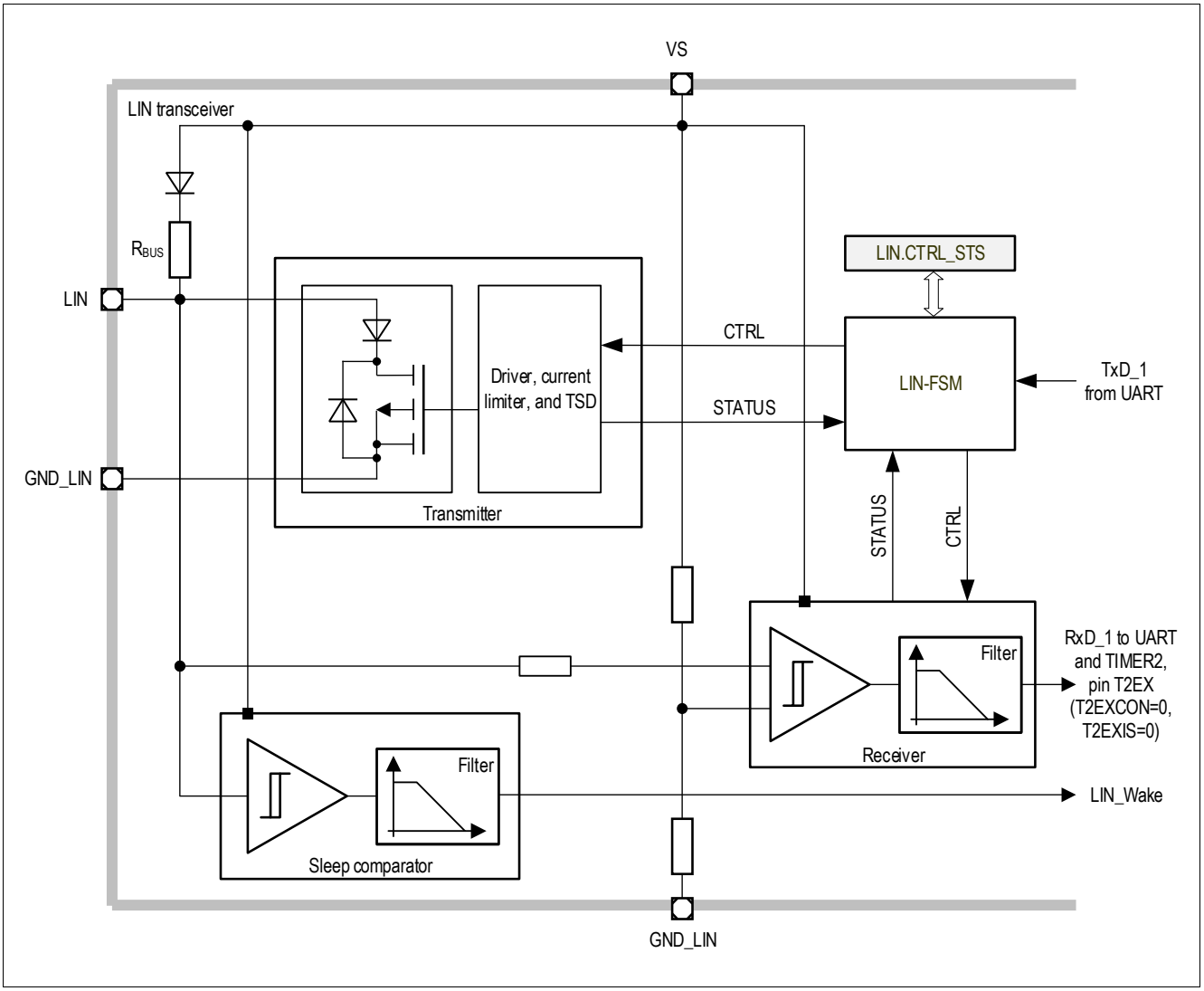


Figure 21 LIN transceiver block diagram

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20 High-speed synchronous serial interface (SSC1/SSC2)

20.1 Features

- Master and Slave mode operation
  - Full-duplex or half-duplex operation
- Transmit- and receive-buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: least significant bit (LSB) or most significant bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a “transmitter empty” condition
  - On a “receiver full” condition
  - On an error condition (receive, phase, baud rate, or transmission error)

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20.2 Introduction

The high-speed synchronous serial interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (Master mode), using its own 16-bit baud rate generator, or can be received from an external master (Slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices as well as devices using other synchronous serial interfaces.

Data is transmitted or received on the TXD and RXD lines, which are normally connected to the MTSR (Master Transmit, Slave Receive) and MRST (Master Receive, Slave Transmit) pins. The clock signal is output via the MS_CLK (Master Serial Shift Clock) line or input via the SS_CLK (Slave Serial Shift Clock) line. Both lines are normally connected to the SCLK pin. Transmission and reception of data are double-buffered.

20.2.1 Block diagram

Figure 22 shows all functionally relevant interfaces associated with the SSC kernel.

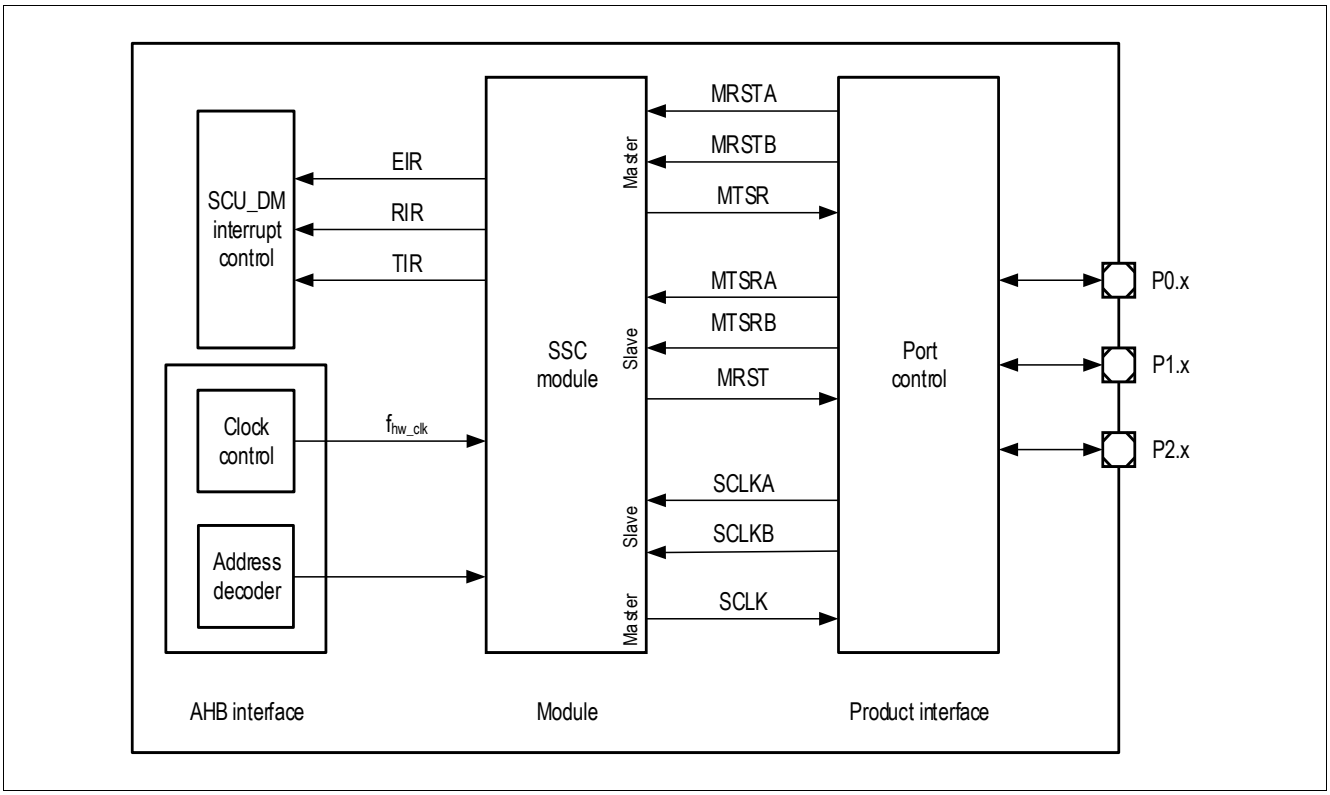


Figure 22 SSC interface diagram

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21 Measurement unit

21.1 Features

- 1 x 8-bit ADC with 10 inputs. Attenuators allow measuring high-voltage input signals.
- Supply voltage attenuators for attenuating **VBAT_SENSE**, **VS**, **VDDP** and **VDDC**.
- VBG monitoring of the 8-bit ADC to guarantee functional safety requirements.
- Bridge driver diagnosis measurement (VDH, VCP).
- Temperature sensor for monitoring the chip temperature and PMU regulator temperature.
- Supplement block with reference voltage generation, bias current generation, voltage buffer for NVM reference voltage, voltage buffer for analog module reference voltage, and a test interface.

21.2 Introduction

The measurement unit is a functional unit that comprises the following submodules:

Table 14 Measurement functions and associated modules

Module name	Module	Functions
Central function unit	Bandgap reference circuit	The bandgap reference submodule provides two reference voltages: 1. A trimmable reference voltage for the 8-bit ADC. A local dedicated bandgap circuit ensures that the reference voltage does not drop, e.g., because of crosstalk or ground voltage shift. 2. The reference voltage for the NVM module.
8-bit ADC (ADC2)	8-bit ADC module with 10 multiplexed inputs and including high-voltage input attenuators	• 5 high-voltage inputs supporting the full supply range (2.5 V...30.7 V(FS)) • 2 medium-voltage inputs (0..5 V/7 V FS). • 3 low-voltage inputs (0..1.2 V/1.6 V FS) (See the following figure for the allocation of the inputs).
10-bit ADC (ADC1)	10-bit ADC module with 8 multiplexed inputs	Five (5 V) analog inputs from port 2.x.
14 Bit ADCs (ADC3, ADC4)	14 Bit Sigma Delta ADC module	Two differential analog inputs from Port 2.x
VDH input voltage attenuator	VDH input voltage attenuator	Scales down V(VDH) to the input voltage range of ADC1.CH6.

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Measurement unit

Table 14 Measurement functions and associated modules (cont'd)

Module name	Module	Functions
Temperature sensor	Temperature sensor with two multiplexed sensing elements: • Sensor located on the PMU • Sensor located on the central chip	Generates an output voltage that is a linear function of the local chip (junction) temperature.
Core measurement module	Digital signal processing and ADC2 control unit	1. Generates the control signal for the 8-bit ADC2 and the synchronous clock for the switched capacitor circuits. 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

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21.2.1 Block diagram

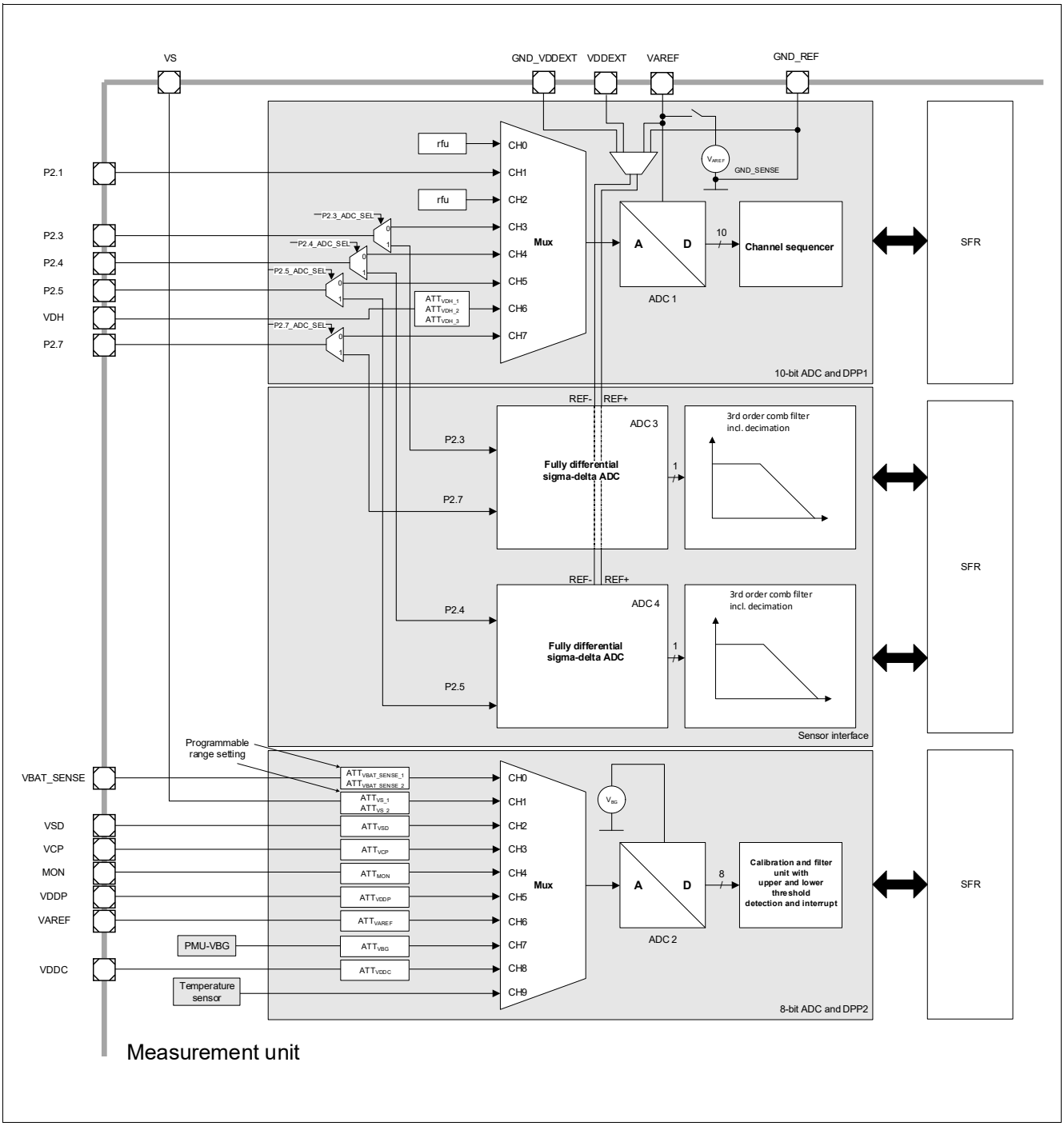


Figure 23 Measurement unit, overview

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22 Measurement core module (incl. ADC2)

22.1 Features

- 10 individually programmable channels, split into two groups of user-configurable and non-configurable channels, respectively.
- Individually programmable channel prioritization scheme for the measurement unit.
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel.
- Two channel configurations:
  - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis.
  - Two individually programmable trigger thresholds with limit hysteresis settings.
- Individually programmable interrupts and statuses for all channel thresholds.

22.2 Introduction

The basic function of this block is the digital postprocessing of several digitized analog measurement signals by filtering, level comparison, and interrupt generation. The measurement postprocessing block consists of ten identical channel units attached to the outputs of the 10-channel 8-bit ADC (ADC2). It processes ten channels, where the channel sequence and prioritization is programmable within a wide range.

22.2.1 Block diagram

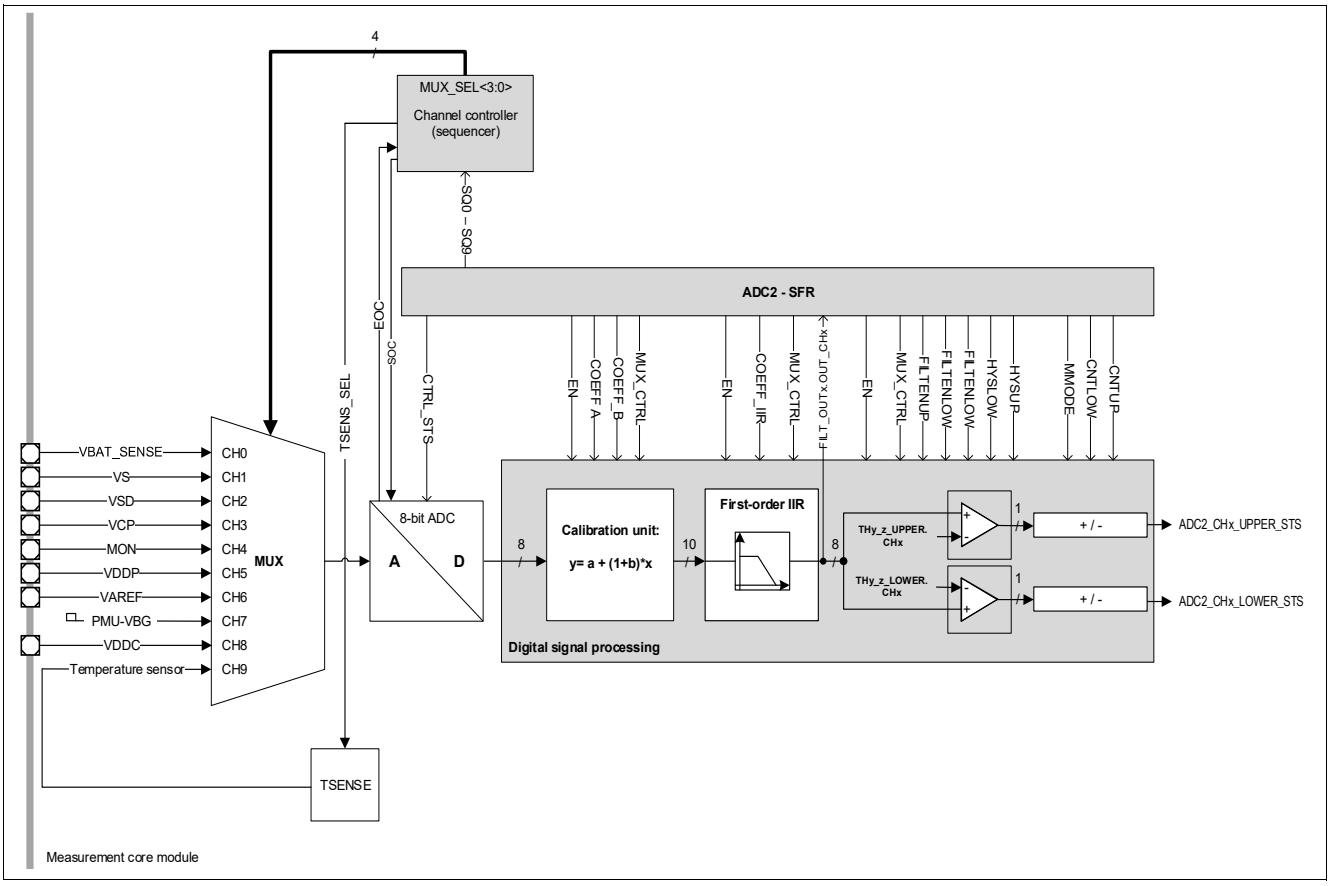


Figure 24 Module block diagram

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22.2.2 Measurement core module mode overview

The basic function of this unit is the digital signal processing of several digitized analog measurement signals by filtering, level comparison, and interrupt generation. The measurement core module processes ten channels in a quasi-parallel process.

As shown in the figure above, the ADC2 postprocessing unit consists of a channel controller (sequencer), a 10-channel demultiplexer, and the signal-processing block, which filters and compares the sampled ADC2 values for each channel individually. The channel control block controls the multiplexer sequencing on the analog side, before the ADC2, and in the digital domain, behind the ADC2. The channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used, e.g., to give supply voltage channels a higher priority than the other channel measurements. In addition, the measurement core module offers two different postprocessing measurement modes for over- and undervoltage detection and for two-level threshold detection.

The channel controller (sequencer) runs in one of the following modes:

- Normal Sequencer: Channels are selected according to the 10 sequence registers which contain individual enablers for each of the 10 channels.
- Exceptional Interrupt Measurement: Following a hardware event, a high-priority channel is inserted into the current sequence. The current actual measurement is not destroyed.
- Exceptional Sequence Measurement: Following a hardware event, a complete sequence is inserted after the current measurement is finished. The current sequence is interrupted by the exception sequence.

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23 10-bit analog-to-digital converter (ADC1)

23.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels.
- Flexible results handling
  - 10-bit resolution.
- Flexible source selection due to sequencer:
  - Insert one exceptional sequence (ESM).
  - Insert an interrupt measurement into the current sequence (EIM), single or up to 128 times.
  - Software mode.
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference.
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales.
- Support of suspended and power-saving modes.
- Result data protection for slow CPU access (Wait-for-Read mode).
- Programmable clock divider.
- Integrated sample and hold circuitry.

23.2 Introduction

The TLE9868QXB20 includes a high-performance 10-bit analog-to-digital converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN1 and AN3 to AN5, AN7.

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23.2.1 Block diagram

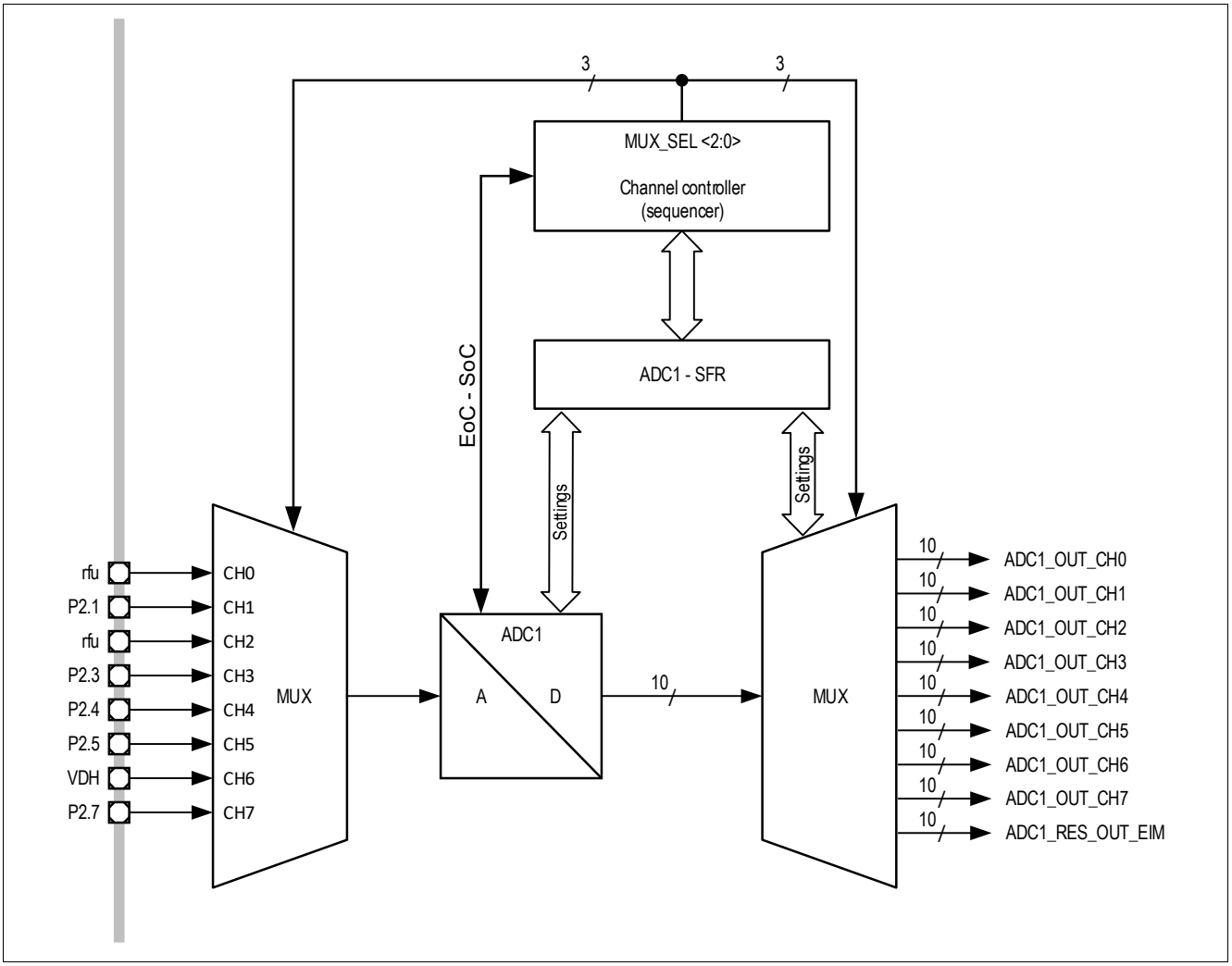


Figure 25 ADC1 top-level block diagram

As shown in the figure above, the ADC1 postprocessing block consists of a channel controller (Sequencer) and an 8-channel demultiplexer. The channel control block controls the multiplexer sequencing on the analog side, before the ADC1, and in the digital domain, behind the ADC1. The channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used, e.g., to give supply voltage channels a higher priority than the other channel measurements.

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24 14-Bit Sigma Delta ADC (ADC3 / ADC4)

24.1 Features

Module features:

- Full differential capacitive input
- 14 bit resolution
- Full differential scale: $V_{diff,lin}$
- Extended differential input range with reduced accuracy: $V_{diff,nonlin}$
- Sampling frequency: $f_{ADC3/4}$
- Programmable oversampling ratio: *OSR*
- High supply rejection ratio
- Internal clock jittering

24.2 Functional description

The 2 integrated 14 Bit Sigma Delta ADCs are building a Sensor Interface for an external AMR / GMR Sensor. The application configuration is shown below.

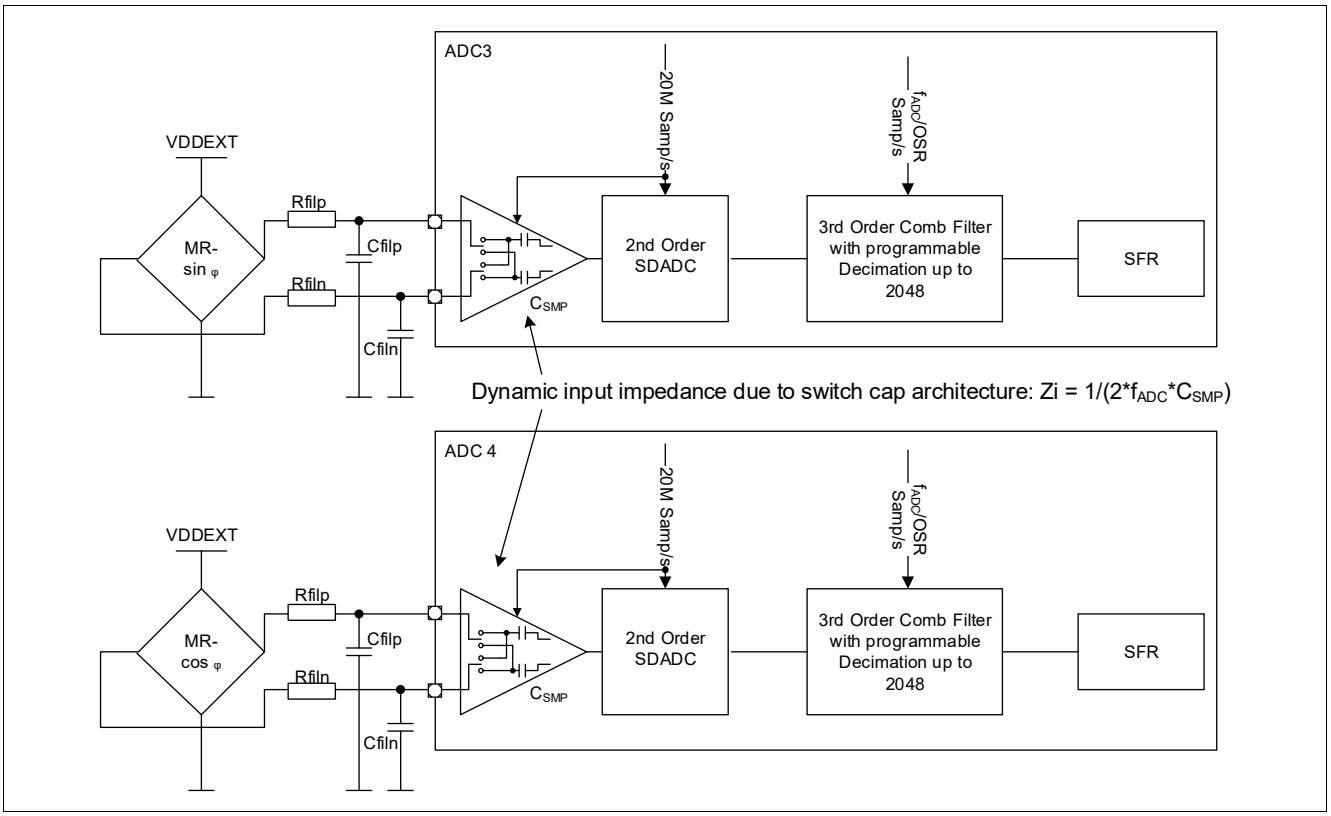


Figure 26 Application of integrated Sigma Delta ADCs

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24.2.1 Input voltage range of SDADC

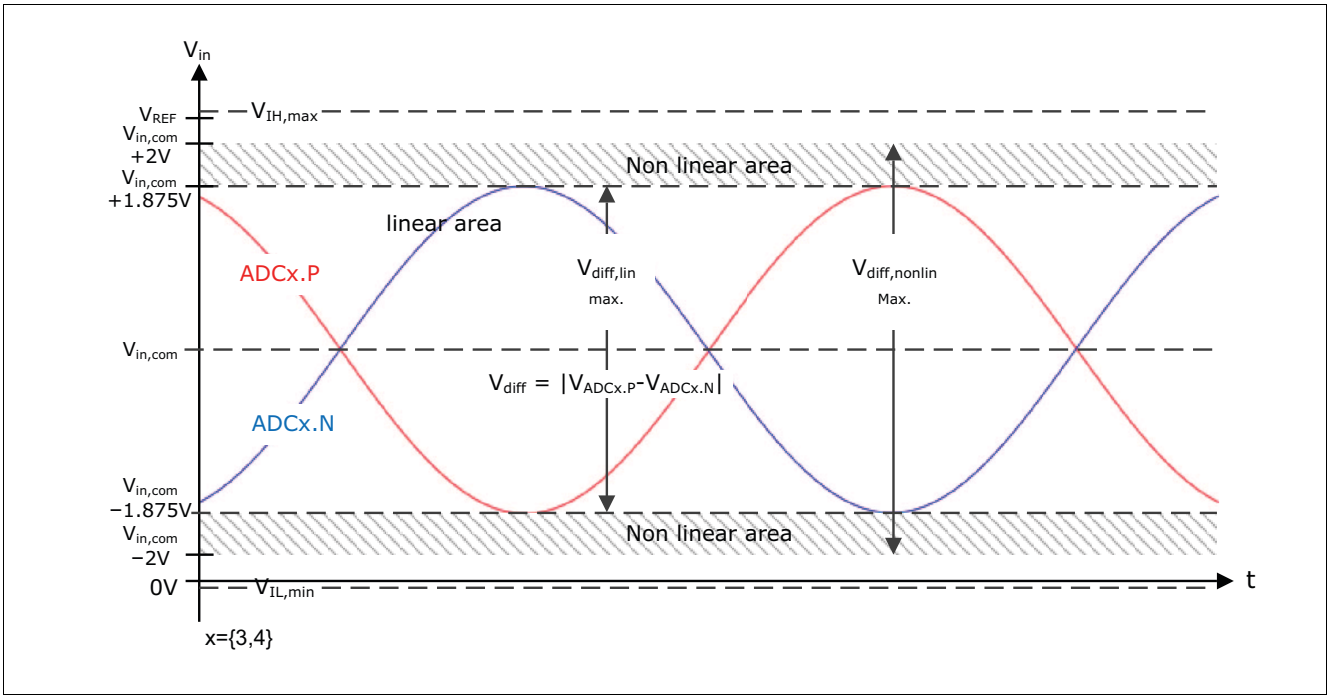


Figure 27 Input voltage range

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25 High-voltage monitor input

25.1 Features

- High-voltage input with V_{MONth} threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power-saving modes
- Level change sensitivity configurable for transitions from low to high, high to low, or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input level can be monitored if the module is enabled (PMU_MON_CNF).

To use the Wake function when the IC is in a low-power mode, the monitoring pin is switched to Sleep mode via the SFR bit EN.

25.2.1 Block diagram

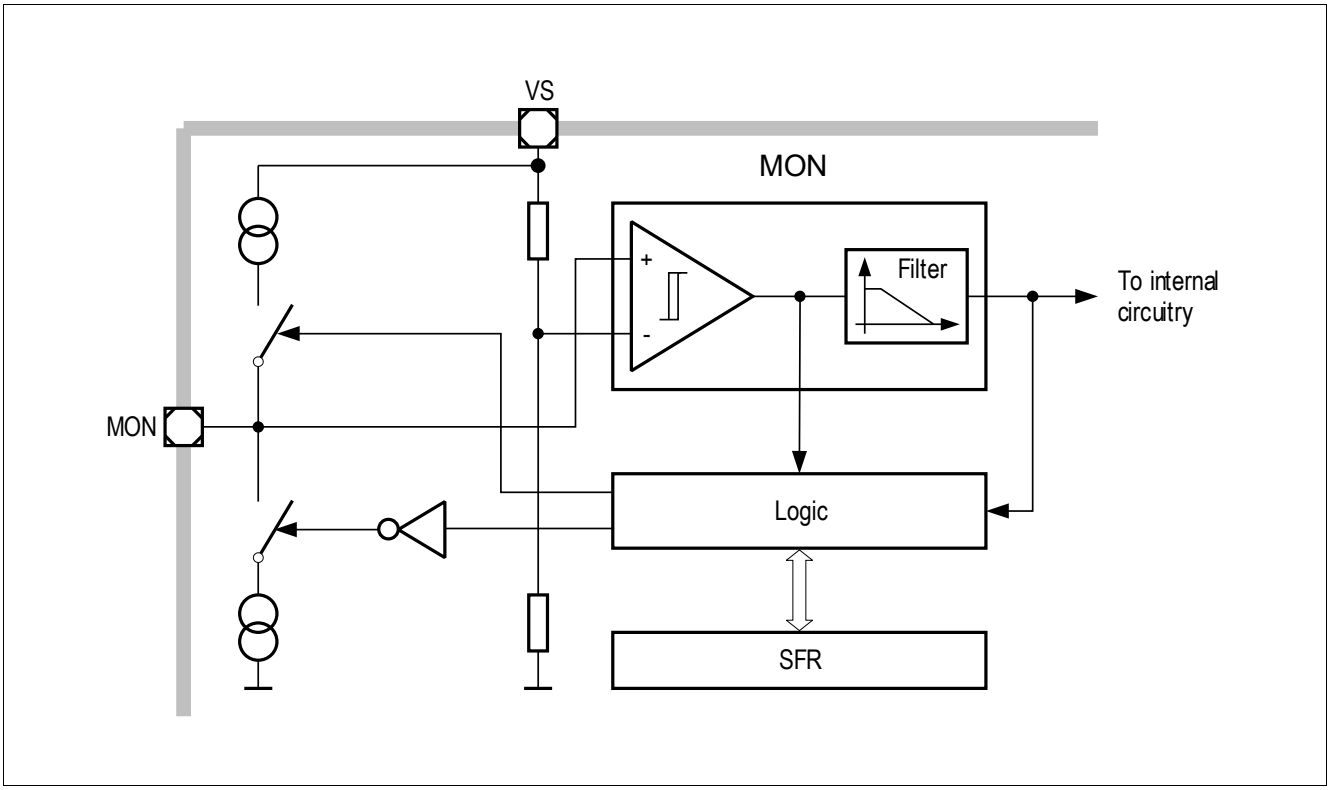


Figure 28 High-voltage monitor input block diagram

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26 Bridge driver (incl. charge pump)

26.1 Features

The MOSFET driver is intended to drive external normal-level NFET transistors in bridge configurations. The driver provides many diagnostic functions for detecting faults.

Functional features

- External power NFET transistor driver stage with driver capability of Q_{tot_max}.
- Adjustable cross-conduction protection.
- Supply voltage (VSD) monitoring incl. adjustable over- and undervoltage shutdown with configurable interrupt signalling.
- VSD operating range: V_{SD_AM}.
- VDS comparators for short-circuit-detection in both on- and off-states.
- Open-load detection in the off-state.
- The maximum PWM frequency is defined for 25 kHz.

26.2 Introduction

The MOSFET driver stage can be used for controlling external power NFET transistors (normal level). The module output is controlled by the SFR or the System PWM Machine (CCU6).

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26.2.1 Block diagram

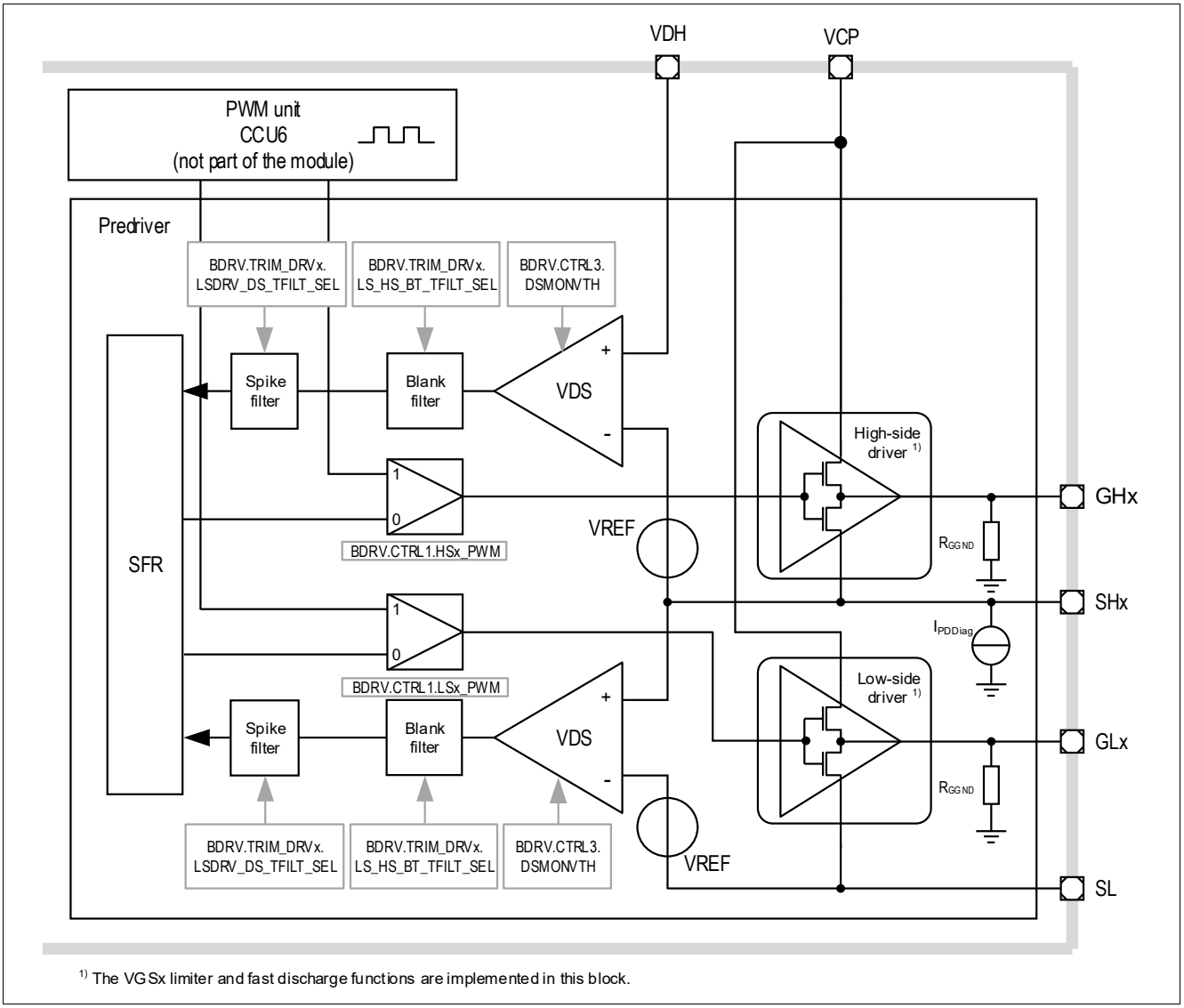


Figure 29 Bridge driver module block diagram (incl. system connections)

26.2.2 General

Protection functions

- Overcurrent detection and shutdown feature for external MOSFET based on drain-source measurements.
- Programmable minimum cross-current protection time.
- Open-load detection feature in the off-state for external MOSFET.

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27 Application information

27.1 Electric drive application

Figure 30 shows the TLE9868QXB20 in an electric drive application setup controlling a DC-brush motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition, or quality of the device.

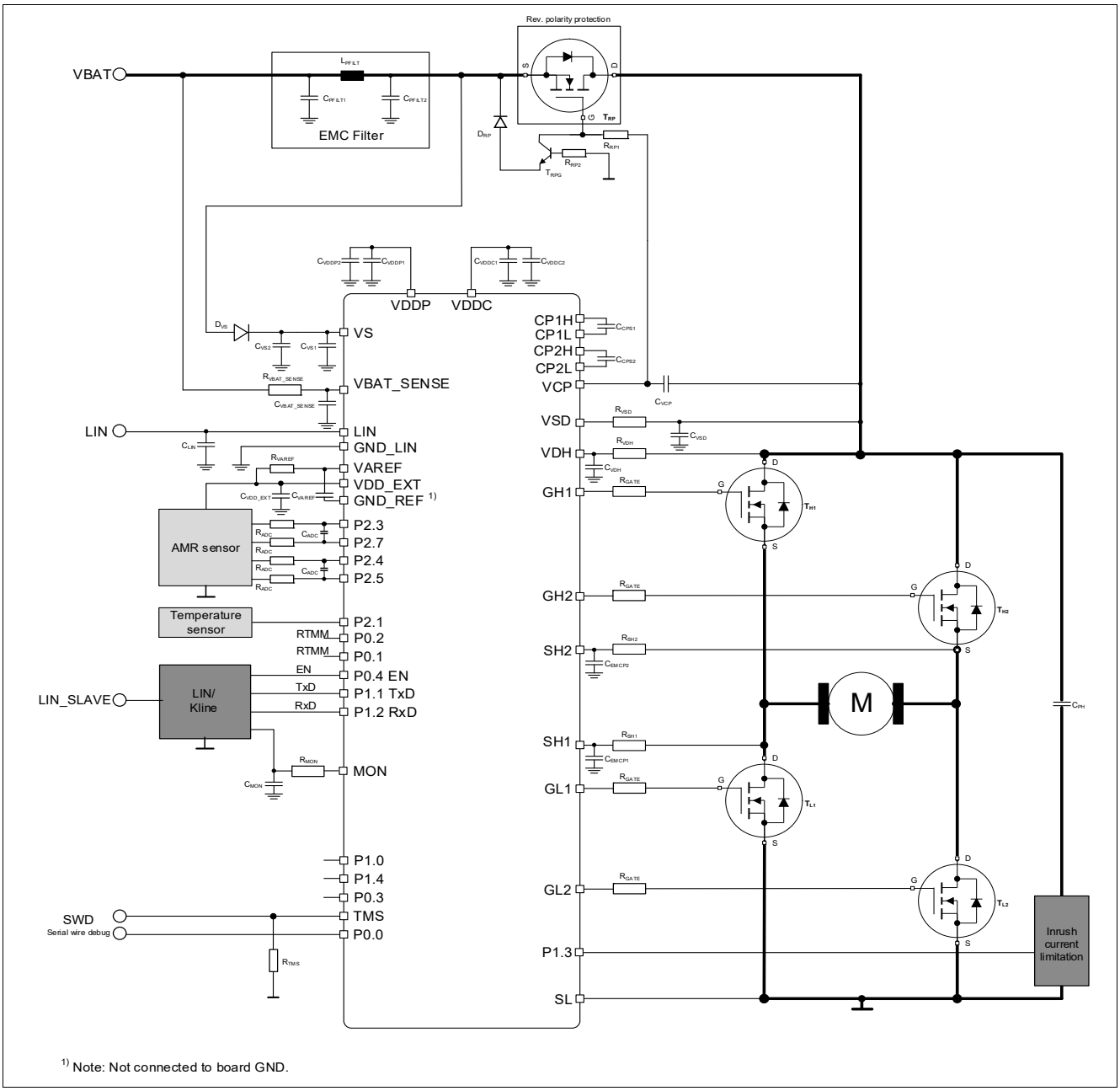


Figure 30 Simplified sample application diagram

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

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Application information

The 4-Channel H-Bridge allows to drive the motor in both directions. Settings are done via LIN. Synchronization with a second motor can be done with an external LIN/KLine transceiver. Motor position and speed is sensed with the sensor connected via analog input or SPI.

Table 15 External component (BOM)

Symbol	Function	Component
C_{VS1}	Blocking capacitor at VS pin	≥ 100 nF ceramic, ESR < 1 Ω
C_{VS2}	Blocking capacitor at VS pin	> 2.2 µF Elco[1)]
C_{VDDP1}	Blocking capacitor at VDDP pin	See P_2.1.2
C_{VDDP2}	Blocking capacitor at VDDP pin	See P_2.1.20
$C_{VDDEXT1}$	Blocking capacitor at VDDEXT pin	See P_2.3.22
$C_{VDDEXT2}$	Blocking capacitor at VDDEXT pin	See P_2.3.20
C_{VDDC1}	Blocking capacitor at VDDC pin	See P_2.2.1
C_{VDDC2}	Blocking capacitor at VDDC pin	See P_2.2.17
C_{VAREF}	Blocking capacitor at VAREF pin	See P_9.1.1
C_{LIN}	Standard C for LIN slave	220 pF
C_{ADC}	Filter C for sensor interface	39 nF (for OSR = 512)
C_{VSD}	Filter C for charge pump end driver	1 µF
C_{CP1}	Charge pump capacitor	220 nF
C_{CP2}	Charge pump capacitor	220 nF
C_{VCP}	Charge pump capacitor	470 nF
C_{MON}	Filter C for ISO pulses	10 nF
C_{VDH}	Capacitor	3.3 nF
C_{EMCP1}, C_{EMCP2}	Capacitor	1 nF
C_{PFILT1}, C_{PFILT2}	Capacitor	Application specific
C_{PH}	Capacitor	Depending on usecase
C_{VBAT_SENSE}	Filter C for ISO pulses	10 nF
R_{MON}	Resistor at MON pin	3.9 kΩ
R_{VBAT_SENSE}	Resistor at VBAT_SENSE pin	1 kΩ
R_{VSD}	Limitation of reverse current due to transient (-2 V, 8 ms)	2.2 Ω
R_{VDH}	Resistor	1 kΩ
R_{GATE}	Gate resistor	2.2 Ω
R_{ADC}	Filter resistor	1 KΩ (for OSR = 512)
R_{VAREF}	Resistor at VAREF for filtering of reference voltage	200 Ω (for OSR = 512)
R_{RP1}	Resistor to charge reverse polarity transistor gate	3.3 KΩ
R_{RP2}	Resistor for reverse polarity discharge transistor	10 KΩ
T_{H1}, T_{H2}, T_{L1}, T_{L2}	H-Bridge, N-Channel MOSFET	IPD90N04S4-05
T_{RP}	Reverse Polarity, N-Channel MOSFET	IPD90N04S4-05
T_{RPG}	Reverse Diode for Transistor TRP	–
D_{RP}	Diode to discharge Reverse Polarity Gate	–

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Table 15 External component (BOM) (cont'd)

Symbol	Function	Component
D_{VS}	Reverse-polarity protection diode	–
R_{TMS}	Pull-down resistance at TMS pin	500 Ω

1) The capacitor must be dimensioned so as to ensure that operations which modify the content of the flash are never interrupted (e.g., in case of power loss).

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27.2 ESD immunity according to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “gun test” (150 pF, 330 Ω) have been performed. The results and test conditions will be available in a test report.

Table 16 ESD “gun test”

Performed test	Result	Unit	Remarks
ESD at pin LIN, versus GND[1)]	> 6	kV	Positive pulse
ESD at pin LIN, versus GND[1)]	< -6	kV	Negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100 nF, R_{MON} = 1 kΩ, C_{LIN} = 220 pF, C_{VS} = > 20 µF ELCO + 100 nF ESR < 1 Ω, C_{VSD} = 1 µF, R_{VSD} = 2 Ω.

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28 Electrical characteristics

This chapter includes all relevant electrical characteristics of the product TLE9868QXB20.

28.1 General characteristics

28.1.1 Absolute maximum ratings

Table 17 Absolute maximum ratings[1)]

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages – supply pins							
Supply voltage VS	V_S	-0.3	–	40	V	Load dump	P_1.1.1
Supply voltage VSD	V_{SD}	-0.3	–	48	V	–	P_1.1.2
Supply voltage VSD	$V_{SD_max_extend}$	-2.8	–	48	V	[2)] Series resistor R_{VSD} = 2.2 Ω, t = 8 ms	P_1.1.32
Voltage range VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_1.1.3
Voltage range VDDP	$V_{DDP_max_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with $\Delta V_S/\Delta t \geq 1$ V/µs; duration: $t \leq 150$ µs; $C_{VDDP} \leq 570$ nF	P_1.1.41
Voltage range VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_1.1.4
Voltage range VDDEXT	$V_{DDEXT_max_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with $\Delta V_S/\Delta t \geq 1$ V/µs; duration: $t \leq 150$ µs; $C_{VDDEXT} \leq 570$ nF	P_1.1.42
Voltage range VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_1.1.5
Voltages – high-voltage pins							
Battery voltage VBAT_SENSE	V_{BAT_SENSE}	-28	–	40	V	[3)]	P_1.1.6
Input voltage at LIN	V_{LIN}	-28	–	40	V	–	P_1.1.7
Input voltage at MON	$V_{MON_maxrate}$	-28	–	40	V	[3)]	P_1.1.8
Input voltage at VDH	$V_{VDH_maxrate}$	-2.8	–	40	V	[4)]	P_1.1.38
Voltage range at GHx	V_{GH}	-8.0	–	48	V	[5)]	P_1.1.9
Voltage range at GHx vs. SHx	V_{GHvsSH}	-0.3	–	14	V	–	P_1.1.44
Voltage range at SHx	V_{SH}	-8.0	–	48	V	–	P_1.1.11
Voltage range at SL	V_{SL}	-8.0	–	48	V	–	P_1.1.48
Voltage range at GLx	V_{GL}	-8.0	–	48	V	[6)]	P_1.1.13
Voltage range at GLx vs. SL	V_{GLvsSL}	-0.3	–	14	V	–	P_1.1.45

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Table 17 Absolute maximum ratings[1)] (cont'd)

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	–	48	V	[7)]	P_1.1.15
Voltages – GPIOs							
Voltage on any port pin[8)]	V_{in}	-0.3	–	V_{DDP} +0.3	V	[9)] $V_{IN} < V_{DDPmax}$	P_1.1.16
Current at VCP pin							
Max. current at VCP pin	I_{VCP}	-15	–	–	mA	–	P_1.1.35
Injection current at GPIOs							
Injection current on any port pin	I_{GPIONM}	-5	–	5	mA	[10)]	P_1.1.34
Sum of all injected currents in Normal mode	I_{GPIOAM_sum}	-50	–	50	mA	[10)]	P_1.1.30
Sum of all injected currents in Sleep mode	$I_{GPIOSleep_sum}$	-5	–	5	mA	[10)]	P_1.1.37
Other voltages							
Input voltage VAREF	V_{AREF}	-0.3	–	V_{DDP} +0.3	V	–	P_1.1.17
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_1.1.18
Storage temperature	T_{stg}	-55	–	150	°C	–	P_1.1.19
ESD susceptibility							
ESD susceptibility all pins	V_{ESD1}	-2	–	2	kV	[11)] HBM	P_1.1.20
ESD susceptibility pins MON, VS, VSD, VBAT_SENSE vs.GND	V_{ESD2}	-4	–	4	kV	[12)] HBM	P_1.1.21
ESD susceptibility pins LIN vs. GND_LIN	V_{ESD3}	-6	–	6	kV	[11)] HBM	P_1.1.22
ESD susceptibility CDM all pins vs. GND	V_{ESD_CDM1}	-500	–	500	V	[13)]	P_1.1.28
ESD susceptibility CDM pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) vs. GND	V_{ESD_CDM2}	-750	–	750	V	[13)]	P_1.1.43

1) Not subject to production test, specified by design.
2) Conditions and minimum values are derived from application conditions for reverse polarity events.
3) The minimum voltage of -28 V applies only with an external 3.9 kΩ series resistor.
4) The minimum voltage of -2.8 V applies only with an external 1 kΩ series resistor.

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5) To achieve the maximum ratings on this pin, the following relationships with parameter P_1.1.44 have to be observed: $V_{GH} < V_{SH} + V_{GHvsSH_min}$ and $V_{SH} < V_{GH} + 0.3$ V.
6) To achieve the maximum ratings on this pin, the following relationships with parameter P_1.1.45 have to be observed: $V_{GL} < V_{SL} + V_{GLvsSL_min}$ and $V_{SL} < V_{GL} + 0.3$ V.
7) These limits can be kept if the maximum current drawn out of the pin does not exceed the limit of 200 µA.
8) See the XTAL parameter specification, when GPIOs (Port pins P2.0 and P2.2) are used as XTAL.
9) Includes TMS and RESET.
10) P_1.1.16 must not been exceeded in the injection current.
11) ESD susceptibility based on the HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
12) MON with external circuitry of a series resistor with 3.9 kΩ and 10 nF (at connector); VS with an external ceramic capacitor with 100 nF; VSD with an external capacitor with 470 nF; VDH with external circuitry of a series resistor with 1 kΩ and 3.3 nF (at pin).
13) ESD susceptibility based on the HBM according to ANSI/ESDA/JEDEC JESD22-C101F.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered to be outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

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28.1.2 Functional range

Table 18 Functional range

T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended supply voltage in Active mode	$V_{S_AM_extend}$	28	–	40	V	1)2) Extended supply range leads to parameter deviation.	P_1.2.16
Supply voltage in Active mode for MOSFET driver supply	V_{SD_AM}	5.1	–	28	V	–	P_1.2.18
Extended supply voltage in Active mode for MOSFET driver supply	$V_{SD_AM_extend}$	28	–	32	V	1)2)4) Extended supply range leads to parameter deviation.	P_1.2.17
Specified supply voltage for LIN transceiver	$V_{S_AM_LIN}$	5.5	–	18	V	Parameter specification.	P_1.2.2
Extended supply voltage for LIN transceiver	$V_{S_AM_LIN}$	4.8	–	28	V	2) Extended supply range leads to parameter deviation.	P_1.2.14
Supply voltage in Active mode with reduced functionality (retaining full operation for microcontroller and flash)	V_{S_AMmin}	3.0	–	5.5	V	3)	P_1.2.3
Supply voltage in Sleep mode	V_{S_Sleep}	3.0	–	28	V	–	P_1.2.4
Supply voltage transients slew rate	$\Delta V_S/\Delta t$	-1	–	1	V/µs	4)	P_1.2.5
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	4)	P_1.2.7
Operating frequency	f_{sys}	5	–	20	MHz	5)	P_1.2.8
Junction temperature	T_j	-40	–	150	°C	–	P_1.2.9

1) This operation voltage range is only allowed for a short duration: $t_{max} \leq 400$ ms (continuous operation at this voltage is not allowed), f_{sys} = 24 MHz, I_{VDDP} = 10 mA, I_{VDDEXT} = 5 mA. In addition, the power dissipation caused by the charge pump and the MOSFET driver has to be considered.

2) Parameter deviations mean that the electrical parameters of the device may present values outside the range specified within the minimum and maximum values.

3) Functionality is reduced (for example, cranking pulse); parameter deviations are possible: The electrical parameters of the device may present values outside the range specified within the minimum and maximum values.

4) Not subject to production test, specified by design.

5) Function not specified when limits are exceeded.

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28.1.3 Current consumption

Table 19 Electrical characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at VS pin							
Current consumption in Active mode at VS pin	I_{Vs}	–	30	35	mA	[1] f_{sys} = 20 MHz No loads on pins, LIN in recessive state	P_1.3.1
Current consumption in Active mode at VSD pin	I_{VSD}	–	–	40	mA	20 kHz PWM on bridge driver	P_1.3.8
Current consumption in Slow-down mode	I_{SDM}	–	–	30	mA	f_{sys} = 5 MHz; LIN communication running; charge pump on (reverse polarity FET on), external low-side FET static on (Motor Break mode); VDDEXT on; Sensor input read via SDADC and calculate angle ($f_{ADC3/4}$ = 5 MHz); all other modules set to power down; V_S = 13.5 V	P_1.3.6
Current consumption in Sleep mode	I_{Sleep}	–	30	35	µA	[2] System in Sleep mode, microcontroller not powered, wake-capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: -40°C ≤ T_j ≤ 85°C; V_S = 5.5 V to 18 V	P_1.3.3
Current consumption in Sleep mode, extended range	I_{Sleep_extend}	–	90	200	µA	[2] System in Sleep mode, microcontroller not powered, wake-capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: -40°C ≤ T_j ≤ 150°C; V_S = 5.5 V to 18 V	P_1.3.15

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Table 19 Electrical characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep mode	I_{Sleep}	–	–	33	µA	2) System in Sleep mode, microcontroller not powered, wake-capable via LIN and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: -40°C ≤ T_j ≤ 40°C; V_S = 5.5 V to 18 V	P_1.3.9
Current consumption in Sleep mode with cyclic wake	I_{Cyclic}	–	–	110	µA	2) -40°C ≤ T_j ≤ 85°C; V_S = 5.5 V to 18 V; t_{Cyclic_ON} = 4 ms; t_{Cyclic_OFF} = 2048 ms	P_1.3.4

1) Current on V_S, ADC1/2 active, timer running, LIN active (recessive).

2) Incl. leakage currents from VBAT_SENSE, VDH, VSD and MON.

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified under the conditions noted in the related electrical characteristics table.

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28.1.4 Thermal resistance

Table 20 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to soldering point	R_{thJSP}	–	6	–	K/W	1) Measured to exposed pad	P_1.4.1
Junction to ambient	R_{thJA}	–	33	–	K/W	1)2)	P_1.4.2
Junction to top	$\Psi_{JTOP\ 2s2p}$	–	8	–	K/W	1)2)	P_1.4.3

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 with natural convection on an FR4 2s2p board. Board: 76.2 × 114.3 × 1.5 mm^3 with two inner copper layers (35 µm strong), with thermal dissipation via array under the exposed pad contacting the first inner copper layer and 300 mm^2 of cooling area on the bottom layer (70 µm).

28.1.5 Timing characteristics

The transition times between the system modes are specified here. Generally, the timings are defined from the time when the corresponding bits in register PMCON0 are set until the sequence is terminated.

Table 21 System timing[1)]

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up time when running on battery	t_{start}	–	–	3	ms	Battery ramp-up time until the start of code execution	P_1.5.6
Wake-up time when running on battery	$t_{startSW}$	–	–	1.5	ms	Battery ramp-up time until the MCU reset is released; V_S > 3 V and RESET = 1	P_1.5.1
Time to exit sleep	$t_{sleep\ -\ exit}$	–	–	1.5	ms	Rising/falling edge of any wake-up signal (LIN, MON) until the MCU reset is released	P_1.5.2
Time to enter sleep	$t_{sleep\ -\ entry}$	–	–	330	µs	2)	P_1.5.3

1) Not subject to production test, specified by design.

2) Wake events during sleep entry are stored and lead to wake-up after Sleep mode is reached.

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28.2 Power management unit (PMU)

This chapter includes all electrical characteristics of the power management unit.

28.2.1 PMU I/O supply (VDDP) parameters

This chapter describes electrical parameters which are observable on the SoC level. The pad-supply VDDP and the transition times between the system modes are specified in the following table.

Table 22 Electrical characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDP}	0	–	50	mA	1)	P_2.1.1
Specified output current	I_{VDDP}	0	–	30	mA	1)2)	P_2.1.22
Required decoupling capacitance	C_{VDDP1}	0.1	–	2.2	µF	3)4)5) ESR < 1 Ω	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	0.47	–	2.2	µF	3)4)5)	P_2.1.20
Output voltage including line and load regulation in Active mode	V_{DDPOUT}	4.9	5.0	5.1	V	6) I_{load} < 90 mA; V_S > 5.5 V	P_2.1.3
Output voltage including line and load regulation in Active mode	V_{DDPOUT}	4.9	5.0	5.1	V	2)6) I_{load} < 70 mA; V_S > 5.5 V	P_2.1.23
Output drop in Active mode	$V_{SVDDPout}$	–	50	400	mV	7) I_{VDDP} = 30 mA; 3.5 V < V_S < 5.0 V	P_2.1.4
Load regulation in Active mode	$V_{VDDPLOR}$	-50	–	50	mV	2 mA … 90 mA; C = 570 nF	P_2.1.5
Line regulation in Active mode	$V_{VDDPLIR}$	-50	–	50	mV	V_S = 5.5 V … 28 V	P_2.1.6
Overvoltage detection	V_{DDPOV}	5.14	–	5.4	V	V_S > 5.5 V; Overvoltage leads to SUPPLY_NMI	P_2.1.7
Overvoltage detection filter time	t_{FILT_VDDPOV}	–	735	–	µs	3)8)	P_2.1.24
Voltage OK detection threshold	V_{DDPOK}	–	3	–	V	3)	P_2.1.25
Voltage stable detection range[9)]	ΔV_{DDPSTB}	-220	–	220	mV	3)	P_2.1.26
Undervoltage reset	V_{DDPUV}	2.5	2.6	2.7	V	–	P_2.1.8
Overcurrent diagnostic	I_{VDDPOC}	91	–	220	mA	–	P_2.1.9
Overcurrent diagnostic filter time	t_{FILT_VDDPOC}	–	27	–	µs	3)8)	P_2.1.27
Overcurrent diagnostic shutdown time	$t_{FILT_VDDPOC_SD}$	–	290	–	µs	3)8)10)	P_2.1.28

1) Specified output current for port supply and additional other external loads, already excluding VDDC current.

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2) This use case applies when the output current on VDDEXT does not exceed 40 mA.
3) Not subject to production test, specified by design.
4) Ceramic capacitor.
5) Ranges of P_2.1.2 and P_2.1.20 can be added to one ceramic capacitor with ESR < 1 Ω.
6) Load current includes internal supply.
7) Output drop for IVDDP without internal supply current.
8) This filter time is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.
9) The absolute voltage value is the sum of parameters $V_{DDP} + \Delta V_{DDPSTB}$.
10) When $t_{FILT_VDDCOC_SD}$ is passed and the overcurrent condition is still present, the device will enter Sleep mode.

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28.2.2 PMU core supply (VDDC) parameters

This chapter describes electrical parameters which are observable on the SoC level. The core-supply VDDC and the transition times between the system modes are specified in the following table.

Table 23 Electrical characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VDDC1}	0.1	–	1	µF	1)2)3) ESR < 1 Ω	P_2.2.1
Required buffer capacitance for stability (load jumps)	C_{VDDC2}	0.33	–	1	µF	2)3)	P_2.2.17
Output voltage including line regulation in Active mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40 mA	P_2.2.2
Load regulation in Active mode	V_{DDCLOR}	-50	–	50	mV	2 mA … 40 mA; C = 430 nF	P_2.2.3
Line regulation in Active mode	V_{DDCLIR}	-25	–	25	mV	V_{DDP} = 2.5 V … 5.5 V	P_2.2.4
Overvoltage detection	V_{DDCOV}	1.59	1.62	1.68	V	Overvoltage leads to SUPPLY_NMI	P_2.2.5
Overvoltage detection filter time	t_{FILT_VDDCOV}	–	735	–	µs	1)4)	P_2.2.18
Voltage OK detection range[5)]	ΔV_{DDCOK}	-280	–	280	mV	1)	P_2.2.19
Voltage stable detection range[6)]	ΔV_{DDCSTB}	-110	–	110	mV	1)	P_2.2.20
Undervoltage reset	V_{DDVUV}	1.136	1.20	1.264	V	–	P_2.2.6
Overcurrent diagnostic	I_{VDDCOC}	45	–	100	mA	–	P_2.2.7
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	1)4)	P_2.2.21
Overcurrent diagnostic shutdown time	$t_{FILT_VDDCOC_SD}$	–	290	–	µs	1)4)7)	P_2.2.22

1) Not subject to production test, specified by design.
2) Ceramic capacitor.
3) Ranges of P_2.2.1 and P_2.2.17 can be added to one ceramic capacitor with ESR < 1 Ω.
4) This filter time is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.
5) This absolute voltage value is the sum of parameters $V_{DDC} + \Delta V_{DDCSTB}$.
6) This absolute voltage value is the sum of parameters $V_{DDC} + \Delta V_{DDCOK}$.
7) When $t_{FILT_VDDCOC_SD}$ is passed and the overcurrent condition is still present the device will enter Sleep mode.

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28.2.3 VDDEXT voltage regulator (5.0 V) parameters

Table 24 Electrical characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDEXT}	0	–	20	mA	–	P_2.3.1
Specified output current	I_{VDDEXT}	0	–	40	mA	1)	P_2.3.21
Required decoupling capacitance	$C_{VDDEXT1}$	0.1	–	2.2	µF	2)3)4) ESR < 1 Ω	P_2.3.22
Required buffer capacitance for stability (load jumps)	$C_{VDDEXT2}$	1	–	2.2	µF	2)3)4)	P_2.3.20
Output voltage including line and load regulation	V_{DDEXT}	4.9	5.0	5.1	V	4) I_{load} < 20 mA; V_S > 5.5 V	P_2.3.3
Output voltage including line and load regulation	V_{DDEXT}	4.8	5.0	5.2	V	I_{load} < 40 mA; V_S > 5.5 V	P_2.3.23
Output drop in Active mode	V_S-V_{DDEXT}	–	50	300	mV	4) I_{load} < 20 mA; 3 V < V_S < 5.0 V	P_2.3.4
Output drop in Active mode	V_S-V_{DDEXT}	–	–	400	mV	I_{load} < 40 mA; 3 V < V_S < 5.0 V	P_2.3.14
Load regulation in Active mode	$V_{DDEXTLOR}$	-50	–	50	mV	2 mA … 40 mA; C = 200 nF	P_2.3.5
Line regulation in Active mode	$V_{VDDEXTLIR}$	-50	–	50	mV	V_S = 5.5 V … 28 V	P_2.3.6
Power supply ripple rejection in Active mode	$P_{SSRVDDEXT}$	50	–	–	dB	4) V_S = 13.5 V; f = 0 kHz … 1 kHz; V_r = 2 Vpp	P_2.3.7
Overvoltage detection	$V_{VDDEXTOV}$	5.18	–	5.4	V	V_S > 5.5 V	P_2.3.8
Overvoltage detection filter time	$t_{FILT_VDDEXTOV}$	–	735	–	µs	4)5)	P_2.3.24
Voltage OK detection threshold	$V_{VDDEXTOK}$	–	3	–	V	4)	P_2.3.25
Voltage stable detection range[6)]	$\Delta V_{VDDEXTSTB}$	-220	–	220	mV	4)	P_2.3.26
Undervoltage trigger	$V_{VDDEXTUV}$	2.6	2.8	3.0	V	7)	P_2.3.9
Overcurrent diagnostic	$I_{VDDEXTOC}$	50	–	160	mA	–	P_2.3.10
Overcurrent diagnostic filter time	$t_{FILT_VDDEXTOC}$	–	27	–	µs	4)5)	P_2.3.27
Overcurrent diagnostic shutdown time	$t_{FILT_VDDEXTOC_SD}$	–	290	–	µs	4)5)	P_2.3.28

1) This use case requires the reduced utilization of VDDP output current by 20 mA, see P_2.1.22.
2) Ceramic capacitor.
3) Ranges of P_2.3.22 and P_2.3.20 can be added to one ceramic capacitor with ESR < 1 Ω.
4) Not subject to production test, specified by design.
5) This filter time is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.
6) The absolute voltage value is the sum of parameters $V_{DDEXT} + \Delta V_{DDEXTSTB}$.
7) When the undervoltage condition is met, the VDDEXT_CTRL.bit.SHORT bit is set.

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28.2.4 VPRE voltage regulator (PMU subblock) parameters

The PMU VPRE regulator acts as a supply for the VDDP and VDDEXT voltage regulators.

Table 25 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VPRE}	–	–	110	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

28.2.4.1 Load-sharing scenario for the VPRE regulator

The figure below shows the load-sharing scenario for VPRE regulator.

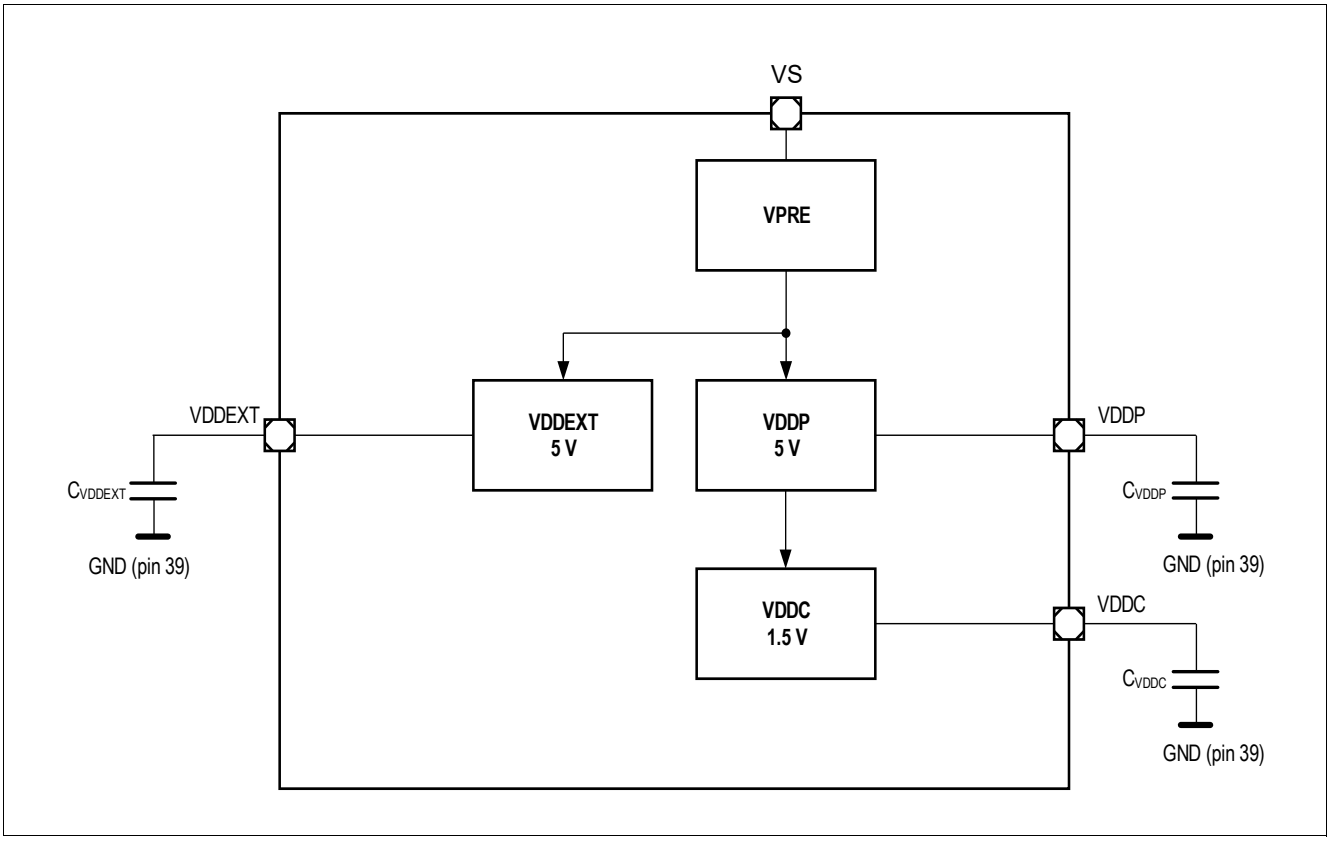


Figure 31 Load-sharing scenario for the VPRE regulator

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28.2.5 Power-down voltage regulator (PMU subblock) parameters

The PMU power-down voltage regulator consists of two subblocks:

- Power-down preregulator: VDD5VPD
- Power-down core regulator: VDD1V5_PD (Supply used for the GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameters.

Table 26 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDD1V5_PD							
Power-on reset threshold	$V_{DD1V5_PD_RSTTH}$	1.2	–	1.5	V	1)	P_2.5.1

1) Not subject to production test, specified by design.

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28.3 System clocks

28.3.1 Parameters of oscillators and PLLs

Table 27 Electrical characteristics of the system clocks

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PMU oscillators (power management unit)							
Frequency of LP_CLK	f_{LP_CLK}	14	18	22	MHz	This clock is used during startup and can be used when the PLL fails.	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	This clock is used for cyclic wakes.	P_3.1.2
CGU oscillator (clock generation unit microcontroller)							
Short-term frequency deviation[1)]	f_{TRIMST}	-0.4	–	0.4	%	[2)3)] Within any 10 ms, e.g., after synchronization to a LIN frame. (The PLL settings must not change in these 10 ms.)	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.5	–	1.5	%	Including temperature and lifetime deviation	P_3.1.4
CGU-OSC start-up time	t_{OSC}	–	–	10	µs	[3)] Start-up time OSC from Sleep mode, power supply stable	P_3.1.5
PLL (clock generation unit microcontroller) [3)]							
VCO frequency range mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL = “0”	P_3.1.6
VCO frequency range mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL = “1”	P_3.1.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_3.1.8
XTAL1 input frequency range	f_{OSC}	4	–	16	MHz	–	P_3.1.9
Output frequency range	f_{PLL}	0.04687	–	80	MHz	–	P_3.1.10
Free-running frequency mode 0	$f_{VCOfree_0}$	–	–	38	MHz	VCOSEL = “0”	P_3.1.11
Free-running frequency mode 1	$f_{VCOfree_1}$	–	–	76	MHz	VCOSEL = “1”	P_3.1.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_3.1.13
Peak period jitter	t_{jp}	-500	–	500	ps	[4)] For K = 1	P_3.1.14

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Table 27 Electrical characteristics of the system clocks (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Accumulated jitter	jacc	–	–	5	ns	[4] For K = 1	P_3.1.15
Lock-in time	t_L	–	–	200	µs	–	P_3.1.16

1) The typical oscillator frequency is 5 MHz.
2) V_{DDC} = 1.5 V, T_j = 25°C.
3) Not subject to production test, specified by design.
4) This parameter is valid for PLL operation with an external clock source and thus reflects the real PLL performance.

28.3.2 External clock parameters XTAL1, XTAL2

Table 28 Functional range

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).[1]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range limits for signal on XTAL1	V_{IX1_SR}	-1.7 + V_{DDC}	–	1.7	V	[2]	P_3.2.1
Input voltage (amplitude) on XTAL1	V_{AX1_SR}	0.3 × V_{DDC}	–	–	V	[3] Peak-to-peak voltage	P_3.2.2
XTAL1 input current	I_{IL}	–	–	±20	µA	0 V < V_{IN} < V_{DDI}	P_3.2.3
Oscillator frequency	f_{OSC}	4	–	24	MHz	Clock signal	P_3.2.4
Oscillator frequency	f_{OSC}	4	–	16	MHz	Crystal or resonator	P_3.2.5
High time	t_1	6	–	–	ns	–	P_3.2.6
Low time	t_2	6	–	–	ns	–	P_3.2.7
Rise time	t_3	–	8	8	ns	–	P_3.2.8
Fall time	t_4	–	8	8	ns	–	P_3.2.9

1) This parameter table is not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

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28.4 Flash memory

This chapter includes the parameters for the 128 kByte embedded flash module.

28.4.1 Flash parameters

Table 29 Flash characteristics[1)]

V_S = 3.0 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	[3)] 3 V ≤ V_S ≤ 28 V	P_4.1.1
Erase time per sector or page	t_{ER}	–	4[2)]	4.5	ms	[3)] 3 V ≤ V_S ≤ 28 V	P_4.1.2
Data retention time	t_{RET}	20	–	–	year	1,000 erase/program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	year	[4)] 1,000 erase/ program cycles T_j = 30°C	P_4.1.9
Flash erase endurance for pages in user sectors	N_{ER}	30	–	–	kilocycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[5)] Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kilocycles	[6)]	P_4.1.6

1) Not subject to production test, specified by design.

2) Programming and erase times depend on the internal flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.

3) While the flash memory is being programmed or erased, flash read operation is not possible to be performed.

4) Determined by extrapolating of lifetime tests.

5) T_j = 25°C.

6) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles, this limit will not be violated. For data sectors, the integrated EEPROM emulation firmware routines handle this limit automatically. For wordline erases in code sectors (without EEPROM emulation), it is recommended to execute a software-based refresh, which use the integrated NVMBRNG random number generator to statistically start a refresh.

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28.5 Parallel ports (GPIO)

28.5.1 Description of the keep and force currents

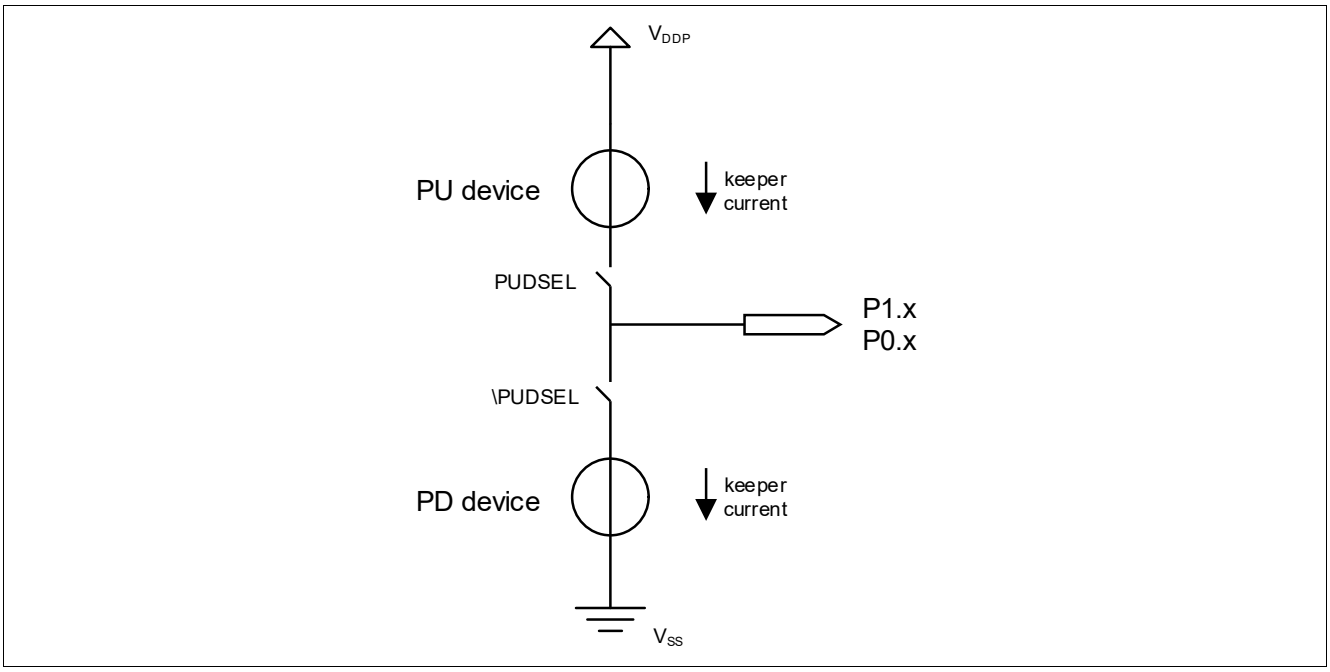


Figure 32 Pull-up/down device

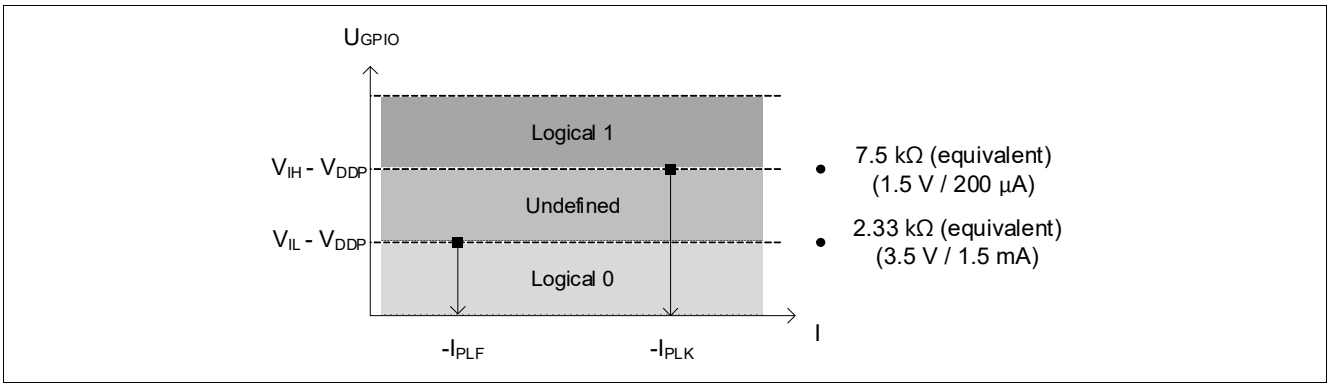


Figure 33 Pull-up keep and force currents

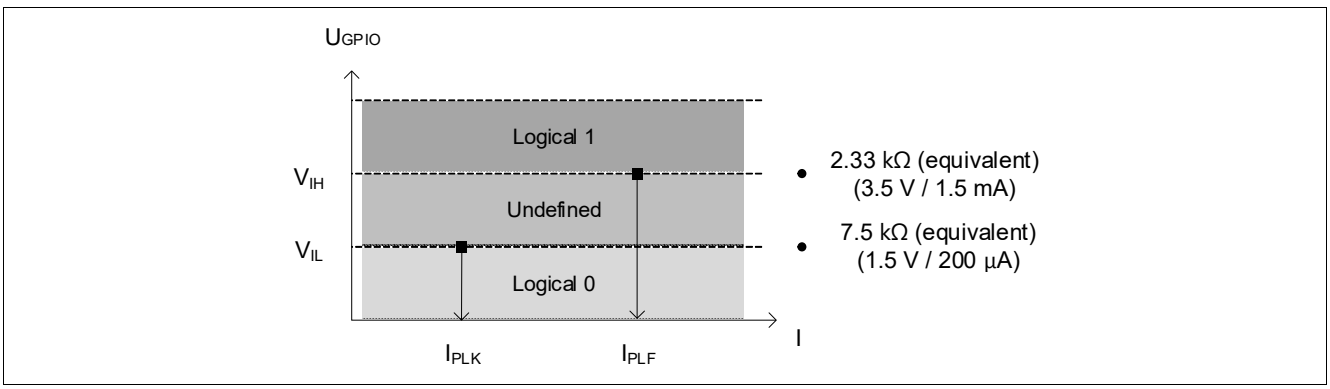


Figure 34 Pull-down keep and force currents

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28.5.2 DC parameters of port 0, port 1, TMS, and reset

Note: Operating conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the maximum allowed current that can be taken out of VDDP.

Table 30 Current limits for port output drivers[1)]

Port output driver mode	Maximum output current (I_{OLmax}, - I_{OHmax})		Maximum output current (I_{OLnom}, - I_{OHnom})		Number
	$V_{DDP} \geq 4.5$ V	2.6 V < V_{DDP} < 4.5 V	$V_{DDP} \geq 4.5$ V	2.6 V < V_{DDP} < 4.5 V	
Strong driver[2)]	5 mA	3 mA	1.6 mA	1.0 mA	P_5.1.15
Medium driver[3)]	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.1.1
Weak driver[3)]	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.1.2

1) Not subject to production test, specified by design.
2) Not available for port pins P0.4, P1.0, P1.1, and P1.2.
3) All P0.x and P1.x pins.

Table 31 DC characteristics of port 0, port 1, TMS, and reset

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input hysteresis	HYS_{P0_P1}	0.11 × V_{DDP}	–	–	V	[1)] Series resistance = 0 Ω; 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.1.5
Input hysteresis	$HYS_{P0_P1_exend}$	–	0.09 × V_{DDP}	–	V	[1)] Series resistance = 0 Ω; 2.6 V ≤ V_{DDP} ≤ 4.5 V	P_5.1.16
Input low voltage	V_{IL}	-0.3	–	0.3 × V_{DDP}	V	[2)] 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 × V_{DDP}	–	V	[1)] 2.6 V ≤ V_{DDP} ≤ 4.5 V	P_5.1.17
Input high voltage	V_{IH}	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	[2)] 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 × V_{DDP}	V_{DDP} + 0.3	V	[1)] 2.6 V ≤ V_{DDP} ≤ 4.5 V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	[3)4)] $I_{OL} \leq I_{OLmax}$	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	[3)5)] $I_{OL} \leq I_{OLnom}$	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	[3)4)] $I_{OH} \geq I_{OHmax}$	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	[3)5)] $I_{OH} \geq I_{OHnom}$	P_5.1.9
Input leakage current	$I_{OZ_extend1}$	-500	–	500	nA	-40°C ≤ T_j ≤ 25°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.20
Input leakage current	I_{OZ1}	-5	–	5	µA	[6)] 25°C < T_j ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	$I_{OZ_extend2}$	-15	–	15	µA	85°C < T_j ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11

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Table 31 DC characteristics of port 0, port 1, TMS, and reset (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pull level keep current	I_{PLK}	-200	–	200	µA	7) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (down)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	1.5	mA	7) $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (down)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset pin timing							
Reset pin input filter time	t_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5 V, specified for 4.5 V < V_{DDP} < 5.5 V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9 V < V_{DDP} < 5.1 V, I_{OL} = 4 mA, I_{OH} = -4 mA, specified for 4.5 V < V_{DDP} < 5.5 V.

5) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→*GND*, V_{OH}→V_{DDP}). Tested at 4.9 V < V_{DDP} < 5.1 V, I_{OL} = 1 mA, I_{OH} = -1 mA.

6) The given values are worst-case values. In production tests, this leakage current is only tested at 150°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_j = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times Tj)}$ [µA]. For example, at a temperature of 95°C, the resulting leakage current is 3.2 µA.
Leakage derating depending on the voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for the maximum temperature.

7) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
These values apply to the fixed pull devices in dedicated pins and to the user-selectable pull devices in general-purpose IO pins.

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28.5.3 DC parameters of port 2

These parameters apply to the IO voltage range 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 32 DC characteristics of port 2

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 × V_{DDP}	V	1) 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.2.1
Input low voltage	V_{IL_extend}	-0.3	0.42 × V_{DDP}	–	V	2) 2.6 V ≤ V_{DDP} ≤ 4.5 V	P_5.2.10
Input high voltage	V_{IH}	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	1) 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.2.2
Input high voltage	V_{IH_extend}	–	0.52 × V_{DDP}	V_{DDP} + 0.3	V	2) 2.6 V ≤ V_{DDP} ≤ 4.5 V	P_5.2.11
Input hysteresis	HYS_{P2}	0.11 × V_{DDP}	–	–	V	2) Series resistance = 0 Ω; 4.5 V ≤ V_{DDP} ≤ 5.5 V	P_5.2.3
Input hysteresis	HYS_{P2_extend}	–	0.09 × V_{DDP}	–	V	2) Series resistance = 0 Ω; 2.6 V ≤ V_{DDP} < 4.5 V	P_5.2.12
Input leakage current	I_{OZ2}	-400	–	400	nA	T_j ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.2.4
Pull-level keep current3)	I_{PLK}	-30	–	30	µA	4) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (down)	P_5.2.5
Pull-level force current3)	I_{PLF}	-750	–	750	µA	4) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (down)	P_5.2.6
Pull-level keep current for port pin P2.1	$I_{PLK_P2_1}$	-200	–	200	µA	4) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (down)	P_5.2.8
Pull- level force current for port pin P2.1	$I_{PLF_P2_1}$	-1.5	–	1.5	mA	4) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (down)	P_5.2.9
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5 V, specified for 4.5 V < V_{DDP} < 5.5 V.
2) Not subject to production test, specified by design.
3) Not P2.1.
4) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: V_{PIN} ≥ V_{IH} for a pull-up; V_{PIN} ≤ V_{IL} for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: V_{PIN} ≤ V_{IL} for a pull-up; V_{PIN} ≥ V_{IH} for a pull-down.

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28.6 LIN transceiver

28.6.1 Electrical characteristics

Table 33 Electrical characteristics of the LIN transceiver

V_s = 5.5 V to 18 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus receiver interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 × V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN spec 2.2 (par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 × V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN spec 2.2 (par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN spec 2.2 (par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN spec 2.2 (par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is the sum of $t_{WK,bus}$ and the adjustable digital filter time. The digital filter time can be adjusted by setting the PMU.CNF_WAKE_FILTER.CNF_LIN_FT register	P_6.1.8
Bus transmitter interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high level	P_6.1.9
Bus dominant output voltage	$V_{BUS,do}$	–	–	0.22 × V_S	V	Driver dominant voltage R_L = 500 Ω	P_6.1.78

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Table 33 Electrical characteristics of the LIN transceiver (cont'd)

V_s = 5.5 V to 18 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current limitation for driver-dominant state driver on V_{BUS} = 18 V; LIN spec 2.2 (par. 12)	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	5	–	µs	[6] The overall bus short circuit filter time is the sum of $t_{BUS,sc}$ and the digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS_NO_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 V < V_{BUS} < 18 V; LIN spec 2.2 (par. 15)	P_6.1.11
Leakage current	$I_{BUS_NO_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN spec 2.2 (par. 16)	P_6.1.12
Leakage current	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN spec 2.2 (par. 13)	P_6.1.13
Leakage current	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN spec 2.2 (par. 14)	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode, LIN spec 2.2 (par. 26)	P_6.1.15
On-state resistance	R_{ON}	–	20	–	Ω	[6] V_S > 5.5 V, I_{ds} = 150 mA, T_j = 27°C;	P_6.1.72
AC characteristics - transceiver Normal Slope mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN spec 2.2 (par. 31)	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN spec 2.2 (par. 31)	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN spec 2.2 (par. 32)	P_6.1.18
Duty cycle D1 Normal Slope mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] Duty cycle D1 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$ / 2 t_{bit}; LIN spec 2.2 (par. 27)	P_6.1.19

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Table 33 Electrical characteristics of the LIN transceiver (cont'd)

V_s = 5.5 V to 18 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D2 Normal Slope mode (for worst case at 20 kbit/s)	t_{duty2}	–	–	0.581		[4] Duty cycle D2 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$ / 2 t_{bit}; LIN spec 2.2 (par. 28)	P_6.1.20
AC characteristics - transceiver Low Slope mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN spec 2.2 (par. 31)	P_6.1.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN spec 2.2 (par. 31)	P_6.1.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN spec 2.2 (par. 32)	P_6.1.23
Duty cycle D3 (for worst case at 10.4 kbit/s)	t_{duty1}	0.417	–	–		[4] Duty cycle D3 $TH_{Rec}(max) = 0.778 \times V_S$; $TH_{Dom}(max) = 0.616 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$ / 2 t_{bit}; LIN spec 2.2 (par. 29)	P_6.1.24
Duty cycle D4 (for worst case at 10.4 kbit/s)	t_{duty2}	–	–	0.590		[4] Duty cycle D4 $TH_{Rec}(min) = 0.389 \times V_S$; $TH_{Dom}(min) = 0.251 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 96 µs; D4 = $t_{bus_rec(max)}$ / 2 t_{bit}; LIN spec 2.2 (par. 30)	P_6.1.25
AC characteristics - transceiver Fast Slope mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.27
Receiver delay symmetry	$t_{sym,R}$	-1.5	–	1.5	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$	P_6.1.28

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Table 33 Electrical characteristics of the LIN transceiver (cont'd)

V_s = 5.5 V to 18 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D5 (used for 62.5 kbit/s)	t_{duty1}	0.395	–	–		[5] Duty cycle D5 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 16 µs; D5 = $t_{bus_rec(min)}$ / 2 t_{bit}	P_6.1.29
Duty cycle D6 (used for 62.5 kbit/s)	t_{duty2}	–	–	0.581		[5] Duty cycle D6 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; V_S = 5.5 V … 18 V; t_{bit} = 16 µs; D6 = $t_{bus_rec(max)}$ / 2 t_{bit}	P_6.1.30
AC characteristics - Flash mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.31
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.5	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$	P_6.1.33
Duty cycle D7 (used for 250 kbit/s programming)	t_{duty1}	0.399	–	–		[5] Duty cycle D7 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus_rec(min)}$ / 2 t_{bit}	P_6.1.34
Duty cycle D8 (used for 250 kbit/s programming)	t_{duty2}	–	–	0.578		[5] Duty cycle D8 $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus_rec(max)}$ / 2 t_{bit}	P_6.1.35
LIN input capacity	C_{LIN_IN}	–	15	30	pF	[6]	P_6.1.69
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal shutdown (junction temperature)							
Thermal shutdown temperature	T_{jSD}	190	200	215	°C	[6]	P_6.1.65
Thermal shutdown hysteresis	ΔT	–	10	–	K	[6]	P_6.1.66

1) Maximum limit specified by design.

2) $V_{BUS_CNT} = (V_{th_dom} + V_{th\ rec})/ 2$.

3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$.

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4) Bus load concerning LIN spec 2.2:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load:
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}.
6) Not subject to production test, specified by design.

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28.7 High-speed synchronous serial interface

28.7.1 SSC timing parameters

The table below provides the SSC timing in the TLE9868QXB20.

Table 34 SSC master mode timing (operating conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) $2 \times T_{SSC}$	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

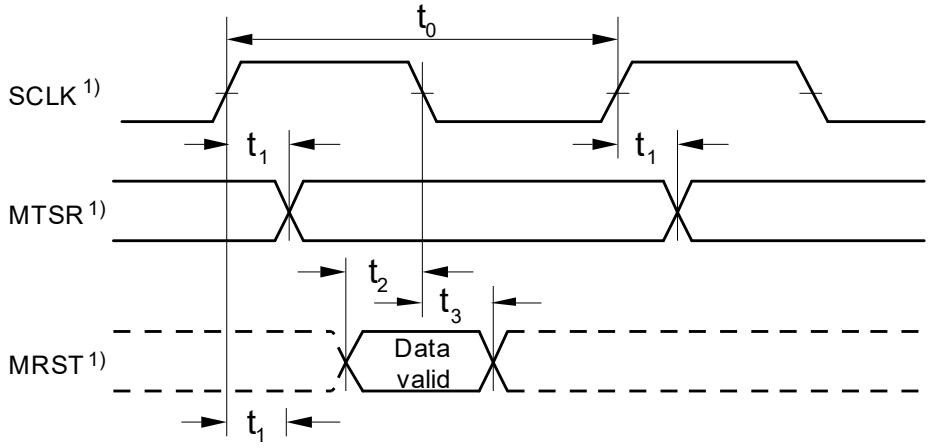


Figure 35 SSC master mode timing

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28.8 Measurement unit

28.8.1 System voltage measurement parameters

Table 35 Supply voltage signal conditioning

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Measurement output voltage range at VAREF5	V_{A5}	0	–	5	V	–	P_8.1.15
Measurement output voltage range at VAREF1V2	V_{A1V2}	0	–	1.23	V	–	P_8.1.16
Battery/supply voltage measurement V_{BAT_SENSE}/V_S							
Input-to-output voltage attenuation: V_S	ATT_{VS_1}	–	0.055	–		SFR setting 1	P_8.1.41
Input-to-output voltage attenuation: V_{BAT_SENSE}	$ATT_{VBAT_SENSE_1}$	–	0.055	–		SFR setting 1	P_8.1.60
Nominal operating input voltage range V_{BAT_SENSE} and V_S	$V_{BAT_SENSE,range1}$, $V_{S,range1}$	3	–	22	V	[1] SFR setting 1; max. value corresponds to typ. ADC full scale input; 3 V < V_{BAT_SENSE}/V_S < 28 V	P_8.1.1
Accuracy of V_{BAT_SENSE}/V_S after calibration	$\Delta V_{BAT_SENSE,range1}$, $V_{S,range1}$	-220	–	220	mV	[2] SFR setting 1, V_S = 5.5 V to 18 V	P_8.1.70
Input-to-output voltage attenuation: V_S	ATT_{VS_2}	–	0.039	–		SFR setting 2	P_8.1.42
Input-to-output voltage attenuation: V_{BAT_SENSE}	$ATT_{VBAT_SENSE_2}$	–	0.039	–		SFR setting 2	P_8.1.61
Nominal operating input voltage range V_{BAT_SENSE} and V_S	$V_{BAT_SENSE,range2}$, $V_{S,range2}$	3	–	31	V	[1] SFR setting 2; max. value corresponds to typ. ADC full scale input; 3 V < V_{BAT_SENSE}/V_S < 28 V	P_8.1.40
Accuracy of V_{BAT_SENSE}/V_S after calibration	$\Delta V_{BAT_SENSE,range2}$, $V_{S,range2}$	-370	–	370	mV	[2] SFR setting 2, V_S = 5.5 V to 18 V	P_8.1.44
Measurement input leakage current for V_{BAT_SENSE}	$I_{leak_VBAT_SENSE,measure}$	0	–	4.0	µA	PD_N = 0 (off-state), V_{BAT_SENSE} = 13.5 V	P_8.1.72
Drivers supply voltage measurement V_{SD}							
Input-to-output voltage attenuation: V_{SD}	ATT_{VSD}	–	0.039	–		–	P_8.1.21

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Table 35 Supply voltage signal conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating input voltage range V_{SD}	$V_{SD,range}$	2.5	–	31	V	1)	P_8.1.2
Accuracy of V_{SD} sense after calibration	ΔV_{SD}	-320	–	320	mV	2) V_S = 5.5 V to 18 V	P_8.1.47
Charge pump voltage measurement V_{CP}							
Input-to-output voltage attenuation: V_{CP}	ATT_{VCP}	–	0.023	–		–	P_8.1.56
Nominal operating input voltage range V_{CP}	$V_{CP,range}$	2.5	–	52	V	1)	P_8.1.7
Accuracy of V_{CP} sense after calibration	ΔV_{CP}	-650	–	650	mV	2) V_S = 5.5 V to 18 V	P_8.1.62
Pad supply voltage measurement V_{VDDP}							
Input-to-output voltage attenuation: V_{DDP}	ATT_{VDDP}	–	0.164	–		–	P_8.1.33
Nominal operating input voltage range V_{DDP}	$V_{DDP,range}$	0	–	7.50	V	1)	P_8.1.50
Accuracy of V_{DDP} sense after calibration	ΔV_{DDP_SENSE}	-75	–	75	mV	2)3) V_S = 5.5 V to 18 V	P_8.1.5
10-bit ADC reference voltage measurement V_{AREF}							
Input-to-output voltage attenuation: V_{AREF}	ATT_{VAREF}	–	0.219	–		–	P_8.1.22
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-55	–	55	mV	2) V_S = 5.5 V to 18 V	P_8.1.48
8-bit ADC reference voltage measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52
Value of ADC2-V_{BG} measurement after calibration	V_{BG_PMU}	1.01	1.07	1.18	V	2)	P_8.1.73
Core supply voltage measurement V_{DDC}							
Input-to-output voltage attenuation: V_{DDC}	ATT_{VDDC}	–	0.75	–		–	P_8.1.34
Nominal operating input voltage range V_{DDC}	$V_{DDC,range}$	0.8	–	1.64	V	1)	P_8.1.53

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Table 35 Supply voltage signal conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Accuracy of V_{DDC} sense after calibration	ΔV_{DDC_SENSE}	-22	–	22	mV	2) V_S = 5.5 V to 18 V	P_8.1.6
VDH input voltage measurement $V_{VDH10BITADC}$							
VDH input-to-output voltage attenuation	ATT_{VDH_1}	–	0.166	–		SFR setting 1	P_8.1.64
VDH input-to-output voltage attenuation	ATT_{VDH_2}	–	0.224	–		SFR setting 2	P_8.1.65
VDH input to output voltage attenuation	ATT_{VDH_3}	–	0.226	–		1) SFR setting 2, -40°C ≤ T_j ≤ 85°C	P_8.1.75
Nominal operating input voltage range V_{VDH}, range 1	$V_{VDH,range1}$	–	–	30	V	SFR setting 1	P_8.1.66
Nominal operating input voltage range V_{VDH}, range 2	$V_{VDH,range2}$	–	–	20	V	SFR setting 2	P_8.1.67
V_{VDH} 10-bit ADC, range 1	$\Delta V_{VDHADC10B}$	-300	–	300	mV	4) V_{VDH} = 5.5 V to 17.5 V, -40°C ≤ T_j ≤ 150°C	P_8.1.39
V_{VDH} 10-bit ADC, range 3	$\Delta V_{VDHADC10B}$	-200	–	200	mV	1)4) V_{VDH} = 5.5 V to 17.5 V, -40°C ≤ T_j ≤ 85°C, ATT_{VDH_3}	P_8.1.71
V_{VDH} 10-bit ADC, range 2	$\Delta V_{VDHADC10B_extend_T}$	-400	–	400	mV	4) V_{VDH} = 5.5 V to 17.5 V, -40°C ≤ T_j ≤ 150°C	P_8.1.74
10-bit ADC measurement, input resistance for VDH	$R_{in_VDH,measure}$	200	390	470	kΩ	PD_N = 1 (on-state)	P_8.1.3
Measurement input leakage current for V_{VDH}	$I_{leak_VDH,\ measure}$	-0.05	–	2.0	µA	PD_N = 0 (off-state), V_{VDH} = 13.5 V	P_8.1.10

1) Not subject to production test, specified by design.
2) The accuracies stated include the following tolerance:
ADC2 offset error - P_8.3.19
ADC2 gain error - P_8.3.20
V_{BG} - P_8.3.1
3) Accuracy is valid for a calibrated device.
4) The accuracies stated include the ADC1 total unadjusted error (TUE_{10B}) which includes the V_{AREF} tolerance.

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28.8.2 Central temperature sensor parameters

Table 36 Electrical characteristics of the temperature sensor module

V_S = 3.0 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0 = 273 K (0°C)	*a*	–	0.666	–	V	1) T_0 = 273 K (0°C)	P_8.2.2
Temperature sensitivity b	*b*	–	2.31	–	mV/K	1)	P_8.2.4
Accuracy_1	*Acc_1*	-10	–	10	°C	1)2)3) -40°C < T_j < 85°C	P_8.2.5
Accuracy_2	*Acc_2*	-10	–	10	°C	1)2)3) 125°C < T_j < 150°C	P_8.2.6
Accuracy_3	*Acc_3*	-5	–	5	°C	1)2)3) 85°C < T_j < 125°C	P_8.2.7

1) Not subject to production test, specified by design.

2) Accuracy with reference to on-chip temperature calibration measurement, valid for Mode1.

3) The accuracies stated include the following tolerance:
ADC2 offset error - P_8.3.19
ADC2 gain error - P_8.3.20
V_{BG} - P_8.3.1

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28.8.3 ADC2 VBG

28.8.3.1 ADC2 reference voltage VBG

Table 37 DC specifications

V_S = 3.0 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	V_{BG}	1.199	1.211	1.223	V	1)	P_8.3.1

1) Not subject to production test, specified by design.

28.8.3.2 ADC2 specifications

Table 38 DC specifications

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Resolution	*RES*	–	8	–	bit	Full	P_8.3.18
Guaranteed offset error	EA_{OFF_8Bit}	-2.0	±0.3	2.0	LSB	Not calibrated	P_8.3.19
Gain error	EA_{Gain_8Bit}	-2.0	±0.5	2.0	%FSR	Not calibrated	P_8.3.20
Differential non-linearity (DNL)	EA_{DNL_8Bit}	-0.8	±0	0.8	LSB	Full	P_8.3.21
Integral non-linearity (INL)	EA_{INL_8Bit}	-1.2	±0	1.2	LSB	–	P_8.3.22

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28.9 ADC1 reference voltage - VAREF

28.9.1 Electrical characteristics of VAREF

Table 39 Electrical characteristics of VAREF

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required buffer capacitance	C_{VAREF}	0.1	–	1	µF	ESR < 1 Ω	P_9.1.1
Reference output voltage	V_{AREF}	4.95	5	5.05	V	V_S > 5.5 V	P_9.1.2
DC supply voltage rejection	$DC_{PSRVAREF}$	30	–	–	dB	1)	P_9.1.3
Supply voltage ripple rejection	$AC_{PSRVAREF}$	26	–	–	dB	1) V_S = 13.5 V; f = 0 kHz … 1 kHz; V_r = 2 Vpp	P_9.1.4
Turn-on time	t_{so}	–	–	200	µs	1) C_{ext} = 100 nF PD_N to 99.9% of final value	P_9.1.5
Input resistance at VAREF pin	$R_{IN,VAREF}$	–	100	–	kΩ	1) Input impedance in case of VAREF is applied from external input	P_9.1.20

1) Not subject to production test, specified by design.

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28.9.2 Electrical characteristics of the ADC1 (10-bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating conditions apply.

Table 40 A/D converter characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	20	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 × t_{ADC}	(13 + STC) × t_{ADCI} + 2 × t_{ADC}	(13 + STC) × t_{ADCI} + 2 × t_{ADC}	–	1)4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{ADC}	(11 + STC) × t_{ADCI} + 2 × t_{ADC}	(11 + STC) × t_{ADCI} + 2 × t_{ADC}	–	1)	P_9.2.6
Wake-up time from analog power-down, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wake-up time from analog power-down, slow mode	t_{WAS}	–	–	15	µs	1)5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	-2	±1	2	counts	6)7) Reference is internal V_{AREF}	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	-12	±6	12	counts	6)7) Reference is internal V_{AREF}	P_9.2.22
DNL error	EA_{DNL}	-3	±0.8	3	counts	–	P_9.2.10
INL error	$EA_{INL_int_VAREF}$	-5	±0.8	5	counts	Reference is internal V_{AREF}	P_9.2.11
Gain error	$EA_{GAIN_int_VAREF}$	-10	±0.4	10	counts	Reference is internal V_{AREF}	P_9.2.12
Offset error	EA_{OFF}	-2	±0.5	2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	1)5)8)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	1)5)8)	P_9.2.15

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Table 40 A/D converter characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	1)5)8)	P_9.2.16
Total capacitance of the reference input	C_{AREFT}	–	–	15	pF	1)5)8)	P_9.2.17
Switched capacitance of the reference input	C_{AREFS}	–	–	7	pF	1)5)8)	P_9.2.18
Resistance of the reference input path	R_{AREF}	–	–	2	kΩ	1)5)8)	P_9.2.19

1) Not subject to production test, specified by design.

2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion results in these cases will be 0000_H or $03FF_H$, respectively.

3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.

4) This parameter includes the sample time (and the additional sample time specified by STC), the time to determine the digital results and the time to load the result register with the conversion result.

5) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs.

6) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
All error specifications are based on measurement methods standardized by IEEE 1241.2000.

7) The specified TUE is valid only if the absolute sum of input overload currents (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

8) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage), typical values can be used for the calculation. At room temperature and nominal supply voltage, the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

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28.10 14-Bit sigma delta ADC (ADC3 / ADC4)

28.10.1 Analog/Digital converter parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating conditions apply.

Table 41 A/D converter ADC3/4 characteristics

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog clock frequency	$f_{ADC3/4}$	5	–	20	MHz	–	P_10.1.20
Single ended input capacitance	C_{in1}	–	2	–	pF	1)2)	P_10.1.1
Oversampling ratio	*OSR*	128	–	2048		2) Decimation factor	P_10.1.2
ADC full scale voltage (differential)	V_{Fs}	3.75	–	–	V	2) At $V_{DIFF} = \pm V_{FS}$, DD.max resp. DD.min is reached	P_10.1.3
Input voltage	V_{in}	0	–	V_{REF}	V	Input voltage on ADCx.P or ADCx.N V_{REF} can be VAREF or VREF5V x = {3,4}	P_10.1.21
Differential non-linear input voltage	$V_{diff,nonlin}$	-4.0	–	4.0	V	2) $V_{diff} = V_{ADCx.P} - V_{ADCx.N}$ $V_{ADCx.P}$, $V_{ADCx.P}$ within V_{in} range x = {3,4}	P_10.1.4
Differential linear input voltage	$V_{diff,lin}$	-3.75	–	3.75	V	2) $V_{diff} = V_{ADCx.P} - V_{ADCx.N}$ $V_{ADCx.P}$, $V_{ADCx.P}$ within V_{in} range x = {3,4}	P_10.1.6
Input common mode range	$V_{in,com}$	0.48 × V_{REF}	–	0.52 × V_{REF}	V	V_{REF} can be VAREF or VREF5V	P_10.1.7
Input frequency	f_{in}	0	–	1	kHz	2)	P_10.1.8
RMS noise	V_{rms}	–	0.69	1.15	mV	Tested with OSR = 128 and V_{REF} = VREF5V	P_10.1.22
Effective resolution	RES_{eff}	11.7	12.4	–	bit	Calculated, $RES_{eff} = ld(V_{Fs} / V_{RMS})$	P_10.1.23

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Table 41 A/D converter ADC3/4 characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Effective number of bits	*ENOB*	–	11.7	–	bit	2) ENOB = (SNDR-1.76 dB)/6.02 dB	P_10.1.24
SNDR with a fully differential sinus -6dBFS	*SNDR*	–	72	–	dB	2)	P_10.1.10
Digital filtered data of raw ADC values	DD	-16384	–	16383	LSB	2) Represented in two's complement $DD = (V_{diff}/V_{REF}) \times ATT_{adc34} \times (2^{14} - 1)$	P_10.1.13
ADC34 input attenuator	ATT_{adc34}	–	4/3	–		–	P_10.1.25
Dynamic input impedance	Z_{IN}	–	250	–	kΩ	2)	P_10.1.15
ADC gain ratio	G_{ADC3} / G_{ADC4}	0.990	1	1.010		–	P_10.1.17
ADC offset drift	$OFF_{ADC3/4}$	–	5.4	–	mV	–	P_10.1.18

1) In addition to pin capacitance C_{IO}, see P_5.2.7.

2) Not subject to production test, specified by design.

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28.11 High-voltage monitoring input

28.11.1 Electrical characteristics

Table 42 Electrical characteristics of the monitoring input

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
MON input pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	Without external serial resistor R_s (with R_s: DV = $I_{PD/PU}$ × R_s); V_S = 5.5 V to 18 V; -40°C ≤ T_j ≤ 85°C	P_11.1.1
Wake-up/monitoring threshold voltage extended range	V_{MONth_extend}	0.4 × V_S	0.5 × V_S	0.65 × V_S	V	Without external serial resistor R_s (with R_s: DV = $I_{PD/PU}$ × R_s)	P_11.1.16
Threshold hysteresis	$V_{MONth,hys}$	0.015 × V_S	0.05 × V_S	0.1 × V_S	V	In all modes; without external serial resistor R_s (with R_s: dV = $I_{PD/PU}$ × R_s); V_S = 5.5 V to 18 V	P_11.1.12
Threshold hysteresis	$V_{MONth,hys}$	0.02 × V_S	0.06 × V_S	0.12 × V_S	V	In all modes; without external serial resistor R_s (with R_s: dV = $I_{PD/PU}$ × R_s); V_S = 18 V to 28 V	P_11.1.2
Pull-up current	$I_{PU, MON}$	-20	-10	-1	µA	0.6 × V_S	P_11.1.3
Pull-down current	$I_{PD, MON}$	3	10	20	µA	0.4 × V_S	P_11.1.4
Input leakage current	$I_{LK,MON}$	-2.5	–	2.5	µA	[1] 0 V < V_{MON_IN} < 28 V	P_11.1.5
Timing							
Wake-up filter time (internal analog filter delay)	$t_{FT,MON}$	–	500	–	ns	[2] The overall filter time for MON wake-up is the sum of $t_{FT,MON}$ and the adjustable digital filter time. The digital filter time can be adjusted by setting the PMU.CNF_WAKE_FILTER. CNF_MON_FT register	P_11.1.6

1) Input leakage is valid for the disabled state.

2) With pull-up, pull-down current disabled.

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28.12 MOSFET driver

28.12.1 Electrical characteristics

Table 43 Electrical characteristics of the MOSFET driver

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
MOSFET driver output							
Maximum total charge driver capability	Q_{tot_max}	–	–	100	nC	[1] Due to charge pump current capability, six MOSFETs and additional external capacitors with a total charge of maximal 100 nC can be driven simultaneously at a PWM frequency of 25 kHz.	P_12.1.20
Maximum total charge driver capability (three-phase PWM)	$Q_{tot_max,20kHz}$	–	–	150	nC	[1] Due to charge pump current capability, six MOSFETs and additional external capacitors with a total charge of maximal 150 nC can be driven simultaneously at a PWM frequency of 20 kHz. $V_{SD,min} \geq 6.5$ V for $V_{GS,min} \geq 7$ V	P_12.1.120
Source current - charge current (low gate supply voltage VSD)	I_{Sou_lowVSD}	150	–	–	mA	[1] $V_{SD} \geq 5.1$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 20% to 50% of V_{Gxx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.65
Sink current - discharge current (low gate supply voltage VSD)	I_{Sink_lowVSD}	150	–	–	mA	[1] $V_{SD} \geq 5.1$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 50% to 20% of V_{Gxx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.66
Source current - charge current - high-side driver	I_{Soumax_HS}	230	345	450	mA	$V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 20% to 50% of V_{GHx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.78
Sink current - discharge current - high-side driver	$I_{Sinkmax_HS}$	230	330	450	mA	$V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sink} = C_{Load} \times$ slew rate (from 80% to 50% of V_{GHx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.79

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Table 43 Electrical characteristics of the MOSFET driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Source current - charge current - low-side driver	I_{Soumax_LS}	200	295	375	mA	$V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 20% to 50% of V_{GLx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.80
Sink current - discharge current - low-side driver	$I_{Sinkmax_LS}$	200	314	375	mA	$V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sink} = C_{Load} \times$ slew rate (from 80% to 50% of V_{GLx1}), $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.81
Source current - charge current (low gate voltage)	I_{Soumin}	–	40	–	mA	[1] $V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 20% to 50% of V_{Gxx1}), $I_{CHARGE} = I_{DISCHG}$ = 3(min)	P_12.1.33
Sink current - discharge current	$I_{Sinkmin}$	–	40	–	mA	[1] $V_{SD} \geq 8$ V, C_{Load} = 10 nF, $I_{Sou} = C_{Load} \times$ slew rate (= 80% to 20% of V_{Gxx1}), $I_{CHARGE} = I_{DISCHG}$ = 3(min)	P_12.1.34
High-level output voltage Gxx vs. Sxx	V_{Gxx1}	10	–	14	V	[2] $V_{SD} \geq 8$ V, C_{Load} = 10 nF, I_{CP} = 2.5 mA	P_12.1.3
High-level output voltage GHx vs. SHx	V_{Gxx2}	8	–	14	V	[1][2] V_{SD} = 6.4 V, C_{Load} = 10 nF, I_{CP} = 2.5 mA	P_12.1.4
High-level output voltage GHx vs. SHx	V_{Gxx4}	7	–	–	V	[2] V_{SD} = 5.1 V, C_{Load} = 10 nF, I_{CP} = 2.5 mA	P_12.1.62
High-level output voltage GLx vs. GND	V_{Gxx6}	8	–	14	V	[1][3] V_{SD} = 6.4 V, C_{Load} = 10 nF, I_{CP} = 2.5 mA	P_12.1.6
High-level output voltage GLx vs. GND	V_{Gxx8}	7	–	–	V	[2] V_{SD} = 5.1 V, C_{Load} = 10 nF, I_{CP} = 2.5 mA	P_12.1.63
Rise time	t_{rise3_3nf}	–	200	–	ns	[1] C_{Load} = 3.3 nF, $V_{SD} \geq 8$ V, 25% to 75% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.8
Fall time	t_{fall3_3nf}	–	200	–	ns	[1] C_{Load} = 3.3 nF, $V_{SD} \geq 8$ V, 75% to 25% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.9
Rise time	$t_{risemax}$	100	250	450	ns	C_{Load} = 10 nF, $V_{SD} \geq 8$ V, 25% to 75% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.57

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Table 43 Electrical characteristics of the MOSFET driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fall time	$t_{fallmax}$	100	250	450	ns	C_{Load} = 10 nF, $V_{SD} \geq$ 8 V, 75% to 25% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.58
Rise time	$t_{risemin}$	1.25	2.5	5	µs	1) C_{Load} = 10 nF, $V_{SD} \geq$ 8 V, 25% to 75% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 3(min)	P_12.1.14
Fall time	$t_{fallmin}$	1.25	2.5	5	µs	1) C_{Load} = 10 nF, $V_{SD} \geq$ 8 V, 75% to 25% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 3(min)	P_12.1.15
Absolute difference between rise and fall for all LSx	$t_{r_f(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, $V_{SD} \geq$ 8 V, 25% to 75% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.35
Absolute difference between rise and fall for all HSx	$t_{r_f(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, $V_{SD} \geq$ 8 V, 25% to 75% of V_{Gxx1}, $I_{CHARGE} = I_{DISCHG}$ = 31(max)	P_12.1.36
Resistor between GHx/GLx and GND	R_{GGND}	30	40	50	kΩ	1)	P_12.1.11
Resistor between SHx and GND	R_{SHGN}	30	40	50	kΩ	1)3) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0.6 V typ. before it is discharged through the resistor	P_12.1.10
Low-RDSON mode (boosted discharge mode)	R_{ONCCP}	–	9	12	Ω	V_{VSD} = 13.5 V, $V_{VCP} = V_{VSD}$ + 14.0 V; $I_{CHARGE} = I_{DISCHG}$ = 31(max); 50 mA forced into Gx, Sx grounded	P_12.1.50
Input propagation time (LS on)	$t_{P(ILN)min}$	–	1.5	3	µs	1) C_{Load} = 10 nF, I_{Charge} = 3(min), 25% of V_{Gxx1}	P_12.1.37

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Table 43 Electrical characteristics of the MOSFET driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input propagation time (LS off)	$t_{P(ILF)min}$	–	1.5	3	µs	[1] C_{Load} = 10 nF, $I_{Discharge}$ = 3(min), 75% of V_{Gxx1}	P_12.1.38
Input propagation time (HS on)	$t_{P(IHN)min}$	–	1.5	3	µs	[1] C_{Load} = 10 nF, I_{Charge} = 3(min), 25% of V_{Gxx1}	P_12.1.39
Input propagation time (HS off)	$t_{P(IHF)min}$	–	1.5	3	µs	[1] C_{Load} = 10 nF, $I_{Discharge}$ = 3(min), 75% of V_{Gxx1}	P_12.1.40
Input propagation time (LS on)	$t_{P(ILN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} = 31(max), 25% of V_{Gxx1}	P_12.1.26
Input propagation time (LS off)	$t_{P(ILF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ = 31(max), 75% of V_{Gxx1}	P_12.1.27
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} = 31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ = 31(max), 75% of V_{Gxx1}	P_12.1.29
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} = 31(max), 25% of V_{Gxx1}	P_12.1.30
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ = 31(max), 75% of V_{Gxx1}	P_12.1.41
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} = 31(max), 25% of V_{Gxx1}	P_12.1.42
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ = 31(max), 75% of V_{Gxx1}	P_12.1.43

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Table 43 Electrical characteristics of the MOSFET driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Drain source monitoring							
Drain source monitoring threshold	$V_{DSMONVTH}$	–	–	–	V	DRV_CTRL3.DSMONVTH<2:0> xxx	P_12.1.46
		0.07	0.25	0.40		000	
		0.35	0.50	0.650		001	
		0.55	0.75	0.90		010	
		0.65	1.00	1.25		011	
		0.90	1.25	1.45		100	
		1.00	1.5	1.80		101	
		1.20	1.75	2.10		110	
		1.40	2.00	2.40		111	
Open load diagnostic currents							
Pull-up diagnostic current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnostic current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin2}	8.5	–	–	V	V_{VSD} = 5.1 V, I_{CP} = 2.5 mA, C_{CP1}, C_{CP2} = 220 nF, bridge driver enabled	P_12.1.64
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V ≤ V_{VSD} ≤ 28 V, I_{CP} = 10 mA, C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250 kHz	P_12.1.49
Turn-on time	t_{ON_VCP}	10	24	40	µs	[1)4)] 8 V ≤ V_{VSD} ≤ 28 V, I_{CP} = 2.5 mA, (25%) of V_{CP}, C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250 kHz	P_12.1.59
Rise time	t_{rise_VCP}	20	60	88	µs	[1)5)] 8 V ≤ V_{VSD} ≤ 28 V, I_{CP} = 2.5 mA, (25% to 75%) of V_{CP}, C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250 kHz	P_12.1.60

1) Not subject to production test, specified by design.

2) The condition I_{CP} = 2.5 mA emulates 4 MOSFET switching at 25 kHz with a C_{Load} = 3.3nF. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.

3) This resistance is connected through a diode between SHx and GHx to ground.

4) This time applies when the DRV_CP_CTRL_STS.bit.CP_EN bit is set.

5) This time applies when the DRV_CP_CLK_CTRL.bit.CPCLK_EN bit is set.

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29 Package information

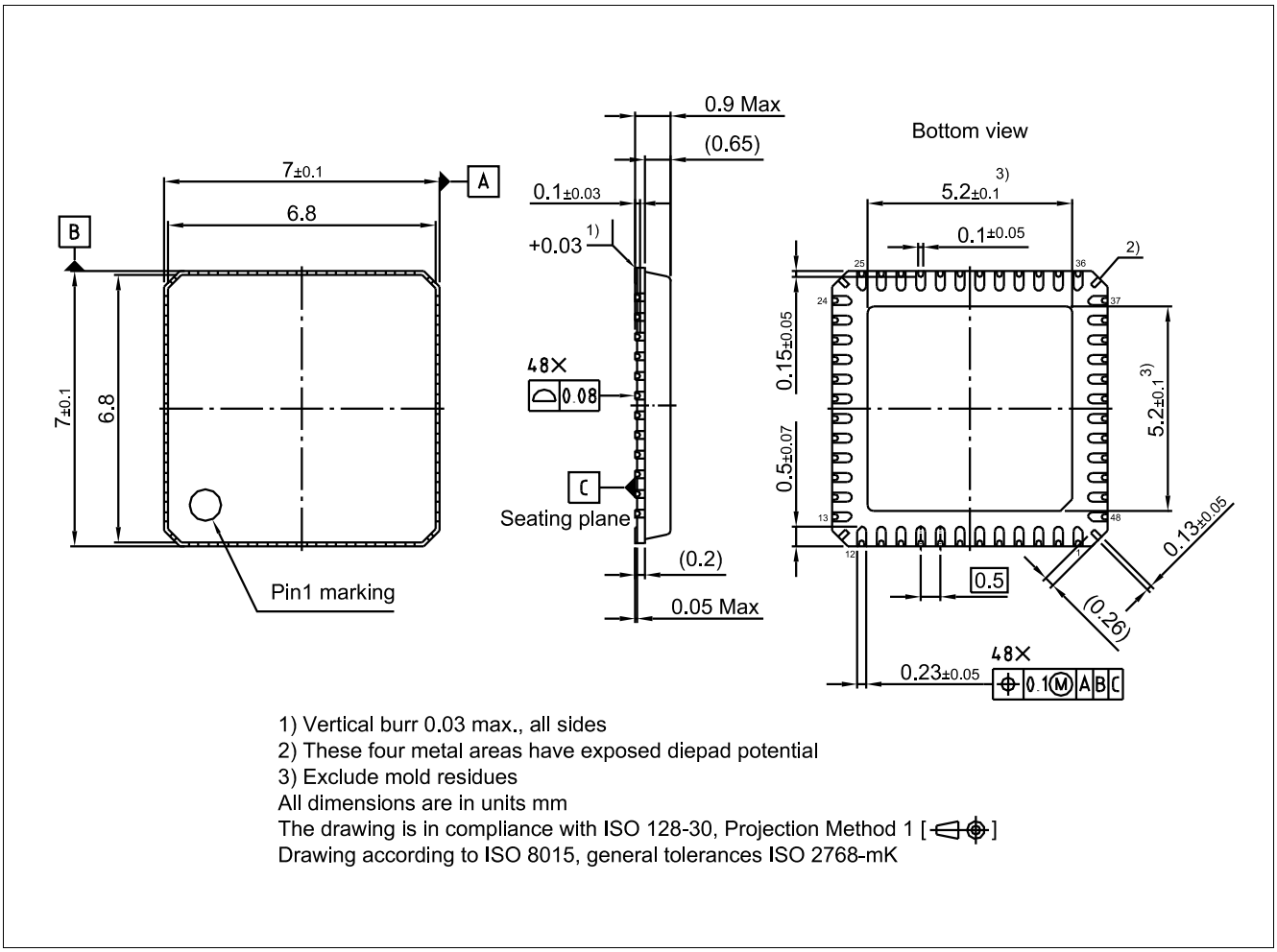
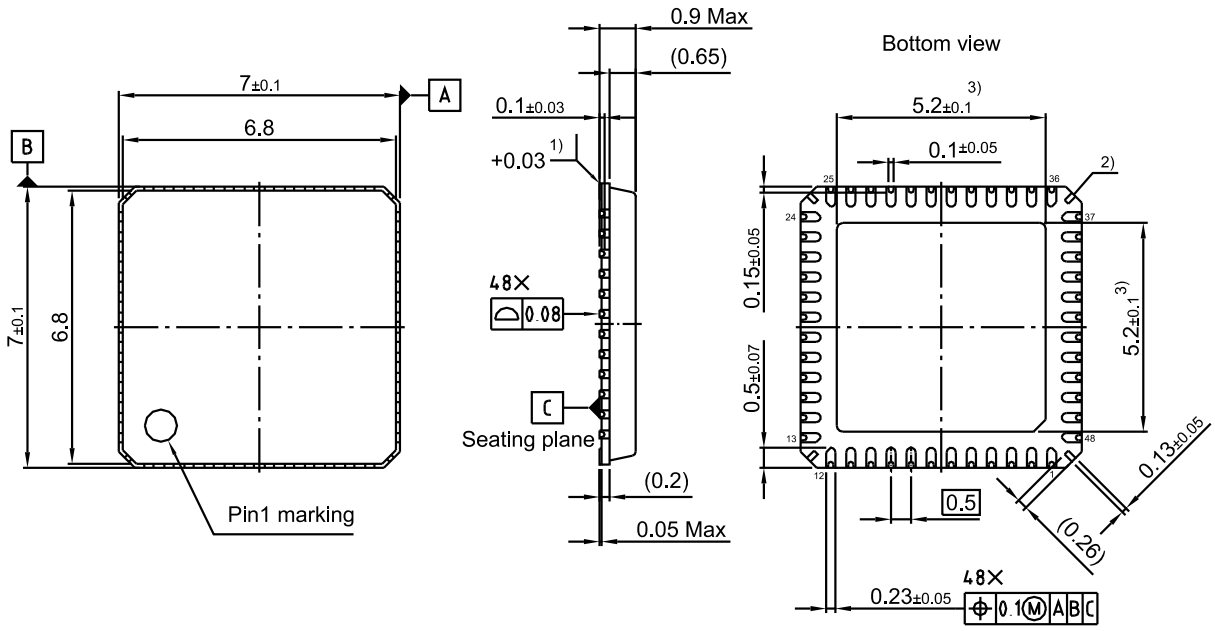


Figure 36 Package outline VQFN-48-31 with LTI (BF step)[1)]

1) Dimensions in mm

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Package information



1) Vertical burr 0.03 max., all sides
2) These four metal areas have exposed diepad potential
3) Exclude mold residues
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 37 Package outline VQFN-48-37 with LTI (UH and UI step)[1)]

1) Dimensions in mm

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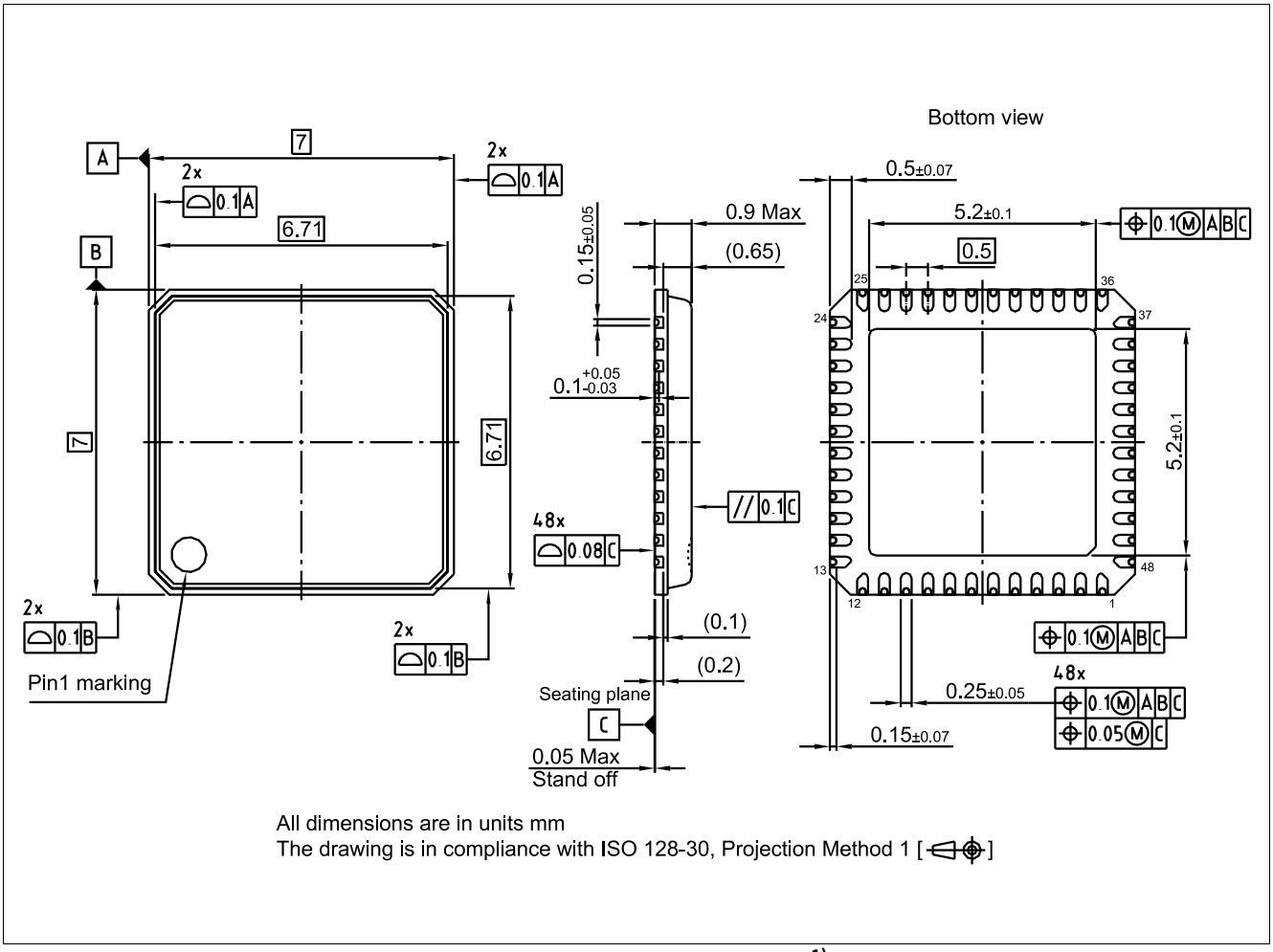


Figure 38 Package outline VQFN-48-79 with LTI (UH and UI step)[1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

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30 Revision history

Revision history	
Item	**Subjects (major changes since previous revision)**
Rev. 2.2, 2025-09-15	
All	• Added package option VQFN-48-37 • Editorial changes
GPIO ports and peripheral I/O	• **Table 9**: The UART2 signals “TXD2_0” and “TXD2_1” have been renamed to “TXD2”.
Rev. 2.11, 2024-04-08	
Front page	• Added an OPN number for the UI step
Rev. 2.1, 2023-10-23	
Front page	• Editorial changes: Added “Arm® Cortex®-M3” and “MOTIX™” • Added UI step • Features: Changed from “Single power supply from 5.5 V to 27 V” to “Single power supply from 5.5 V to 28 V”
Overview and Device register types	• Table “Pin definitions and functions”, Symbol “Reset”, Pin Number “22”: Changed “Reset state” from “–” to “PU” • Changed from “Sleep mode is activated after 5 consecutive watchdog failures or in case of supply failure (5 times)” to “Sleep mode is activated after 5 watchdog failures or in case of supply failure (5 times).”
System control unit – digital modules (SCU-DM)	• Editorial changes
Address space organization	• Figure “Memory map”: Changed address labels
Memory control unit	• Features: Changed “Memory protection functions for all system memory types (D-flash, P-flash, RAM)” to “Memory protection for D-flash and P-flash system memory”.
GPIO ports and peripheral I/O	• P2.3: Changed CTRAP#_1 to $\overline{\text{CTRAP\#_1}}$
14-Bit Sigma Delta ADC (ADC3 / ADC4)	• Removed chapter “Interpretation of SDADC output code”.

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Revision history

Revision history

Item	Subjects (major changes since previous revision)
Electrical characteristics	• Changed table title “DC characteristics of port0 and port1” to “DC characteristics of port 0, port 1, TMS, and reset” • Added footnote “The accuracies stated include the ADC1 total unadjusted error (TUE_{10B}) which includes the V_{AREF} tolerance.” to the following parameters: – P_8.1.39 – P_8.1.71 – P_8.1.74 • Added footnote “The accuracies stated include the following tolerance: ADC2 offset error - P_8.3.19 ADC2 gain error - P_8.3.20 V_{BG} - P_8.3.1” to the following parameters – P_8.1.70 – P_8.1.73 – P_8.1.44 – P_8.1.47 – P_8.1.62 – P_8.1.68 – P_8.1.5 – P_8.1.48 – P_8.1.6 – P_8.2.5 – P_8.2.6 – P_8.2.7 • P_9.2.5 and P_9.2.6, values: Changed “t_{SYS}” to “t_{ADC}”

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Revision history

Revision history	
Item	**Subjects (major changes since previous revision)**
Rev. 2.0, 2022-04-14	
All	• Editorial changes • Package : Added package “VQFN-48-79”
Introduction	• "Sleep Mode with Cyclic Wake-Up": “…. Followed by the Sleep and Stop Mode command“: Deleted “and Stop”
Electrical characteristics	• P_1.1.44, P_1.1.45: Changed values from "min=14 V, typ=, max=" to "min=-0.3 V, typ=, max=14 V" • P_1.1.48 added, VSL min=-8 V, max=48 V. • P_1.2.3: Changed footnote from “Reduced functionality (e.g., cranking pulse); parameter deviation possible.” to “Functionality is reduced (for example, cranking pulse); parameter deviations are possible: The electrical parameters of the device may present values outside the range specified within the minimum and maximum values.” • P_1.2.16, P_1.2.17, P_1.2.14: Added footnote “Parameter deviations mean that the electrical parameters of the device may present values outside the range specified within the minimum and maximum values.” • P_1.4.2, P_10.1.1: Footnote added "Not subject to production test, specified by design." • P_1.4.3: new parameter added, "Thermal Resistance": Parameter: "Junction to top", Symbol: "ΨJTOP 2s2p", Values: typical: "8", Unit: K/W. • P_2.1.2, P_2.1.20: Footnote added: "Ranges of P_2.1.2 and P_2.1.20 can be added to one ceramic capacitor with ESR < 1 Ω." P_2.2.1, P_2.2.17: Footnote added: "Ranges of P_2.2.1 and P_2.2.17 can be added to one ceramic capacitor with ESR < 1 Ω." P_2.3.22, P_2.3.20: Footnote added: "Ranges of P_2.3.22 and P_2.3.20 can be added to one ceramic capacitor with ESR < 1 Ω." • P_4.1.1, P_4.1.2: Footnote added: "While the flash memory is being programmed or erased, flash read operation is not possible to be performed." • P_11.1.1, Note, added: “-40°C ≤ T_j ≤ 85°C” • P_11.1.11: Deleted P_11.1.16: Added • P_12.1.4, P_12.1.6: Added 14 V as max value. • P_12.1.20: Changed in “Test Condition: “Due to charge pump current capability, ~~only~~ ~~three~~six MOSFETs and...” • P_12.1.24: Deleted • P_12.1.120: Added
Rev. 1.1, 2017-06-19	
all	Changed to 4 kByte RAM Deleted Note in chapter “NVM Module” Added P_1.3.6, P_6.1.72
Rev. 1.0, 2017-02-03	
All	Initial release.

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