



PXN012-100QS

N-channel 100 V, 12 mOhm, standard level Trench MOSFET in MLPAK33

21 September 2023

Product data sheet

1. General description

General purpose MOSFET for standard applications, 50 A, standard level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Standard level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

4. Quick reference data

Table 1. Quick reference data

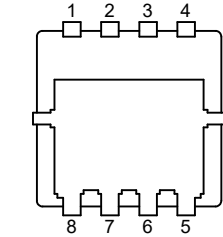
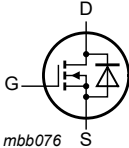
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C		-	-	100	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	50	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	58	W
T _j	junction temperature			-55	-	150	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	10.6	12	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11 ; Fig. 12		-	5.5	-	nC
Q _{G(tot)}	total gate charge			-	22	-	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 23.2 A; V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	[1]	-	-	53.8	mJ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q _r	recovered charge	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C; Fig. 15	[2]	-	27	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN012-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN012-100QS	7AN

8. Limiting values

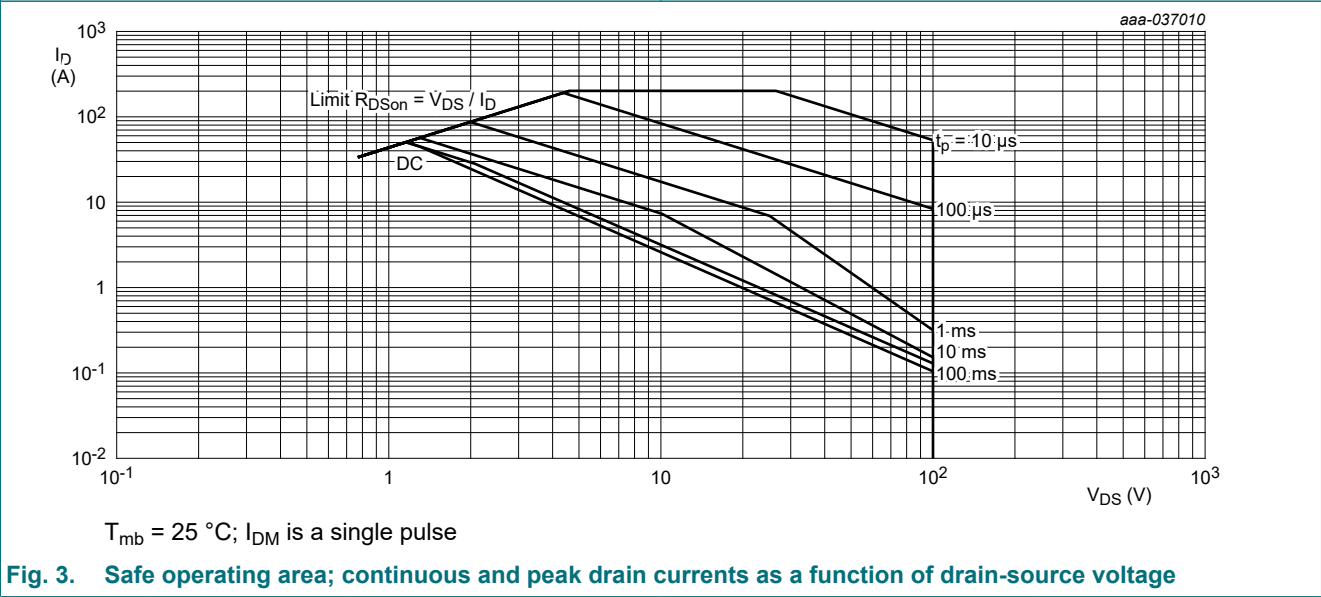
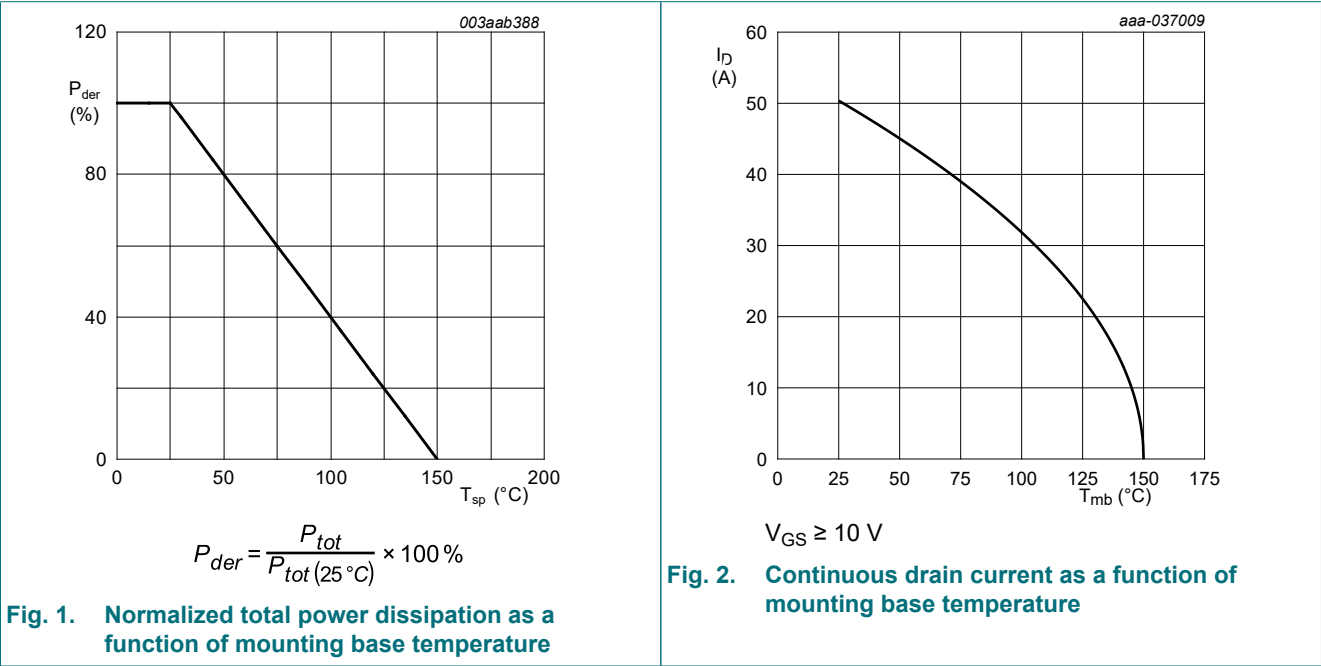
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_J = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _J ≤ 150 °C		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	58	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	50	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	32	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	201	A
T _{stg}	storage temperature			-55	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	48	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	201	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 23.2 A; V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	[1]	-	53.8	mJ
I _{AS}	non-repetitive avalanche current	T _{j(init)} = 25 °C	[1]	-	23.2	A

[1] Protected by 100% test



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.79	2.15	K/W

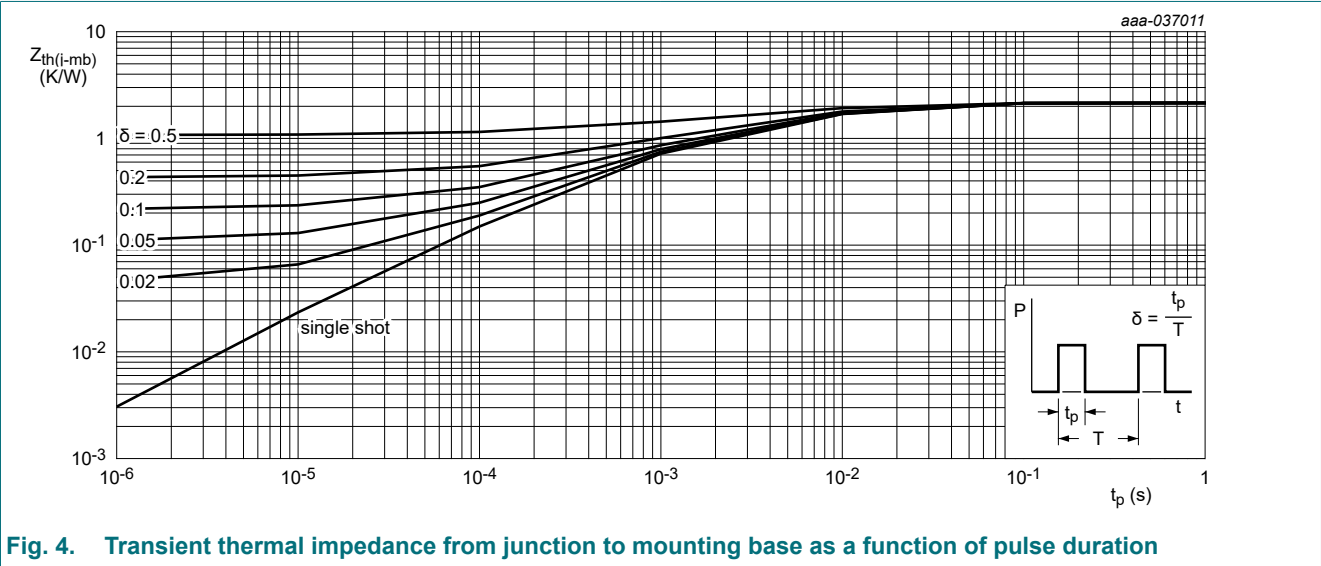


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

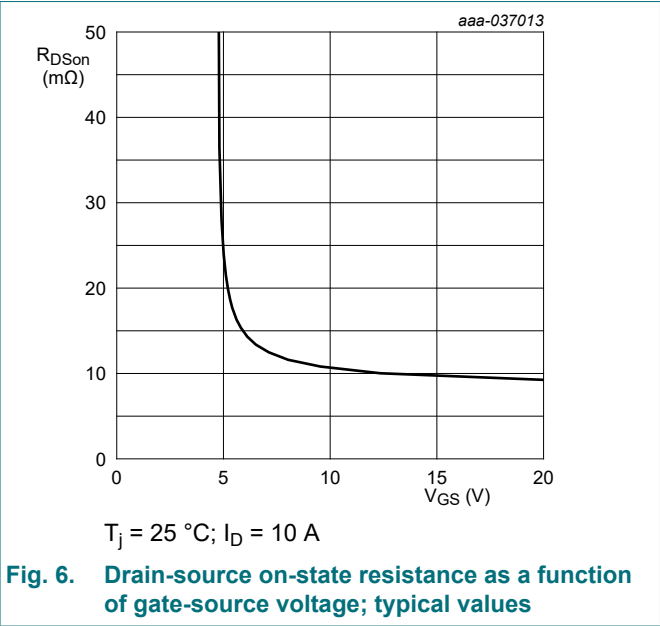
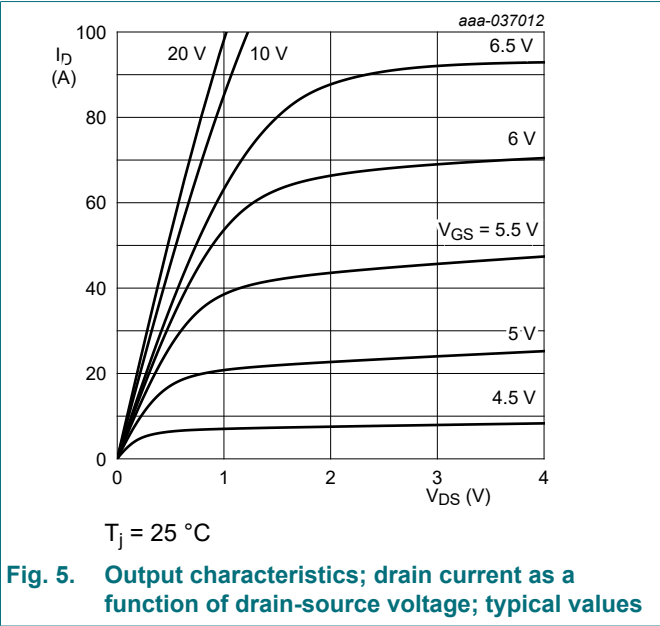
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_J = -55\text{ }^\circ\text{C}$	-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 8	2	3	4	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = 150\text{ }^\circ\text{C}$	-	1.8	-	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_J = -55\text{ }^\circ\text{C}$	-	3.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$	-	-9.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	0.01	1	μA
		$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 150\text{ }^\circ\text{C}$	-	9	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 9	-	10.6	12	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_J = 150\text{ }^\circ\text{C}$; Fig. 10	-	-	23	m Ω
R_G	gate resistance	$f = 1\text{ MHz}$; $T_J = 25\text{ }^\circ\text{C}$	-	1	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11; Fig. 12		-	22	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	11	-	nC
Q _{GS}	gate-source charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 11; Fig. 12		-	6	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	3.8	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	2.1	-	nC
Q _{GD}	gate-drain charge			-	5.5	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 10 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 11; Fig. 12		-	4.6	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 13		-	1313	-	pF
C _{oss}	output capacitance			-	456	-	pF
C _{rss}	reverse transfer capacitance			-	16	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6.7	-	ns
t _r	rise time			-	5.8	-	ns
t _{d(off)}	turn-off delay time			-	14	-	ns
t _f	fall time			-	9.7	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz; T _j = 25 °C		-	35	-	nC
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 14		-	0.83	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 15		-	33	-	ns
Q _r	recovered charge		[1]	-	27	-	nC

[1] includes capacitive recovery



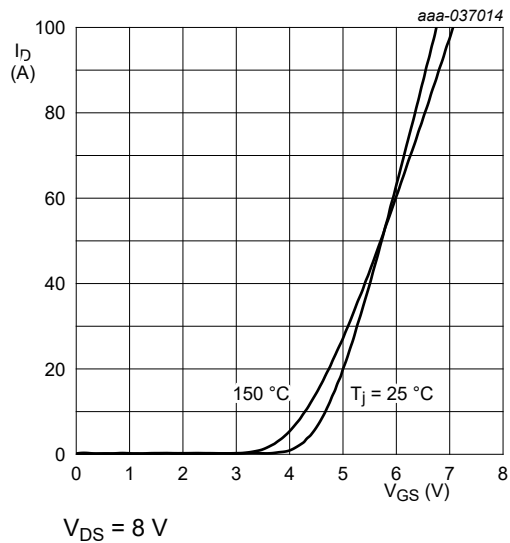


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

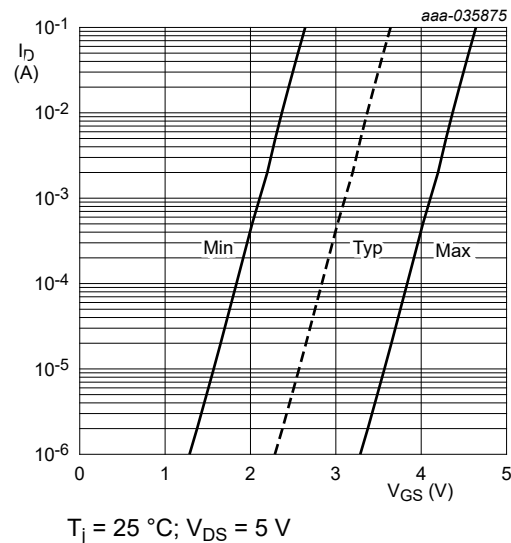


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

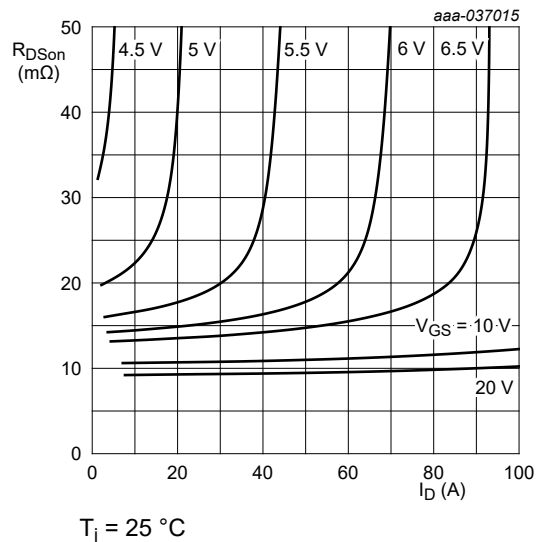


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

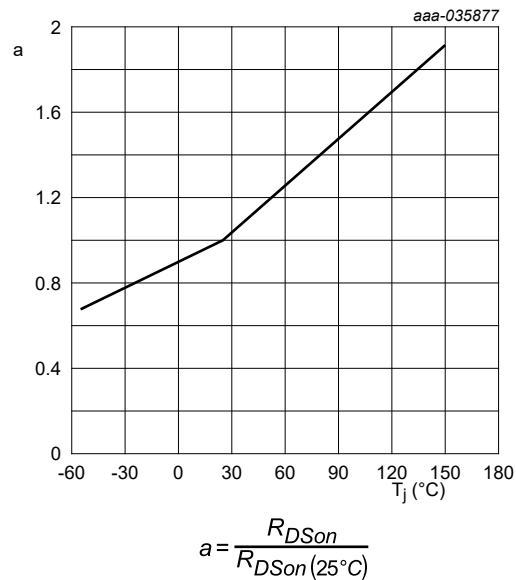


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

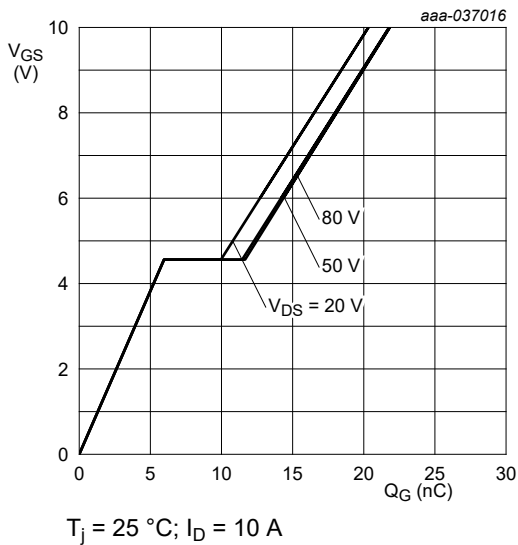


Fig. 11. Gate-source voltage as a function of gate charge; typical values

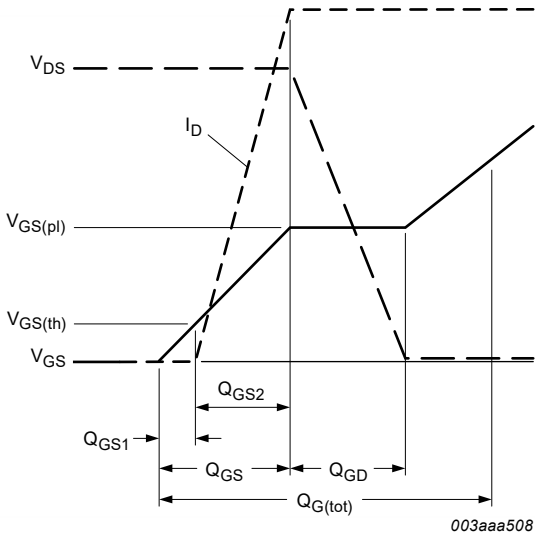


Fig. 12. Gate charge waveform definitions

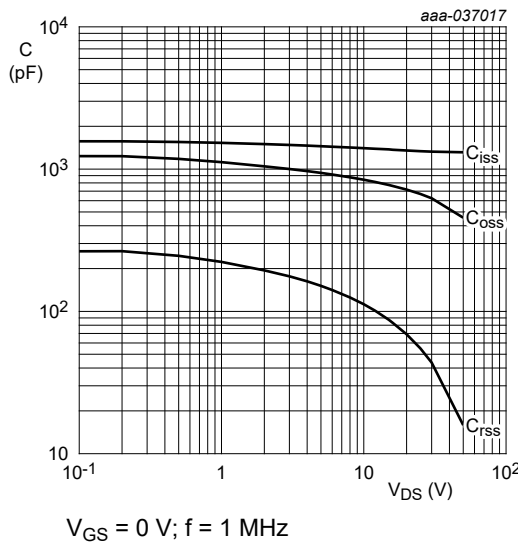


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

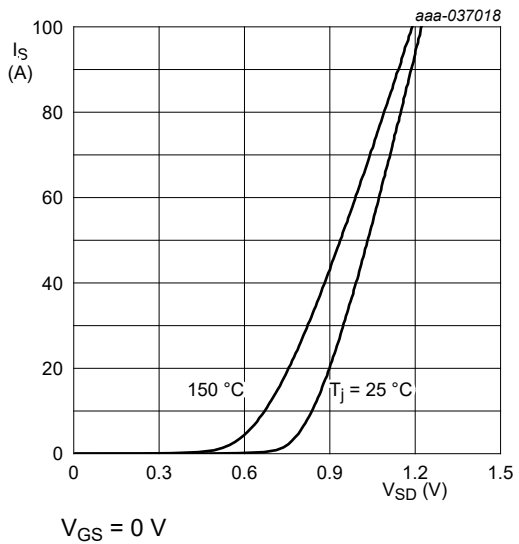


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

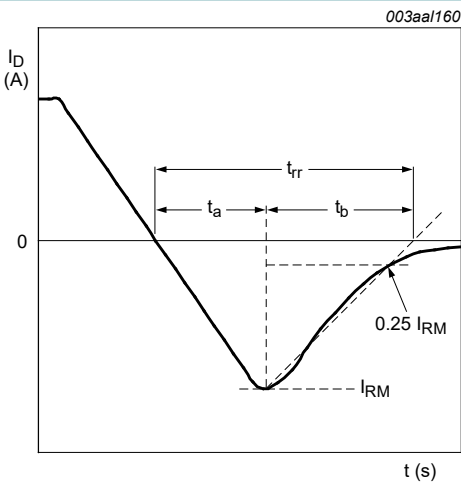


Fig. 15. Reverse recovery timing definition

11. Package outline

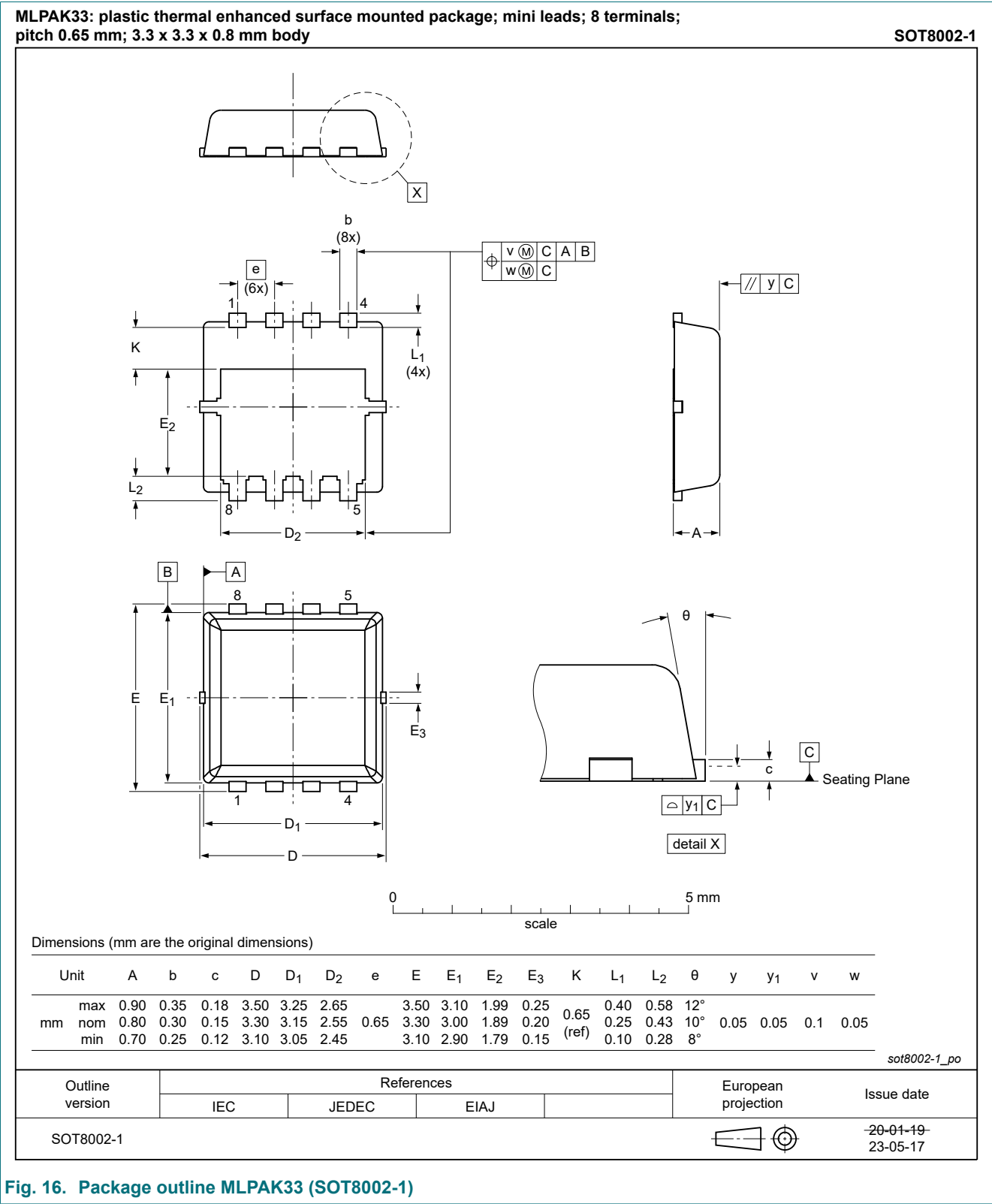


Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

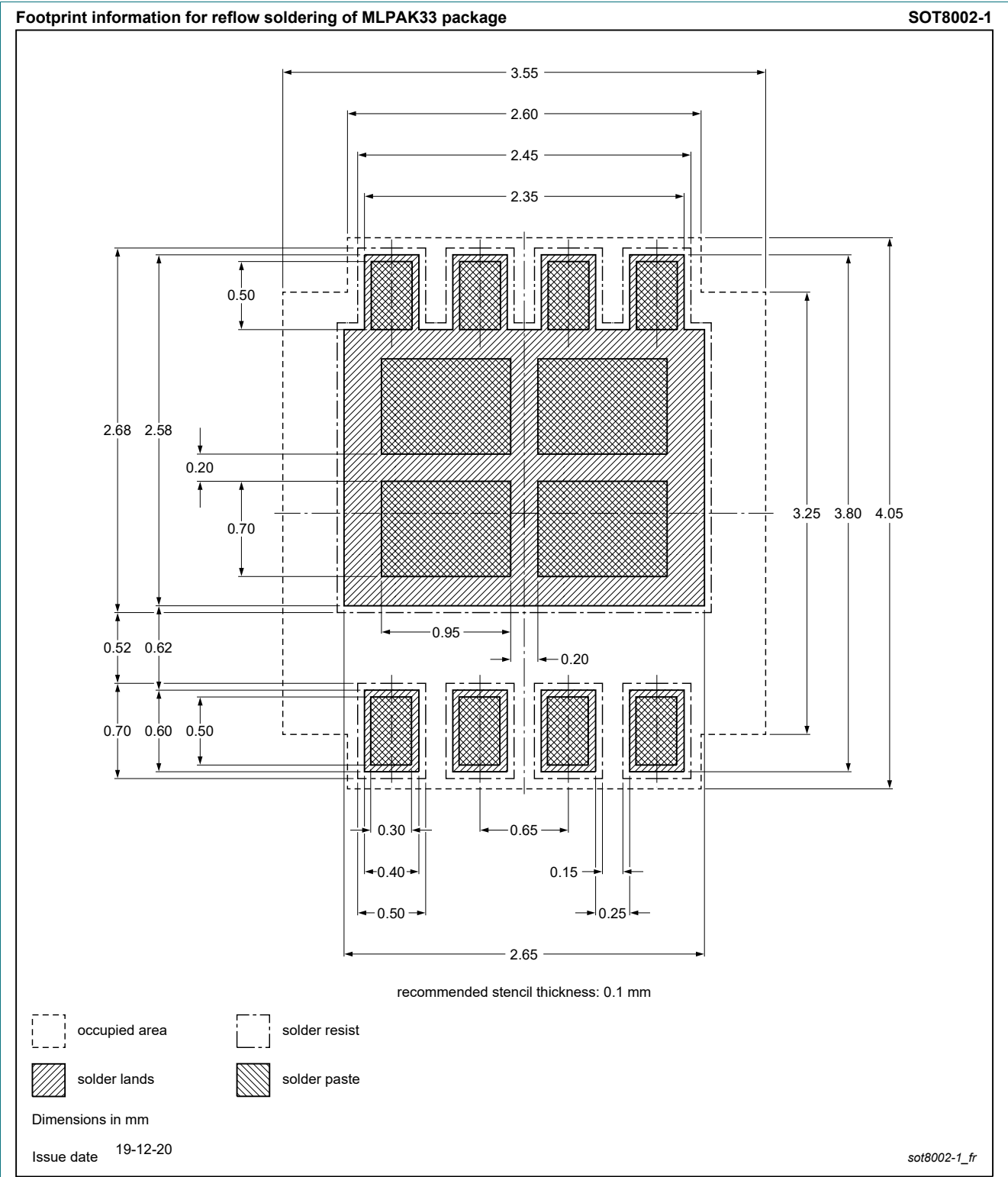


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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