

## DS15EA101 0.15 to 1.5 Gbps Adaptive Cable Equalizer with LOS Detection

Check for Samples: [DS15EA101](#)

### FEATURES

- Automatic Equalization of Coaxial, Twin-Ax and Twisted Pair Cables
- High Data Rates: 150 Mbps to 1.5+ Gbps
- Up to 35 dB of Boost at 750 MHz
- LOS Detection and Output Enable
- Single-Ended or Differential Input
- 50Ω Differential Outputs
- Low Power Operation, 210 mW (typ) at 1.5 Gbps
- Industrial -40°C to +85°C Temperature
- Space-Saving 4 x 4 mm WQFN-16 Package

### APPLICATIONS

- Cable Extension Applications
- Security Cameras
- Remote LCDs and LED Panels
- Data Recovery Equalization

### DESCRIPTION

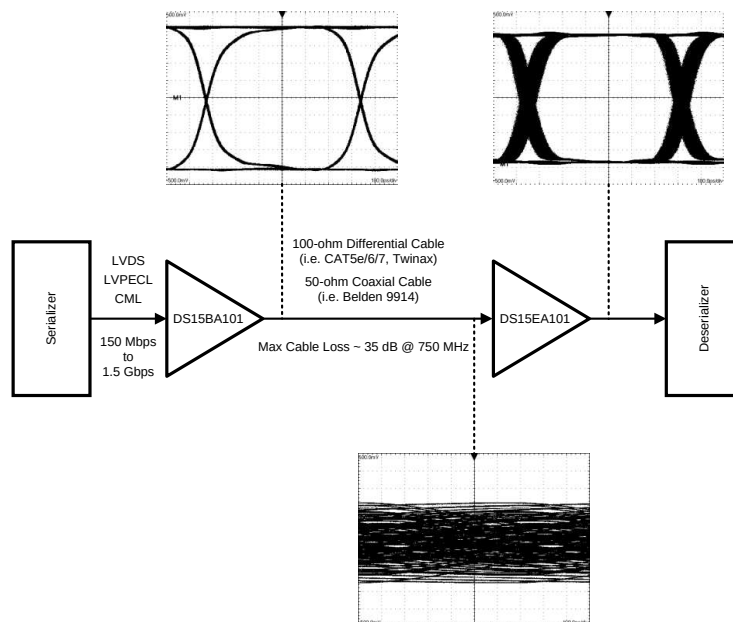
The DS15EA101 is an adaptive equalizer optimized for equalizing data transmitted over copper cables. The DS15EA101 operates over a wide range of data rates from 150 Mbps to 1.5+ Gbps and automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 35 dB at 750 MHz.

The DS15EA101 allows either single-ended or differential input drive. This enables equalization of coaxial cables as well as differential twin-ax and twisted pair cables.

Additional features include an LOS output and an output enable which, when tied together, disable the output when no signal is present.

The DS15EA101 is powered from a single 3.3V supply and consumes 210 mW at 1.5 Gbps. It operates over the full -40°C to +85°C industrial temperature range and is available in a space saving 4 x 4 mm WQFN-16 package which allows for high density placement of components in multi-channel applications.

### Typical Application



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)</sup>

|                                                                                |                        |
|--------------------------------------------------------------------------------|------------------------|
| Supply Voltage                                                                 | -0.5V to 3.6V          |
| Input Voltage (all inputs)                                                     | -0.3V to $V_{CC}+0.3V$ |
| Storage Temperature Range                                                      | -65°C to +150°C        |
| Junction Temperature                                                           | +150°C                 |
| Lead Temperature<br>(Soldering 4 Sec)                                          | +260°C                 |
| Package Thermal Resistance<br>$\theta_{JA}$ RGH0016A<br>$\theta_{JC}$ RGH0016A | +42.1°C/W<br>+8.2°C/W  |
| ESD Rating (HBM)                                                               | 8 kV                   |
| ESD Rating (MM)                                                                | 250V                   |

- (1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

## Recommended Operating Conditions

|                                                  |                |
|--------------------------------------------------|----------------|
| Supply Voltage ( $V_{CC}$ )                      | 3.3V $\pm 5\%$ |
| Input Coupling Capacitance                       | 1.0 $\mu F$    |
| Loop Capacitor (Connected between CAP+ and CAP-) | 1.0 $\mu F$    |
| Operating Free Air Temperature ( $T_A$ )         | -40°C to +85°C |

## DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified <sup>(1)</sup> <sup>(2)</sup>.

| Symbol       | Parameter                     | Conditions                     | Reference       | Min | Typ                  | Max | Units             |
|--------------|-------------------------------|--------------------------------|-----------------|-----|----------------------|-----|-------------------|
| $V_{CM}$     | Input Common Mode Voltage     |                                | IN+, IN-        |     | 1.9                  |     | V                 |
| $V_{IN}$     | Input Voltage                 |                                |                 |     | (3)(4)950            |     | mV <sub>P-P</sub> |
| $V_{OS}$     | Output Common Mode Voltage    |                                | OUT+, OUT-      |     | $V_{CC} - V_{OUT}/2$ |     | V                 |
| $V_{OUT}$    | Output Voltage Swing          | 50 $\Omega$ load, differential |                 |     | 750                  |     | mV <sub>P-P</sub> |
| $V_{LOS}$    | LOS Output Voltage            | Valid signal not present       | LOS             | 2.6 |                      |     | V                 |
|              |                               | Valid signal present           |                 |     |                      | 0.4 | V                 |
| $V_{IN(EN)}$ | $\overline{EN}$ Input Voltage | Min to disable outputs         | $\overline{EN}$ | 3.0 |                      |     | V                 |
|              |                               | Max to enable outputs          |                 |     |                      | 0.8 | V                 |
| $I_{CC}$     | Supply Current                | (5)                            |                 |     | 63                   | 77  | mA                |

- (1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to 0 volts.  
 (2) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .  
 (3) Specification is ensured by characterization.  
 (4) The maximum input voltage amplitude assumes a DC-balanced signal.  
 (5) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased.

## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified <sup>(1)</sup>.

| Symbol           | Parameter                                     | Conditions                                            | Reference  | Min | Typ  | Max  | Units |
|------------------|-----------------------------------------------|-------------------------------------------------------|------------|-----|------|------|-------|
| BR <sub>IN</sub> | Input Data Rate                               |                                                       | IN+, IN-   | 150 |      | 1500 | Mbps  |
| t <sub>TRJ</sub> | Total Residual Jitter @ BER-12 <sup>(2)</sup> | 1.5 Gbps<br>25m CAT5e (Belden 1700A), <sup>(1)</sup>  |            |     | 0.25 |      | UI    |
|                  |                                               | 1.0 Gbps<br>50m CAT5e (Belden 1700A), <sup>(1)</sup>  |            |     | 0.25 |      | UI    |
|                  |                                               | 0.5 Gbps<br>100m CAT5e (Belden 1700A), <sup>(1)</sup> |            |     | 0.25 |      | UI    |
|                  |                                               | 1.5 Gbps<br>50m CAT7 (Siemon Tera), <sup>(1)</sup>    |            |     | 0.25 |      | UI    |
|                  |                                               | 1.5 Gbps<br>75m CAT7 (Siemon Tera), <sup>(1)</sup>    |            |     | 0.30 |      | UI    |
|                  |                                               | 1.0 Gbps<br>100m CAT7 (Siemon Tera), <sup>(1)</sup>   |            |     | 0.40 |      | UI    |
|                  |                                               | 1.5 Gbps<br>200m Belden 9914, <sup>(1)</sup>          |            |     | 0.25 |      | UI    |
| t <sub>TLH</sub> | Transition Time from Low to High              | 20% – 80%, <sup>(3)</sup>                             | OUT+, OUT- |     | 100  | 220  | ps    |
| t <sub>THL</sub> | Transition Time from High to Low              | 20% – 80%, <sup>(3)</sup>                             |            |     | 100  | 220  | ps    |
| R <sub>OUT</sub> | Output Resistance                             | single-ended, <sup>(4)</sup>                          |            |     | 50   |      | Ω     |

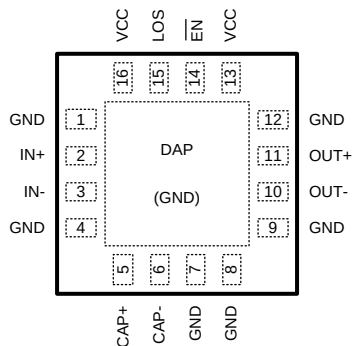
(1) Typical values are stated for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C.

(2) The total residual jitter at BER-12 was calculated as DJ+14.1xRJ, where DJ is deterministic jitter and RJ is random jitter. The jitter is expressed as a portion of a unit interval (UI). One UI is a reciprocal of a bit rate (or data rate). For example, a 1.5 Gbps (gigabit per second) signal has 1 / (1.5 Gb/s) = 666.67 ps (picosecond) unit interval. A 0.25 UI jitter is equivalent to 0.25 x 666.67 ps = 166.67 ps.

(3) Specification is ensured by characterization.

(4) Specification is ensured by design.

## CONNECTION DIAGRAM



**16-Pad WQFN**  
**Package Number RGH0016A**

## PIN DESCRIPTIONS

| Pin # | Name                   | Description                         |
|-------|------------------------|-------------------------------------|
| 1     | GND                    | Ground pin.                         |
| 2     | IN+                    | Non-inverting input pin.            |
| 3     | IN-                    | Inverting input pin.                |
| 4     | GND                    | Ground pin.                         |
| 5     | CAP+                   | Loop filter positive pin.           |
| 6     | CAP-                   | Loop filter negative pin.           |
| 7     | GND                    | Ground pin.                         |
| 8     | GND                    | Ground pin.                         |
| 9     | GND                    | Ground pin.                         |
| 10    | OUT-                   | Inverting output pin.               |
| 11    | OUT+                   | Non-inverting output pin.           |
| 12    | GND                    | Ground pin.                         |
| 13    | VCC                    | Power supply pin.                   |
| 14    | $\overline{\text{EN}}$ | Output enable pin.                  |
| 15    | LOS                    | Los of signal circuitry output pin. |
| 16    | VCC                    | Power supply pin.                   |

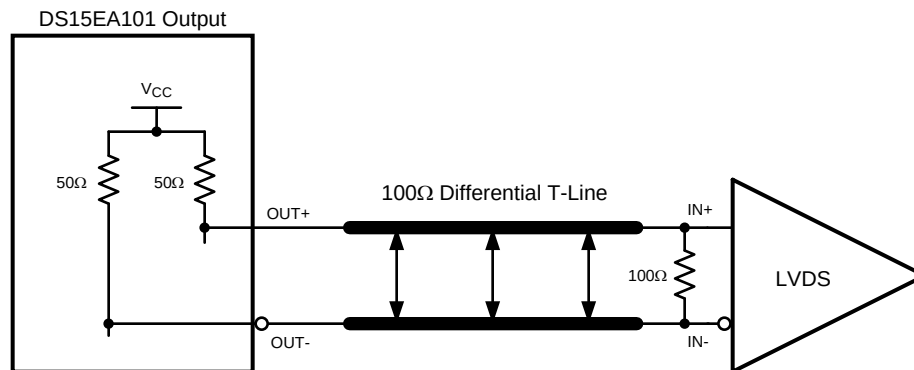
## DEVICE OPERATION

### Input Interfacing

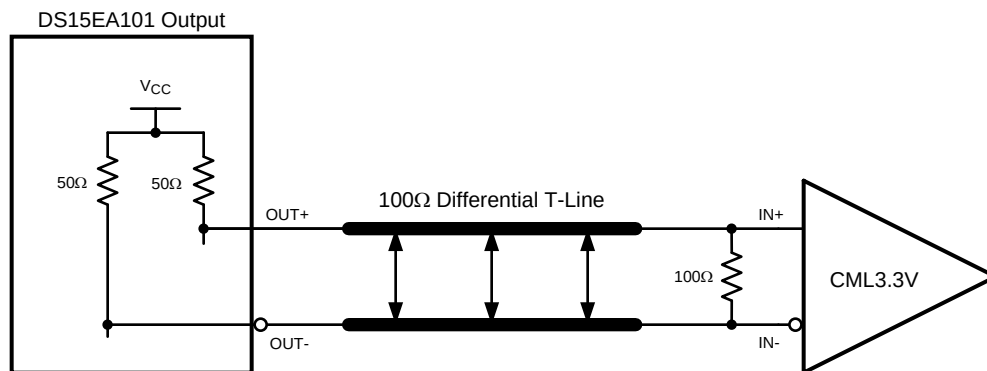
The DS15EA101 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported. If the signal is differential, its amplitude must be 800 mVp-p  $\pm 10\%$  (400 mV single-ended). If the signal is single-ended, its amplitude must be 800 mV  $\pm 10\%$ .

### Output Interfacing

The DS15EA101 uses current mode outputs. They are internally terminated with 50 $\Omega$ . The following two figures illustrate typical DC-coupled interface to common differential receivers and assume that the receivers have high impedance inputs. While most receivers have an input common mode voltage range that can accommodate CML signals, it is recommended to check respective receiver's datasheet prior to implementing the suggested interface implementations.



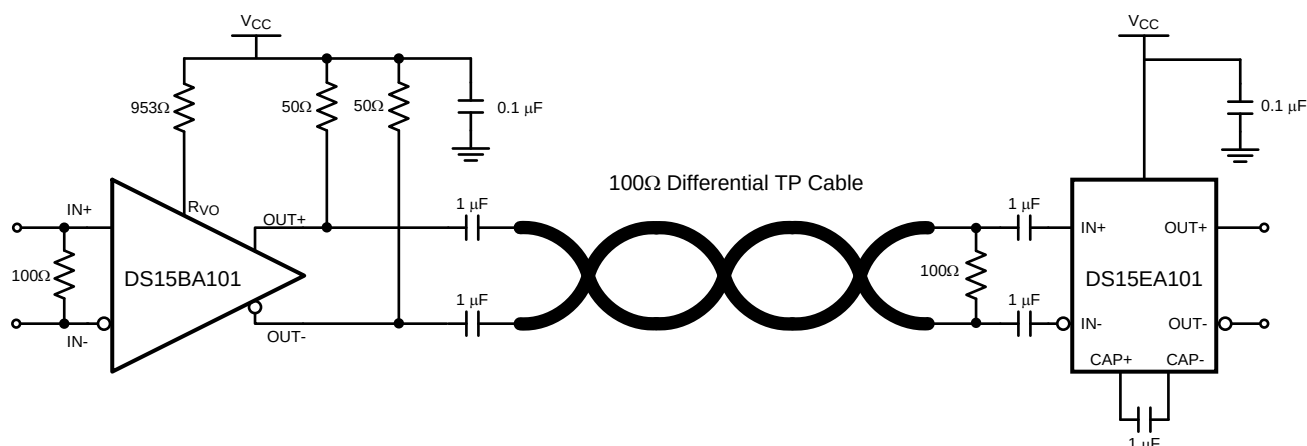
**Figure 1. Typical DS15EA101 Output DC-Coupled Interface to an LVDS Receiver**



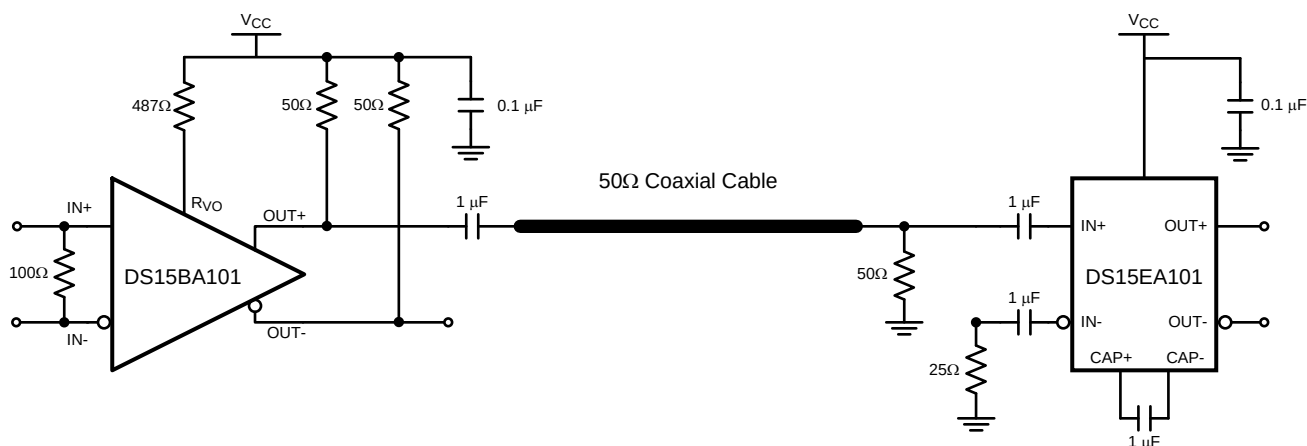
**Figure 2. Typical DS15EA101 Output DC-Coupled Interface to a CML Receiver**

### Cable Extender Application

The DS15EA101 together with the DS15BA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and field programmable gate arrays (FPGAs) over 100 $\Omega$  differential (i.e. CAT5e/6/7 and twinax) and 50 $\Omega$  coaxial cables. Setting correct DS15BA101 output amplitude and proper cable termination are keys for optimal operation. The following two figures show recommended chipset configuration for 100 $\Omega$  differential and 50 $\Omega$  coaxial cables.



**Figure 3. Cable Extender Chipset Connection Diagram for 100Ω Differential Cables**



**Figure 4. Cable Extender Chipset Connection Diagram for 50Ω Coaxial Cables**

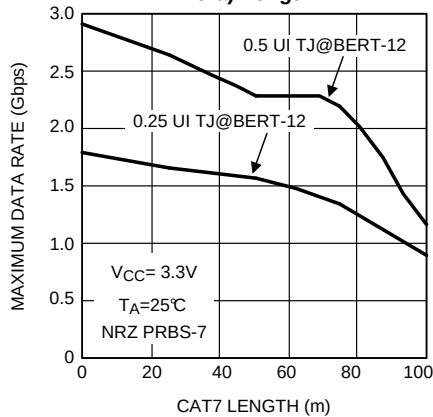
## Reference Design

There is a complete reference design (P/N: DriveCable02EVK) available for evaluation of the cable extender chipset (DS15BA101 and DS15EA101).

For more information visit <http://www.ti.com/tool/drivecable02evk>

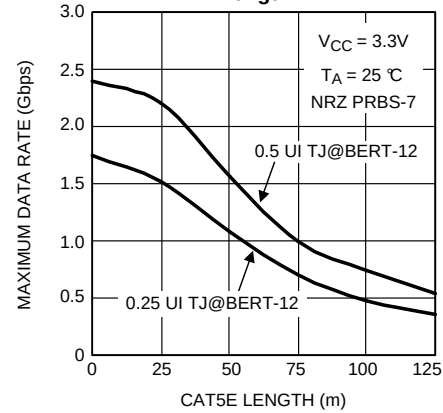
## Typical Performance

**Maximum Data Rate as a Function of CAT7 (Siemon CAT7 Tera) Length**



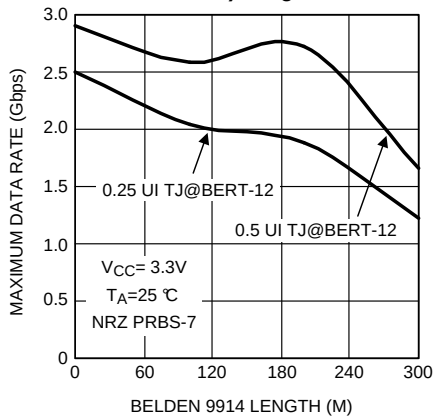
**Figure 5.**

**Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length**



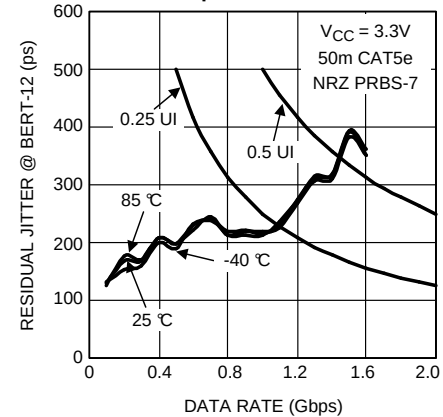
**Figure 6.**

**Maximum Data Rate as a Function of 50Ω Coaxial (Belden 9914) Length**



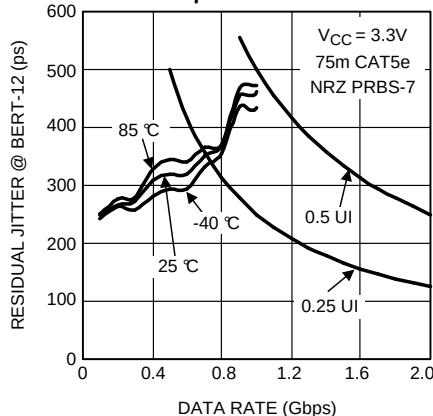
**Figure 7.**

**Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 50m CAT5e**



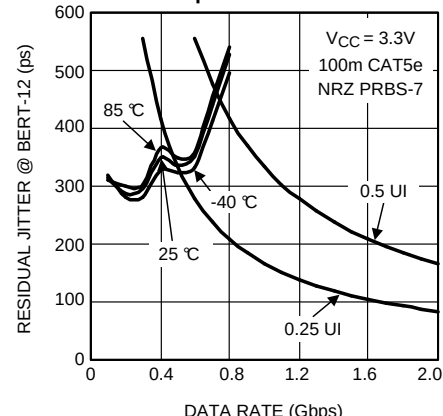
**Figure 8.**

**Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 75m CAT5e**



**Figure 9.**

**Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 100m CAT5e**



**Figure 10.**

### Typical Performance (continued)

**A 1.5 Gbps NRZ PRBS-7 After 25m CAT5e**  
V:100 mV / DIV, H:100 ps / DIV

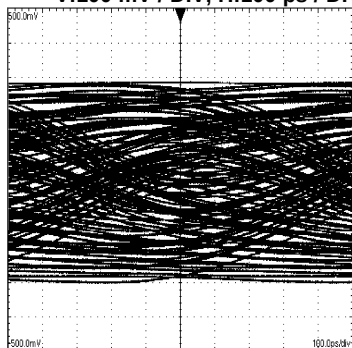


Figure 11.

**An Equalized 1.5 Gbps NRZ PRBS-7 After 25m CAT5e**  
V:100 mV / DIV, H:100 ps / DIV

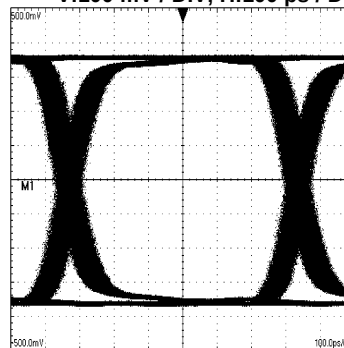


Figure 12.

**A 1.0 Gbps NRZ PRBS-7 After 50m CAT5e**  
V:100 mV / DIV, H:150 ps / DIV

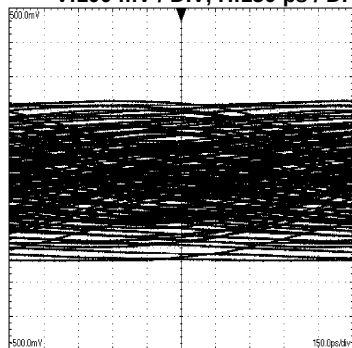


Figure 13.

**An Equalized 1.0 Gbps NRZ PRBS-7 After 50m CAT5e**  
V:100 mV / DIV, H:150 ps / DIV

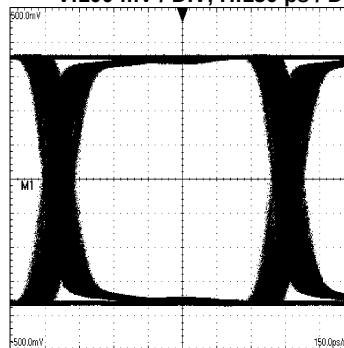


Figure 14.

**A 0.5 Gbps NRZ PRBS-7 After 100m CAT5e**  
V:100 mV / DIV, H:400 ps / DIV

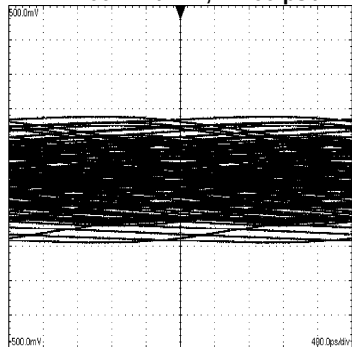


Figure 15.

**An Equalized 0.5 Gbps NRZ PRBS-7 After 100m CAT5e**  
V:100 mV / DIV, H:400 ps / DIV

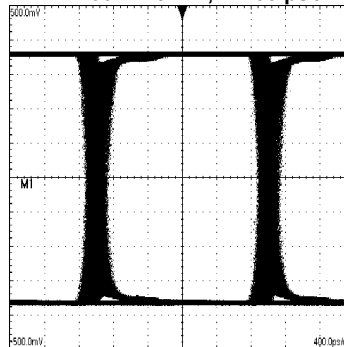


Figure 16.



## Typical Performance (continued)

**A 1.5 Gbps NRZ PRBS-7 After 50m CAT7**  
V:100 mV / DIV, H:100 ps / DIV

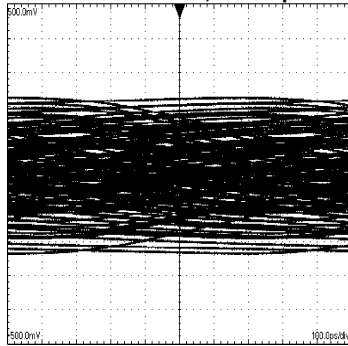


Figure 17.

**An Equalized 1.5 Gbps NRZ PRBS-7 After 50m CAT7**  
V:100 mV / DIV, H:100 ps / DIV

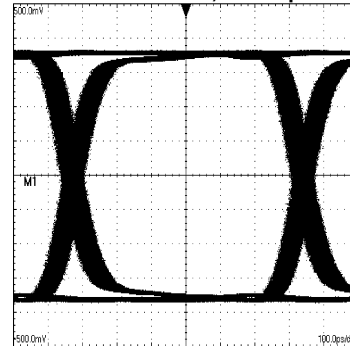


Figure 18.

**An Equalized 1.5 Gbps NRZ PRBS-7 After 75m CAT7**  
V:100 mV / DIV, H:100 ps / DIV

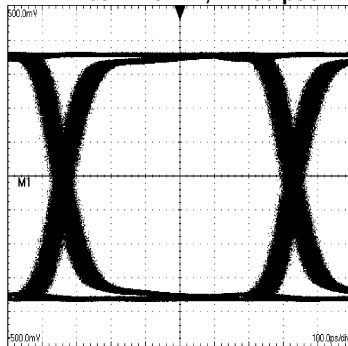


Figure 19.

**A 1.5 Gbps NRZ PRBS-7 After 75m CAT7**  
V:100 mV / DIV, H:100 ps / DIV

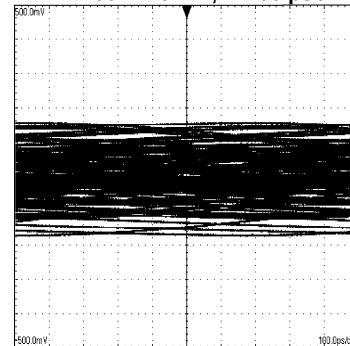


Figure 20.

**A 1.0 Gbps NRZ PRBS-7 After 100m CAT7**  
V:100 mV / DIV, H:150 ps / DIV

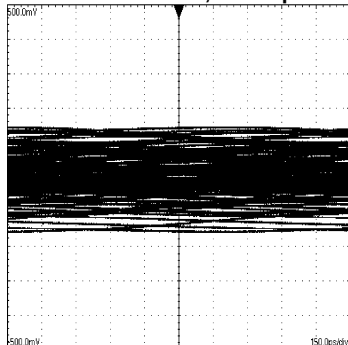


Figure 21.

**An Equalized 1.0 Gbps NRZ PRBS-7 After 100m CAT7**  
V:100 mV / DIV, H:150 ps / DIV

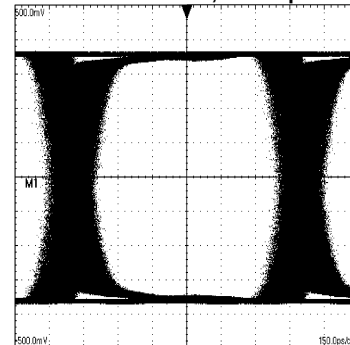
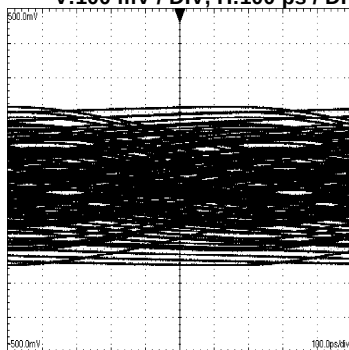


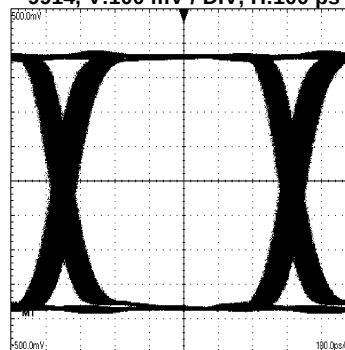
Figure 22.

**Typical Performance (continued)**

A 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914  
V:100 mV / DIV, H:100 ps / DIV

**Figure 23.**

An Equalized 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914, V:100 mV / DIV, H:100 ps / DIV

**Figure 24.**

## REVISION HISTORY

### Changes from Revision G (April 2013) to Revision H

### Page

- Changed layout of National Data Sheet to TI format ..... [10](#)

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| DS15EA101SQ/NOPB  | ACTIVE        | WQFN         | RGH                | 16   | 1000           | Green (RoHS<br>& no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | 15EA101                  | <a href="#">Samples</a> |
| DS15EA101SQE/NOPB | ACTIVE        | WQFN         | RGH                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | 15EA101                  | <a href="#">Samples</a> |
| DS15EA101SQX/NOPB | ACTIVE        | WQFN         | RGH                | 16   | 4500           | Green (RoHS<br>& no Sb/Br) | CU SN            | Level-3-260C-168 HR  | -40 to 85    | 15EA101                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

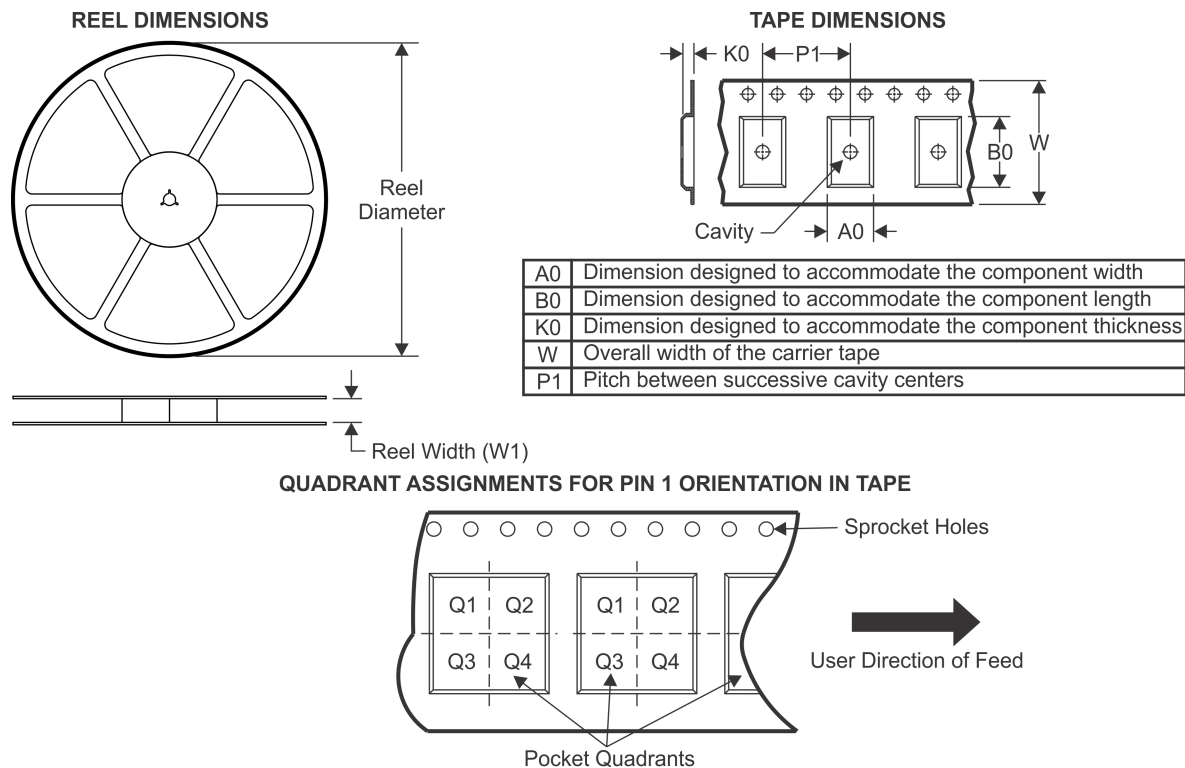
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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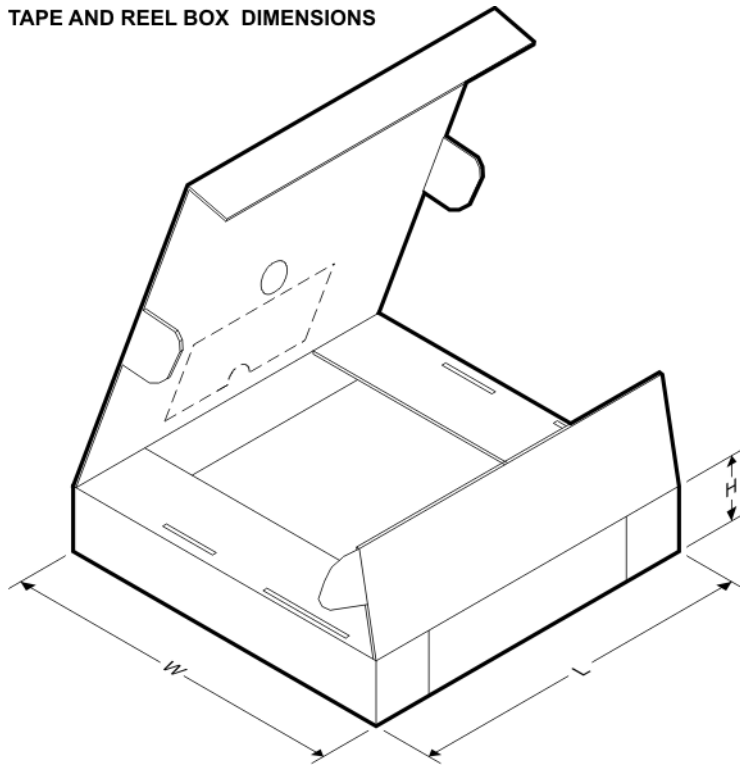
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS15EA101SQ/NOPB  | WQFN         | RGH             | 16   | 1000 | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| DS15EA101SQE/NOPB | WQFN         | RGH             | 16   | 250  | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| DS15EA101SQX/NOPB | WQFN         | RGH             | 16   | 4500 | 330.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS15EA101SQ/NOPB  | WQFN         | RGH             | 16   | 1000 | 210.0       | 185.0      | 35.0        |
| DS15EA101SQE/NOPB | WQFN         | RGH             | 16   | 250  | 210.0       | 185.0      | 35.0        |
| DS15EA101SQX/NOPB | WQFN         | RGH             | 16   | 4500 | 367.0       | 367.0      | 35.0        |

WQFN - 0.8 mm max height

**Top View:** Shows a rectangular footprint with a width of 4.1 (3.9) and a height of 4.1 (3.9). A shaded area in the top-left corner is labeled "PIN 1 INDEX AREA". A square feature in the center is labeled "PIN 1 ID (OPTIONAL)".

**Side View:** Shows the profile of the connector with a maximum height of 0.8 MAX. The base is labeled "SEATING PLANE".

**Detail View:** Shows a cross-section of the optional terminal with dimensions 0.3, 0.2, 0.5, and 0.3. It is labeled "DETAIL OPTIONAL TERMINAL TYPICAL".

**Pin Configuration Table:**

|   |          |   |       |       |
|---|----------|---|-------|-------|
| ⊕ | 0.1 (M)  | C | A (S) | B (S) |
|   | 0.05 (M) | C |       |       |

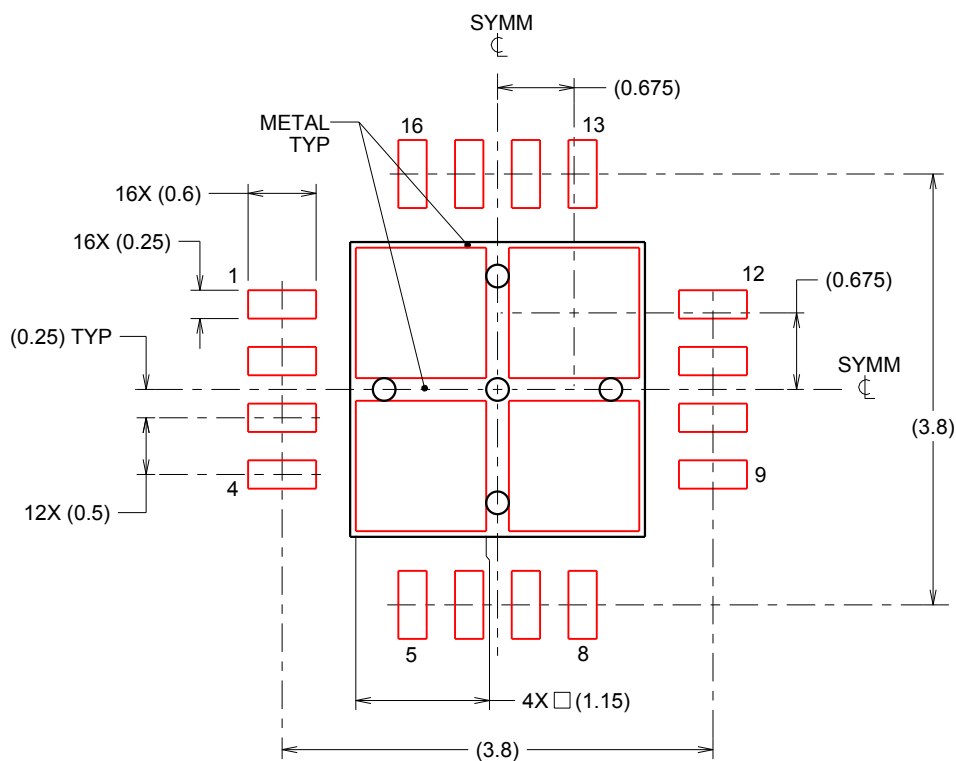
**Dimensions and Features:**

- Top View: 4.1 (3.9) width, 4.1 (3.9) height, 2.6 ± 0.1 central square, 5 and 8 pin counts, 16X 0.5 (0.3) dimensions.
- Side View: 0.8 MAX height, SEATING PLANE.
- Detail View: 0.3, 0.2, 0.5, 0.3 dimensions.
- Pin Configuration Table: 0.1 (M), 0.05 (M), C, A (S), B (S).

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.







**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
78% PRINTED SOLDER COVERAGE BY AREA  
SCALE:15X

4214978/A 10/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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|                               |                                                                                          |
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