Optical Image Stabilization (OIS) / Open-Auto Focus (AF) Controller & Driver integrating an on-chip 32-bit DSP

LC898124EP2XC

WLCSP27, 3.89x1.30, 0.4P
CASE 567NJ

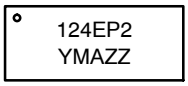
OVERVIEW

LC898124EP2XC is a system LSI integrating an onchip 32−bit DSP, an EEPROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Open−AF (Auto Focus) control and constant current drivers.

FEATURES

- On−chip 32−bit DSP
  - Built−in software for digital servo filter
  - Built−in software for Gyro filter
- Memory
  - EEPROM
  - ROM
  - SRAM
- Peripherals
  - AD converter: Input 4−ch
  - DA converter: Output 2−ch
  - 2−wire Serial I/F circuit (with clock stretch function)
  - Hall Bias circuit x2−ch
  - Hall Amp x2−ch
  - OSC (Oscillator)
  - LDO (Low Drop−Out regulator)
  - Digital Gyro I/F for various types of gyro (SPI Bus)
  - Interrupt I/F
- Driver
  - OIS
    Constant current linear driver (x2−ch, I_{full} = 160 mA)
  - OP−AF (bidirection)
    Constant current linear driver (x1−ch, I_{full} = 130 mA)
- Package
  - WLCSP27 (3.89 mm x 1.30 mm), thickness Max. 0.33 mm, with back coat
  - Pb−Free and Halogen Free compliance
- Power Supply Voltage
  - AD / DA / VGA / LDO / OSC: AVDD30 = 2.6 V to 3.3 V
  - Driver: VM = 1.8 V to 3.3 V
  - Core Logic: Generated by on−chip LDO DVDD15 = typ. 1.59 V
  - 1.8 V I/O: Generated by on−chip LDO typ. 1.80 V
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

MARKING DIAGRAM



124EP2	= Specific Device Code
Y	= Year
M	= Month
A	= Assembly Site
ZZ	= Lot Number

ORDERING INFORMATION

Device	Package	Shipping†
LC898124EP2XC−MH	WLCSP27 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

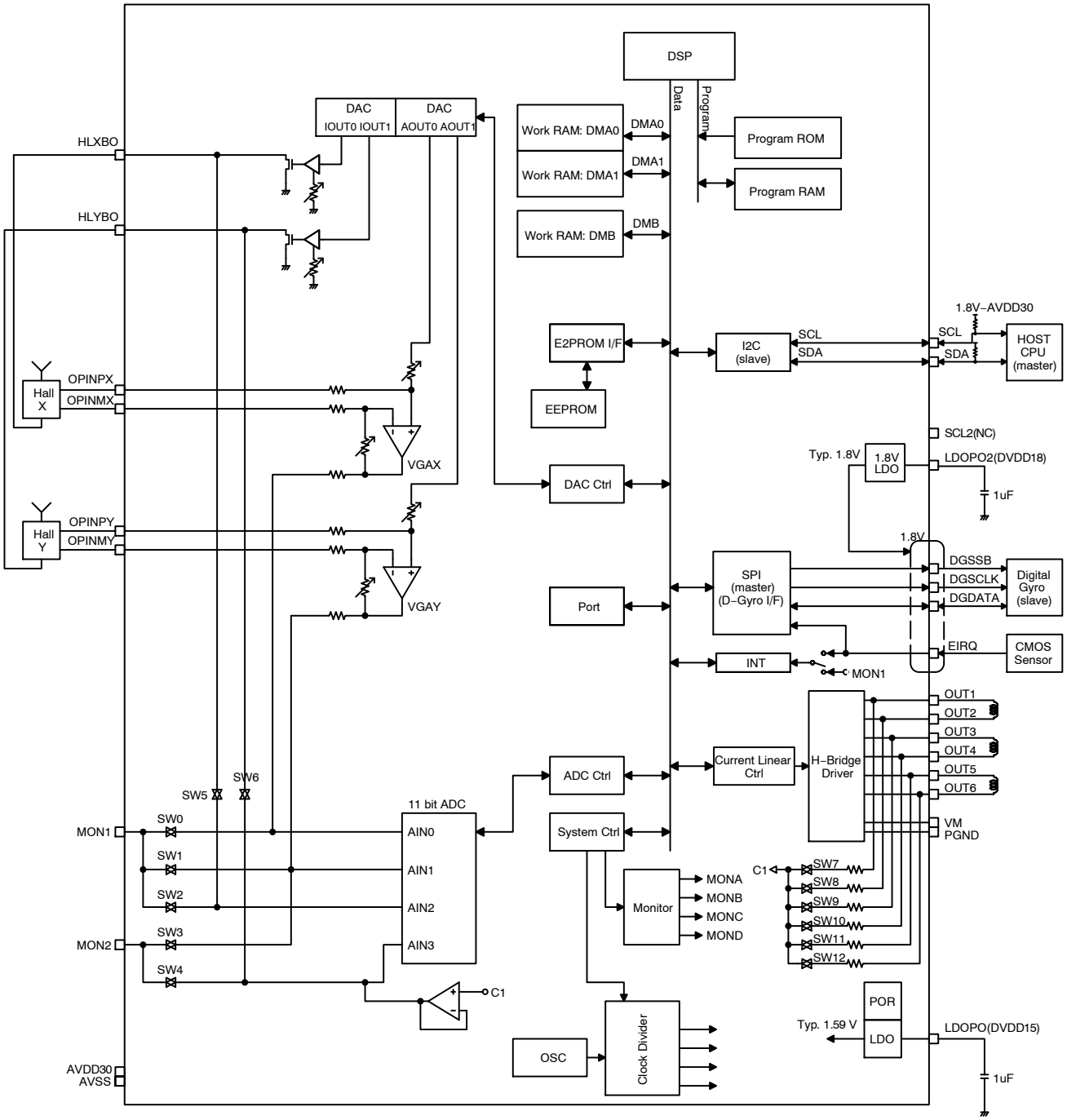


Figure 1. Block Diagram

APPLICATION DIAGRAM

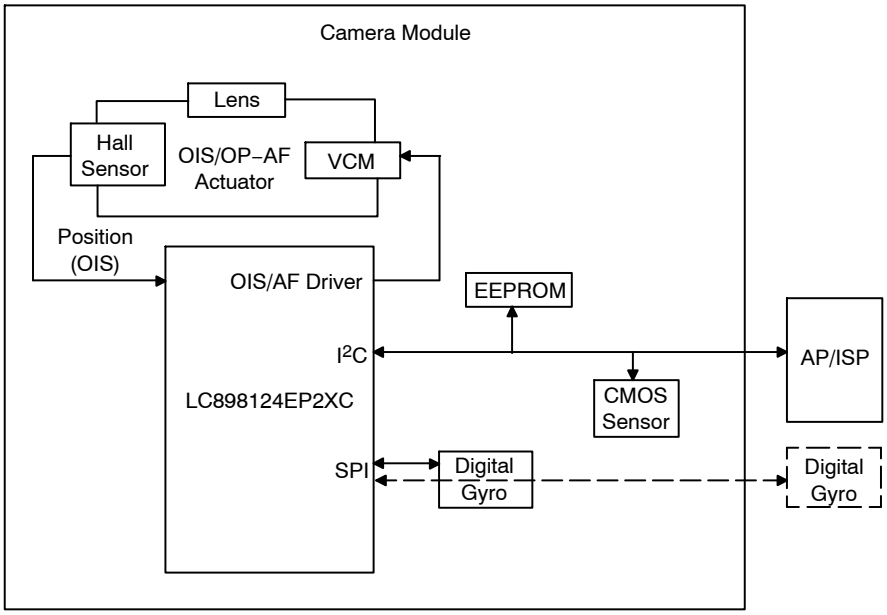


Figure 2. Application Diagram

PIN LAYOUT

Table 1. BOTTOM VIEW

C	OUT4	OUT3	OUT2	OUT1	OPINPX	HLXBO	MON2	EIRQ	DGDATA
B	VM	PGND	OPINPY	OPINMY	OPINMX	HLYBO	LDPO2	SDA	DGSCLK
A	OUT5	OUT6	AVSS	AVDD30	LDPO	MON1	SCL2	SCL	DGSSB
	1	2	3	4	5	6	7	8	9

Driver VDD/VSS Internal VDD Output 1.8 V I/O

Table 2. PIN DESCRIPTION

NO.	Pin	I/O	I/O Spec	Primary Function	Sub Functions	Init
1	MON1	B		Servo Monitor Analog In/Out	2−wire serial Data	Z
					Interrupt Input	
2	MON2	B		Servo Monitor Analog In/Out	2−wire serial Clock	Z
3	SCL	B	OD	2−wire serial HOST I/F Clock Slave		Z
4	SDA	B	OD	2−wire serial HOST I/F Data Slave		Z
5	LDPO2	P		Internal 1.8 V LDO Power Output		Z
6	SCL2	B		NC		Z
7	DGSSB	B		Digital Gyro Data I/F Chip Select Out (3/4−wire Master)	3/4−wire I/F Chip Select In (Read only)	Z
8	DGSCLK	B		Digital Gyro Data I/F Clock Out (3/4−wire Master)	3/4−wire I/F Clock In (Read only)	Z
9	EIRQ	B	OD	Interrupt Input	Digital Gyro Data I/F Data In (4−wire Master)	Z
10	DGDATA	B		Digital Gyro Data I/F Data (3−wire Master)	Digital Gyro Data I/F Data Out (4−wire Master)	Z
					3/4−wire I/F Data In (Read only)	
11	HLXBO	O		OIS Hall X Bias Output		Z
12	HLYBO	O		OIS Hall Y Bias Output		Z
13	OPINMX	I		OIS Hall X Opamp Input Minus		Z
14	OPINPX	I		OIS Hall X Opamp Input Plus		−
15	OPINMY	I		OIS Hall Y Opamp Input Minus		−
16	OPINPY	I		OIS Hall Y Opamp Input Plus		−
17	OUT1	O		OIS Driver Output		Z
18	OUT2	O		OIS Driver Output		Z
19	OUT3	O		OIS Driver Output		Z
20	OUT4	O		OIS Driver Output		Z
21	OUT5	O		Open−AF Driver Output		Z
22	OUT6	O		Open−AF Driver Output		Z
23	AVDD30	P		Analog Power (2.6 V to 3.3 V)		−
24	AVSS	P		Analog GND		−
25	VM	P		Driver Power (1.8 V to 3.3 V)		−
26	PGND	P		Driver GND		
27	LDPO	P		Internal 1.59 V LDO Power Output		

1. Process when pins are not used:
   PIN TYPE “O” − Ensure that it is set to OPEN.
   PIN TYPE “I” − OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused.
   (Please contact **onsemi** for more information about selection of V_{DD} or V_{SS}.)
   PIN TYPE “B” − If you are unsure about processing method on the pin description of pin layout table, please contact us.
2. Note that incorrect processing of unused pins may result in defects.

ELECTRICAL CHARACTERISTICS

Table 3. ABSOLUTE MAXIMUM RATINGS (at AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	$V_{AD}30$ max	Ta ≤ 25°C	–0.3 to 4.6	V
	VM max	Ta ≤ 25°C	–0.3 to 4.6	V
Input / Output Voltage	$V_{AI}30$, $V_{AO}30$	Ta ≤ 25°C	–0.3 to $V_{AD}30$+0.3	V
	$V_{MI}30$, $V_{MO}30$	Ta ≤ 25°C	–0.3 to $V_{M}30$+0.3	V
Input Voltage	V18*	Ta ≤ 25°C	–0.3 to 1.98	V
Storage Temperature	Tstg		–55 to 125	°C
Operating Temperature	Topr1	Read for EEPROM	–30 to 85	°C
	Topr2	Program & Erase for EEPROM	–30 to 70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
* DGSSB, DGSCLK, DGDATA, EIRQ

Table 4. ALLOWABLE OPERATING RATINGS (at T_A = –30 to 85°C, AVSS = 0 V, PGND = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
3.0 V POWER SUPPLY (AVDD30)					
Power Supply Voltage	$V_{AD}30$	2.6	2.8	3.3	V
Input Voltage Range	V_{INA}	0	–	$V_{AD}30$	V
3.0 V POWER SUPPLY (VM)					
Power Supply Voltage	$V_{M}30$	1.8	2.8	The lower of 3.3 and AVDD30 +0.5	V
Input Voltage Range	V_{INM}	0	–	$V_{M}30$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. D.C. CHARACTERISTICS: INPUT/OUTPUT
(at T_A = –30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.6 to 3.3. V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	Applicable Pins
High–level Input Voltage	VIH	CMOS schmitt	1.26			V	DGSSB, DGSCLK, DGDATA, EIRQ
Low–level Input Voltage	VIL				0.4	V	
High–level Input Voltage	VIH	CMOS schmitt	1.4			V	SCL, SDA
Low–level Input Voltage	VIL				0.4	V	
High–level Input Voltage	VIH	CMOS schmitt	0.75AVDD30			V	MON1, MON2
Low–level Input Voltage	VIL				0.25AVDD30	V	
High–level Output Voltage	VOH	IOH = –1 mA	1.51		1.89	V	DGSSB, DGSCLK, DGDATA
Low–level Output Voltage	VOL	IOL = 1 mA			0.2	V	DGSSB, DGSCLK, DGDATA, EIRQ
High–level Output Voltage	VOH	IOH = –2 mA	AVDD30–0.3			V	MON1, MON2
Low–level Output Voltage	VOL	IOL = 2 mA			0.3	V	
Low–level Output Voltage	VOL	IOL = 2 mA			0.2	V	SCL, SDA
Analog Input Voltage	VAI		AVSS		AVDD30	V	MON1, MON2

Table 5. D.C. CHARACTERISTICS: INPUT/OUTPUT (continued)
(at T_A = −30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.6 to 3.3. V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit	Applicable Pins
Pull Up Resistor	Rup		50		250	kΩ	DGSSB, DGSCLK, DGDATA, MON1, MON2
Pull Down Resistor	Rdn		50		220	kΩ	DGSSB, DGSCLK, DGDATA, EIRQ, MON1, MON2

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. DRIVER OUTPUT (at T_A = 25°C, V_{SS} = 0 V, PGND = 0 V, AVDD = VM = 2.8 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	Ifull	Full code		160		mA
Output Current OUT5, OUT6		Full Code OP−AF(bidirection)		130		mA

Table 7. NON−VOLATILE MEMORY CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Circuit
Endurance	EN				1000	Cycles	EEPROM
Data Retention	RT		10			Years	
Write Time	tWT				20	ms	

AC CHARACTERISTICS

V_{DD} Supply Timing

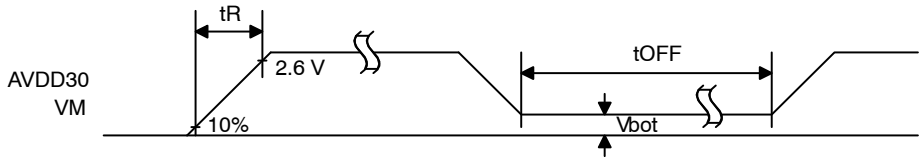


Figure 3. V_{DD} Supply Timing

Table 8. V_{DD} SUPPLY TIMING

Item	Symbol	Min	Typ	Max	Units
Rise Time	tR			3	ms
Wait Time	tW	100			ms
Bottom Voltage	Vbot			0.2	V

Injection order between AVDD30 and VM is below.

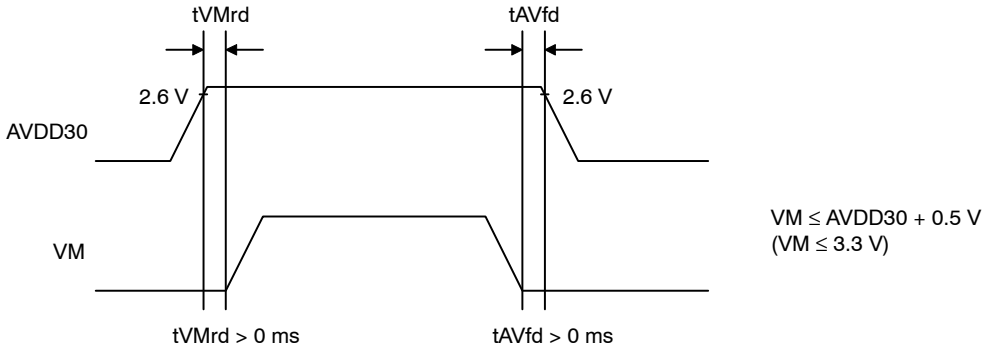


Figure 4.

SDA, SCL tolerate 3 V input at the time of power off.

The data in the EEPROM may be rewritten unintentionally if you do not keep specifications.
And it is forbidden to power off during EEPROM access. The data in the EEPROM may be rewritten unintentionally.

AC SPECIFICATION

The Figure 5 shows interface timing definition and Table 9 shows electric characteristics.
The communication protocol is compatible with I^2C (Fast mode Plus).
This circuit has clock stretch function.

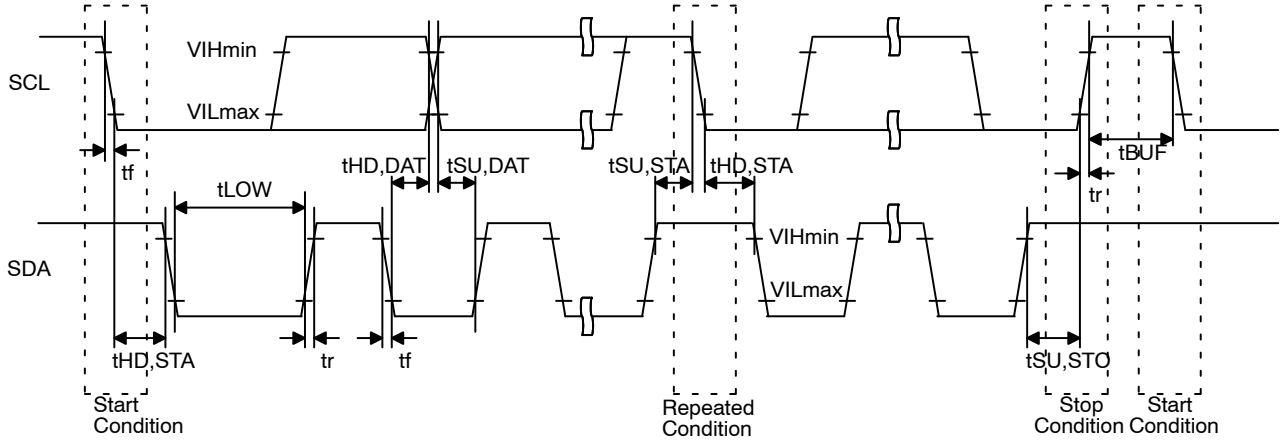


Figure 5. 2−wire Serial Interface Timing Definition

Table 9. ELECTRIC CHARACTERISTICS FOR 2−WIRE SERIAL INTERFACE (AC CHARACTERISTICS)

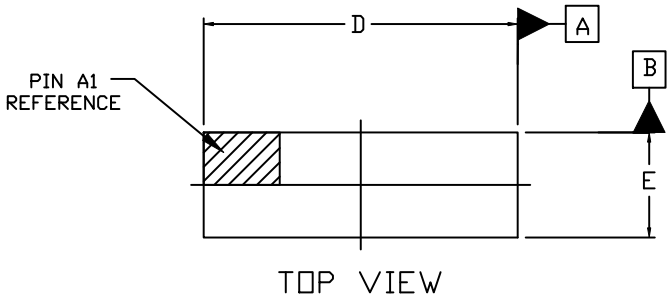
Item	Symbol	Pin Name	Min	Typ	Max	Units
SCL Clock Frequency	Fscl	SCL			1000	kHz
START Condition Hold Time	tHD,STA	SCL SDA	0.26			µs
SCL Clock Low Period	tLOW	SCL	0.5			µs
SCL Clock High Period	tHIGH	SCL	0.26			µs
Setup Time for Repetition START Condition	tSU,STA	SCL SDA	0.26			µs
Data Hold Time	tHD,DAT	SCL SDA	0 (Note 1)		0.9	µs
Data Setup Time	tSU,DAT	SCL SDA	50			ns
SDA, SCL Rising Time	tr	SCL SDA			120	ns
SDA, SCL Falling Time	tf	SCL SDA			120	ns
STOP Condition Setup Time	tSU,STO	SCL SDA	0.26			µs
Bus Free Time between STOP and START	tBUF	SCL SDA	0.5			µs

1. Although the I^2C specification defines a condition that 300 ns of hold time is required internally, This LSI is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

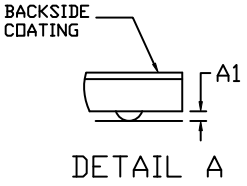
SCALE 4:1

WLCSP27, 3.89x1.30, 0.4P
CASE 567NJ
ISSUE A

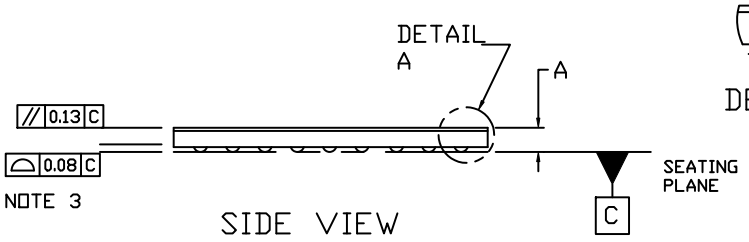
DATE 22 SEP 2020



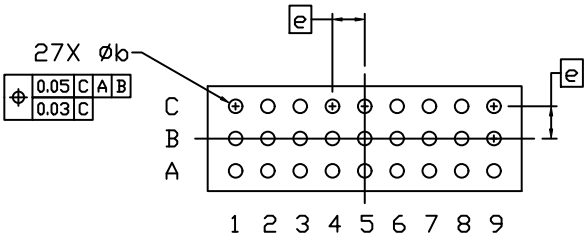
TOP VIEW



DETAIL A



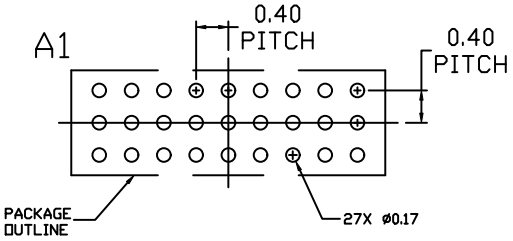
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.04 REF		
b	0.12	0.17	0.22
D	3.84	3.89	3.94
E	1.25	1.30	1.35
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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